

# 國立台北科技大學

## 電機工程系

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### 數位邏輯實習

#### 課程簡介



教師：張陽郎、沐海  
助教：黃俊傑、林煒哲

# 講義資料參考FTP:

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<ftp://download:download@140.124.40.155/>

-> 111-2 電機一甲 DLE Handout

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# Chang, Yang-Lang

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# 簡介

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- 電子設計自動化 (Electronic Design Automatic, EDA)
  - 電腦輔助設計 (Computer Auxiliary Design, CAD)
  - 數位電路設計發展的過程
    - 電晶體層次 (Transistor-Level) 設計
    - 邏輯閘層次 (Gate-Level) 設計
    - 硬體描述語言 (Hardware Description Language, HDL)
  - 微處理器 (Micro-Processor)
  - 微控制器 (Micro-Controller)
  - 特殊應用積體電路 (Application Specific IC, ASIC)
  - 現場可程式化閘陣列 (Field Programmable Gate Array, FPGA)
  - CPLD (Complex Programmable Logic Device)
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# 電子設計自動化

## Electronic Design Automatic, EDA

### EDA Industry Working Groups

<http://www.eda.org/>

The screenshot shows an Internet Explorer browser window with the address bar displaying <http://www.eda.org/>. The page title is "EDA.ORG Home Page - Internet Explorer". The browser's menu bar includes "檔案(F)", "編輯(E)", "檢視(V)", "我的最愛(A)", "工具(T)", and "說明(H)". The toolbar contains icons for "上一頁", "後一頁", "停止", "刷新", "地址", "搜尋", "我的最愛", "打印", "收藏夹", "工具", "帮助", and "移至". The main content area of the website has a header with the text: "Dedicated to the support, open exchange and dissemination of in-development standards from" followed by the large heading "EDA Industry Working Groups". Below this is a subtitle: "The Electronic Design Automation (EDA) and Electronic Computer-Aided Design (ECAD) one-stop resource on the WWW! (with a historical focus on HDL's due to our origin and sponsors)". On the right side of the header, there is a "Sponsored by" section with the Accellera logo and links to "Stanford University", "Sun Microsystems", and "About this serve". A note in green text states: "(green groups appear to be dormant) (italicized groups are of interest but not hosted at this site)". The main content is divided into two columns. The left column is titled "Accellera" and lists several groups: "Accellera Designer's Forum", "Open Verification Library" (formerly OVI Assertion, see also OpenVerification.org), "Other:" (including C/C++ Class Library Standardization Working Group (alc-cwg), Interface Technical Committee (itc), and Open Kit (openkit) Technical Committee), "System Level Design:" (including Language (slds, sldi) Study Group (also former OVI Architecture Language Committee), Core Working Group (slds-cwg), Rosetta Working Group (slds-rosetta), and Semantics Working Group (slds-semantics)), and "SystemVerilog:". The right column is titled "IEEE Design Automation Standards Committee (DASC)" and lists various standards and committees: "P1076 Standard VHDL Language Reference Manual (VASG)" (including VHDL-200x and Issues Screening and Analysis Committee (ISAC)), "VHDL Programming Language Interface Task Force (VHPI)", "P1076.1 Standard VHDL Analog and Mixed-Signal Extensions (VHDL-AMS)", "P1076.1.1 Standard VHDL Analog and Mixed-Signal Extensions - Packages for Multiple Energy Domain Support (StdPkgs)", "P1076.4 Standard VITAL ASIC (Application Specific Integrated Circuit) Modelin Specification (VITAL)", "P1076.6 Standard for VHDL Register Transfer Level (RTL) Synthesis (SIWG)", "P1364.1 Standard for Verilog Register Transfer Level Synthesis (VLOG-Synth)", "P1481 Standard for Integrated Circuit (IC) Open Library Architecture (OLA) (IEEE1481R)", and "P1499 Standard Interface for Hardware Description Models of Electronic Components (OMF)".

EDA.ORG Home Page - Internet Explorer

檔案(F) 編輯(E) 檢視(V) 我的最愛(A) 工具(T) 說明(H) Google EDA

← 上一頁 → 下一頁 停止 刷新 地址 搜尋 我的最愛 打印 收藏夹 工具 帮助 移至

網址(D) <http://www.eda.org/>

Dedicated to the support, open exchange and dissemination of in-development standards from

## EDA Industry Working Groups

The Electronic Design Automation (EDA) and Electronic Computer-Aided Design (ECAD) one-stop resource on the WWW!  
(with a historical focus on HDL's due to our origin and sponsors)

Sponsored by  
  
[Stanford University](#)  
[Sun Microsystems](#)  
[About this serve](#)

(green groups appear to be dormant) (italicized groups are of interest but not hosted at this site)

### Accellera

- Accellera [Designer's Forum](#)
- [Open Verification Library](#)  
(formerly OVI [Assertion](#)) (see also [OpenVerification.org](#))
- Other:
  - C/C++ Class Library Standardization Working Group ([alc-cwg](#))
  - Interface Technical Committee ([itc](#))
  - Open Kit ([openkit](#)) Technical Committee
- System Level Design:
  - Language ([slds](#), [sldi](#)) Study Group  
(also former OVI [Architecture Language](#) Committee)
  - Core Working Group ([slds-cwg](#))
  - Rosetta Working Group ([slds-rosetta](#))
  - Semantics Working Group ([slds-semantics](#))
- [SystemVerilog](#) :

### IEEE Design Automation Standards Committee (DASC)

- **P1076** Standard VHDL Language Reference Manual ([VASG](#))
  - [VHDL-200x](#): the next revision
  - Issues Screening and Analysis Committee ([ISAC](#))
  - VHDL Programming Language Interface Task Force ([VHPI](#))
- **P1076.1** Standard VHDL Analog and Mixed-Signal Extensions ([VHDL-AMS](#))
- **P1076.1.1** Standard VHDL Analog and Mixed-Signal Extensions - Packages for Multiple Energy Domain Support ([StdPkgs](#))
- **P1076.4** Standard VITAL ASIC (Application Specific Integrated Circuit) Modelin Specification ([VITAL](#))
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- **P1364.1** Standard for Verilog Register Transfer Level Synthesis ([VLOG-Synth](#))
- **P1481** Standard for Integrated Circuit (IC) Open Library Architecture (OLA) ([IEEE1481R](#))
- **P1499** Standard Interface for Hardware Description Models of Electronic Components ([OMF](#))

# 參考書籍

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- 主要上課為自編之PPT講義
  - 參考用書：  
數位邏輯設計(VHDL入門實務)台科大
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# 課程大綱

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## 課程內容綱要：

- 第 1 週 開學課程及相關規定說明
- 第 2 週 DE2-70 Quartus II 軟體簡介及使用
- 第 3 週 組合邏輯：同位產生器，多工器
- 第 4 週 組合邏輯：七段解碼器，解多工器
- 第 5 週 清明節補假
- 第 6 週 組合邏輯：邏輯運算單元 (2對1多工器)
- 第 7 週 算數邏輯：半加器與全加器
- 第 8 週 算數邏輯：四位元加減器
- 第 9 週 期 中 考 期末專題企劃書
- 第 10 週 算數邏輯：三位元乘法器
- 第 11 週 順序邏輯：正反器，暫存器
- 第 12 週 順序邏輯：狀態機，RAM
- 第 13 週 順序邏輯：二位元同步計數器 10模數計數器
- 第 14 週 期末專題展示
- 第 15 週 期末專題展示
- 第 16 週 期末專題展示
- 第 17 週 端午節調整放假
- 第 18 週 期 末 考 期末專題補交

## 作業編號

dl\_hw#01\_10xxxxxx  
dl\_hw#02\_10xxxxxx  
dl\_hw#03\_10xxxxxx  
dl\_hw#04\_10xxxxxx  
  
dl\_hw#05\_10xxxxxx  
dl\_hw#06\_10xxxxxx  
dl\_hw#07\_10xxxxxx  
dl\_proposal\_10xxxxxx  
dl\_hw#10\_10xxxxxx  
dl\_hw#11\_10xxxxxx  
dl\_hw#12\_10xxxxxx  
dl\_hw#13\_10xxxxxx  
dl\_final\_10xxxxxx  
dl\_final\_10xxxxxx  
dl\_final\_10xxxxxx  
  
dl\_final\_10xxxxxx

# 成績

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- 實作完成-含每週實習實作及作業 (60 %)、
  - 期末專題製作 (40 %)。
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# 這是本課程在LINE中的群組

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- 歡迎修課同學參加
- 發言時請先自報家門(學號/姓名)
- 遠距教學時，會將視訊會議的 **Google**連結貼在 **LINE**群組中



# 作業規定

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- 每一次每位同學交一份實習作業，繳交期限為下次上課前一天晚 12:00 pm 時間截止，遲交將與清除。
  - 實習作業請以 Power Point \*.ppt 格式書寫(內容含：1. 原理與操作，2. 實作記錄，3. 問題討論與心得。請參考範例。)
  - 若於上傳後發現有問題(想重寫)，請將檔案名稱更改為“dl\_hw#01\_10xxxxXxx\_1.\*”依此類推。
  - 上若未依照規定書寫，一律零分計算。若發現有"作業檔案"相互COPY雷同甚至是相同狀況現象發生，亦將全部以零分計算。
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# 作業FTP上傳

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## □ FTP上傳作業檔案格式:

檔案名稱請以上述之“作業編號”為名,例如:學號為10xxxxxxx將繳交第1週實習作業,則請使用 “dl\_hw#01\_10xxxxxxx.\*” 為你的檔案名稱(依此類推).若當次的實習作業為繳交多個檔案,請事先在你的電腦上先建立一個 “dl\_hw#01\_10xxxxxxx” 檔案夾,並將你的多個檔案放入其中,再上傳到指定的 FTP 路徑上。

## □ 指定的 FTP上傳實習作業檔案 路徑:

<ftp://upload:upload@140.124.40.155>

-> 111-2 電機一甲 DLE

-> DLE Hws/ hw?? (hw?? 為當次作業編號)

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## 其他注意事項

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- 請班代於上課前確定點名，服務股長於下課後安排當天值日生，幫忙電腦電源的關閉確認及電腦教室的清潔及桌椅之排列整齊。
  - 若有其他規定，將以上課宣佈為準。
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