Zheng Yu

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Education

Northwestern University
Ph.D. Student in Computer Science — *Sept. 2022 - Present*

Shanghai Jiao Tong University
Bachelor of Computer Science in Computer Science, member of ACM Class — *Sept. 2018 - June. 2022*

Research Experience

Research Intern — July. 2021 – Present
Pennsylvania State University, USA (Online) — *Mentors: Xinyu Xing*

- Focused on microcontroller(MCU) firmware emulation and fuzzing.
- Core developer of Qiling framework which is a binary analysis framework.

Research Intern — Feb. 2021 – April. 2021
Southern University of Science and Technology — *Mentors: Yinqian Zhang*

- Focused on the design of remote attestation protocol on TEE platform.
- Develop and improve RISC-V trusted computing platform Keystone-Enclave.

Undergraduate Research Assistant — July 2020 – 2022
Sustainable Architectures and Infrastructure Laboratory (SAIL) — *Mentors: Chao Li*

- Focused on Data Center Systems and Architectures, Cloud computing Power.
- Submitted a paper to the International Symposium on Computer Architecture (ISCA).
- Prof Chao Li's evaluation of me is "He has the potential to become an outstanding graduate student"

Teaching Experience

Teaching Assistant — June. 2019 – Sept. 2019
Shanghai Jiao Tong University

- As teaching assistant in Programming Design Course (CS151)
- Design programming assignments and course projects for students
- The students think I am a helpful and responsible teaching assistant

Honors & Awards

Zhiyuan Honor Scholarship — SJTU
Top 2% in SJTU — *2018, 2019, 2020*

The 35nd China National Olympiad in Informatics — CCF
Silver Medal — *2017*

The 12nd National College Student Information Security Contest — EZS
Second Prize — *2019*

Projects

Pymx | *Compiler, Python* — [Link]

- Pymx is a compiler written in Python3 for a Java-like language.
- Support to generate rv32im target assembly code.
- Implemented many optimization methods, including global value numbering, dead code eliminate and SSA.
- The performance of the assembly code generated by the compiler is better than that generated by gcc with O1.

RV32-CPU | *FPGA, Verilog* — [Link]

- The project is a RISCV-CPU with tomasulo algorithm.
- Run perfectly in FPGA with 100MHz.
- Support out-of-order execution and pipeline on FPGA.

Qiling | *MCU, Python* — [Link]

- Add support for STM32 and GD32V series MCU simulation.
- Add support for new arch, RISCV and Cortex-M.
- Able to semi-automatically generate code for peripheral simulation.

Atari-AI | *RL, Pytorch* [Link]

- Reinforcement learning agent for Atari games.
- Good performance in multiple game environments.

Technical Skills

Languages: C/C++, Rust, Java, Python, Solidity, Verilog
Frameworks: Pytorch, Flask, Tornado, Qiling, Angr
Developer Tools: Git, VSCode, Emacs, Docker, Vivado, Android Studio
Hardware: STM32, Arduino, NXP, FPGA