Zheng Yu

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Education

Northwestern University
Ph.D. Student in Computer Science — *Sept. 2022 - Present*

Shanghai Jiao Tong University
Bachelor of Computer Science in Computer Science, member of ACM Class — *Sept. 2018 - June. 2022*

Research Experience

Research Intern — July. 2021 – July. 2022
Northwestern University, USA (Online) — *Mentors: Xinyu Xing*

- Focused on microcontroller (MCU) firmware emulation and fuzzing.
- As a core developer of Qiling binary analysis framework.

Research Intern — Feb. 2021 – April. 2021
Southern University of Science and Technology — *Mentors: Yinqian Zhang*

- Focused on the design of remote attestation protocol on TEE platform.
- Develop and improve RISC-V trusted computing platform Keystone-Enclave.

Undergraduate Research Assistant — July 2020 – 2022
Sustainable Architectures and Infrastructure Laboratory (SAIL) — *Mentors: Chao Li*

- Focused on Data Center Systems and Architectures, Cloud computing Power.
- Prof Chao Li's evaluation of me is "He has the potential to become an outstanding graduate student"

Teaching Experience

Teaching Assistant — June. 2019 – Sept. 2019
Shanghai Jiao Tong University

- As teaching assistant in Programming Design Course (CS151)
- Design programming assignments and course projects for students
- The students think I am a helpful and responsible teaching assistant

Honors & Awards

Zhiyuan Honor Scholarship — SJTU
Top 2% in SJTU — *2018, 2019, 2020, 2021*

The 35nd China National Olympiad in Informatics — CCF
Silver Medal — *2017*

The 12nd National College Student Information Security Contest — EZS
Second Prize — *2019*

Projects

Pymx | *Compiler, Python* — [Link]

- Pymx is a compiler written in Python3 for compiling a Java-like language.
- Supports compile the source code into rv32im assembly code.
- Implemented many optimization methods, including global value numbering, dead code eliminate and SSA.
- The performance of the assembly code generated by the compiler is better than that generated by gcc with O1.

RV32-CPU | *FPGA, Verilog* — [Link]

- This project is a RISC-V cpu with tomasulo algorithm implemented in Verilog HDL,
- The project works fine at 100M on the fpga and it did not show any errors during the experiment.
- Supports many useful features, include out-of-order execution, instruction cache, load buffer, etc.
- All the code of this project is original, not borrowed from any project.

Qiling | *MCU, Python* [Link]

- Add MCU emulation module to the project, which can emulate MCUs from three top vendors.
- Add support for Cortex-M and RISCV architectures.
- Support fuzzing test of MCU firmware using afl.

Atari-AI | *RL, Pytorch* [Link]

- Reinforcement learning agent for Atari games.
- Good performance in multiple game environments.

Technical Skills

Languages: C/C++, Python, Rust, Javascript, Verilog
Frameworks: Angr, Unicorn, IDA, Qiling, Flask
Developer Tools: Git, VSCode, Emacs, Docker, Vivado, Android Studio
Hardware: STM32, Arduino, NXP, FPGA