Zheng Yu

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EDUCATION

Northwestern University	Evanston, IL
Ph.D. Student, Computer Science Department, Advised by Xinyu Xing	Sep 2022 - Present
• Research Interests: AI Security, Software Security	
• Focused on improving the security of software and AI systems.	
Northwestern University	Evanston, IL
M.S. Student, Computer Science Department	Sep 2022 - Dec 2024
Shanghai Jiao Tong University	Shanghai, China
Bachelor of Computer Science, Member of ACM Class	Sep 2018 - June 2022
Yali High School	Hunan, China
High School Student, focused on Algorithmic Competition	Sep 2015 - June 2018
Experience	
Visiting Researcher	Jun 2025 – Sept 2025
CrySp Lab, University of Waterloo	Advised by: Meng Xu
Teaching Assistant	Sep $2024 - Dec 2024$
Introduction of Computer Security (COMP_SCI 350), Northwestern University	•
Project Mentor	${ m Apr}\ 2022-{ m Oct}\ 2022$
Summer of Code 2022, Google	-
Security Engineer	June $2021 - May 2022$
$JD.com,\ Inc.$	
Research Assistant	${\rm Feb~2021-April~2021}$
RITAS Lab, Southern University of Science and Technology	Advised by: Yinqian Zhang
Research Assistant	July 2020 – June 2022
SAIL Lab, Shanghai Jiao Tong University	Advised by: Chao Li
Website Operation	Sep 2019 - Sep 2021
Network & Information Center, Shanghai Jiao Tong University	
Teaching Assistant	June $2019 - Sep 2019$
Programming Design Course (CS151), Shanghai Jiao Tong University	
Publication	

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- PortGPT: Towards Automated Backporting Using Large Language Models Zhenq Yu*: Zhaoyanq Li*: Jingyi Song; Meng Xu; Yuxuan Luo; Dongliang Mu (IEEE S&P 2026)
- PatchAgent: A Practical Program Repair Agent Mimicking Human Expertise Zheng Yu; Ziyi Guo; Yuhang Wu; Jiahao Yu; Meng Xu; Dongliang Mu; Yan Chen; Xinyu Xing (USENIX Security 2025)
- ShadowBound: Efficient Heap Memory Protection Through Advanced Metadata Management and Customized Compiler Optimization - **Zheng Yu**; Ganxiang Yang; Xinyu Xing (USENIX Security 2024)
- LLM-Fuzzer: Scaling Assessment of Large Language Model Jailbreaks Jiahao Yu; Xinwei Lin; Zheng Yu; Xinyu Xinq (USENIX Security 2024)
- CAMP: Compiler and Allocator-based Heap Memory Protection Zhenpeng Lin; Zheng Yu; Ziyi Guo; Simone Campanoni; Peter Dinda; Xinyu Xing (USENIX Security 2024)
- FIRST: Exploiting the Multi-Dimensional Attributes of Functions for Power-Aware Serverless Computing -Lu Zhang; Chao Li; Xinkai Wang; Weiqi Feng; **Zheng Yu**; Quan Chen; Jingwen Leng; Minyi Guo; Pu Yang; Shang Yue (IPDPS 2023)

• Reversing MCU with Firmware Emulation - **Zheng Yu**; KAI JERN LAU; MuChen Su; Anh Quynh NGUYEN (BlackHat Europe 2022)

Honors & Awards

Advanced Final Competition at AIxCC Northwestern University 42-b3yond-6uq 2024 5th at Defcon 23 CTF Finals DEFCON StrawHat Team 2023 7th at Defcon 22 CTF Finals DEFCON StrawHat Team 2022 **Outstanding Graduates** SJTU Outstanding Graduate of Shanghai Jiaotong University 2022 Zhiyuan Honor Scholarship SJTU Top 2% in SJTU 2018, 2019, 2020, 2021 The 35th China National Olympiad in Informatics CCF Silver Medal (top 100) 2017

Projects

PatchAgent | Security, Python

[Link]

- Developed a program repair agent that mimics human expertise.
- Implemented a novel program repair algorithm based on large language models.

ShadowBound | Security, C/C++

 $[\underline{\text{Link}}]$

- Developed a novel heap memory protection mechanism based on advanced metadata management.
- Implemented a customized compiler optimization to reduce runtime overhead.

GPT-Fuzzer | AI, Python

[Link]

- Developed a fuzzer for large language models
- Implemented a novel method to scale the assessment of language model jailbreaks.

CAMP | Security, C/C++

[Link]

- Developed a compiler and allocator-based heap memory protection mechanism.
- Implemented a novel compiler optimization to reduce runtime overhead.

Qiling $\mid MCU, Python$

[Link]

- Integrated an MCU emulation module, capable of emulating microcontrollers from three leading vendors.
- Extended support for Cortex-M and RISC-V architectures.

Pymx | Compiler, Python

[Link]

- Developed Pymx, a Python3-based compiler for a Java-like language.
- Compiles source code into RV32IM assembly language.

$\mathbf{RV32\text{-}CPU} \mid \mathit{FPGA}, \ \mathit{Verilog}$

[Link]

- Designed a RISC-V CPU with the Tomasulo algorithm implemented in Verilog HDL.
- Implemented features such as out-of-order execution, instruction cache, and load buffer.

ACADEMIC SERVICE

Program Committee Member	2025, 2026
International Conference on Learning Representations (ICLR)	
Program Committee Member Conference on Neural Information Processing Systems (NeurIPS)	2024, 2025
Program Committee Member International Conference on Machine Learning (ICML)	2025
Program Committee Member Artificial Intelligence and Statistics Conference (AISTATS)	2025
Program Committee Member The Association for the Advancement of Artificial Intelligence Undergraduate Consortium (AAAI-UC)	2025
Program Committee Member International Conference on Edge Computing and IoT (ICECI)	2024
Artifact Committee Member ACM SIGSAC Conference on Computer and Communications Security (CCS)	2023, 2024, 2025
Artifact Committee Member USENIX Security Symposium (USENIX Security)	2024, 2025
Artifact Committee Member Network and Distributed System Security (NDSS)	2025
Artifact Committee Member USENIX Annual Technical Conference (ATC)	2024
Artifact Committee Member USENIX Symposium on Operating Systems Design and Implementation (OSDI)	2024
Artifact Committee Member International Symposium on Software Testing and Analysis (ISSTA)	2024
Journal Reviewer IEEE Transactions on Dependable and Secure Computing (TDSC)	2024
Journal Reviewer PeerJ Computer Science (PeerJ CS)	2023, 2024
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TECHNICAL SKILLS

Languages: Chinese (Native), English (Fluent)

Programming Languages: C/C++, Python, Java, Javascript, Rust, Verilog

Frameworks: MySQL, Spark, Angr, Unicorn, IDA, Qiling, Ghidra

Developer Tools: Git, VSCode, Emacs, Docker, Vivado