AIRA RISC-V CPU Manual

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This project is a trivial RISC-V CPU with tomasulo algorithm implemented in Verilog HDL, which is a course project of Computer Architecture, ACM Class @ SJTU.

1 Design & Architecture

1.1 Environment

Device Name	Aira
ISA	RISCV 32I
FPGA	Basys3

1.2 Out-of-order Execution

The main feature of the Aira RISC-V is to support out-of-order execution, some algorithm used in the Aira RISC-V are brefly introduced in the table below:

Features	RISC-V CPU
Dynamic Scheduling	Tomasulo Algorithm
Piplining	3-stages pipeline (Fetch, Dispatch, Execute)
Multiple FU	2 Arithmetic/Logic Units and 1 Load/Store Unit

1.2.1 Details

- In order to achieve fetch one instruction four cycles, every cycle the fetcher will send pc and pc+4 to the I-cache.

- The fetcher receive instruction at negedge.
- For JAL instruction, fetcher calculate the target address and modify pc directly.
- Allocator rename register at dispatch stage.
- Every EX unit has a reserved station.

1.2.2 Design Diagram

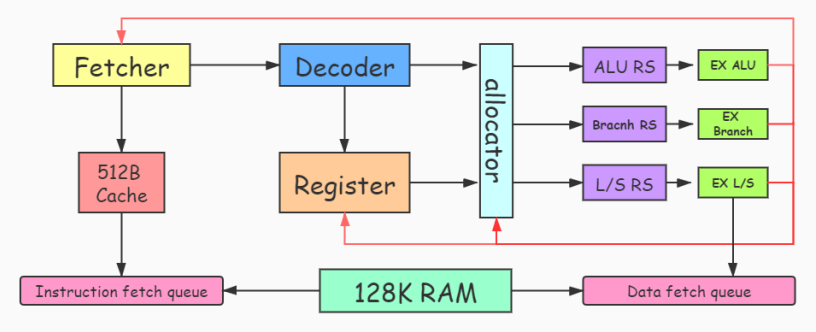

图 1: Aira RISC-V CPU design diagram

1.3 Cache

Parameter	Data
Type	Instruction Cache
Size	512B
Set Associative	2-way associative
Replacement Policy	FIFO

1.4 Other Features

Using LED light for output and debug, and segment display as timer.

2 Performance

The highest frequency that the CPU can reach is 200MHz, here are time consuming of some test points:

testcase	time(s)	IPC
pi	1.10	0.377
bulgarian	0.54	0.604
hanoi	0.76	0.783
queens	0.81	0.779

from the waveform, we can see multiple ex unit works at same time.

3 References

1. John L. Hennessy, David A. Patterson, et al. Computer Architecture: A Quantitative Approach, Fifth Edition, 2012.
2. 雷思磊. 自己动手写 CPU. 电子工业出版社, 2014.
3. RISC-V ISA Specification

4 Gallery

4.1 heart.c

图 2: heart