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Online Condition Monitoring of Electrolytic Capacitors in DC-DC Interleaved Boost Converters, Adopting a Model-Free Predictive Controller

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***Abstract*— Aluminum electrolytic capacitors (AECs) are widely used in the DC link of power converters, such as the DC-DC interleaved boost converter (IBC), which offers many advantages over the conventional amplifier converter. It is well known that AECs failures represent the major cause for breakdown of power electronics equipment. Hence, the development of robust control strategies, that allow to evaluate the electrolytic capacitor state, while keeping the performance of the converter control strategies, even under the occurrence of a capacitor fault, gains further emphasis. For that purpose, model-based predictive control (MBPC) applied to power electronics is a hot research topic that has been receiving the attention of researchers, given its advantages in terms of robustness, reduced tuning effort and, when applicable, fault tolerance. In turn, model-free predictive control (MFPC) is an underdeveloped research topic, that requires further efforts. To the best of the authors' knowledge, the literature does not report any MFPC strategy aimed at DC-DC converters. Accordingly, this paper proposes the combination of a novel MFPC strategy with the Short Time Fourier Transform (STFT) method, aiming to perform an online estimation of the ESR and C parameters, thus allowing a continuous evaluation of the electrolytic capacitor condition and, consequently, avoid a total system failure. The effectiveness of the proposed strategy is verified by several experimental tests.**

Keywords*— *DC-DC interleaved boost converters; Electrolytic capacitors; Equivalent series resistance (ESR); Capacitance (C); Short Time Fourier Transform (STFT); Model-free predictive control (MFPC).

I. INTRODUCTION

DC-link capacitors represent an important component of the majority of the power electronic converters, contributing to cost, size and failure rate on a considerable scale [1], [2]. Aluminum electrolytic capacitors (AECs) are one of the most age-affected components. Nearly 30% of the failures in converters are related to AECs, thus representing the main root of breakdowns on power electronics. Failures on AECs generally lead to an increase in the equivalent series resistance (ESR) and a decrease in capacitance (C). Typically, the increase in the ESR above 200 % of its initial value, and the reduction in C below 80 % of its initial value are generally considered indicators of a failure [1], [3]. The degradation of AECs highly deteriorates the reliability and efficiency of the systems [2]. With the increase in the quest for more energy efficient systems, the improvement of reliability and availability of power converters becomes an important area of research, particularly within the scope of applications such as renewable energy sources, hybrid vehicles, and many other safety-critical applications [3], [4]. For such applications, DC-DC power converters develop particularly relevant functions of power conditioning. To overcome the major disadvantages of DC-DC power converters, such as high voltage and current ripples, and low efficiency, interleaving strategies are seen as a prospective solution. The interleaved boost converter (IBC) offers multiple advantages over the traditional boost converter, such as minimum voltage and current ripples, low switching losses, higher efficiency, compactness, and reliability [5]. The IBC is composed of a number of conventional boost converters, called phases or legs, connected in parallel, that share a common DC link [6]. These advantages qualify the IBC for uses in advanced applications. The relatively complex structure and behaviour of IBCs implies the use of robust control strategies, with the aim of maintaining stable system operation, even in case of failure of AECs.

The literature reports a multitude of model-based predictive control (MBPC) strategies applied to DC-DC converters, which provide improvements like high prediction accuracy or reduced computational effort. MBPC schemes have been proposed for single-switch boost converters [7], multilevel converters [8], or interleaved DC-DC converters [9], to name but a few. Unfortunately, the performance of MBPC strategies becomes seriously affected in the presence of unknown variations of the system parameters or when the model of the system is not fully established. Model-free predictive control (MFPC) provides an optimal control strategy capable of overcoming the drawbacks of MBPC, allowing to minimise the design effort, while providing robustness against parameters' uncertainty. MFPC has been lately considered for control of applications such as electric motor drives [10] or doubly-fed induction generators [11]. To obtain a model-free control approach, state-of-the-art

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solutions predict the future behaviour of those systems using ultra-local models [10], [11], recursive least-square self-commissioning models [12] or adaptive integral backstepping models [13]. These MFPC methods are dedicated to DC-AC converters, reason why further investigation in MFPC for DC-DC converters is crucial. The literature survey reveals that MFPC approaches suitable to address the fast dynamics of DC-DC converters have not been developed yet. In this work, the design of the converter controller is based on a novel MFPC strategy, to skip all the negative effects of model dependency, parameters uncertainty and, most importantly, deviation on the capacitor parameters induced by failures of these power converter components. The MFPC strategy comprises an outer voltage loop to control the DC-bus, and an inner current loop to ensure equal current sharing between the three legs of the IBC.

Regarding AECs fault diagnostics, most of the proposed methods are based on monitoring the ESR and C [14]. The real-time online computation model for C and ESR is established according to the analysis of the voltage ripple measured on the capacitor. By using an ESR estimation circuit, that requires only a few op-amps, passive elements, and a low-cost microcontroller, a condition monitoring technique for industrial power converters has been presented in [4]. In [15], the monitoring of the electrolytic capacitor condition is based on the evaluation of its impedance at twice the grid frequency (100 Hz). This technique was applied to a single-phase grid-connected PV system, where the grid power fluctuates at twice the fundamental grid frequency. Another method, based on analysing the output voltage step response with respect to a decrease in the capacitance, has been proposed to detect capacitor wear-out at the output stage of a step-down DC-DC converter [16]. In [17], an online method is presented for monitoring the state of AECs in a PV system connected to the single-phase network, by injecting harmonic frequency current into the network, using the solar inverter overnight. The impedances of the capacitors are evaluated at multiple frequencies. Using these impedance values, the ESR and C values are estimated with the least mean squares (LMS) algorithm. In [18], a new online monitoring scheme is proposed for the output electrolytic capacitor of the discontinuous conduction mode (DCM) flyback converter. In [19], the proposed method enables accurate estimation of the capacitor's core temperature. Along with the capacitor's ESR, the core temperature can be effectively used to monitor the health of an AEC. An online condition monitoring method based on a state observer method is presented in [20]. In [21], an online ESR estimation method is proposed for the output capacitor of a boost converter, using only the output voltage ripple and the inductor current. In [22], a quasi-online monitoring method of the output capacitor and boost inductor of a DCM boost converter is presented and validated. In [23], [24], the Short Time Least Square Prony's (STLSP) method has been proposed for online estimation and tracking of the ESR and C for a DC-DC boost converter.

In this paper, a novel approach for capacitor fault detection and control of a three-phase interleaved boost converter is proposed. The control task of this strategy uses a model-free predictive controller to ensure fast dynamics and robustness, even under faulty operation, while the fault detection task uses the Short Time Fourier Transform (STFT) method [25] to perform an online estimation of the ESR parameter, thus allowing a continuous evaluation of the electrolytic capacitor's condition.

II. AECs: Characteristics and Equivalent Circuit

AECs are composed of electrodes (one is the anode and the other is the cathode), electrolytic paper, electrolyte, and an oxide film, as shown in Fig. 1 [1], [4]. The dielectric is an oxide layer (Al_2O_3), which is formed electrochemically on the surface of the electrodes [26]. The surface of the electrodes is etched to increase the effective surface area. In non-solid aluminum electrolytic capacitors, the fluid electrolyte, forming the second plate of the capacitor, penetrates the pores of the anode oxide layer to provide the maximum surface contact and high capacitance values [26]**.** Due to the physical design and construction, a capacitor is not only characterised by a capacitance (C), but also by an equivalent series resistance (ESR) and an equivalent series inductance (ESL). The simplified equivalent circuit of an AEC is shown in Fig. 1.

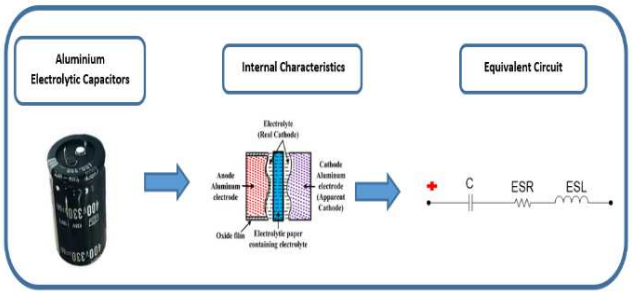

Fig. 1. Structure of an aluminum electrolytic capacitor [22].

III. Converter Architecture

The DC-DC interleaved boost converter (IBC) is used in different applications due to its extreme versatility. It is commonly employed to reduce the size of the filter components, the voltage and current ripple, and to increase the output power and efficiency [6]. The three-phase interleaved boost converter, presented in Fig. 2, consists of three paralleled boost converters operated by gating commands with 120° phase-shift among each other, sharing the same duty cycle. The choice of N=3 phases is justified by a compromise regarding the volume of the inductors.

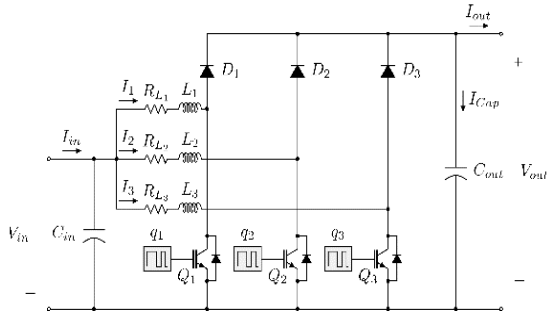

Fig. 2. Three-phase interleaved DC-DC boost converter.

IV. Ultra-local model of the converter

The generic expression defining the ultra-local model of a system is:

$$y' = F + \alpha u \quad \textbf{(1)}$$

where y denotes the system outputs, F is a variable containing the known and unknown parameters of the system, as well as the disturbances of the system, and α is a coefficient used to adjust the order of magnitude of the system inputs u. In the particular case of the three-phase interleaved boost DC-DC converter, the inputs and outputs of the system are the switching duty cycle $d_{1...3}$ and the inductor currents $I_{1...3}$, respectively:

$$Y = \begin{bmatrix} I_1 & I_2 & I_3 \end{bmatrix}^T, U = \begin{bmatrix} d_1 & d_2 & d_3 \end{bmatrix}^T \quad \textbf{(2)}$$

Using the Euler backward method to convert the derivative of the converter state variables into the discrete-time domain, the ultra-local model is:

$$Y(k+j) = \left(F + \alpha U(k+j-1)\right) T_S + Y(k+j-1) \quad \textbf{(3)}$$

where $Y(k+j)$ denotes the predicted inductor currents at the instant $k+j$, j expresses the prediction horizon, and T_s refers to the sampling time. For each iteration, the estimation of F $\left(\hat{F}\right)$ is computed as [9]:

$$\hat{F} = -\frac{3}{j^3 T_S} \sum_{i=1}^{j} A \quad \textbf{(4)}$$

where A is given by:

$$A = \left(j - 2(i-1)\right) y_n(k-1) + (j-2i)\, y_n(k) + \\ + \alpha_n (i-1) T_S \left(j - (i-1)\right) u_n(k-1) + \alpha_n i T_S (j-i) u_n(k) \quad \textbf{(5)}$$

The selection of the cost function is a critical aspect defining the performance of any MFPC strategy. For improved performance and reduced tunning effort, this paper proposes the following three cost functions, with fully normalised quantities:

$$J = \begin{cases} \left(\dfrac{I_1^* - I_1(k+j)}{I_1(k+j)}\right)^2 + \left(\dfrac{I_1(k+j) - I_2(k+j)}{I_1(k+j)}\right)^2 + d_1^2 \\ \left(\dfrac{I_2^* - I_2(k+j)}{I_2(k+j)}\right)^2 + \left(\dfrac{I_2(k+j) - I_3(k+j)}{I_2(k+j)}\right)^2 + d_2^2 \\ \left(\dfrac{I_3^* - I_3(k+j)}{I_3(k+j)}\right)^2 + \left(\dfrac{I_3(k+j) - I_1(k+j)}{I_3(k+j)}\right)^2 + d_3^2 \end{cases} \quad \textbf{(6)}$$

where $I_{1...3}^*$ denote the reference values for the phase currents. Since it is commonplace to define a reference for the converter output voltage, these reference values are obtained from the output voltage reference. The three cost functions are applied concurrently, at each time step, to determine the three optimal duty cycles.

The normalisation of the terms of the cost function obviates the requirement of design of weighting factors, thus providing an additional important advancement of the proposed MFPC strategy over the literature. The computational effort is effectively reduced through the adoption of a finite set of state variables. The range of duty cycle is discretised in steps of 0.01. For each time step, the prediction of the future system behaviour considers only seven distinctive values for the duty cycle, located around the current value applied to the system. Accordingly, at the instant k, the computation involves the following set of state variables:

$$d_n(k+1) \in \left[d_n(k) - 0.03 \quad d_n - 0.02 \quad \ldots \quad d_n + 0.02 \quad d_n(k) + 0.03\right].$$

V. Capacitor Fault Detection Algorithm

The main objective of the proposed MFPC strategy is to guarantee a constant DC bus voltage, even under a capacitor fault at the converter output. The second task comprises the development of a Fault Detection Algorithm (FDA), allowing an online evaluation of the capacitor state. The proposed FDA is based on the STFT method, which performs an online estimation of the capacitor ESR and C, through the information provided by the capacitor voltage and current ripples (Fig. 3). For the FDA, it should be emphasised that the objective is to estimate and monitor the ESR and C, as these parameters provide a relevant indicator of the condition of the capacitor. Any change in the ESR is reflected in the ratio of the capacitor voltage ripple to current ripple. At any given moment, this ratio is equal to the impedance of the capacitor. The latter is dominated by ESR in the high-frequency range. Therefore, it is possible to calculate ESR and C using the following expressions [23]-[26]:

$$ESR = \frac{V_{fsw}}{I_{fsw}} \quad \textbf{(7)}$$

$$X_C = \frac{V_{fm}}{I_{fm}} \Rightarrow C = \frac{1}{2\pi f_m X_C} \quad \textbf{(8)}$$

where V_{fsw} and I_{fsw} are the amplitudes of the voltage and current harmonics, respectively, measured at the converter switching frequency, while V_{fm} and I_{fm} denote the amplitudes of the voltage and current harmonics, respectively, measured at the fundamental frequency.

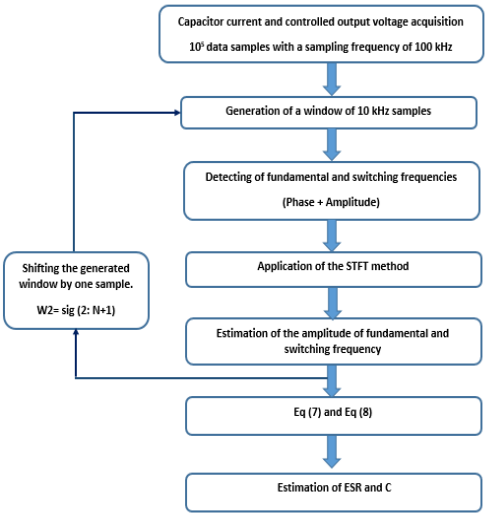

Fig. 3. Explanatory scheme of the proposed FDA.

VI. Experimental Results

The experimental configuration is illustrated in Fig. 4, while the block diagram of the system used to verify the effectiveness of the proposed MFPC and FDA is shown in Fig. 5. The experimental setup of the 3-phase interleaved boost converter, shown in Fig. 5, comprises three inductors of 10 mH and a DC bus capacitor of 220 µF.

A DC power supply of 48 V is integrated at the input of the converter, while the load side integrates a variable programmable resistive load (R). The switching frequency is set to 5 kHz.

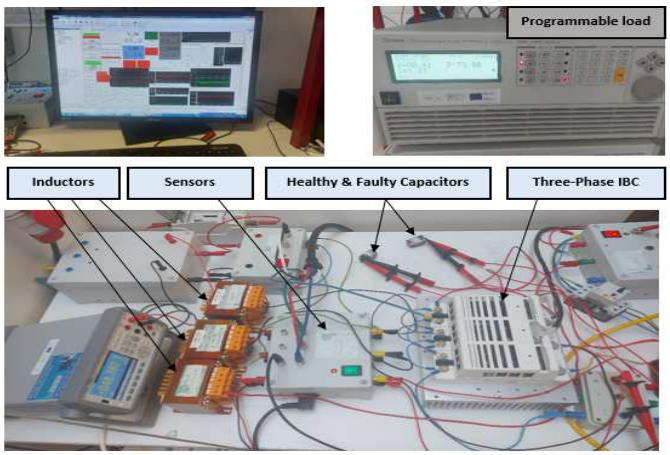

Fig. 4. Experimental setup of the 3-phase interleaved boost converter.

A. Healthy State

The goal is to investigate the system's behavior and demonstrate the robustness of the proposed controller/FDA in various operating modes. The converter is programmed in such a way that the system's output voltage follows its reference independent of internal disturbances (parametric fluctuation or malfunction in the converter, for example) or external disturbances (change in load, temperature, etc.). The experimental results depicted in Fig. 6 shows that the measured output voltage (Vc) perfectly follows the desired output, during variations of the reference signal. Fig. 6 shows that a fast and smooth transient response is obtained, on the one hand, and small voltage ripple is observed at steady-state, on the other hand. After imposing the updated voltage reference, at $t = 3\ s$, the output voltage reaches 100 % of the new reference value within 40 *ms*. On the other hand, the experimental results confirm that the proposed MFPC ensures minor distortion of the current waveforms. These findings illustrate the suggested MFPC strategy's rapid dynamics and strong tracking performance.

B. Faulty State

A robust control should maintain all dynamics and tracking performance even if one or more converter components fail. To that end, the proposed controller's resilience was evaluated in the presence of a capacitor defect. The goal is to identify the existence of a capacitor defect while also making system dynamics and tracking performance insensitive to the presence of such faults. The FDA was built in parallel with the converter controller to achieve this aim. The proposed FDA computes and tracks the ESR and C parameters using capacitor current and voltage signals. The STFT technique is used to analyze these signals.

Two electrolytic capacitors were connected in parallel on the IBC converter's output side in order to induce a capacitor failure abruptly. A bidirectional switch controls the commutation of healthy and faulty capacitors. The ESR and C parameters of both healthy and faulty capacitors are measured using an RLC meter, configured to perform the measurements at the fundamental and switching frequencies. Table I shows the obtained values.

TABLE I
The measured **ESR** and **C** values

Healthy Capacitor	0.285 Ω	200.49 µF
Aged Capacitor	0.757 Ω	188.96 µF

The proposed FDA resorts to the capacitor voltage and current signals, which were acquired using a NI-USB-6366 series data acquisition card. The sampling rate for data acquisition was set to 100 kHz.

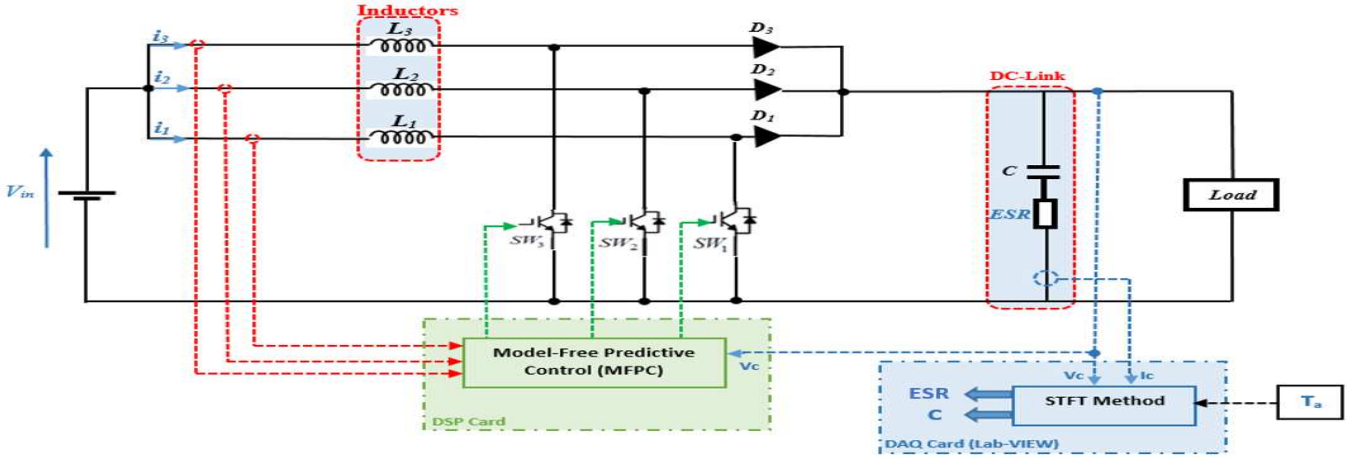

Fig. 5. Block diagram of the 3-phase interleaved boost converter, corresponding controller, and FDA.

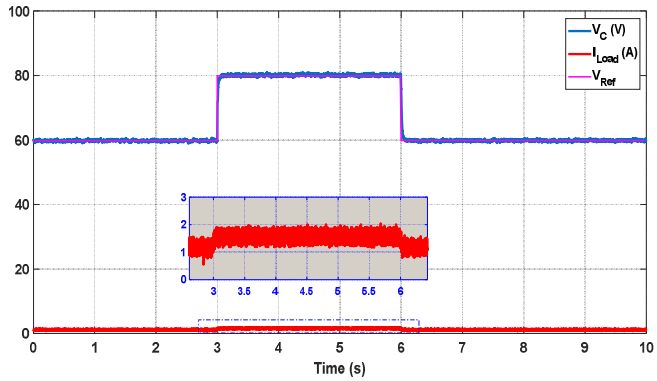

Fig. 6. Converter output voltage, corresponding reference value, and converter output current.

The STFT method was developed in Matlab code and placed into the Lab-VIEW software through the Matlab script node for online execution of the suggested FDA. The proposed method's additional phases, such as low-pass filtering and down-sampling, were carried out directly using Lab-VIEW palettes. While the IBC was operating with a healthy electrolytic capacitor, the acquisition of capacitor voltage and current signals began. After a few seconds, the bidirectional switch was commuted to the aged capacitor. Fig. 7 shows the output voltage of the IBC in both states (healthy and faulty). The results show that the output voltage effectively follows its reference after a small transient period, even in the presence of the faulty capacitor.

Fig. 8 shows the evolution of the output voltage and current in the presence of a transient variation in the voltage reference value, followed by an abrupt fault in the capacitor. The results show that the output voltage effectively tracks the imposed reference after a small period, even in the presence of two transients: one of them related to the update of the output voltage reference; and the second one related to a major fault in the capacitor. After switching to the aged capacitor, the DC output voltage suffers a small and short transient, before recovering again its reference value. It can also be noticed that the capacitor fault does not influence the load current.

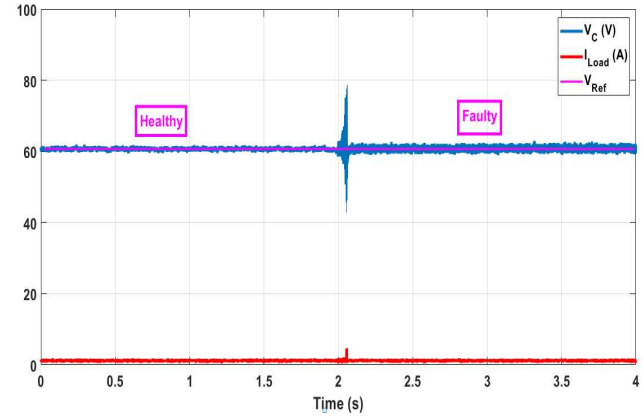

Fig. 7. Output voltage and load current in the presence of a fault in the capacitor.

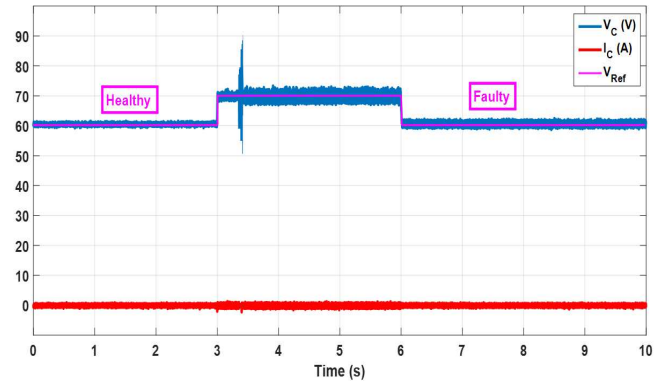

Fig. 8. Output voltage, corresponding reference value, and capacitor current, measured in the presence of a fault in the capacitor.

Fig. 9 depicts the estimated ESR and C values, observed for the operation conditions considered in Fig. 8. Fig. 9 shows that before the occurrence of a capacitor fault, the mean values of the estimated ESR and C are equal to 0.273 Ω and 196 µF, respectively. Compared with the measurements made with the RLC meter, the relative errors are 4,3 % and 2,24 %, respectively. Fig. 9 also shows a significant increase in the ESR parameter and a decrease in the C value after the occurrence of a capacitor fault. The estimated ESR and C converge to new mean values of 0.739 Ω (270.7 % increase) and 188.96 µF (96.4 % decrease), respectively, corresponding to relative errors of 2.4 % and 2.1 %, respectively. These findings agree with the theoretical expectations and demonstrate that the proposed FDA can accurately estimate and track the electrolytic capacitor's effective parameters. Concurrently, the used MFPC indicates a very significant insensitivity to capacitor failure.

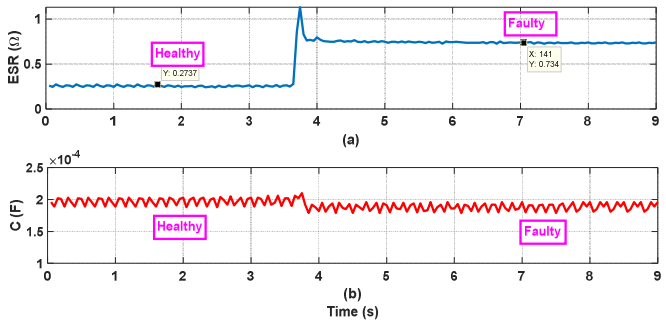

Fig. 9. (a) ESR; and (b) C values estimated for healthy and faulty electrolytic capacitors, using the STFT Method.

VII. Conclusion

In this paper, a fault detection and control strategy have been proposed and applied to a DC-DC interleaved boost converter. The control task relies on a novel MFPC approach. Along with the insensitivity against parameters variation, the proposed MFPC demonstrates good indicators in both steady- and transient-states, even in the presence of capacitor faults. Fast settling time and small voltage and current ripple are attained, considering multiple operation scenarios. The fault detection task uses the STFT method to perform an online

estimation of the ESR and C parameters, which allows a continuous evaluation of the electrolytic capacitor state, using only the capacitor voltage and current signals. The strengths and merits of the proposed fault diagnostic strategy are demonstrated by the excellent ability of the method to detect capacitor faults, even in the scenarios under evaluation in this paper, where the control strategy masks the fault signatures. Therefore, the performance of the proposed fault diagnostic strategy is not affected by the adopted control strategy.

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REFERENCES

[1] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," IEEE Trans. Ind. Appl., vol. 50, no. 5, pp. 3569–3578, Sept.-Oct. 2014.

[2] W. Miao, X. Liu, K. H. Lam, and P. W. T. Pong, "Condition monitoring of electrolytic capacitors in boost converters by magnetic sensors," IEEE Sens. J., vol. 19, no. 22, pp. 10393–10402, Nov. 2019.

[3] P. Sundararajan, M. H. M. Sathik, F. Sasongko, C. S. Tan, M. Tariq, and R. Simanjorang, "Online condition monitoring system for DC-link capacitor in industrial power converters," IEEE Trans. Ind. Appl., vol. 54, no. 5, pp. 4775–4785, Sept.-Oct. 2018.

[4] A. M. R. Amaral and A. J. M. Cardoso, "On-line fault detection of aluminium electrolytic capacitors, in step-down DC–DC converters, using input current and output voltage ripple," IET Power Electron., vol. 5, no. 3, pp. 315–322, Mar. 2012.

[5] B. S. Revathi and M. Prabhakar, "Non isolated high gain DC-DC converter topologies for PV applications–A comprehensive review," Renew. Sustain. Energy Rev., vol. 66, pp. 920–933, 2016.

[6] M. Y. Hammoudi, R. Saadi, A. J. M. Cardoso, M. E. H. Benbouzid, and M. Sahraoui, "Practical implementation of H-infinity control for fuel cell-interleaved boost converter," Int. J. Model. Simul., vol. 40, no. 1, pp. 44–61, 2020.

[7] P. Karamanakos, T. Geyer, and S. Manias, "Direct Voltage Control of DC-DC Boost Converters Using Enumeration-Based Model Predictive Control," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 968–978, Feb. 2014

[8] B. Wang, V. R. K. Kanamarlapudi, L. Xian, X. Peng, K. T. Tan, and P. L. So, "Model predictive voltage control for single-inductor multiple-output DC–DC converter with reduced cross regulation," IEEE Trans. Ind. Electron., vol. 63, no. 7, pp. 4187–4197, July 2016.

[9] Y. Liang, Z. Liang, D. Zhao, Y. Huangfu, L. Guo, and B. Zhao, "Model predictive control of interleaved dc-dc boost converter with current compensation," in 2019 IEEE International Conference on Industrial Technology (ICIT), Melbourne, VIC, Australia, 2019, pp. 1701–1706.

[10] Y. Zhang, J. Jin, and L. Huang, "Model-Free Predictive Current Control of PMSM Drives Based on Extended State Observer Using Ultralocal Model," IEEE Trans. Ind. Electron., vol. 68, no. 2, pp. 993–1003, Feb. 2021

[11] Y. Zhang, T. Jiang, and J. Jiao, "Model-free predictive current control of dfig based on an extended state observer under unbalanced and distorted grid," IEEE Trans. Power Electron., vol. 35, no. 8, pp. 8130–8139, Aug. 2020.

[12] F. Tinazzi, P. G. Carlet, S. Bolognani, and M. Zigliotto, "Motor parameter-free predictive current control of synchronous motors by recursive least-square self-commissioning model," IEEE Trans. Ind. Electron., vol. 67, no. 11, pp. 9093–9100, Nov. 2019.

[13] H. Li, X. Li, Z. Chen, J. Mao, and J. Huang, "Model-Free Adaptive Integral Backstepping Control for PMSM Drive Systems," J. Power Electron., vol. 19, no. 5, pp. 1193–1202, Sep. 2019.

[14] Z. Zhao, P. Davari, W. G. Lu, H. Wang, and F. Blaabjerg, "An overview of condition monitoring techniques for capacitors in DC-link applications," IEEE Trans. Power Electron., vol. 36, no. 4, pp. 3692-3716, April 2021.

[15] M. W. Ahmad, N. Agarwal, P. N. Kumar, and S. Anand, "Low-frequency impedance monitoring and corresponding failure criteria for aluminum electrolytic capacitors," IEEE Trans. Ind. Electron., vol. 64, no. 7, pp. 5657–5666, July 2017.

[16] J. Hannonen, J. Honkanen, J.-P. Ström, T. Kärkkäinen, S. Räisänen, and P. Silventoinen, "Capacitor aging detection in a DC–DC converter output stage," IEEE Trans. Ind. Appl., vol. 52, no. 4, pp. 3224–3233, July-Aug. 2016.

[17] N. Agarwal, M. W. Ahmad, and S. Anand, "Quasi-online technique for health monitoring of capacitor in single-phase solar inverter," IEEE Trans. Power Electron., vol. 33, no. 6, pp. 5283–5291, June 2017.

[18] K. Yao et al., "A noninvasive online monitoring method of output capacitor's C and ESR for DCM flyback converter," IEEE Trans. Power Electron., vol. 34, no. 6, pp. 5748–5763, June 2018.

[19] S. Prasanth et al., "Condition monitoring of electrolytic capacitor based on ESR estimation and thermal impedance model using improved power loss computation," in 2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia), Niigata, Japan, 2018, pp. 416–421.

[20] J. Meng, E.-X. Chen, and S.-J. Ge, "Online E-cap condition monitoring method based on state observer," in 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, China, 2018, pp. 1–6.

[21] L. Ren, C. Gong, and Y. Zhao, "An online ESR estimation method for output capacitor of boost converter," IEEE Trans. Power Electron., vol. 34, no. 10, pp. 10153–10165, Oct. 2019.

[22] L. Li et al., "A Quasi-Online Monitoring Method of Output Capacitor and Boost Inductor for DCM Boost Converter," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 2205–2211.

[23] K. Laadjal, M. Sahraoui, A. J. M. Cardoso, and A. M. R. Amaral, "Online estimation of aluminum electrolytic-capacitor parameters using a modified Prony's method," IEEE Trans. Ind. Appl., vol. 54, no. 5, pp. 4764–4774, Sept.-Oct. 2018.

[24] K. Laadjal, M. Sahraoui, M. Y. Hammoudi, A. J. M. Cardoso, A. M. R. Amaral, and K. Yahia, "Diagnosis of Electrolytic Capacitors in Three-Phase Interleaved Boost Converters Controlled by Mixed Weighted Sensitivity H∞ Design Control," in IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, vol. 1, pp. 1678–1683.

[25] K. Laadjal, M. Sahraoui, and A. J. M. Cardoso, "On-Line Fault Diagnosis of DC-Link Electrolytic Capacitors in Boost Converters, Using the STFT Technique," IEEE Trans. Power Electron., vol. 36, no. 6, pp. 6303–6312, June 2021.

[26] A. J. M. Cardoso, Diagnosis and Fault Tolerance of Electrical Machines and Power Electronics. The Institution of Engineering and Technology, London, UK, (ISBN: 978-1-78561-531-3), 2018.