



Developing a Capacitor Model for Virtual Twin-Based Health Monitoring

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Table of Contents

1 Introduction	4
2 Project Background	4
3 Project Research	5
3.1 RC Low-Pass Filter	6
3.2 State-Space Model	6
3.3 Failure Conditions of Capacitors	7
3.4 Artificially Aging Capacitors	8
4 Solution Process	8
4.1 Developing the Low-Pass Filter	8
4.1.1 Designing the Low-Pass Filter	8
4.1.2 Building the Low-Pass Filter	10
4.2 Designing the Test Setup	12
4.2.1 Auxiliary Equipment	12
4.2.1.1 Oscilloscope	13
4.2.1.2 Function Generator	13
4.2.1.3 Computer	13
4.2.1.4 Sencore LC102 LCR Meter	13
4.2.1.5 HIOKI IM3536 LCR Meter	14
4.2.2 Safety Procedures	14
4.2.3 Redesigning the Perfboard Setup	15
4.3 Taking Measurements	16
4.4 Developing the Model	17
4.4.1 Choosing the State-Space Model	17
4.4.2 Developing the State-Space Model	17
4.4.3 Updating the State-Space Model	18
4.5 Methodology of Failing Capacitors	19
4.5.1 Measuring Capacitor Characteristics	19
4.5.2 Artificial Aging	19
5 Final Results	21
5.1 Fall Results	22
5.2 Spring Results	22
6 Future Work	24
7 Team Reflection	25
8 Conclusions	26
References	27
Appendix A: Procedure for taking measurements of an electrolytic capacitor.	29
Appendix B: Procedure for artificially aging an electrolytic capacitor with heat.	30

Appendix C: GitHub Repository of 2024/2025 Capstone Project Portfolio.	31
Appendix D: GitHub Repository of Claire Hopfensperger's Health Monitoring System.	32

1 Introduction

We heavily rely on electronic circuits in every part of our daily lives. Most items we interact with contain electronic circuits, and because of our dependence on electronic circuits, ensuring their correct and safe functionality and being able to determine when they might fail is imperative. Tools exist for circuit simulation and analysis, but currently, there are no widespread methods of circuit health analysis and failure prediction. If there were an accurate and reliable way to test electronic circuits and predict when they may fail, potential consequences such as loss of income or even as extreme as loss of life could be avoided.

This project's goal is to develop an accurate and reliable “digital twin”, or virtual model and simulation, of a resistor-capacitor (RC) low-pass filter to analyze the contained capacitor's health and to create a database of capacitor health throughout its lifespan for future advancement of the digital twin. We hope that by developing a thorough digital twin of the capacitor in an RC low-pass filter for capacitor health monitoring, our work could be the basis for more complex health monitoring and failure prediction systems, saving systems from extended maintenance downtime and ensuring that failures are identified before they happen.

In this report, we first explain the background of the project (*Section 2 Project Background*), expanding on health monitoring techniques, what a digital twin is, and previous work done by Miami University senior capstone students as well as the related research. Next, we go through our research we executed to establish our foundation of knowledge for this project (*Section 3 Project Research*). Next, we explore the steps we went through to work toward our project goal, including alternative solutions and design decision explanations (*Section 4 Solution Process*). Finally, we analyze our project results of what we have achieved in the fall and spring semesters (*Section 5 Final Results*) and reflect on what this project holds in store for the future (*Section 6 Future Work*) and our project accomplishments (*Section 7 Conclusions*).

2 Project Background

Health monitoring and failure detection are important to ensure the reliable and safe operation of electronic systems. Traditionally, health monitoring is done by constantly surveying the system with physical sensors and manual inspections [1]. While this method of health monitoring allows for real-time measurements, it does not always enable real-time or in-depth analysis, and it may require more expensive equipment and more time-consuming implementation [1]. To combat the disadvantages of traditional health monitoring, the research space has been exploring the benefits of utilizing statistical analysis, artificial intelligence, machine learning, control systems, and more techniques for pattern identification that would allow for real-time monitoring, analysis, and failure detection. One specific methodology being explored is using a digital twin of the system, as explained by Bofill [1].

A digital twin is a simulated model of a physical system. The digital twin contains detailed information about the physical system's behavior at any point in its lifespan [1]. By comparing the physical system to its digital counterpart, slight differences can be detected, allowing for early failure detection and prediction. The digital twin method enables more precise measurements than traditional health monitoring methods [1].

In the past two iterations of this capstone project, the previous groups worked to create models of a buck converter and a boost converter, both commonly used voltage converters in power electronics, for capacitor health monitoring and failure detection. One group utilized a Brute Force Algorithm to match the experimental data to the correlating model of a boost converter [2], and the other group used state space representation to create their digital twin model of a buck converter for graphical data comparison [3]. They compared experimental and ideal data to predict capacitor health based on changes in the capacitor's ripple voltage. For our project, we wanted to reduce the complexity of the system under test (SUT) so that we could characterize the digital twin development process and better understand the basic principles of using a digital twin for capacitor health monitoring.

Similar to the previous two capstone project groups, we will continue to study the lifespan of the aluminum electrolytic capacitor (AEC). AECs' performance is greatly affected by aging, and since they are widely used in power electronics and other systems, they are often one of the main causes of system failure. Specifically, AECs are responsible for about 30% of power converter failures [4]. In power electronics, a single AEC or a bank of AECs is used, and when one capacitor fails, the entire system can malfunction. One method to ensure reliable system performance is to replace all of the included capacitors [5]. By developing a reliable method of determining the health of an AEC, we can help companies avoid costly mass capacitor replacements by pinpointing when specific capacitors need to be replaced to avoid system malfunctions or failures and increase product safety margins.

3 Project Research

In this section, we explain the topics we researched in order to gain knowledge and build a better understanding of these topics to advance our project. We investigate what an RC low-pass filter is, the general structure of a state-space model, the failure conditions of capacitors, and a method to artificially age capacitors.

3.1 RC Low-Pass Filter

Low-pass filters are commonly used in a large variety of electronic circuits as their design is simple and easily implementable. The most basic type of low-pass filter is the RC low-pass filter, and we will be using this filter as our SUT.

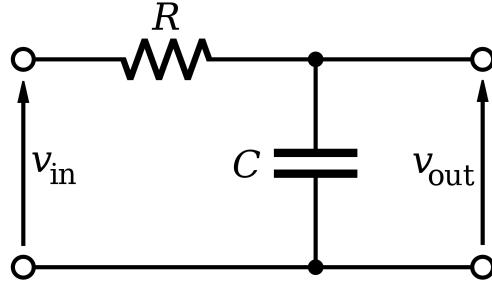


Figure 1: A schematic of an RC low-pass filter (from [6]), the project SUT.

The RC low-pass filter shown in Figure 1 is relatively simple because it only includes a voltage source, a resistor, and a capacitor. The simplicity of the circuit design allows us to start with a basic circuit model and build up from this first-principles starting point

A lowpass filter allows signals to pass through below a specific frequency, also known as the cut-off frequency, by applying high attenuation to the frequencies above it [7].

$$f_c = \frac{1}{2\pi \times R \times C} \quad (1)$$

The cut-off frequency, f_c , is determined by the values of the filter's equivalent resistance and capacitance as seen in (1). When we build our lowpass filter, we first determine the cut-off frequency, which then allows us to determine our resistor and capacitor values (*see Section 4.1.1 Designing the Low-Pass Filter*).

3.2 State-Space Model

Our digital twin relies upon an accurate transient model of the RC low-pass filter circuit. We have decided to model our circuit with a simple state space model. The general form of a state space model is described below. Middlebrook et al. [8] provided us with a process that we used for our similar derivation.

$$x = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_m \end{bmatrix} \quad (2)$$

For a state space model, we first need to represent the circuit as a state x in the form of (2), where each element x_1, x_2, \dots, x_m represents a part of the circuit with memory. Linear Electrical circuits only have two components: memory capacitors and inductors. We say these components have memory because the voltage across a capacitor and the current across an inductor cannot change instantaneously, and therefore, these values need to be recorded in the state. With this state x , we now must consider how the state changes in relation to the current state and the current input to the circuit.

$$\dot{x} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \vdots \\ \dot{x}_m \end{bmatrix} = A \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_m \end{bmatrix} + Bu(t) \quad (3)$$

This is then written in the form of (3) where A is a square matrix, B is a column vector, and $u(t)$ is the scalar input of the circuit. Lastly, consider the output of the circuit y .

$$y = C \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_m \end{bmatrix} + Du(t) \quad (4)$$

This is written in the form of (4), where C is a row vector and D is a scalar. With this model built, there are many packages in languages such as MATLAB that allow for simulation of a state space model.

3.3 Failure Conditions of Capacitors

AEC failure is defined as the capacitance decreasing by 20% and/or the equivalent series resistance (ESR) doubling [5]. These values can be used when performing artificial aging of the

AECs to track the performance of the aging process. Once we develop the digital twin, we plan to use this criterion in order to determine if the capacitor under test is near or in failure.

3.4 Artificially Aging Capacitors

To artificially age capacitors, we followed the general process executed in “Physics Based Electrolytic Capacitor Degradation Models for Prognostic Studies under Thermal Overstress” [10]. Kulkarni et al. explain that when a capacitor experiences high temperatures, the internal temperature increases, causing the electrolyte to evaporate. When the electrolyte evaporates, the capacitor degrades, with the capacitance expected to decrease and the ESR expected to increase [10]. To get the capacitance and ESR values, Kulkarni et al. measured the impedance of the capacitors 15 minutes after removing them from the heating process. ESR is the real component of the measured impedance, and capacitance is the imaginary component of the measured impedance [10].

4 Solution Process

In this section, we explore the research process we went through this semester to advance our capstone project. The main steps are (1) developing the low-pass filter, (2) designing the test setup, (3) taking measurements, (4) developing the model, and (5) artificially aging capacitors.

4.1 Developing the Low-Pass Filter

As discussed in *Section 3.1 RC Low-Pass Filter*, we used an RC low-pass filter as our SUT due to its simplicity, which allows us to build a basic circuit model. Some alternative options for our SUT were a buck converter or boost converter, which are simple and widely used power converters. We chose the low-pass filter over the power converters because we wanted an even simpler circuit for our digital twin development. Using a simpler circuit allows us to more reliably determine what factors influence system behavior and performance. We believe that with this approach, we could make an accurate and reliable model of the low-pass filter. Then, we could use it to develop more advanced models of power converters.

4.1.1 Designing the Low-Pass Filter

Before we could build our low-pass filter, we needed to decide how we wanted to design our filter. In order to make the design decisions of resistor and capacitor values, we first had to decide what cut-off frequency we wanted our low-pass filter to have. We decided that our cut-off frequency should be 10 kHz for several reasons: (1) A 10 kHz cut-off frequency is easy to achieve with common and small resistor and capacitor values, (2) 10 kHz is a relatively low

frequency but still high enough that we can observe alternating current (AC) dynamics, (3) we have access to equipment that is capable of providing and measuring signals at 10 kHz, and (4) we run a lower risk of injury when operating at 10 kHz and 5 V than if we operate at higher frequencies or voltages.

Once we decided on our cut-off frequency value of 10 kHz, we then needed to determine what resistor and capacitor values to use. To do so, we used (1) and tested different variations of resistor and capacitor values to find a combination that we thought was reasonable. We ultimately decided on values of $C = 100 \text{ nF}$ and $R = 160 \Omega$. We also decided to use two 320Ω resistors in parallel to achieve the 160Ω equivalent resistance because 320Ω resistors are readily available. Notably, when solving for R with $f_c = 10 \text{ kHz}$ and $C = 100 \text{ nF}$, we get a resistance of about 159Ω , but we are not concerned about rounding to 160Ω given the varying tolerances of the available resistors.

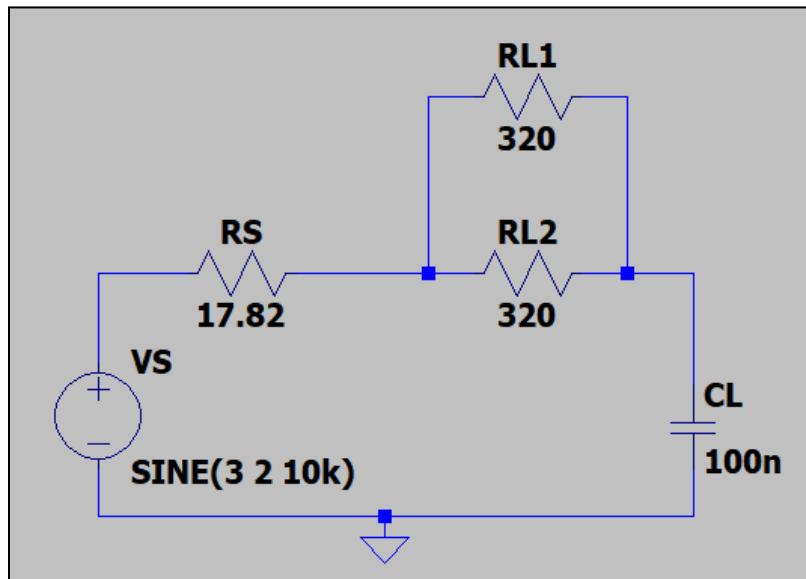


Figure 2: LTspice model of our low-pass filter circuit with two 320Ω resistors ($RL1$, $RL2$) in parallel, a 100 nF capacitor (CL), a source voltage ($VS(t) = 3 + 2\sin(2 * \pi * (10 \text{ kHz}) * t) \text{ V}$), and a source resistance (17.82Ω).

Once we chose the values for the resistors and the capacitor that would be in our low-pass filter, we ordered our circuit components [11, 12] and designed our circuit in LTspice, as seen in Figure 2, to have a reference circuit and also the ability to simulate the voltage and current behavior of the filter.

We decided that the source voltage would be a 2 V amplitude sinusoidal wave with a 3 V direct current (DC) offset so that the voltage alternates between 1 V and 5 V. We did not want the source voltage to go below 0 V because our capacitor is polar, so sending a negative voltage

through it will damage it. We also decided to limit our maximum source voltage to 5 V because it was within the operating voltages allowed for our capacitor of 100 V maximum, and would safely operate at this voltage without running risk to anyone taking measurements. We generate our source voltage using a Tektronix AFG 3022B dual-channel Arbitrary Function Generator from the ECE 493 laboratory.

$$R_{\text{Source}} = (V_{\text{FunctionGenerator}}/V_S - 1) * R_L \quad (5)$$

The source resistance was experimentally determined to be 17.82Ω using (5). We expected it to be closer to 50Ω , but it was different because we operated the signal generator in High Impedance (High-Z) mode.

4.1.2 Building the Low-Pass Filter

We first built our low-pass filter on a perfboard, or perforated circuit board, so that we can solder the components together in order to ensure more secure connections than if we only built our filter on a breadboard. A breadboard was acceptable for the initial mockup of the circuit and to ensure that everything was connected correctly, but then building it on the perfboard ensured that there would be minimal measurement errors from loose connections. Secure component connections were an important consideration for our setup because secure connections would allow us to take more reliable measurements.

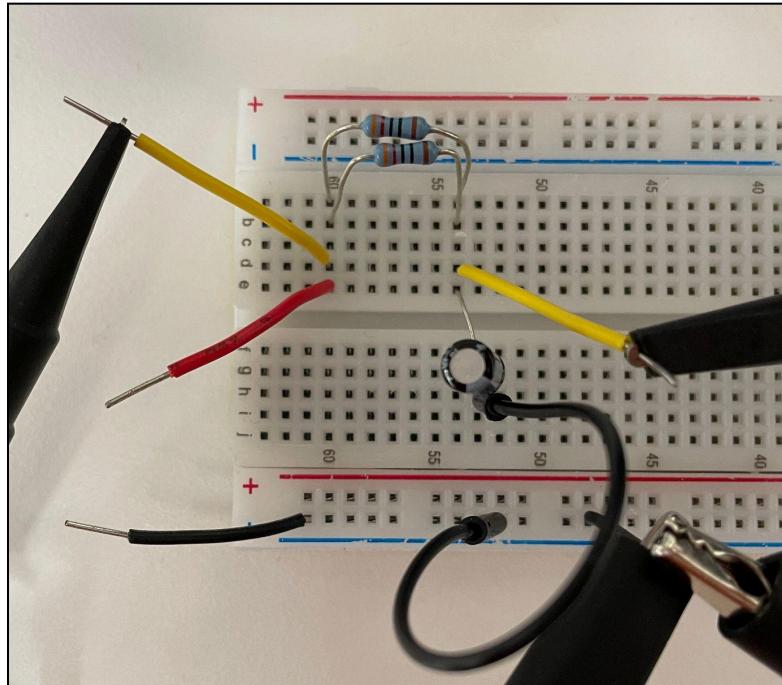


Figure 3: Low-pass filter built on breadboard. Red wire is voltage input, black wire is ground, and yellow wires are for the oscilloscope probes to reach the signals.

We first built our circuit on a breadboard, as seen in Figure 3, to verify that the components we ordered worked in our circuit design.

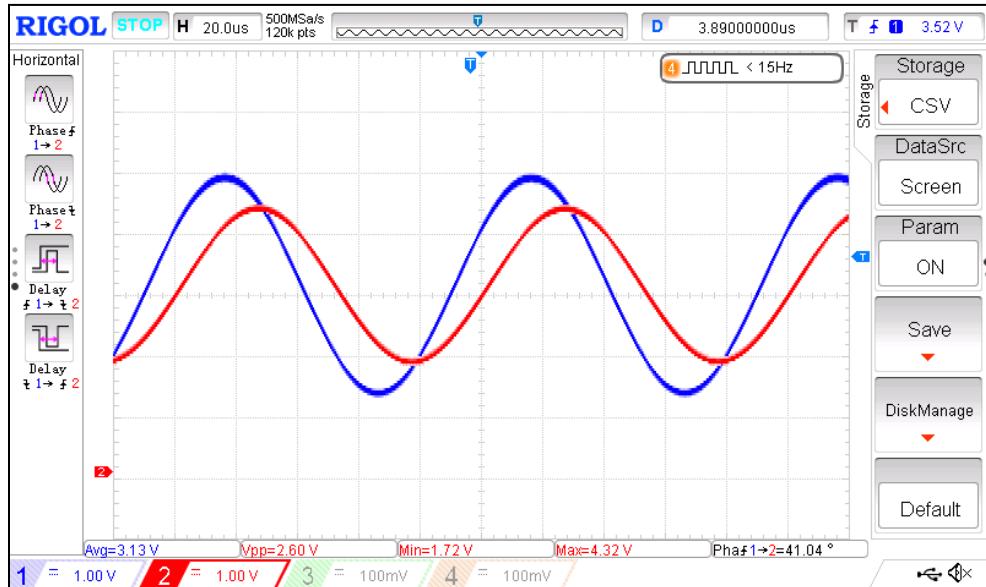


Figure 4: Oscilloscope capture of breadboard low-pass filter (Figure 3) source voltage (channel 1, blue line) and capacitor voltage (channel 2, red line).

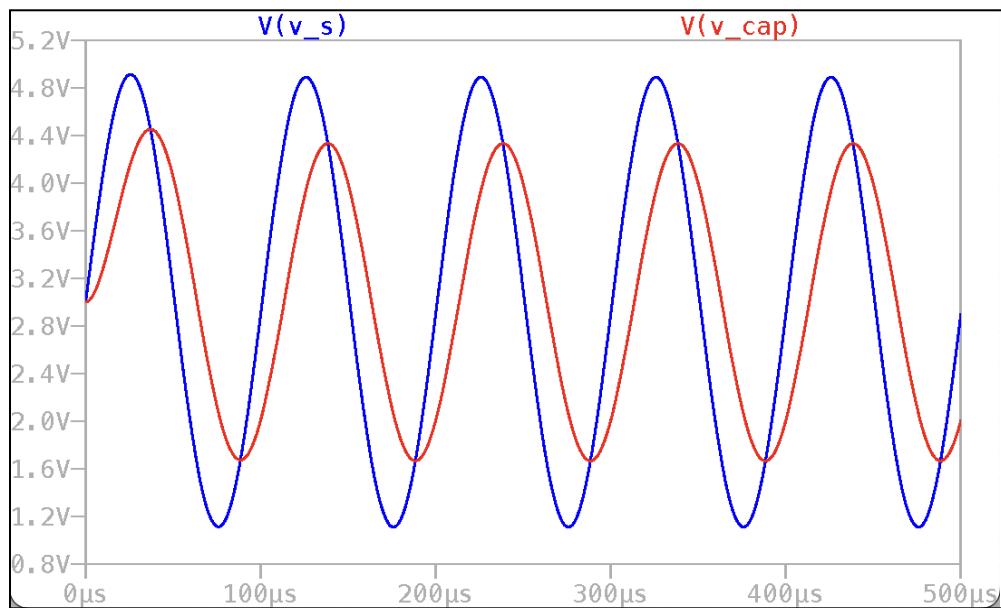


Figure 5: LTspice simulation of low-pass filter (Figure 2) source voltage (dark blue line) and capacitor voltage (red line).

To ensure our breadboard low-pass filter functioned as expected, we compared the source and capacitor voltage waveforms of our LTspice model and our physical filter. The behavior and shape of the breadboard filter voltages in Figure 4 closely resemble the LTspice model voltages in Figure 5, with minor differences that we can attribute to real-world environmental factors and potentially insecure connections between the components and connecting wires in the breadboard. These minor differences were the reason that we decided to take all final measurements from a circuit soldered onto a perfboard.

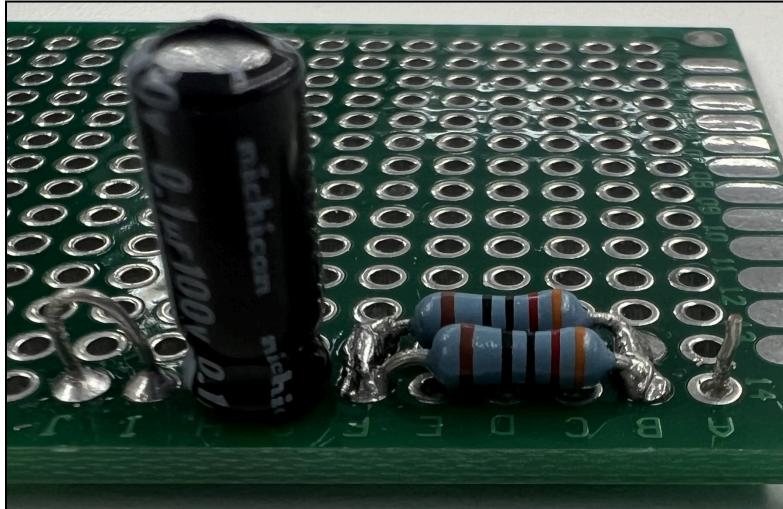


Figure 6: First assembled test low-pass filter circuit.

Because the breadboard low-pass filter functioned as expected, we felt comfortable moving forward with soldering components together on a perfboard, as seen in Figure 6. The perfboard circuit is the same design as in Figures 2 and 3, but we left a loop on the left and a test point on the right to allow for probe connectivity for our function generator and oscilloscope probes. The build in Figure 6 was the first iteration of our perfboard low-pass filter, and we went on to build another variation for further testing purposes.

4.2 Designing the Test Setup

Our initial testing setup was our low-pass filter soldered onto a perfboard with attachment points for our probes, as seen in Figure 6.

4.2.1 Auxiliary Equipment

We used several essential tools to support our experiments, including an oscilloscope for waveform visualization, a function generator for signal input, and a computer for data collection, analysis, and simulation.

4.2.1.1 Oscilloscope

We used a Rigol DS1054Z Digital Oscilloscope, which has 4 available channels, to take readings with a 50 MHz range and can sample at up to 1 GSa/s to ensure that we had as much data as possible for analysis and processing. It also had features to allow us to export the waveforms being seen/captured to a USB drive connected to the oscilloscope as a screen capture or as a comma-separated value (CSV) file. It also gave us the ability to connect it directly to a computer and pull data in real-time from the oscilloscope.

4.2.1.2 Function Generator

We used the Tektronix AFG 3022B dual-channel Arbitrary Function Generator from ECE 493's laboratory because it was easily accessible and could provide our source voltage (1 V - 5 V sinusoid) at our desired frequency (10 kHz). This function generator has a maximum output of 20V peak to peak, which is still only about 40% of the maximum voltage that our capacitor could manage. However, we chose the 5 V range for safety and not to try to overdrive the function generator.

4.2.1.3 Computer

One option for gathering data from the oscilloscope was to use a Raspberry Pi single-board computer running the Raspbian operating system (OS). This option is a poor choice as there is no official software for the Rigol Oscilloscope that we are using on Linux, and community efforts to enable access to the data stream were many years old and not designed/built for use on an ARM-based system. A better option is to use an Intel Next Unit of Computing (NUC) small form factor Windows computer. We were able to get the Intel NUC working with the oscilloscope, and the setup also enabled us to pull data directly from the oscilloscope into MATLAB for analysis.

4.2.1.4 Sencore LC102 LCR Meter

This piece of equipment uses the RC time constant as the capacitor is charged to 5V across a 15k Ohm resistor with a resolution of .0001 uF. It is set up with the specifications of the capacitor from the manufacturer, voltage rating, expected capacitance, and tolerance and can give a good/bad reading depending on whether the capacitor has breached the tolerance threshold that was entered.

4.2.1.5 HIOKI IM3536 LCR Meter

This meter must be calibrated before taking measurements. This is done by calibrating as an open circuit and then as a short circuit. We used the ‘frame’ feature of this meter to record capacitance and ESR readings across a frequency range of 100 Hz to 8 MHz. Each frame must be set up with the following parameters: 3V input AC voltage, 3V input DC offset, and frequency. Each frame records 2 measurements specified by the user, capacitance and ESR. After the frames for all desired frequency points are set up, the meter is placed in continuous mode, executes all desired frames, and saves the data as a CSV to a USB drive.

4.2.2 Safety Procedures

After taking initial manual measurements, we began thermally aging capacitors and testing these aged capacitors. Testing aged or failed capacitors increases safety concerns due to the lack of predictability of their behavior and the potential for the capacitor to vent electrolyte or even explode. To decrease these risks, we developed some safety precautions to adhere to when resuming additional testing.

The safety precautions we developed are:

- Ensure anyone who is involved with taking measurements knows the location of the nearest eyewash station to the lab where we were taking measurements (Figure 7).

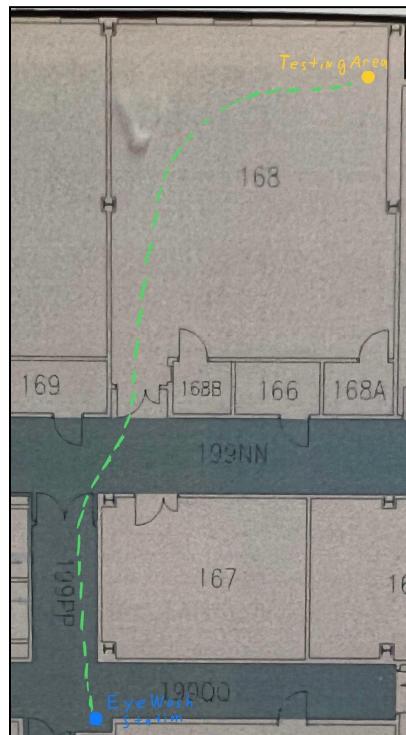


Figure 7: Testing location (yellow dot) and nearest Emergency Eyewash Station (blue dot).

- Using eye protection, a pair of UVEX clear lens Z87/Z94.3 rated safety goggles were sourced and located at/with the testing station for use by any group member when performing measurements.
- A 3D-printed enclosure was designed and made for testing in case of a catastrophic failure of any of the capacitors once we started using procedures to artificially age them.
- Wear long pants and closed-toed shoes.

4.2.3 Redesigning the Perfboard Setup

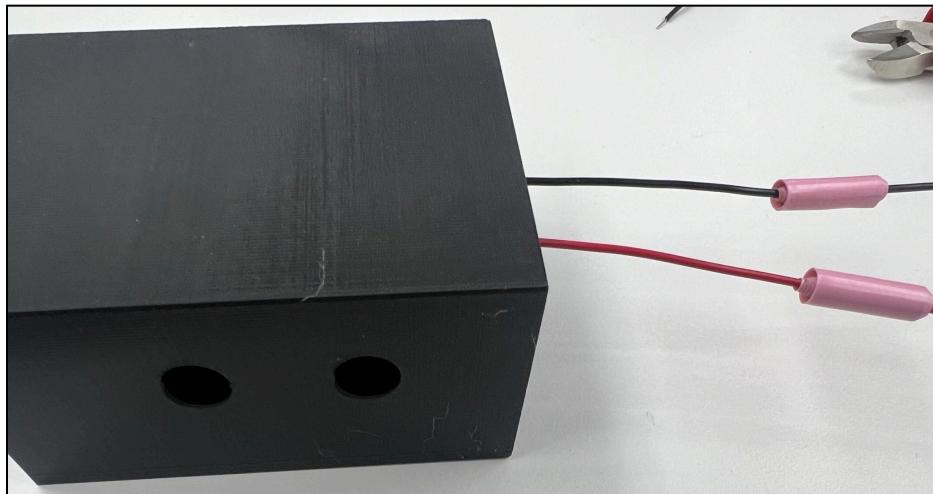


Figure 8: 3D-printed protective box with signal wires and probe ports.

Since our perfboard low-pass filter is relatively small, we designed a box, shown in Figure 8, that the perfboard can slide into and remain covered. The box shields us from any volatile reactions that may occur while still allowing access to our input signal and oscilloscope probes so that we can take measurements.

The box was designed in Solidworks to fit the perfboard that we have been using, and it took three design iterations to get everything sized and positioned correctly. The box was printed in PLA+ on a Prusa Mk3s+ printer with a 0.4 mm layer height.

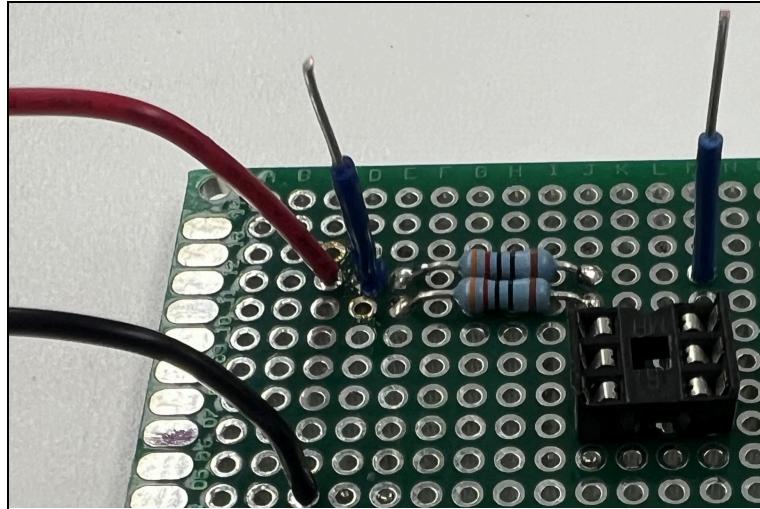


Figure 9: New test low-pass filter with IC socket and two blue wires for oscilloscope probes.

Once the final box design was printed, we assembled a new low-pass filter on a new perfboard to slide into the safety box, shown in Figure 9. This circuit was set up with an integrated circuit (IC) socket to allow us to change out the capacitor under test easily and to test multiple failure states.

4.3 Taking Measurements

When taking our first measurements, we ran into issues with the output of the signal generator not reflecting our expected outputs. This was the result of the signal generator not being in High Z mode even though we believed at the time that we had set it up correctly for our experimentation and measurement purposes. Once we corrected this issue, the output signals accurately reflected our expectations, which we mentioned earlier in *Section 4.1.2 Building the Low-Pass Filter*.

One of the things that we needed to ensure whenever setting up the signal generator was that we had an appropriate DC offset to ensure that the minimum voltage of our input signal never went below 0 V. If our input signal went below 0 V, we could cause unintended damage to the capacitor currently under test. We wanted to avoid this risk because we maintain control of the health of the capacitors so that we can make reliable and accurate conclusions about how aging the capacitor affects its health without unknown interferences.

Appendix A covers the procedures for taking all measurements and ensuring that there is consistency across all tests/gathered measurements.

4.4 Developing the Model

To create the RC low-pass filter model, we first chose our state-space model, and then we developed the state-space model.

4.4.1 Choosing the State-Space Model

We could represent our system in several ways: a transfer function, steady state analysis, or a state space model.

Analyzing our system as a simple transfer function allows for analysis of the transient behavior of the low-pass filter. However, a transfer function does not allow for analysis of a nonlinear system, and then it becomes less useful and insightful as systems become more complex. We did not desire to use a transfer function because we do not yet know how the aged capacitors behave and they may behave non-linearly or be very complex.

Alternatively, we could have simply performed steady-state analysis of the circuit and assumed a sinusoidal input. This approach is the quickest method as it requires no simulation but instead just some phasor calculations. Performing steady-state analysis was unappealing as we would prefer not to make assumptions about the input to the circuit and we are very interested in the transient response of the circuit; this method of analysis tells us nothing about the transient response.

A state space model was the next simplest way to represent the circuit that gave us the relevant transient information. And was therefore chosen for our analysis.

4.4.2 Developing the State-Space Model

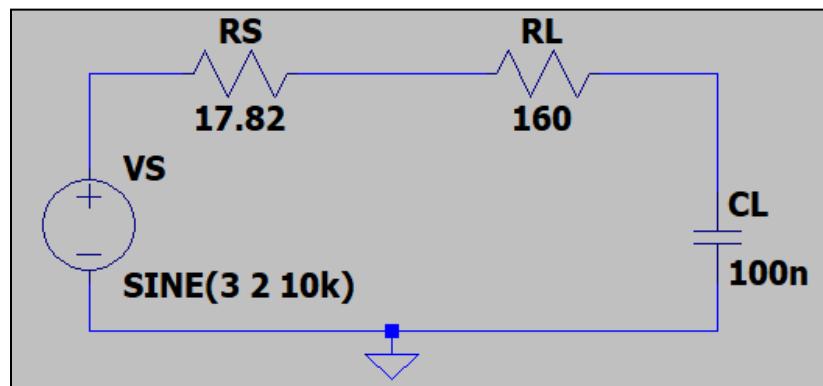


Figure 10: LTspice model of our low-pass filter circuit with an equivalent resistance of 160Ω (**RL**), a 100 nF capacitor (**CL**), a source voltage ($VS(t) = 3 + 2\sin(2 * \pi * (10 \text{ kHz}) * t) \text{ V}$), and a source resistance (17.82Ω).

The state that represents this circuit in Figure 10 is very simple as there is only one element with memory: the capacitor.

$$\mathbf{x} = [V_c] \quad (6)$$

$$\dot{\mathbf{x}} = [\dot{V}_c] = \left[\frac{i_c}{C} \right] \quad (7)$$

$$i_c = \frac{V_S - V_C}{R_S + R_L} \quad (8)$$

Equations (6) and (7) i_c can be represented as (8).

$$i_c = \frac{-1}{R_S + R_L} V_C + \frac{1}{R_S + R_L} u(t) \quad (9)$$

$$\dot{\mathbf{x}} = \left[\frac{-1}{C_L(R_S + R_L)} \right] \mathbf{x} + \left[\frac{1}{C_L(R_S + R_L)} \right] u(t) \quad (10)$$

$$A = \left[\frac{-1}{C_L(R_S + R_L)} \right] \quad B = \left[\frac{1}{C_L(R_S + R_L)} \right] \quad (11)$$

If we take V_S to be $u(t)$ and V_C to be x_1 then we get (9). Thus, resulting in (10), (11), and (12).

$$\mathbf{y} = \mathbf{x} \quad C = [1] \quad D = 0 \quad (12)$$

The output, (12), is also very simple, as it is already the one component of the state.

4.4.3 Updating the State-Space Model

In the spring semester, we updated the state-space model to account for ESR in the capacitor. This results in the A, B, C, and D matrices changing as below in equations (13) and (14).

$$A = \left[\frac{-1}{C_L(R_S + R_L + ESR)} \right] \quad B = \left[\frac{1}{C_L(R_S + R_L + ESR)} \right] \quad (13)$$

$$C = \left[1 - \frac{ESR}{R_S + R_L + ESR} \right] \quad D = \frac{ESR}{R_S + R_L + ESR} \quad (14)$$

4.5 Methodology of Failing Capacitors

To develop our digital twin for future health monitoring, we built a database of capacitor health data throughout an artificial aging process, which was done with extended periods of high temperature. We tracked the capacitors' capacitance and ESR and analyzed whether they met our failure criteria mentioned in *Section 3.3 Fail Conditions of Capacitors*.

Another potential method for artificially aging the capacitors was applying a voltage much higher than the capacitors' rated voltage. This approach came with the risk of immediate capacitor failure instead of slowly aging the capacitors over time, therefore, we chose to artificially age our capacitors with heat.

4.5.1 Measuring Capacitor Characteristics

We took measurements of our 40 capacitors before beginning the artificial aging process and after each heating round. We took measurements when the capacitors were warm, just removed from the heat, and cooled, about 24 hours after being removed from the heat. The capacitance of each was checked with the Sencore LC102 LCR meter, and we measured the capacitors' impedance across a frequency sweep from 100 Hz to 8 MHz with the Hioki IM3536 LCR meter. We used MATLAB to calculate the capacitors' capacitance and ESR with the Hioki impedance measurements, and we found these calculated values to be more accurate than the Sencore's measurements. The Sencore measurement data was inconsistent and unreliable, so we did not move forward with data analysis with this data. The Hioki measurement data, on the other hand, appeared to be more accurate and reliable, so we moved forward with data analysis with this data.

4.5.2 Artificial Aging

By heating capacitors above their rated maximum temperature, we can decrease the amount of time it takes for the capacitors to age due to the interior electrolyte deteriorating or evaporating [10]. Because our capacitors are rated for a maximum of 85°C for a maximum of 2000 hours, we increased the temperature at which we planned to heat them by 40°C to 125°C in hopes that it

would decrease the expected lifespan to about 250 hours, an eighth of the initial maximum lifespan.



Figure 11: Tube furnace used to heat capacitors.

We heated the capacitors in a tube furnace, shown in Figure 11, borrowed to us by Dr. Almquist of the Chemical, Paper, and Biomedical (CPB) Department. The capacitors were heated for 8 roughly 50-hour intervals at a constant 125°C.

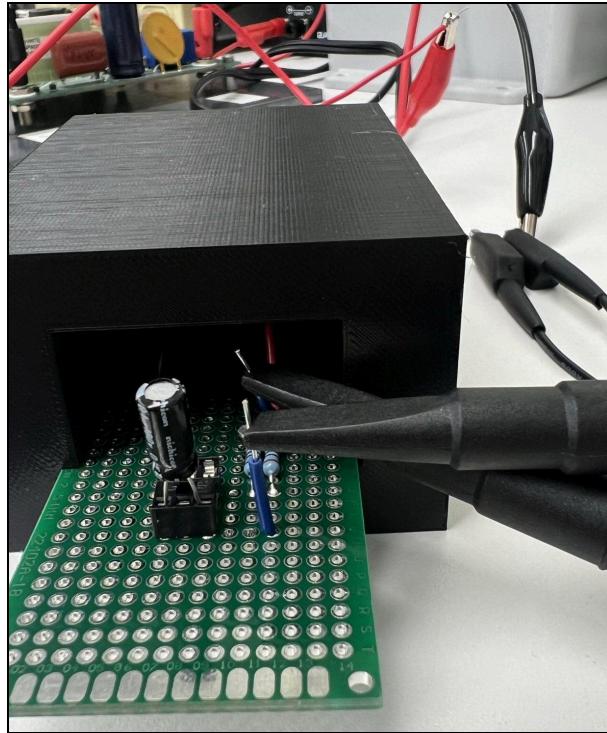


Figure 12: Capacitor in low-pass filter test setup.

After each heating interval, five capacitors were removed and tested in our low-pass filter test setup shown in Figure 12. We captured the capacitor voltage data in a CSV file with the Rigol oscilloscope and saved it to a USB drive to then transfer to our project Google Drive.

As described in *Section 4.2.2 Safety Procedures*, we developed specific safety procedures to follow when testing the capacitors in the low-pass filter test setup in order to ensure our safety as well as the equipment's safety.

The heating process was repeated with the remaining sample size of capacitors until all capacitors had been removed and tested in the low-pass filter. The Rigol-captured capacitor voltage data was compared to our low-pass filter state-space model, which is further explained in *Section 5.2 Spring Results*.

5 Final Results

Our main results were developing the state-space model of a capacitor in a low-pass filter in the fall semester and gathering artificially aged capacitor lifespan data in the spring semester.

5.1 Fall Results

In the fall semester of 2024, we captured experimental data from the physical low-pass filter and accurately timed it with our theoretical data from the state-space model.

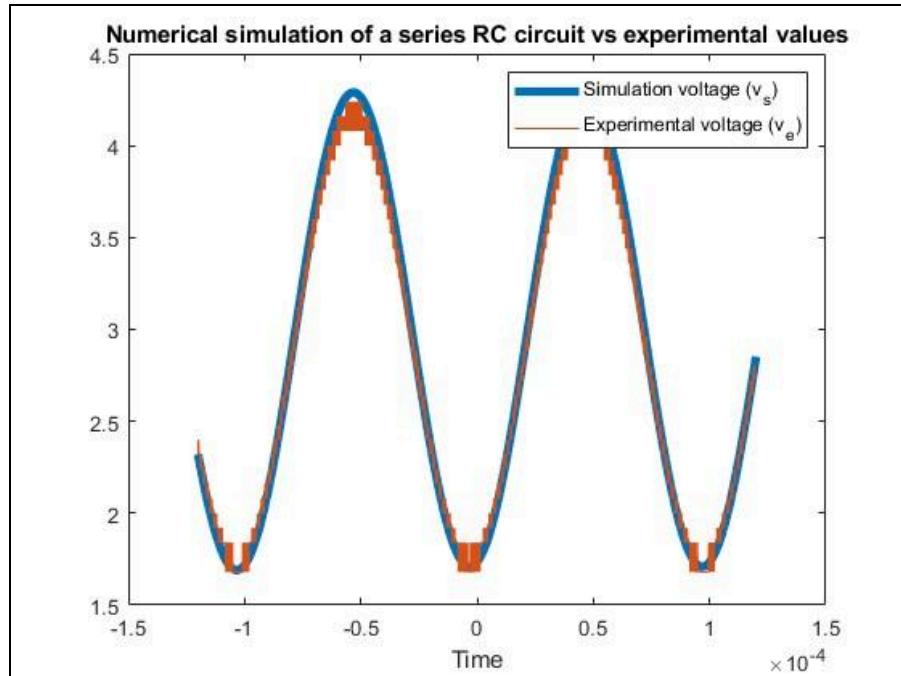


Figure 13: MATLAB voltage vs. time graph of unaged virtual twin capacitor voltage (blue line) synchronized to unaged experimental data capacitor voltage (orange line). RMS error calculated to be 77.9 mV.

Despite the volts per division being high, which causes a lower resolution of results, we can see that our experimental voltage is closely synchronized with our theoretical virtual twin voltage, as seen in Figure 13. To find the average difference between the experimental and theoretical data, we calculated the root mean squared (RMS) error to be 77.9 mV. This result shows that our experimental and theoretical data were not too far off from one another.

5.2 Spring Results

In the spring semester of 2025, we gathered capacitor health data over about 406.5 hours of artificial aging.

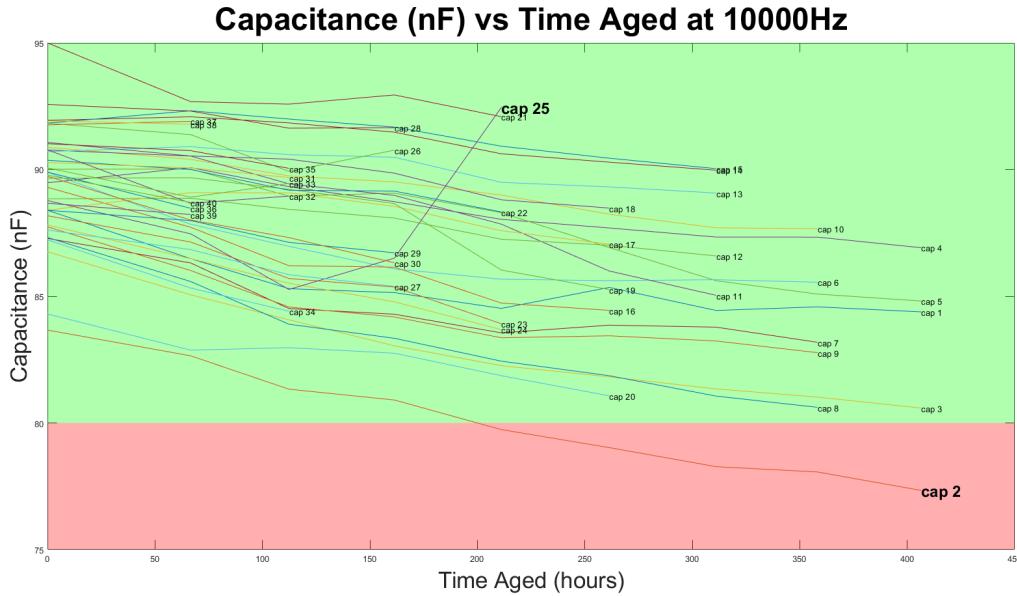


Figure 14: Graph of measured capacitance of 40 capacitors over ~406.5 hours of artificial aging in the tube furnace. The red area is defined as failure (20% decrease in capacitance from the nominal value (100 nF)).

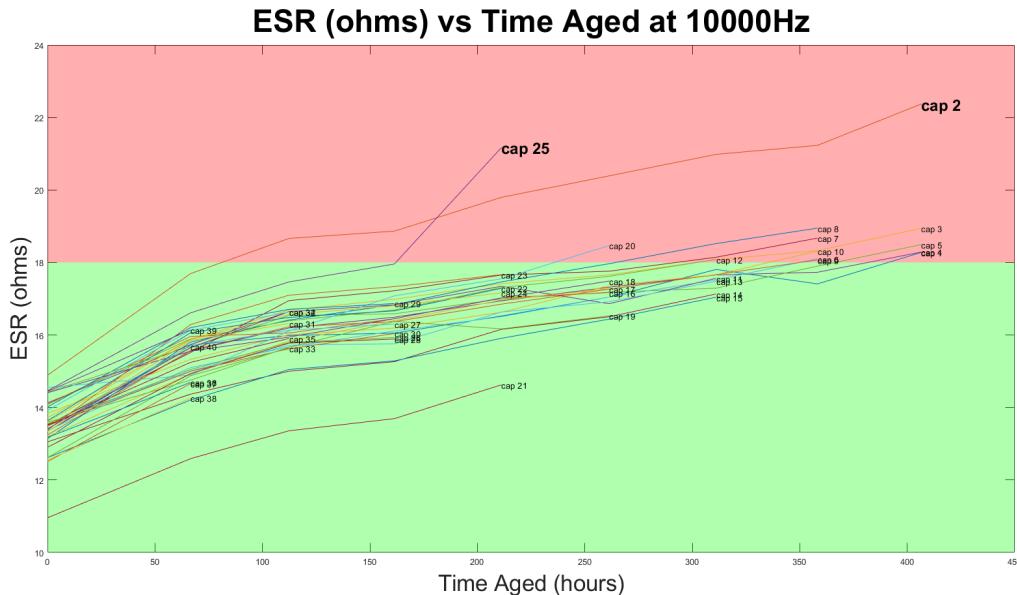


Figure 15: Graph of measured ESR of 40 capacitors over ~406.5 hours of artificial aging in the tube furnace. The red area is defined as beginning to approach failure (above 18 Ω).

Figures 14 and 15 show the capacitors' calculated capacitance and ESR from the Hioki LCR meter's measured impedance values throughout the artificial aging process. In these figures, we can see that the capacitors behaved as expected, with decreasing capacitance and increasing

ESR. While only Capacitor #2 reached our defined failure state in terms of capacitance, this is likely due to our limited artificial aging time. Had we heated the capacitors for more time, we hypothesize that more capacitors would have reached our defined failure state as well.

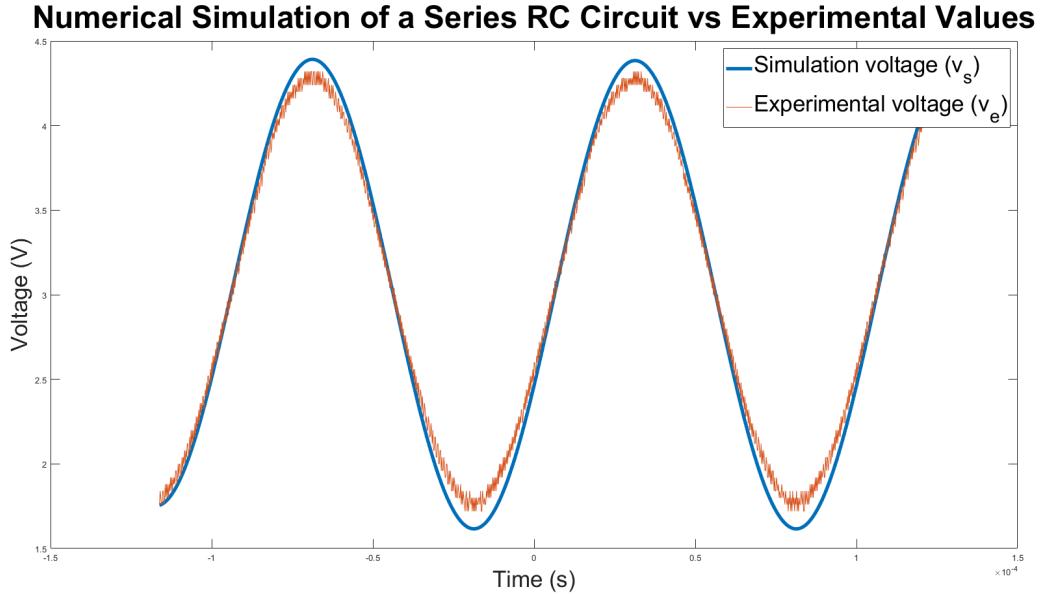


Figure 16: MATLAB voltage vs. time graph of aged virtual twin Capacitor #40 voltage (blue line) synchronized to aged experimental data Capacitor #40 voltage (orange line). RMS error calculated to be 50.8 mV.

We updated our virtual twin model by introducing an ESR variable parameterized by the data from the Hioki. We compared the improved model against the experimental results of aged capacitors captured by the Rigol with more detailed resolution, resulting in Figure 16. Figure 16 shows that the virtual twin still accurately tracks the real circuit after aging, and it tracks better than our fall semester results after updating the model to account for ESR, shown by the decrease in RMS error.

6 Future Work

With this first principles approach as a proof of concept (our portfolio in Appendix C), a more expansive data set could be culminated with more capacitors, at different temperatures, and over a longer time period. Ideally, there should be a control group at room temperature to analyze the exact relationship between the accelerated aging and the ‘natural’ aging of the capacitors.

With a more expansive data set like this, a probabilistic model of a capacitor’s behavior as it ages at different temperatures could be produced. This model, in turn, could be used to predict circuit failure.

Once an effective virtual twin model is developed, it could be integrated with Claire's Raspberry Pi health monitoring system (Appendix D). The health monitoring system enables more condensed health monitoring by directly sampling the physical system and graphing the data against the virtual twin data. By combining a more effective virtual twin model with the health monitoring system, both the model and the system could be further tested and improved.

7 Team Reflection

When working to create technological advancements, it is important to reflect on how our work will affect the people and the environment around us. Here we reflect on the following three items:

- How does your solution affect or may potentially affect public health, safety, and welfare? What are your considerations and reflections on global, cultural, social, environmental, and economic factors in your solution?

Our project's entire goal is to develop a health monitoring method, and eventually a failure prediction system, with the public's health, safety, and welfare in mind. Power electronics can be extremely dangerous when even one internal component fails, which can cause the entire system to fail. We hope that our project work establishes a basis for health monitoring to increase safety and productivity in the power electronics industry, and maybe someday all technical systems.

- Discuss your team's professional and ethical responsibility as engineers and the impact that your solutions may have in the global, economic, environmental and societal context

As engineers, the safety of the public is our responsibility, we should endeavor to produce systems that do not result in unsafe conditions for the public. An application of our research is predicting the failure of capacitors and capacitor-containing circuits. This could reduce electronic waste, increase safety, and increase the cost-effectiveness of replacing wearing components. However, it is also the responsibility of the engineers marketing this technology to understand its limitations. It would be in no one's interest to falsely state a foolproof system, as this could be hazardous.

- How you acquired and applied new knowledge as needed

On several occasions, we were unsure how to operate the various required equipment for the project. All of us became familiar with reading technical manuals for the equipment we were operating, and we also reached out to more knowledgeable professors for help, such as Dr. Almquist for help using the tube furnace. Along with learning how to operate equipment, we also

read several papers concerning the artificial aging of electrolytic capacitors to design our artificial aging process and the different parameters we need to keep in mind while doing so.

8 Conclusions

Throughout this report, we identified what a digital twin is and how it would be useful in capacitor health monitoring. We completed research on our system under test, the RC low-pass filter, and our method of modeling, the state-space model. We explored our project process of building the low-pass filter, developing safety procedures, measuring data, building the state-space model, and artificially aging capacitors to build a capacitor health dataset. We analyzed our results and explored potential future work that could be executed to further advance this project. We concluded with a reflection on our project work and how it will affect the world around us.

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Appendix A: Procedure for taking measurements of an electrolytic capacitor.

Power on the function generator and oscilloscope to allow them to begin warming up; no measurements should be taken until they have been powered on for at least 5 minutes.

Taking the capacitor that is to be measured, place it in the testing rig, ensuring that the grey line indicating which leg of the capacitor is the negative terminal is inserted into the negative side of the rig, away from the resistors and probe attachment points.

On the frequency generator, ensure that the following settings are loaded:

Frequency: 10 kilohertz

Peak to Peak voltage: 4 volts

DC offset: 3 volts

Output mode: High Z

Ensure that the oscilloscope is set up and connected to its probe points.

Turn on the signal from the function generator by pressing the channel output button above the wiring for the channel that is being used.

Have a USB drive inserted into the front USB port of the oscilloscope to take a screenshot of the waveform that is being seen as well as capturing a CSV file of the waveform. To capture the waveform, press the storage button, use the menu buttons on the right side of the screen to ensure you have the flashdrive selected and set a username with them as well, and then hit the menu button on that side for save.

Repeat for any additional capacitors that are to be tested/measured, ensuring that no changes have been made to the settings on the measurement equipment.

Appendix B: Procedure for artificially aging an electrolytic capacitor with heat.

Based on the datasheets for the capacitors [11], they should be able to maintain their rated values for 2000 hours at 85 °C. To artificially age them with heat, we will be using a formula that says that for every 10 degrees over the manufacturer's rated specification [10] that it halves the hour rating. By subjecting them to 125 °C for 250 hours with periodic stopping points to take measurements of how they are performing, aging should be seen.

After following the testing procedures to take an initial set of measurements for the capacitors, load them into test tubes. This is to contain any off-gassing that occurs from them and allows them to be inserted and removed from a tube furnace easily and safely.

Insert the test tubes into the tube furnace, trying to ensure that they are as centered as possible in the tube to avoid any uneven heating of the sample set. Turn on the tube furnace and set it to 125 °C; record the time that heating was started.

After 50 hours, the capacitors should be removed and new measurements taken, following the measurement procedures in Appendix A.

This will then be repeated 8 more times, with measurements being taken every 50 hours to build a set of baselines for capacitor ages across multiple different potential ages. This should allow for a more accurate model to be built.

Appendix C: GitHub Repository of 2024/2025 Capstone Project Portfolio.

https://github.com/clairehopfensperger/ECE449_Virtual_Twin_for_Circuit_Failure

Appendix D: GitHub Repository of Claire Hopfensperger's Health Monitoring System.

https://github.com/clairehopfensperger/OSGC_Research_Virtual_Twinning