



**Virtual Twinning for Circuit Failure Detection**

**College of Engineering and Computing  
Department of Electrical and Computer Engineering**

**ECE 449  
Senior Design Project**

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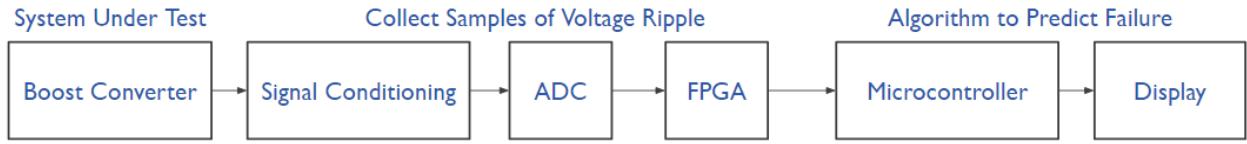
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## 1. Introduction

Aluminum electrolytic capacitors (AEC's) are widely used in power electronics systems to provide a low impedance path for AC current and to provide a constant voltage source in power converters. However, they are one of the most age-affected components, reporting 30% of failures in converters and 60% of failures in general power electronics systems [8, 12]. This is primarily due to loss of the electrolyte leading to a consequential decrease in capacitance and increase in equivalent series resistance (ESR). In an attempt to mitigate this failure, there have been many efforts in academia to monitor the condition of these capacitors, including applications in electrified transportation, wind turbines, and solar photovoltaic systems. However, even successfully developed solutions have not been implemented in industry due to cost associated with high complexity [8, 12].

The objective of this project is to design a low-cost system to monitor the capacitance of DC-link aluminum electrolytic capacitors to predict device failure. We specifically monitor the output voltage ripple of a boost converter, as it is a relatively simple yet versatile topology that is widely used in DC-DC and AC-DC power conversion [12]. The designed system successfully captures the output voltage ripple from the converter using an embedded data logging system, then compares the captured waveforms to experimentally-determined “golden models” using RMS error and a Brute Force Algorithm. A high level diagram of this proposed system is shown in *Figure 1*. As can be seen in this figure, the system under test for the proposed project is a boost converter. The output voltage ripple is then processed through signal conditioning circuitry to scale and shift the ripple so it can be read by the ADC. The data from the ADC is stored on the FPGA's on-board memory. It is then sent to the microcontroller and is passed through the algorithm for comparison with the model data. Lastly, the matched capacitance value is displayed.



**Figure 1:** Block diagram of proposed system

In the following sections, we summarize previous academic work regarding capacitor condition monitoring and introduce the theoretical basis for our proposed solution. We then detail the solution process, display and analyze our final results, and discuss future work to optimize the designed system.

## 2. Project Background

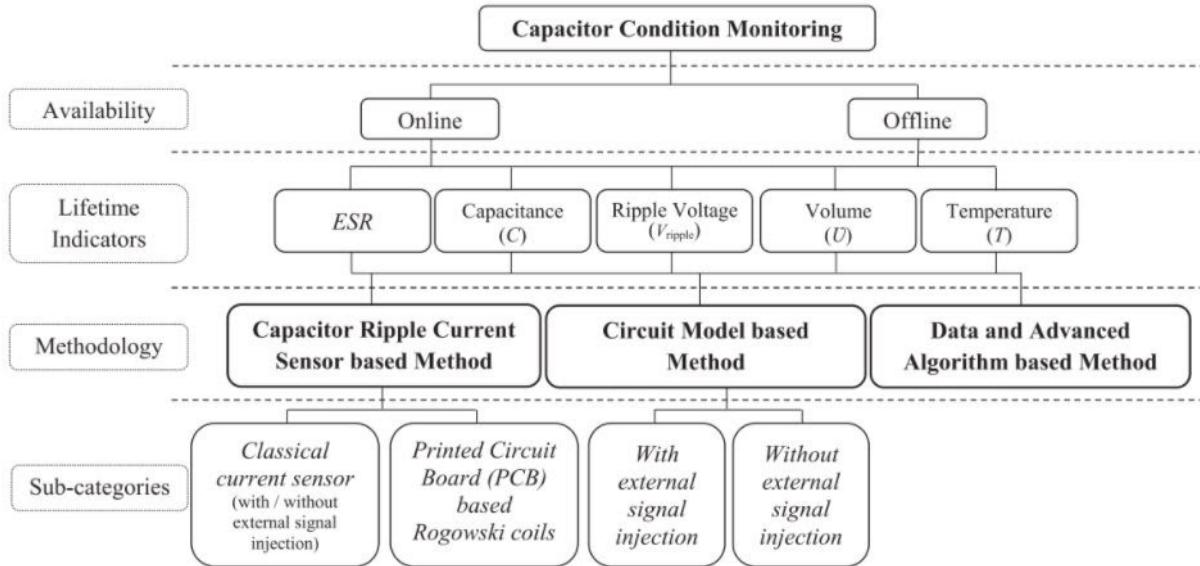
In this section we discuss the significance of capacitor failure and provide the background information necessary to understand our proposed solution. We also describe two examples of what can happen when a capacitor fails to emphasize the importance of a capacitance health monitoring system. We conclude this section by exploring potential applications of the proposed solution and explaining previous research on the topic.

Capacitors may fail due to high stress, manufacturing defects, and wear over time. These failures have serious consequences that can affect the safety and reliability of a system. For example, in December 2014, several Siemens trains in Melbourne experienced capacitor failures in the static inverters beneath the floor, causing them to be removed from service. The explosions caused by capacitor failure pose significant risks to drivers. As a result of such failures, the Rail, Tram, and Bus Union placed a ban on the operation of these trains until appropriate action was taken to protect the drivers [14]. Similarly, a train in England exploded at Guildford station. This explosion was due to a manufacturing defect in the capacitor in an equipment container beneath one of the coaches of the train. Fortunately, only the train and furniture at the station were damaged and no injuries resulted [17]. These failures were due to the self-healing property of film capacitors and breakdown of the polypropylene film. Consequently, estimation of the capacitance and ESR are essential to monitor the condition of AEC's and to predict device failure.

Both of the described scenarios could have been avoided if a simple, cost-effective system for monitoring capacitor health existed. As previously mentioned, such a system would be useful in applications such as electrified transportation, solar panels, wind turbines, and other safety-critical systems. The system could also be used to assess capacitor health during the manufacturing process, as it could detect faulty capacitors before they leave the manufacturing plant.

The prevalence of AEC failure in power converters, and the cost and potential danger of this failure, has led to a broad academic effort to monitor the condition of AEC's. In the last 25 years, numerous scientific publications have analyzed various methodologies to obtain indicators of capacitor health, specifically for applications in single-stage DC-DC converters, DC-AC

inverters, and two-stage AC-DC-AC converters [8]. These methods can be classified by their availability (online or offline analysis), lifetime indicator (ESR, capacitance, ripple voltage, volume, or temperature), and method to obtain the value of the indicator (capacitor ripple current sensor, circuit-based model, or advanced algorithms). *Figure 2* below shows a summary of these capacitor monitoring technologies.



*Figure 2: Summary and classification of capacitor monitoring technologies [8]*

The literature review conducted by Solman et. al concludes that the methodology with the highest level of accuracy is the data and advanced algorithm based model. However, the low cost and complexity associated with sensor based methods is also promising, particularly for online analysis in safety-critical systems [8]. Within the classifications shown in *Figure 2*, the final system designed and tested in this project is offline, uses ESR and capacitance (C) as the lifetime indicators, and implements a capacitor ripple sensor-based method without external signal injection.

Miami University is investigating capacitor health monitoring, both focusing on offline computation and advanced algorithm approaches. V. Sysoeva utilized electromagnetic interference to estimate DC-link metallized polypropylene film capacitor health in a three-phase inverter by applying machine learning techniques to the measured output current frequency domain data [20]. This approach successfully estimated the capacitance health with 90%

accuracy, however it required offline data collection and algorithm training, and involved overall high cost and complexity. J. Knoll calculated capacitance values for a  $\varphi_2$  inverter by comparing captured time domain data to simulated data and applying a genetic algorithm to estimate component values [9]. Preliminary experimental results showed that this approach could successfully distinguish between two capacitance values, however it required stopping the operation of the system to capture and process the data and was financially and computationally costly.

In this section we summarized the prevalence and significance of AEC failure and demonstrated the need for systems to monitor AEC health. We also compiled the most pertinent research conducted in academia and at Miami University, and emphasized the need for future applications to prioritize low cost, low complexity, online analysis for this technology to be applied in industry. The following section provides a theoretical basis for our proposed methodology to estimate capacitance and ESR in DC-link AEC's in boost converters.

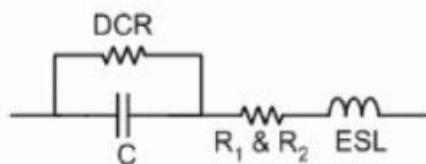
### 3. Project Research

In this section, we discuss the functionality and non-ideal facets of AEC's, explain the operation of a DC-DC boost converter, and justify monitoring the output voltage ripple to determine device failure. We also discuss the proposed Tabu Search Algorithm and compare it to alternative algorithms.

#### 3.1 Aluminum Electrolytic Capacitors

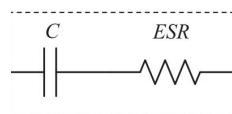
AEC's are one of three types of capacitors available for power electronics applications (the other two being metallized polypropylene film (MPPF) and multilayer ceramic capacitors) [8]. AEC's are the most widely used capacitors as input and output filters for power electronics converters, due to their low cost, high volumetric efficiency, and high voltage rating [12, 1]. The output filter of converters is crucial to maintaining the stability of the converter and regulating its output. As such, the integrity of the output AEC is crucial to device reliability. As previously mentioned, however, they are also one of the most age-affected components and cause up to 60% of converter failures.

Due to the physical composition of AEC's, the capacitor has a capacitance as well as non-ideal resistive and inductive components. *Figure 3* below shows these components: capacitance ( $C$ ), resistance of foil and terminals ( $R_1$ ), temperature sensitive resistance ( $R_2$ ), dielectric leakage resistance (DCR), and equivalent series inductance (ESL) [1].



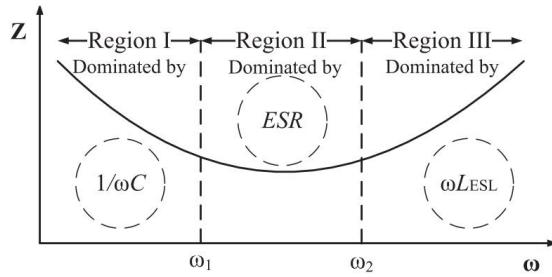
**Figure 3:** Complete Realistic Model of Aluminum Electrolytic Capacitor [1]

This realistic model, however, can be simplified to only include capacitance and ESR (*Figure 4*) for the application in the system under test (SUT) in this project.



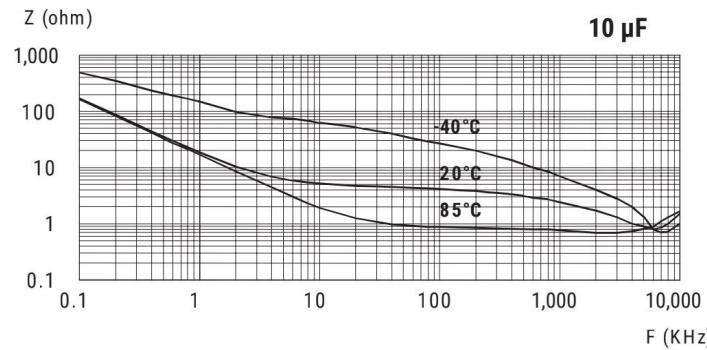
**Figure 4:** Simplified Realistic Model of Aluminum Electrolytic Capacitor

The dielectric leakage resistance is negated in this simplified model as it has a limited effect on the behavior of the capacitor. The equivalent series inductance is removed from the model because its impact on the behavior of AEC's is frequency dependent. *Figure 5* shows this theoretical impedance characteristic of capacitors, in which the behavior of the capacitor is dominated by the capacitance, ESR, then ESL.



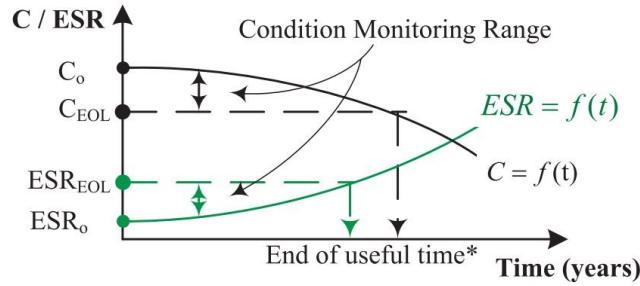
**Figure 5:** Theoretical Impedance Characteristic of Capacitors [1]

The two boost converters tested in this project operate at a switching frequency of 10 kHz and 110kHz, both of which are within the theoretical Region II from *Figure 5*. The impedance characteristic of one brand of capacitors we are monitoring is shown in *Figure 6*. This plot mirrors the theoretical relationship, and shows that from approximately 10-1,000kHz the capacitor is dominated by ESR. For these reasons, the simplified model in *Figure 4* can be used for the analysis and simulation of the converter.



**Figure 6:** Kemet Radial Aluminum Electrolytic Capacitor Impedance Characteristic [11]

Over time, the capacitance value decreases due to changes in the dielectric properties of the oxide layer and loss of the electrolyte [1]. The ESR also increases due to the evaporation of the electrolyte [12]. These degradation trends are shown in *Figure 7*.

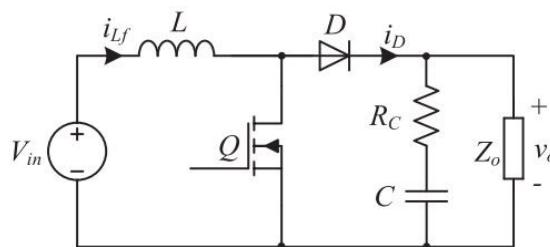


**Figure 7:** Capacitance and ESR Curves Over Time [8]

The end of life criteria for AEC's is widely considered a 20% reduction in capacitance or double the ESR [8]. These criteria can be correlated to capacitor health by comparing the estimated value to a specific cut-off value, observing the difference between the estimated and expected values, or estimating the remaining useful lifetime [8]. This project's methodology estimated the capacitance and ESR values based on the output voltage ripple of the boost converter. Based on the specific application and the system requirements, a cutoff value for the decrease in capacitance or increase in ESR could be applied to determine device failure.

### 3.2 Boost Converters

Having developed a realistic model of AEC's and their end of life criteria, we will now discuss our SUT, a boost converter. The schematic of a simple boost converter, including the ESR ( $R_C$ ) associated with capacitance  $\mathbb{C}$ , is shown in *Figure 8*.



**Figure 8:** Schematic of a Basic Boost Converter [12]

The boost converter is a well-known switched-mode converter that produces a DC output voltage greater in magnitude than the input DC voltage. The converter operation can generally be classified into two modes, continuous conduction mode (CCM) and discontinuous conduction

mode (DCM) [18]. In our project the converter is only ever operated in CCM, and the output voltage is ideally governed by Equation 1 below [7].

$$v_o = \frac{V_{in}}{1-d} \quad (1)$$

*Equation 1* shows that the output voltage is dependent on the input voltage and the duty cycle ( $d$ ) of the switch of the converter. For our work, the most important facet of the boost converter is how the capacitance and ESR values impact easily measurable indicators. The finite capacitance and ESR values result in a fluctuation in the output voltage that aligns with the switching frequency of the converter. *Equations 2 and 3* show that, all other variables held constant, the capacitance  $C$  and ESR  $R_c$  impact the output voltage ripple  $\Delta v_o$ .

$$\Delta v_o = \frac{v_o d}{R_c C f} \quad (2)$$

$$\Delta v_{o,ESR} = i_{Lf} R_c \quad (3)$$

These equations show that the voltage ripple ( $\Delta v_o$ ) is directly proportional to ESR and inversely proportional to capacitance. Applying the understanding of how capacitance decreases and ESR increases with time in AEC's, it follows that the magnitude of the voltage ripple will increase as the capacitor degrades. Eventually, the size of the ripple will cause the converter to fail to regulate the output voltage and/or damage itself. As such, it is critical to be able to monitor the health of the capacitors, and our proposed approach does so by analyzing the output voltage ripple.

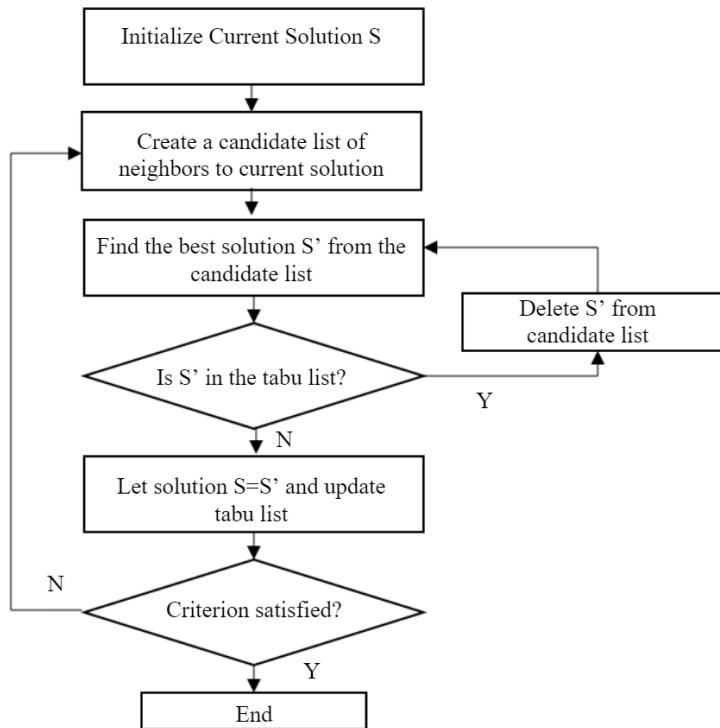
### 3.3 Comparison Methodology

Building on the understanding of the SUT and the properties of the AECs that will be evaluated, we will now explain the primary algorithm techniques that were explored for modeling capacitor health, with a specific emphasis on the algorithm that is recommended to be integrated into a future system: the Tabu Search Algorithm.

Evolutionary algorithms are procedures for finding the ‘best-fit’ solution to a problem using the idea of ‘survival of the fittest’ from biological evolution [4]. One particular Evolutionary Algorithm method that we investigated due to its successes in numerical optimization was the Differential Evolution model [4]. In Differential Evolution, three processes are applied to an initial population: mutation, crossover, and selection [19] to create new

populations. These populations are evaluated with a cost function that selects the population with the lowest cost [16].

The Tabu Search Algorithm is a method for combinatorial optimization that successfully overcomes the problem of getting stuck at a local maxima, that often occurs in other optimization algorithms [15]. It has been successfully used in a wide range of applications such as character recognition and neural networks [5]. Because it is a metaheuristic algorithm, it can also be combined with other algorithms to achieve successful implementation [5]. A flowchart of the Tabu Search Algorithm is shown in *Figure 9* below.



*Figure 9: Tabu Search Algorithm Flowchart [6]*

The preliminary information needed to implement the Tabu Search Algorithm was synthesized from [15], [6], and [5]. As is seen in *Figure 9*, the algorithm starts with an initial solution S, chosen within the range of the function. For our application, the initial solution would be the expected, or rated, value of the capacitor. Next, a list of steps of varying sizes is formed. These step sizes will be used to choose the neighbors of the initial solution that will be evaluated and compared. The steps vary in size to evaluate neighbors near and far from the initial solution. A fitness function is used to measure the success of each candidate. The best

solution  $S'$ , as determined by the fitness function, will then be checked against the Tabu List, which prevents the algorithm from getting stuck at a local maxima. If a potential solution exists in the Tabu list, its neighbors have already been evaluated, so it is deleted from the candidate list and the next-best candidate is chosen. Otherwise,  $S'$  will be added to the Tabu List and will replace the current value of  $S$ . The process will repeat for the new value of  $S$  and will continue looping until the stopping criterion is reached. The stopping criterion can be a set number of iterations or when the result of the fitness function is within a specified range.

Ultimately, the Tabu Search Algorithm is recommended for future integration into the proposed system because of its simplicity, ability to avoid becoming stuck at local maxima, and because the starting point is known. As previously mentioned, the initial solution is the original capacitance. Because of this, time would be saved compared to the Differential Evolution algorithm, in which the population is randomly initialized. That said, the Tabu Search Algorithm is only necessary for a large set of potential solutions. It saves the time that would be spent searching every potential solution in a Brute Force Algorithm, which is the algorithm implemented in the final tested system for this project.

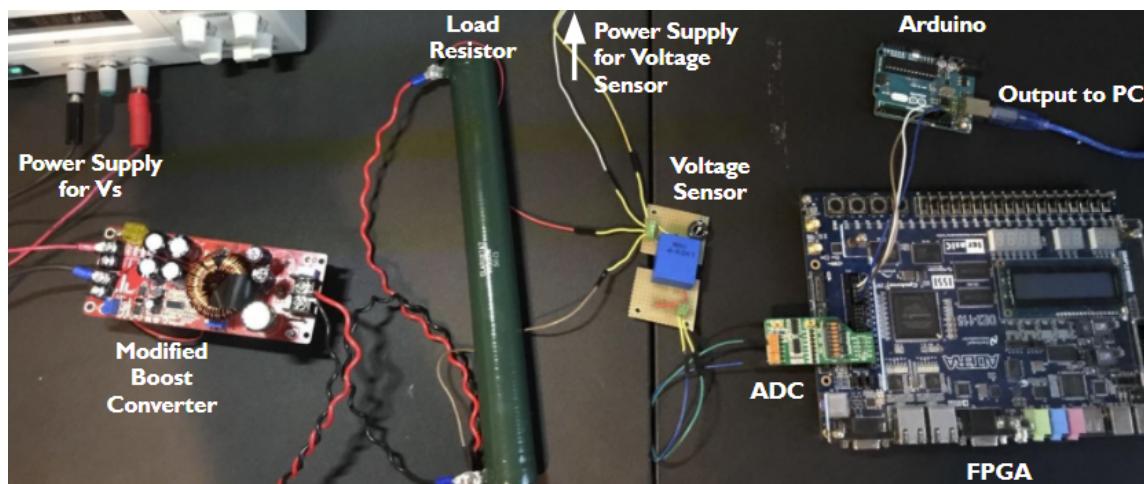
## 4. Solution Process

After reviewing previous research work done to predict capacitance failure and developing a theoretical understanding of our proposed system, we designed a capacitor-health monitoring system. Two potential solutions were considered, which will be detailed in the following section. Ultimately, Design 2 was implemented for this project. This section of the report details the two potential solutions, as well as the design process of the boost converter, Tabu Search Algorithm, and the data logging system to synthesize the system.

### 4.1 Possible System Setups

#### 4.1.1 Design 1

Design 1 is the system design that was initially proposed for this project. The system setup is shown in *Figure 10* with boost converter 1, a load resistor, a voltage sensor, an ADC, FPGA, and an Arduino (note, *Figure 10* is shown with the low frequency ADC connected, but the system design requires the high frequency ADC). This proposed system design would use the Tabu Search algorithm to compare experimental data to LTSpice simulations to determine capacitance and ESR. This design was abandoned, however, as we were unable to get the high frequency ADC working and would not be able to log a high enough resolution of the 110kHz voltage ripple signal and the LTSpice simulations were never accurate enough to yield satisfactory results.

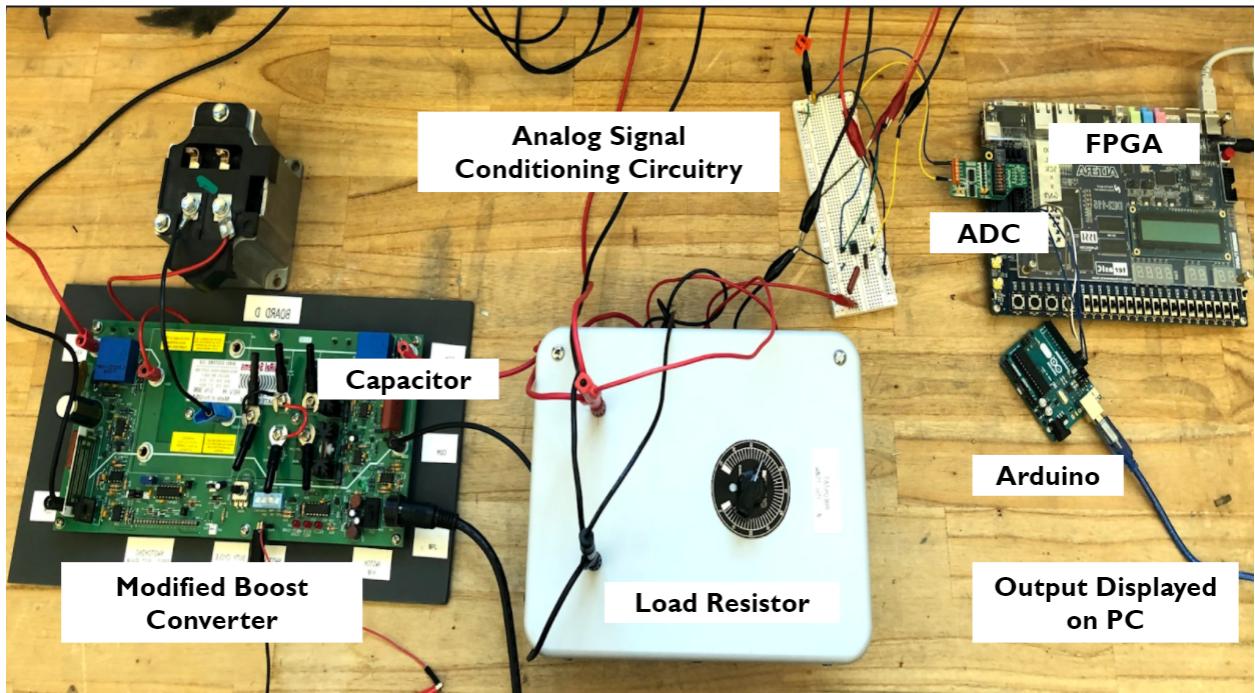


*Figure 10: Design 1 Setup*

#### 4.1.2 Design 2

Design 2 is the final system design that was modified from the initial project proposal.

The system setup is shown in *Figure 11* with boost converter 2, a load resistor, analog signal conditioning circuitry, an ADC, FPGA, and an Arduino. This system uses a Brute Force Algorithm implemented using RMS error between experimentally gathered “model data” and the collected data.



*Figure 11: Design 2 Setup*

#### 4.2 Boost Converter

##### 4.2.1 Boost Converter 1 (Purchased Board)

Design 1 involved using the boost converter purchased specifically for this project (shown in *Figure 12*).

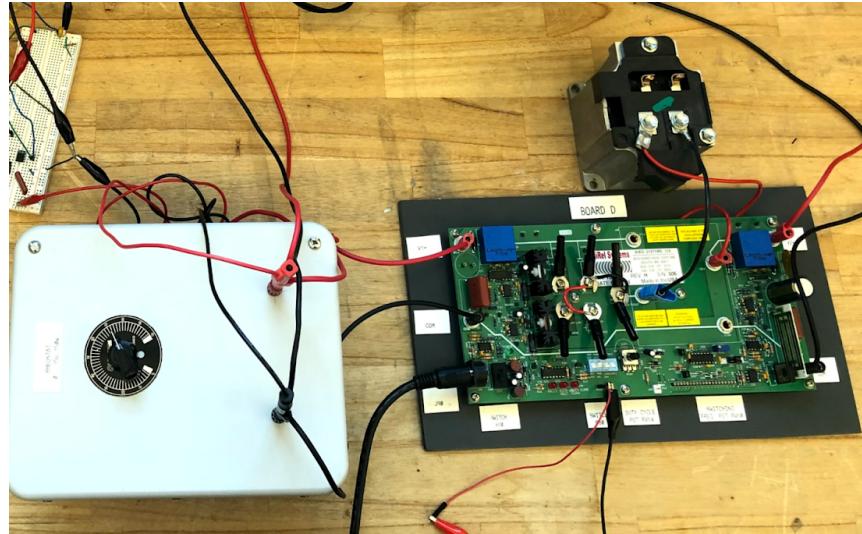


**Figure 12:** Boost Converter 1

In order to test the system and experimentally determine the output voltage ripple, we captured and analyzed the voltage ripple waveforms produced by various capacitors. To accommodate interchangeable capacitors, the original capacitors from the purchased boost converter were removed and pin receptacles were soldered in their place. During this modification, the inductor was also temporarily removed so the inductance could be measured for the LTSpice simulations.

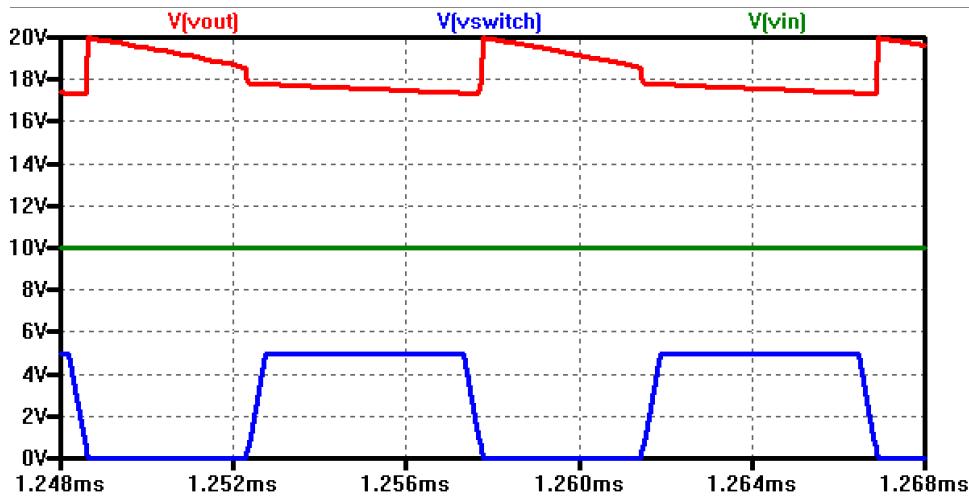
#### **4.2.2 Boost Converter 2 (ECE 493/593 Board)**

During the Spring semester, once it became apparent that we would not be able to get the high frequency ADC working, we looked for alternative options for systems to test. We decided that our best option, to minimize deviation from the initial system proposal, was to modify a boost converter from the power electronics lab and run it using an external pulse-width modulation signal slow enough to be accurately captured by the low frequency ADC. This boost converter, with the selected 370uH inductor and 25 Ohm load resistor, is shown in *Figure 13*.

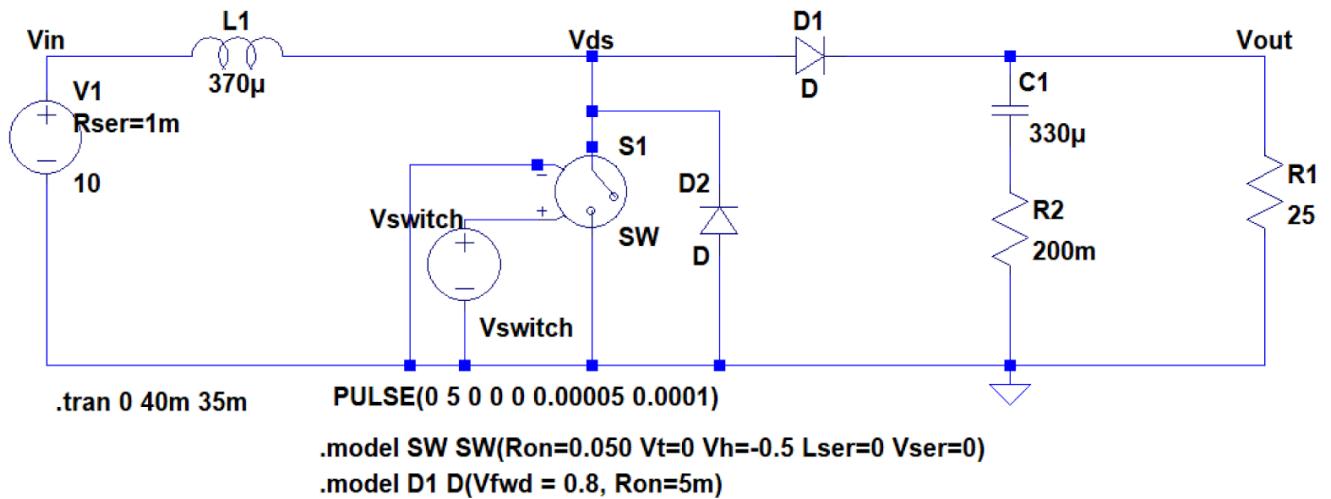


**Figure 13:** Boost Converter 2

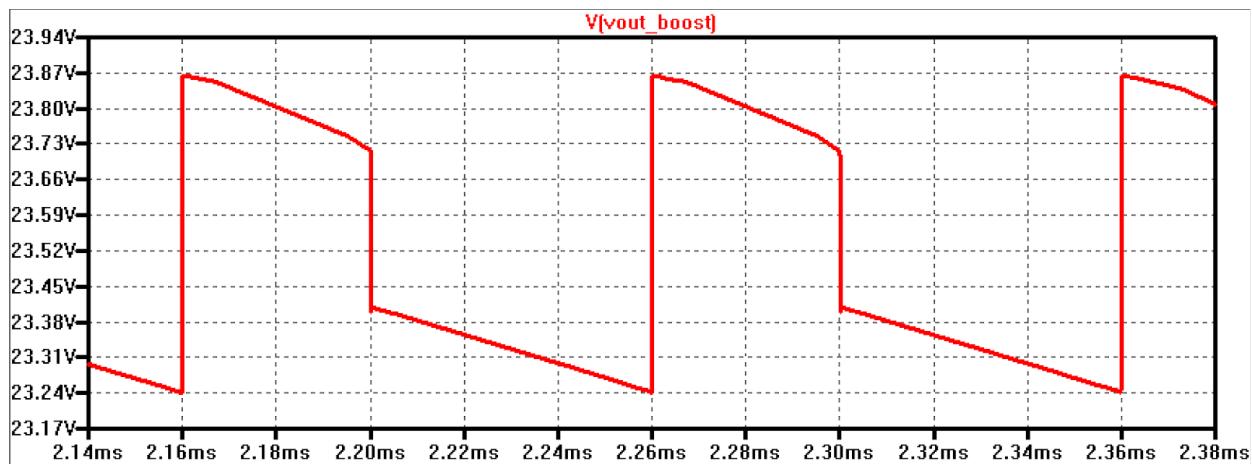
The simulation of this converter is shown in *Figures 14-17*. *Figures 14* and *15* are the simulation output and schematic for the converter without stray inductance and capacitance and *Figures 16* and *17* are the simulation output and schematic for the converter with stray inductance and capacitance. *Figure 17* is the final iteration of the LTSpice simulations for the boost converter. While the waveform was similar to the experimental output, it was not similar enough to yield accurate results when used in the waveform comparison algorithm, which is why the final design uses experimental data as the model data for comparison instead of simulated data.



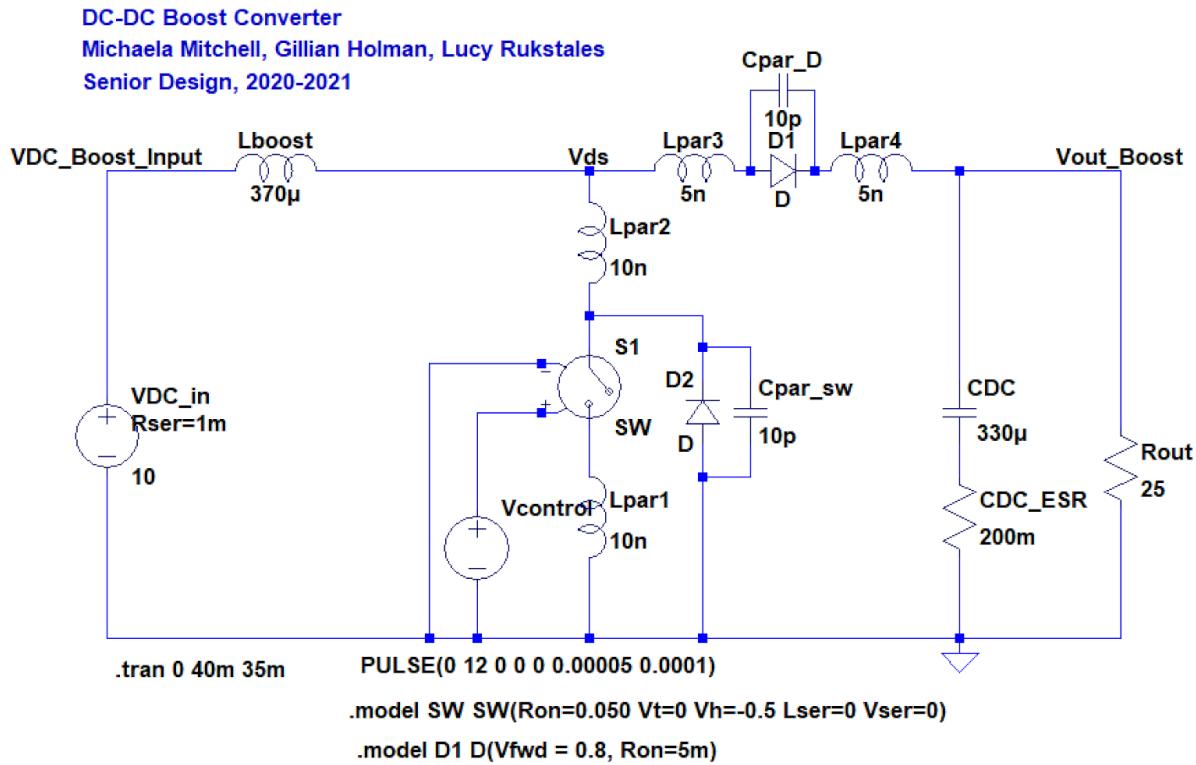
**Figure 14:** Simulation of Boost Converter 2 Without Parasitic Effects



*Figure 15: LTSpice Schematic of Boost Converter 2 Without Parasitic Effects*



*Figure 16: Simulation of Boost Converter 2 With Parasitic Effects*



**Figure 17:** LTSpice Schematic of Boost Converter 2 With Parasitic Effects

### 4.3 Algorithm

#### 4.3.1 Tabu Search Algorithm

Design 1 makes use of the Tabu Search Algorithm, which is necessary due to the large set of model data created by simulations. The Tabu Search Algorithm efficiently searches a large set of data for the desired solution without checking every piece of model data. The algorithm for Design 1 makes use of a fitness function that aligns the model and experimental waveforms using cross correlation before taking the RMS error between the two waveforms. Ultimately, the model waveform that resulted in the smallest RMS error is selected and used to determine the capacitance and ESR that produced the experimental waveform.

##### 4.3.1.1 Tabu Search Example

In order to better-understand the methods used for implementing the Tabu Search Algorithm, an attempt was first made to solve a simple example problem. The problem, from

Hu's "Tabu Search Method with Random Moves for Globally Optimal Designs" [15] was to find the absolute minimum of the function in Equation (4).

$$f_1(x) = 5 + \sin(x) + \sin\left(\frac{10x}{3}\right) + \ln(x) - 0.84x, \quad 2.7 \leq x \leq 7.5 \quad (4)$$

The first attempt was simulated in MATLAB, where the function is plotted in addition to each possible solution that was evaluated. Once the MATLAB simulation found the correct solution, it was then translated to C++. The initial solution was set to 2.7 (the low end of the domain) and a set of 10 step sizes ranging from 4.8 (the domain of the function) down to  $4.8 \times 10^{-9}$  was created. The number of steps was arbitrarily chosen and can be adjusted to fine-tune the algorithm. The stopping condition was chosen to be 14 iterations, which can also be adjusted to improve the accuracy of the algorithm. The algorithm successfully predicted the absolute minimum of the function over the interval: 0.3987 (see Appendix 9.1). While there are easier methods for finding the minimum value of a function, this problem was a good starting point for how to implement the Tabu Search Algorithm.

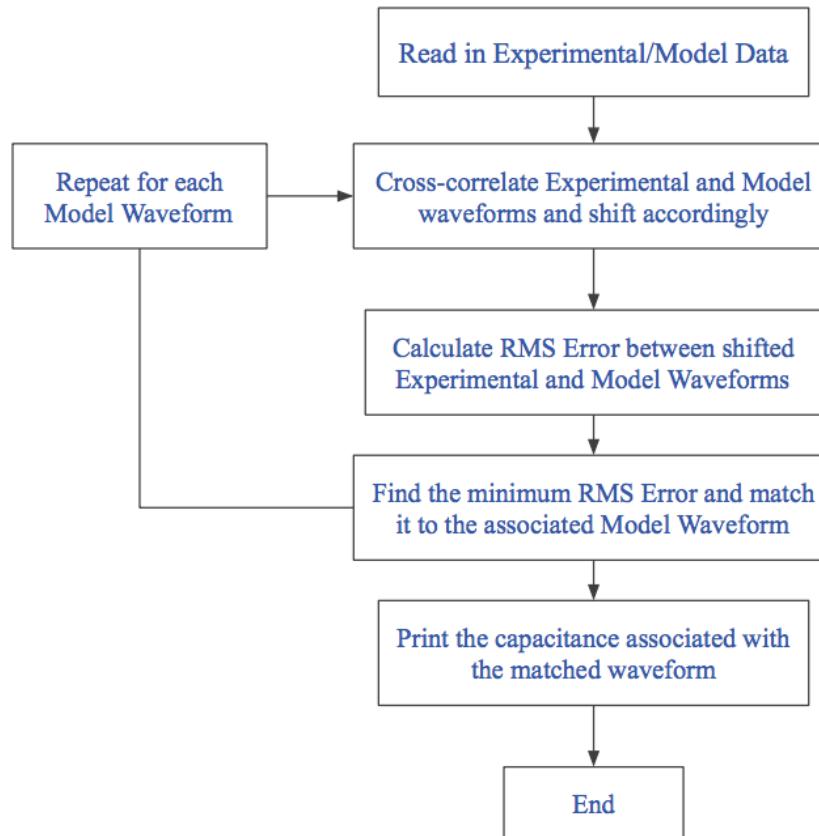
#### 4.3.1.2 Fitness Function

With a functioning outline of the Tabu Search Algorithm, a fitness function needed to be implemented that would effectively evaluate which model voltage ripple best-matches the experimental voltage ripple. This would then be used to determine the capacitance and ESR that produced the experimental voltage ripple. Before the signals can be compared for similarity, they first need to be time-shifted to align the peaks of each signal. A study on Waveform Similarity Analysis [10] demonstrates the use of cross-correlation as a method for aligning signals. This technique was used in the fitness function to first align the experimental voltage ripple with the model ripple it was being compared against. Then, the RMS-error of each point of the two waveforms was computed to quantify their similarity. The model waveform that resulted in the smallest RMS-error was selected as the best-matching waveform.

#### 4.3.2 Brute Force Algorithm

The model waveform data set for Design 2 is made using data collected directly from the SUT, resulting in a much smaller data set than if simulated waveforms were used. This negates the need for the Tabu Search Algorithm. Instead, a brute force algorithm was used, which

compares the experimental waveform to each model waveform. The same fitness function was used in this algorithm. The flowchart for the algorithm used in Design 2 is shown in *Figure 18*.



*Figure 18: Flowchart for Brute Force Algorithm*

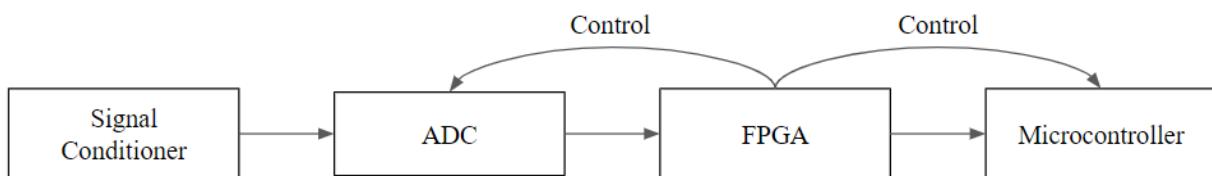
As can be seen in *Figure 18*, the experimental and model data are first read into the system. Then, for each model waveform, a cross-correlation is taken and each waveform is shifted accordingly to align the peaks. The RMS error between the shifted waveforms is then taken. Finally, the model waveform that resulted in the lowest RMS error is selected and the capacitance associated with this waveform is returned as the output capacitance of the boost converter.

It should be noted that the cross correlation piece of the algorithm cannot be used with the slow ADC because of the low resolution and limited number of sampling points. This portion of the algorithm was proven effective, however, when simulated data was compared to a CSV file from the oscilloscope. Therefore, the cross-correlation piece of the algorithm should be re-incorporated when higher-resolution data is available.

#### 4.4 Data Logger

When looking into the work done in [20], it was immediately observed that while running the system, much of the total time was spent collecting data from the system under test (SUT) before performing any analysis. Since this project's design setup would mirror the system used in [20], it was decided that investing time to develop a real-time data logger would be beneficial. In this project, the data logger acts as a bridge between the boost converter and the microcontroller, where the algorithm is performed.

Looking into the specifics of this data logger, four core components were needed, as seen in *Figure 19*. A signal conditioner would be used to scale the signal at the load output of the boost converter to a lower voltage range. This data would be sent to an Analog to Digital Converter (ADC), that would convert the analog data to a digital signal, so that it could easily be read in by an FPGA and stored in memory. This added memory component would allow large quantities of data to be collected, if needed. The FPGA would then forward the sampled data to the microcontroller (an Arduino) where the algorithm would be run. The purpose of placing the FPGA between the ADC and the microcontroller was to reduce the complexity of the microcontroller code; in addition, from our experience level, it is easier to work with closely timed processes on the FPGA, over the microcontroller.



*Figure 19: Data Logger*

##### 4.4.1 Signal Conditioner

When selecting the signal conditioner, two approaches were considered. The first approach was to select a sensor that would linearly scale the boost converter output with roughly a 6:1 scaling ratio. This approach would imply that the voltage ripple, which is only around 4 V<sub>DC</sub>, would be scaled to a relatively small value. Although this isn't inherently bad, an ADC would need to be selected with high precision to distinguish the ripple data. The LEM Voltage Transducer LV 25-P was provided, capable of operating in such a fashion. Testing was

attempted with this sensor, though it was discovered that the sensor's bandwidth was too low to work at the switching frequency of the boost converter in Design 1, that being 110 kHz.

Additionally, this sensor proved to be difficult to work with, so it was not considered for Design 2.

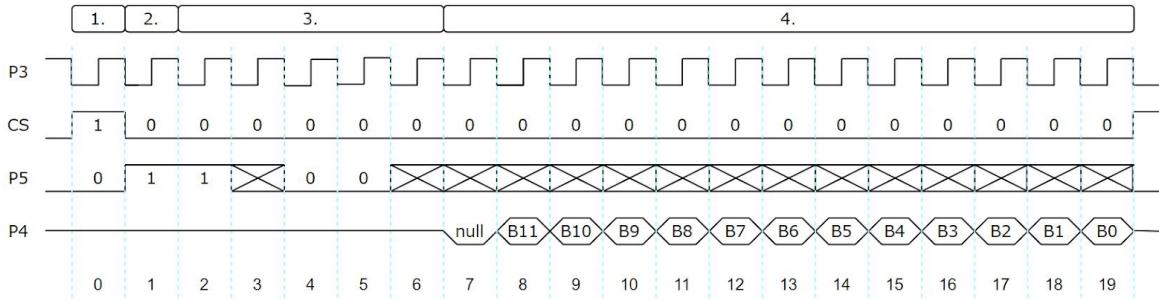
The second approach was to use a passive high-pass filter to remove the DC component of the boost converter output. In theory, this approach requires less hardware circuitry and no external power supply, and would minimally affect the voltage ripple, as no scaling would occur. When attempting to implement this circuitry, it was recommended to incorporate a non-inverting summing amplifier to scale and shift the waveform, and a low-pass filter to remove excess ringing. This signal conditioning circuitry was successful and is now included as a part of Design 2.

#### 4.4.2 Analog to Digital Converter

To translate the data from the sensor to the FPGA, an ADC was selected. When initially selecting this ADC, it was simply stated that the faster the sampling frequency and the greater the precision, the better. Given that the switching frequency of the purchased boost converter for Design 1 is 110 kHz, the Nyquist Theorem places the minimum ADC sampling frequency at 220 kHz, given by Equation (5).

$$f_{sampling} = 2f_{signal} = 2(110 \text{ kHz}) = 220 \text{ kHz} \quad (5)$$

In addition to the minimum sampling frequency of 220 kHz, it was opted to look for an ADC with a precision of 12 bits (arbitrarily decided). When searching online, it was quickly noted that there weren't many high frequency ADC's that were relatively simple to implement, at a low cost. Before investing in a high frequency ADC, a low frequency option was purchased, that being the MIKROE-340 ADC. Working with this ADC, a module was created in Verilog (see Appendix 9.3) to sample 12-bits at a time. To do this, an SPI protocol was used, allowing control to flow between the parent (FPGA) and child (ADC). The control flow can be seen in *Figure 20*, where P3 is a 2 MHz clock (20 cycles in each 100 kHz sample), CS is chip select, P5 is controlled from the FPGA, and P4 is the data line from the ADC.

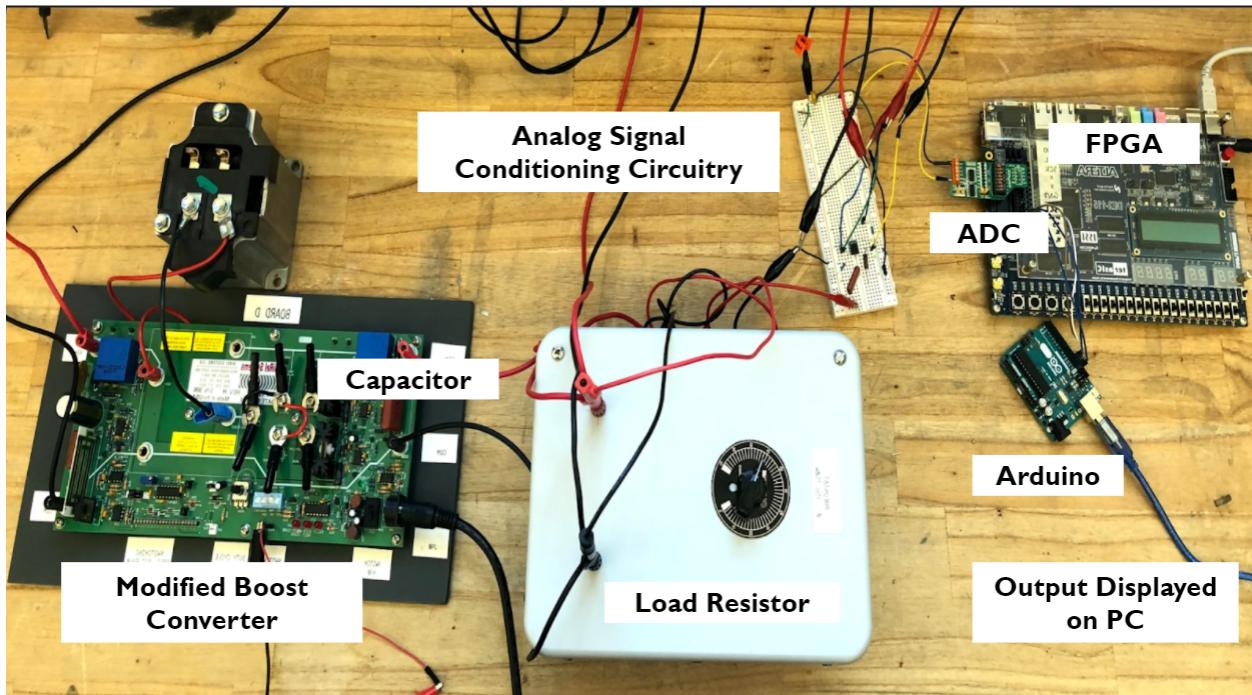


**Figure 20:** SPI interface for low frequency ADC

With the low frequency ADC operating as desired, DC1563A-A was selected to be the high frequency ADC, to work over the 220 kHz sampling minimum for Design 1 [18-C, 13]. With control logic similar to that of the low frequency ADC, it was assumed that the high frequency ADC could be interfaced easily. Unfortunately, trying to operate this ADC was more difficult than expected. Several board modifications were made to try to simplify how signals would be routed to the ADC on the DC1563A-A board. After having great difficulties trying to get the high frequency to work using the FPGA, research was done to try to find a fully written code online. A code was found to operate the DC1563A-A board, using a device similar to an Arduino, called a Linduino [2]. Although the code was intended for the Linduino, it was capable of operating the unmodified high frequency, but only at low frequencies. Due to a lack of time, the Linduino code was discarded as an option, as it was operating at a slower rate than the low frequency ADC. Ultimately, the low frequency ADC was selected for use in Design 2.

## 5. Final Results

Now that the purpose, background information, and approach taken for the solution have been explored, we will explain the results that have been obtained so far. Specifically, this section will discuss the modifications that were made to the purchased boost converter and how these modifications will be beneficial, the current state of the data logging system, and the initial results obtained from the fitness function. For reference, *Figure 21* displays the current test setup.



*Figure 21: Final Experimental Test Setup*

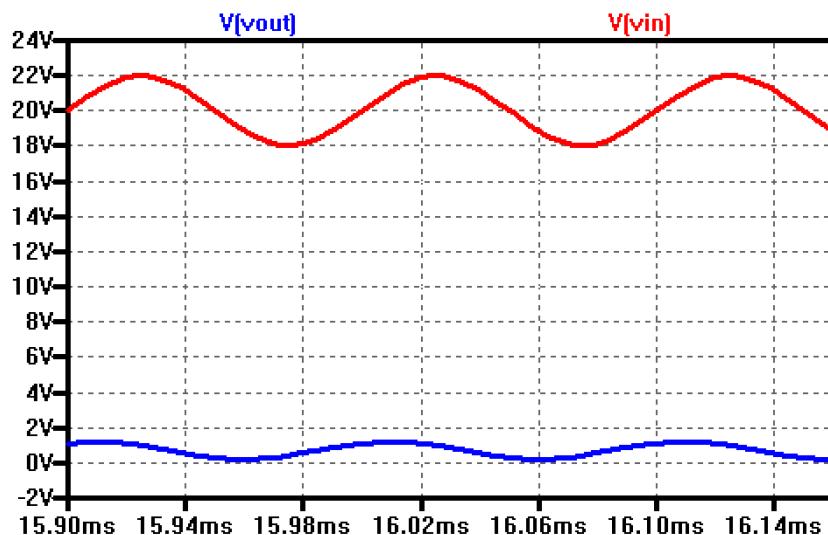
### 5.1 Boost Converter

Boost converter 2, the converter used for the final system, was modified to work with a lower switching frequency and to allow for easy capacitor alterations. We replaced the 106uH inductor with a 370uH inductor and replaced the capacitor with pin receptacles so we could easily test the system with different capacitors.

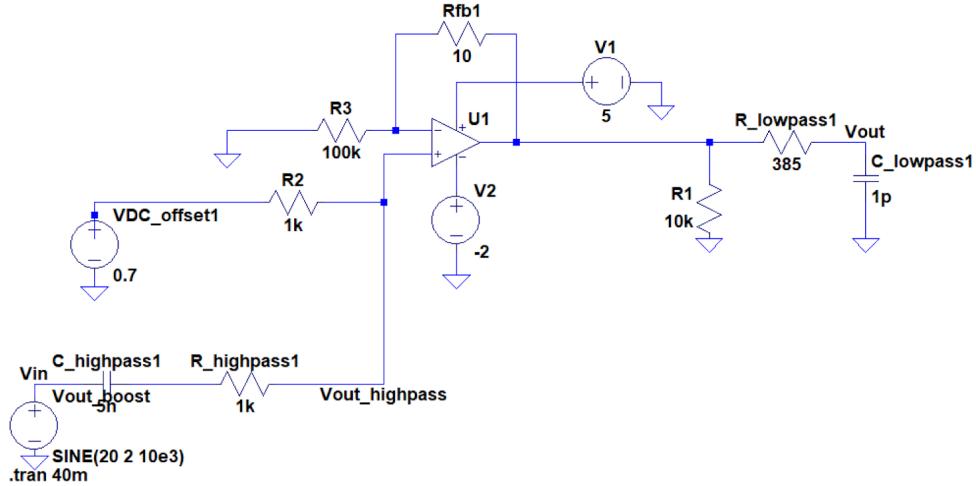
### 5.3 Data Logging System

A data logging system was successfully implemented to read conditioned data from the Boost Converter, to be used by the algorithm on the microcontroller. The current setup works with 34 12-bit samples. These samples are collected by the MIKROE-340 ADC at a rate of 100 kHz. Since the boost converter is operating at a switching frequency of 10 kHz, 10 samples are being collected from each period of the boost converters voltage ripple. These samples are sent from the ADC to the FPGA, upon toggling one of the switches on the FPGA DE2-115 demo board, and are temporarily stored in memory. Once all of the samples have been collected by the FPGA, they are immediately sent to the Arduino. The communication between the ADC and the FPGA, and the FPGA and the Arduino is all performed using common SPI protocols.

The input limitations of the ADC required us to design an analog circuit to condition the output of the boost converter. The input voltage range for the ADC is 0-5 V, and we experimentally determined that the maximum voltage ripple output from the ADC could reach 4 Volts peak-to-peak with an average DC output of 18-19 Volts. The first part of our designed analog signal conditioning circuitry is a high pass filter to remove the DC component of the signal. The AC ripple is then fed into a non inverting summing amplifier that halves the signal magnitude and shifts the signal up to a DC average value of 0.7 V. The output of the op-amp is then fed into a low pass filter to filter out noise and high-frequency ringing. A schematic of this system and the simulation output are shown in *Figures 22 and 23*.



*Figure 22: Simulation Output for Analog Signal Conditioning*



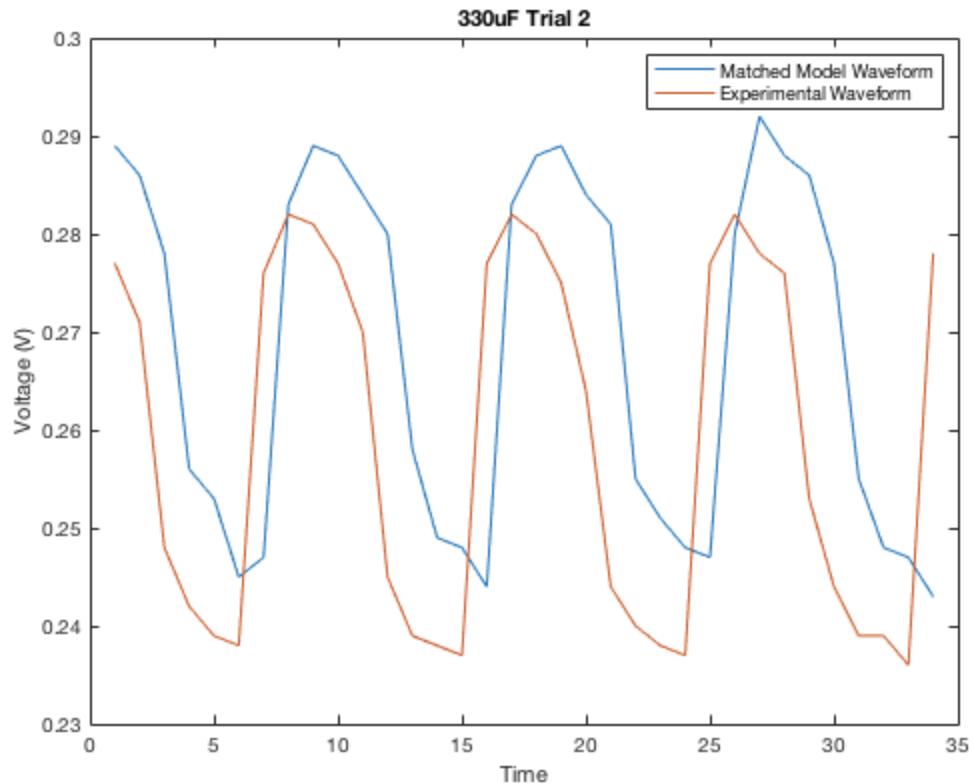
**Figure 23:** LTSpice Schematic for Analog Signal Conditioning

#### 5.4 Algorithm

As was discussed in Section 4, this implementation of the project does not require use of the Tabu Search Algorithm, due to the small number of model waveforms. Instead, a brute force algorithm was used in combination with the fitness function that was developed for comparing waveforms. The final implementation of this algorithm was made in C++ and can be found in Appendix 9.2.2. The algorithm correctly predicted 14/18 capacitances correctly, for an overall accuracy of 78%. The results of this system test are shown in *Table 1* below, with the percent error for each trial. Additionally, *Figure 24* shows one of the experimental waveforms in orange with the matched model waveform in blue. The goal is for the algorithm to predict capacitance with 20 % accuracy, as this is the indicator for device failure. 14/18 capacitances were correctly matched and this number could likely be increased for a larger set of model data.

**Table 1:** Results of Fitness Function Test

		Expected Capacitance					
		330uF	560uF	680uF	820uF	1000uF	2200uF
Predicted Capacitance	330uF	X X					
	560uF		X X	X			
	680uF			X X			
	820uF				X X X X		
	1000uF					X X	
	2200uF						X X X

**Figure 24:** Example of Results Algorithm

## 6. Future Work

Having explained the two solutions pursued in this project, and the final results of the selected design, we will now discuss the items that may be addressed or reconsidered in future project development. The plans for each of these items will improve upon their current functionality and will allow each piece to come together into a single embedded system.

In the data logging system, work with the high frequency ADC should be resumed. Whether using the Arduino or the FPGA to operate the ADC, using the high frequency ADC will allow greater precision in data collection, which will in turn improve the accuracy of the algorithm and/or allow for an increase in the switching frequency of the boost converter.

Currently, only the Brute Force Algorithm is used to compare the captured data to experimental “golden model” data. To improve system accuracy, either more model data should be gathered experimentally or the LTSpice simulations should be fine-tuned to make the simulation waveforms more accurately match the experimental data. Having a larger data set, either of experimental or simulated data, will then require the Tabu Search Algorithm to be integrated into the system.

Potential alternatives for comparing the waveforms could also be explored. Two options are to find a replacement comparison method for the RMS-error and/or to observe a different characteristic of the system for comparison. Finally, the C++ code should be implemented directly on the Arduino, so the system can be fully embedded and operate online, instead of transferring the captured data and processing it offline on a PC.

A robust, low-cost, fully embedded system that effectively predicts capacitor failure can be achieved if the work achieved in this project is improved upon by increasing the resolution of the data logging system, gathering a larger set of data for comparison, optimizing the waveform comparison algorithm, and embedding the algorithm into the microcontroller.

## 7. Discussion

### 7.1 Design Justification

As was described above, we had four main design decisions to make: the system under test (SUT), how to collect and store data from the SUT, the characteristics to observe for device failure, and how to analyze the data. A boost converter was chosen for the SUT because of its simplicity and its wide use in Power Electronics. A low-frequency ADC was selected, with a recommendation to replace it with a high-frequency ADC in future work. Due to unforeseen issues with the high-frequency ADC, it could not be incorporated into this version of the solution. The high frequency ADC will allow for a higher sampling frequency and greater precision. Capacitance (C) and equivalent series resistance (ESR) were chosen as indicators of failure because there is a distinct cut-off value: a 20% reduction in C or double the ESR. Lastly, the Brute force algorithm was chosen because the small number of model waveforms allowed the entire solution space to be efficiently searched, without the need of a more-advanced algorithm. The Tabu Search algorithm is the recommended algorithm for future modifications because of its simple implementation, ability to avoid getting stuck at local maxima, and the known starting point.

### 7.2 Ethical Considerations

As was demonstrated by the examples in Section 2, capacitor failure poses risks to the reliability and safety of a system. While a system that can predict device failure can be useful, it is important to consider the ethical concerns of such a system, if implemented. For example, people may become overly-reliant on the system and fail to perform other important maintenance inspections. Additionally, it is important to note that our design is simply a proof of concept and should not be implemented or relied upon without significant testing, review, and modifications.

### 7.3 Other Lessons Learned

Throughout the past two semesters, our team not only learned technical skills related to boost converter operation, signal conditioning, algorithms, and programming ADCs, but also gained an appreciation for the need to continue learning. Going into this project, we incorrectly thought that we would have much of the information that would be needed for successful completion of the project. Instead, several weeks were spent gaining the background knowledge

required to choose a design alternative and make a plan. The skills we gained in how to find needed information are arguably more important than the technical knowledge acquired.

## 8. Conclusions

Aluminum electrolytic capacitors are a prominent cause of device failure in power electronics systems. While there have been capacitor health-monitoring systems implemented in industry, there is room for improvements such as lower complexity and cost.

In this project, we have conducted a literature review of previous work done in academia and at Miami University to solve this problem. We also developed the theoretical basis for analyzing the output voltage ripple of a boost converter to determine capacitance and equivalent series resistance values for DC-link aluminum electrolytic capacitors to predict device failure. Signal-conditioning circuitry was successfully implemented to safely pass the output voltage ripple through the ADC. Additionally, the data-logging system was proven as an effective method for sample collection. Finally, an algorithm was developed that can be used to predict device failure.

While improvements could be made to increase the accuracy and complexity of the system and to make the system fully-embedded, significant progress has been made and the groundwork for future development has been laid. The current system achieves a 78% accuracy. It is believed that this accuracy can be improved with modifications to the data logging system and means of producing model data. A boost converter simulation was developed with the ability to instantly generate a large number of model waveforms. Improvements to this simulation will allow for a more robust system, as the number of waveforms for comparison would be increased. Lastly, a Tabu Search Algorithm is ready for integration with the data logging system when the model waveform data set is larger. It is believed that the system will be even more effective if the high-frequency ADC, simulation, and Tabu Search Algorithm can be integrated into a single embedded system. This project successfully provided the foundation for such a system.

## 9. Appendix

### 9.1 Tabu Search Algorithm Example

[9.1.1 C++ Tabu Search Algorithm](#)

[9.1.2 MATLAB Tabu Search Algorithm](#)

### 9.2 Final Fitness Function Codes

[9.2.1 MATLAB Final Fitness Function](#)

[9.2.2 C++ Fitness Function](#)

### 9.3 Data Logger

[9.3.1 Top Module](#)

[9.3.2 ADC Read](#)

[9.3.3 Arduino Write](#)

[9.3.4 Arduino Read](#)

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