



## **Virtual Twinning to Analyze and Predict Circuit Failure**

**College of Engineering and Computing  
Department of Electrical and Computer Engineering**

**ECE 448  
Senior Design - Final Report**

**Advisors: Dr. Jamieson and Dr. Scott**

**Authors: Alecea Grosjean, Ethan Barnes, and Jimmy Roach**

**Dec 4, 2023**

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## Introduction

Technology is ingrained in nearly every aspect of our lives. Though it may increase efficiency and reduce human error, the reality is that technology is fallible. Consequences of failed electronics can range from mild financial and temporal inconveniences to the extremes of injuries or loss of life. Ethical engineering practices call for designs to reflect a concern for human safety [1]. Additionally, it's often in the best interest of companies to quickly detect and replace failing hardware to mitigate financial losses from extensive equipment downtimes. These are the motivations for our virtual twinning project.

The goal of our project is to establish a relatively inexpensive condition monitoring method to analyze the similarity between specific measured waveforms of a given power electronic circuit to the simulated waveform of a circuit's "virtual twin" to quantifiably identify circuit failure within a given level of accuracy and with sufficient speed to recognize and replace a component before extensive damage occurs.

Our report begins with a discussion of previous findings in this field, followed by a section highlighting our research and developed theories. We then explain the experimental steps taken using a buck converter circuit as a case study, beginning with building a mathematical model of the circuit's functionality, followed by an explanation of the simulated representation of the circuit using Matlab, and the processed results of the physical circuit. The report concludes with an analysis of our results and details what advancements we plan to make in the future.

## Project Background

Power electronic circuits are vital elements in industries including industrial automation, transportation, telecommunications, and power transmission. Due to their growing integration into systems, there has been much research into ensuring their health and examining their performance through a process known as condition monitoring.

Current condition monitoring methods can be sorted into three different types: degradation indicators monitoring, aging-based modeling, and software-based methods [2]. Degradation indicators monitoring and aging-based modeling consist of utilizing hardware solutions such as sensors. This type of hardware can be expensive and has its own need for maintenance and replacement after failure. This is why modern approaches often seek to fall into the third category of software-based solutions which include the virtual twin approach we utilize in our project.

Though modern condition monitoring for power converter systems can range in methods, the literature is consistent in the identification of capacitors and semiconductors as key devices to monitor for failure [2,3,4]. Failure often occurs in these components due to their sensitivity to transient overvoltages or extreme temperatures [6]. Due to the more simplistic passive nature of the capacitor and our more established collective knowledge, we selected this as the component of focus for our research. Additionally, the literature indicates that degradation indicators for

 Electrolytic capacitors consist of capacitance and a capacitor's equivalent series resistance (ESR), as these impact the shape and amplitude of the capacitor's ripple voltage.

 The combination of this established knowledge in the literature led us to research the development of a software-based condition monitoring system for a buck-converter circuit to predict circuit failure by comparing the experimental performance of the capacitor's ripple voltage to its virtual twin values represented by the mathematical model in [4]. In the following sections, we will develop a theory for virtual twin condition monitoring that has a balance of being simple, scalable, and inexpensive.

## Project Research

Research for implementing this process falls into three main categories: understanding the selected power electronic circuit topology, implementation of a virtual twin or mathematical model of the circuit, and the process for accurately identifying whether the circuit operates without failure. We expand on our understanding of each of these concepts in the following sections with an additional section detailing any assumptions made in our report.

### Buck Converter Circuitry

In power electronics, buck converters are considered one of the simplest power electronic circuits that contain a capacitor component whose behavior can be studied. Additionally, it contains similar components to other commonly utilized power electronic circuits such as boost converters and buck-boost converters which means our research is scalable.

DC-DC Buck converter circuits are also known as step-down converters ~~for their design to reduce an input DC voltage to a consistent lower DC voltage output~~. The topology of a buck converter circuit can be seen below in Figure 1.

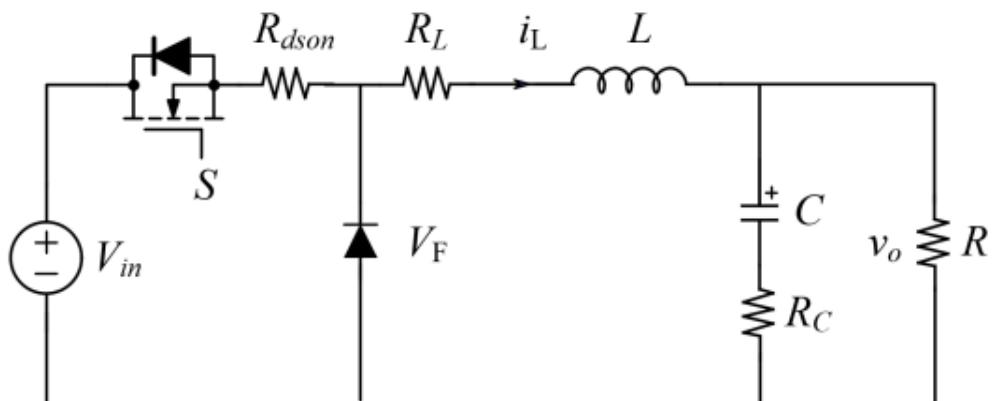


Fig. 1: Buck Converter Circuit Topology

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In this paper, parameters of the buck converter ~~circuit~~ will be represented as follows 

$V_{in}$  is the input DC voltage value of the buck converter circuit,  $S$  is the switching state of the power

semiconductor device (1 represents an “on” state, 0 represents an “off” state),  $R_{dson}$  is the internal resistance of the semiconductor device when it is on,  $V_F$  is the forward voltage of the diode,  $R_L$  is the internal resistance of the inductor ~~with~~ inductance  $L$ ,  $R_C$  is the equivalent series resistance of the capacitor of capacitance  $C$ , and  $R$  is the resistance of the load resistor in parallel with the capacitor ~~(why)~~ we will be focusing on during this report.

The behavior of the circuit’s output ~~is dependent~~ on the values of the parameters above in addition to the duty cycle for the pulse width modulation operation in the circuit. The duty cycle, ~~D~~, represents the ratio of the amount of time the switch is on to the total time of one period of the switching operation. It determines the percentage of the input voltage that will be output by the circuit ~~as seen below in Equation 1.~~

$$V_{out} = D \times V_{in} \text{ for } D = \frac{t_{son}}{T_s}. \quad (1)$$

~~Equation 1: Duty Cycle Effect on Buck Converter Operation~~

Treat equations as text. Include proper punctuation.

Pulse width modulation (PWM) is the technical term for this voltage regulation method using the duty cycle. Under this operation, the buck converter has two states in which it performs: the “on” state and the “off” state. During the “ON” state the circuit appears as seen below in Figure 2. The switch is closed and the input voltage flows through the inductor to reach both the capacitor and load resistor,  $R$ . ~~The diode in this instance~~ is reverse-biased and acts as an inductor which allows the current to charge the capacitor,  $C$ .

These two sections are a bit confusing. PWM is described in the first paragraph and defined in the second. Please rearrange the paragraphs.

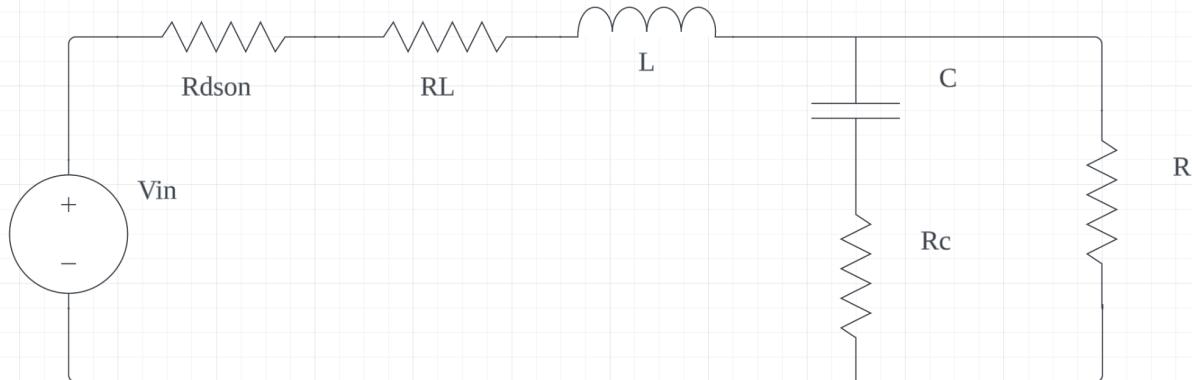


Fig. 2: Buck Converter “ON” State

Be more descriptive with you labels.

During the “OFF” state seen in Figure 3, the switch is opened and the input voltage is no longer provided to the circuit. At this time, the inductor releases its stored energy forcing current to flow through the load resistor and through the diode which is now in forward-bias mode. The

capacitor begins to discharge and provides additional current to the load resistor. ~~This explanation summarizes the operation of a buck converter, but additional details can be found in [6].~~

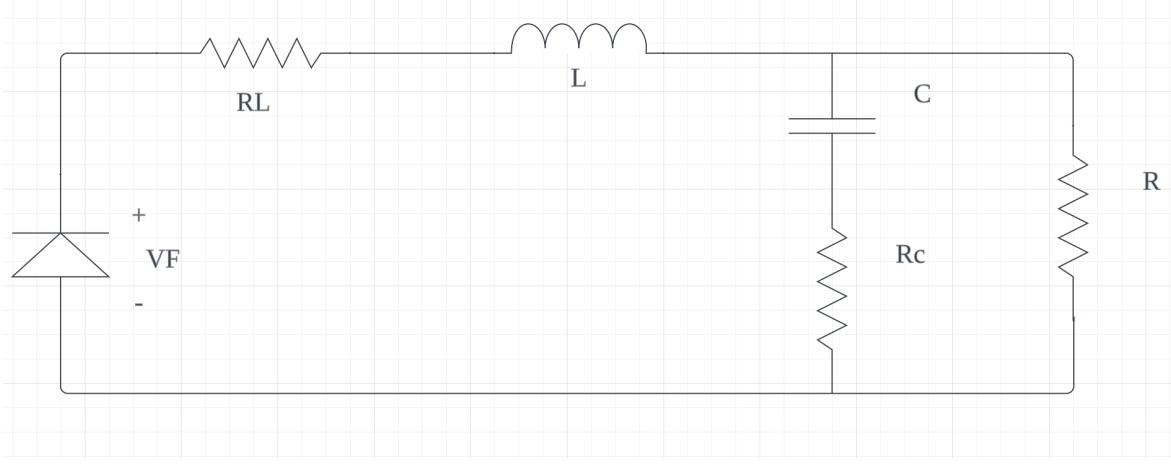


Fig. 3: Buck Converter “OFF” State

With an understanding of how the circuit operates, we noted key values of the current operation of the circuit and exported data into a CSV file to take the next step of modeling an accurate digital twin. Measurements ~~of some important values in our circuit can be found below~~ in Table 1.

Table 1: Physical Buck Converter Values

Component	$V_{in}$	$f_{sw}$	$D$	$V_{out}$
Value	24 V	50 kHz	0.5	11.4 V

## Virtual Twin

The conceptual goal of a virtual twin is to replicate the performance of a physical system through simulation. To predict circuit failure, we needed a baseline for the ideal operation of the circuit to compare the sampled circuit data with. For this reason, we needed a reasonably accurate mathematical model of a buck converter ~~circuit~~ using PWM voltage regulation. During the process of making our digital twin, we learned that it's essential to model the PWM aspect of the circuit. Without the PWM switching frequency, the results would be an “averaged model” and the output ripple we want to analyze ~~could~~ not be seen. To accurately model a buck converter ~~circuit~~, the state space representation from [4] is utilized. ~~The equations can be seen below in Equation 2.~~

$$\begin{bmatrix} \frac{diL}{dt} \\ \frac{dvC}{dt} \\ v_o \end{bmatrix} = \begin{bmatrix} -\left(\frac{A}{L}\right) & -\frac{1}{L}\left(\frac{R}{R_c + R}\right) \\ \frac{1}{C}\left(\frac{R}{R_c + R}\right) & \frac{1}{C}\left(\frac{1}{R_c + R}\right) \\ \left(\frac{R_c R}{R_c + R}\right) & \left(\frac{R}{R_c + R}\right) \end{bmatrix} \times \begin{bmatrix} iL \\ vC \end{bmatrix} + S \begin{bmatrix} \frac{v_{in}}{L} \\ 0 \\ 0 \end{bmatrix} + (1 - S) \begin{bmatrix} \frac{-V_F}{L} \\ 0 \\ 0 \end{bmatrix} \quad (2)$$

for  $A = (S \cdot R_{dson} + RL + (RC R)/(RC + R))$

~~Equation 2: State Space Equations for a Buck Converter~~

Due to the frequent need for matrix mathematical operation, we found it easiest to build a digital model in Matlab, which could later be transferred to other programming languages as needed. A link to our GitHub page with the created code can be found at the end of this report in the Appendix.

The parameter values for ideal operation conditions utilized in our virtual twin were selected based on the certain values we set in our physical circuit seen in Table 1 as well as datasheet information for components. The final variable values utilized in the simulation are listed below in Table 2.

Table 2: Digital Twin Buck Converter Variable Values

Variable	$V_{in}$	$R_{dson}$	$R_L$	L	C	$R_C$	$V_F$	R	$f_{sw}$	D
Value	24 V	0.1 Ω	0.2 Ω	0.001 H	680 μF	0.1366 Ω	0.7 V	10.9 Ω	50 kHz	0.5

The simulation developed was modeled for 0.1 second and the rate of the simulated data was established to be 10 ns as this is the sampling rate of the MSO4034 oscilloscope utilized to collect and store data from the physical circuit. An array representing the time values of each data point was established using the runtime and time step. The values of this time array were utilized in the conditional statement in Equation 3 to create a logical array that modeled the switch state (1 for “on”, 0 for “off”) for each recorded moment in time given the switching period ( $T_{sw}$ ) and the duty cycle.

I do not know what this is. Is it the modulo operator?

$$t \% T_{sw} > T_{sw} * \text{Duty Cycle}$$

~~Equation 3: Logical Expression to Identify Switching State at Time t~~

After these arrays were established, empty arrays were created to store the results of the simulation and a for loop was constructed to calculate the values of the state variables at each time step. In each iteration of the loop, the established parameters and state of the switch in the current point of time in the simulation are entered into the state space equations to generate the change of inductor current and capacitor voltage over the time step as well as the output voltage across the load resistor. These values are used to generate the actual inductor current and capacitor voltage values at each time step and added to the previous iteration value to construct a simulation of the output voltage at each time. At the end of the loop, an array of the simulated output voltage values is created. Each of these steps can be seen below in Figure 4.

```

28 %% Circuit analysis
29 % The S array represents the state of the switch at each point in time
30 vals = zeros([3 size(S,2)]);
31 vo = zeros([1 size(S,2)]);
32
33 for itr = 1:size(S,2)
34     % switch independent component of State Space Equations
35     A = S(itr).*Rdson + RL + RC*R/(RC + R);
36     Se = [-A./L (-1/L*(R/(RC+R)));
37             (1/C*(R/(RC+R))) -(1/C*(1/(RC+R)));
38             (RC*R/(RC+R)) R/(RC+R)];
39
40     % switch dependent components of State Space Equations
41     Son = S(itr).*[vin/L;0;0];
42     Soff = (1-S(itr)).*[-VF/L;0;0];
43
44     % Store delta in vals and Calculate Change
45     vals = Se*[iL;vC] + Son + Soff;
46     iL = Tstep*vals(1) + iL;
47     vC = Tstep*vals(2) + vC;
48     vo(itr) = vals(3);
49 end

```

Fig. 4: MATLAB Code for State Space Equation Buck Converter Model

This approach was selected since it enabled us to specialize the simulation results to more accurately reflect this circuit, unlike other approaches that model a wide variety of circuits in programs like LTSpice where we produced less accurate results. It is important to note that this process is still scalable for other power converters and is suggested for complex linear time-invariant systems. Analysis between our real and simulated data is explained below in the Final Results section of this report.

## Signal Processing Circuit

Figure 5 shows the results of the output signal of the buck converter that we plan to sample as measured by our MSO4034 oscilloscope. The large DC offset in combination with the low voltage ripple of approximately 150 mV makes it difficult to inexpensively sample the signal

I do not agree with this statement. What is expensive? Your setup is inexpensive relative to an oscilloscope and it measures the signal. Also, what does a single product?

with a single product. To make the sampling process easier we constructed a circuit containing a high pass filter and amplifier to first process the data before sending it to an ADC sampling circuit.

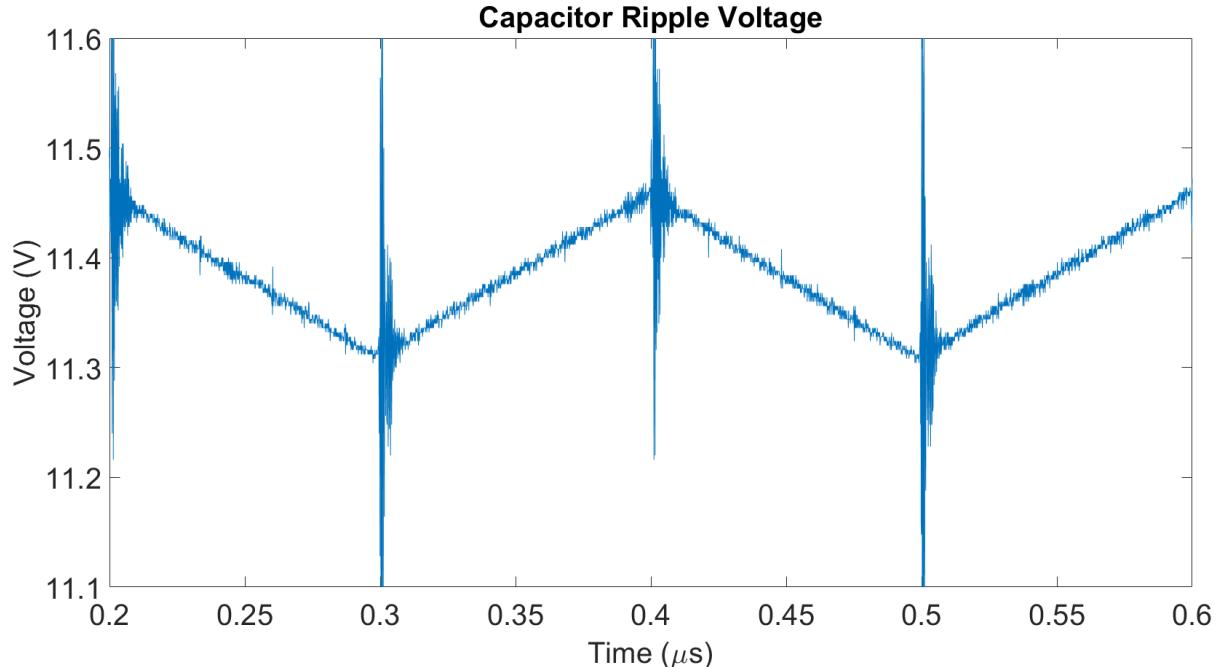


Fig. 5: MATLAB plot of the voltage across the buck converter output at steady state.

Our selected process of capacitor degradation identification, further discussed in the final results section of the report, is only reliant on the shape and magnitude of the voltage ripple, which means the DC offset can be eliminated using a high pass filter. This is done with a  $1\text{PF}$  capacitor and a  $10\text{k}\Omega$  resistor, yielding a cutoff frequency of  $800\text{Hz}$ . Now that the ripple has been separated, the signal ranges between  $\pm 75\text{mV}$ . A  $40\%$  increase in the ESR of the capacitor would cause the peaks to increase by about  $50\text{mV}$ . As changes on the order of a few millivolts are susceptible to noise, we concluded that the signal needed to first be amplified. Our amplifier of choice is the  $\text{OP}620$  IA instrumentation amplifier. It is built specifically for amplifying  $\text{mV}$  or  $\mu\text{V}$  AC inputs, and it has a  $120\text{Hz}$  bandwidth (a potential alternative for a  $120\text{kHz}$  system is the LTC6244). The successful circuit setup for our high pass amplifier circuit as well as the resulting amplified signal is shown in Figure 6.

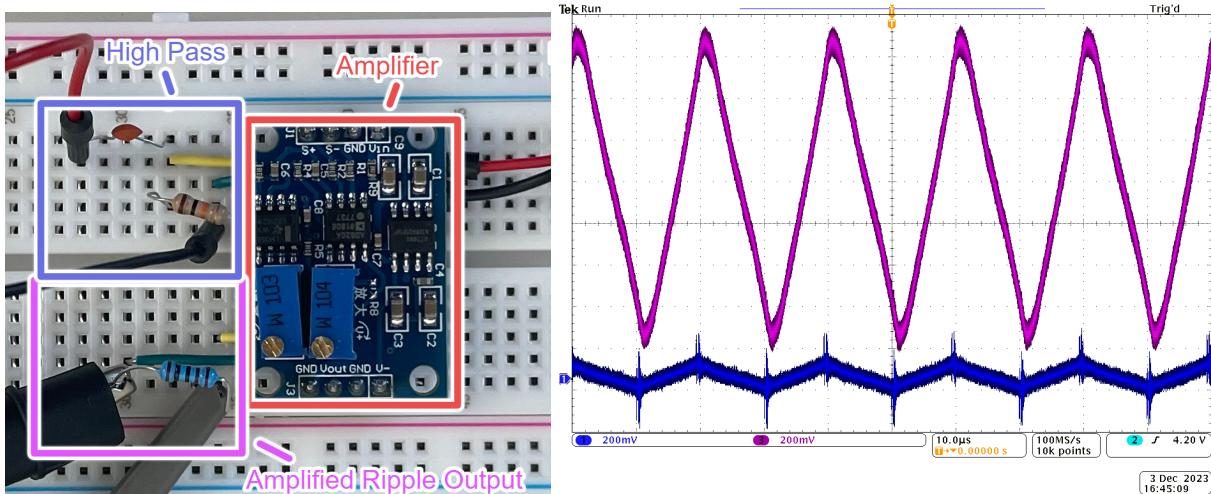


Fig. 6: Signal Processing Circuit (left) and the Corresponding Output Signal (right). The blue waveform is the output of the high pass filter, and the purple waveform is the output of the amplifier.

## Further Assumptions

Environmental conditions can be critical factors in the performance of electrical components and circuits. Conditions that often decrease the reliability of a circuit include temperature, vibration, humidity, dust, pressure, and radiation. For this report, the previously defined buck converter was assumed to operate in normal environmental conditions. We assume the converter is located on Earth at an altitude such that the effects of radiation and air pressure on the circuit are negligible. Additionally, we assume that the converter is appropriately enclosed and shielded to mitigate damages from dust, humidity, and extreme vibrations.

The environmental condition whose impact we consider most in our experiment is temperature. We specifically selected this condition to study due to its critical impact of increased acceleration of electrolytic capacitor lifetime. Research suggests that both ambient and internal temperatures of the capacitor can speed up the degradation process. As these temperatures increase in electrolytic capacitors such as the EEUFC2A681 in our buck converter circuit, and other power converter applications the electrolyte evaporates through the seal, and leakage increases. This results in a higher equivalent series resistance and decreased capacitance. Since the temperature heavily impacts these two properties, we plan to use them to predict failure by real-time comparisons between collected and simulated ideal data. The impacts stated can be seen by simulated data in our results section.

## Solution Process

### Alternative Designs

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As our group researched capacitor degradation our strategies took two specific directions. The first direction focused on measuring the decreasing capacitance. Decreased capacitance is indicated by a change in the shape of the waveform. Specifically, the rising edge of the waveform becomes more concave as capacitance decreases. The second direction we examined was to exclusively focus on the rising amplitude of our waveform due to an increased ESR when the capacitor degrades. Both of these approaches are practical for detecting a failing capacitor. This similarity is discussed further in the final results section. The more complicated of the two approaches is to measure the shape. **This is the approach** we have decided to pursue as it is a scalable approach and is theoretically achievable in our time frame. In the process of deciding to measure shape, we experimented with alternative circuit sampling solutions. These potential solutions included a peak detection circuit, an ADC integrated with an FPGA, and a statistical peak detection program utilizing a Raspberry Pi.

### Peak Detection Circuit

Peak detection circuits are utilized to find the average maximum output of an AC signal. The circuit processes the signal through a diode and capacitor which are connected in series. The ideal output of this circuit is a stable DC signal equal to the peak value of the AC signal. This solution can be used to detect if there is an increase in the amplitude of the waveform. Regarding capacitors, this would indicate an increase in internal resistance and decay. This situation would be beneficial because the output is a DC voltage and it can be measured by an ADC with a low sampling rate. Because of the simplicity behind this circuit, we would opt to use this solution if we did not have the goal of measuring shape.

### FPGA ADC SPI

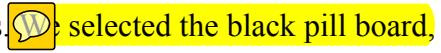
Creating an embedded system using an FPGA and then interfacing with an ADC would provide the most agility out of all of these solutions. This is due to the low-level language an FPGA is programmed with. This low-level language would also be the most complicated to build our simulation in. This assumption combined with the fact that we would need to build the SPI between the ADC and the FPGA was enough reason for our group to eliminate this solution based on time constraints.

### Raspberry Pi

Our group came up with three potential solutions utilizing the GPIO pins on a Raspberry Pi. The first solution was to use the Raspberry Pi as our embedded system in conjunction with the peak detector circuit sampling process. This solution is, again, theoretically the most simple for detecting capacitor decay. However, this was not selected for the same reasons stated above. The second solution was also for measuring amplitude and not shape. This solution involved

using the ADC on the Raspberry Pi which has a sampling rate that is too slow to sample the waveform precisely. The untested theory behind this solution was that the slow ADC could still be used to intermittently sample the circuit voltage. Then a simple statistical model in Python could be used to determine the peak voltage of the collection of the intermittent data points without registering noise. The third potential Raspberry Pi solution also involved the onboard ADC. The concept behind this solution was that if the period of the signal was known it could be used to calculate the waveform from the intermittent sampling. As the sampling program is running it would calculate the difference in time between the first sample and each following sample. Then after collecting several samples the period of the waveform and  $\Delta t$  at each point could be utilized to reconstruct the signal. This idea would be beneficial because it would reduce the amount of physical components used to construct the virtual twin. We decided to avoid this solution after developing a simulation to test this theory. The simulation demonstrated that the period used for calculation needed to be very precise. Far more precise than we believed we would be able to achieve. The program indicated that the signal could be easily miscalculated if the period was off by a fraction. This complexity is the reason we settled on the following solution.

### Final Selection

After constructing the signal processing circuit we needed to select an ADC to sample the 0-2V, 50kHz signal at a sampling rate high enough to capture the shape of the waveform. During discussions, we agreed that a minimum target sampling rate of 500 kHz would be sufficient, but 1 MHz+ was desired. Additionally, capacitor failure causes changes on the order of 5 mVs. Since the gain is around 13x, our ADC needed to differentiate between 66mV intervals. During research, we found a project that uses a black pill board to create a simple oscilloscope capable of exporting waveform data as a csv file. The board uses an STM32 microcontroller that has a built-in ADC. The important parts of the chip are its capability to send information via USB, and the ADC on the STM32. The ADC can be clocked at a maximum of 36MHz, and it has a resolution of 12 bits with a voltage range of  $\pm 3.3V$ . This yields a resolution of 1.6mV. As such, the STM32 is a good choice for a wide range of systems.  selected the black pill board, as it is one of the cheaper implementations of the STM32 processor, operates at 25MHz, and can send data via USB. Exporting the data gives us the flexibility to use a Raspberry Pi to compare the measured and ideal waveforms. It is due to these factors that we selected this board as our final solution for our ADC and embedded system solution.

Once the ADC solution has been tested we will begin the final steps of developing the virtual twin. Starting by developing an embedded system that will utilize the ADC solution to intermittently collect sample periods of the buck converter's output signal. The rate of this collection will vary depending on the virtual twin's final application. Finally, this collection will be compared to the ideal waveform in our simulation. An algorithm will be used to determine the thresholds for capacitor failure in said comparison.

## Final Results

Data for the capacitor ripple voltage was collected from measurements across the load resistor of the buck converter circuit for 10,000 data points and 5 switching periods using our oscilloscope. This was graphed in conjunction with simulated data to analyze the accuracy of the simulation data in modeling the buck converter circuit. As seen by the results in Figure 7 the simulated results closely model the results of the buck converter data.

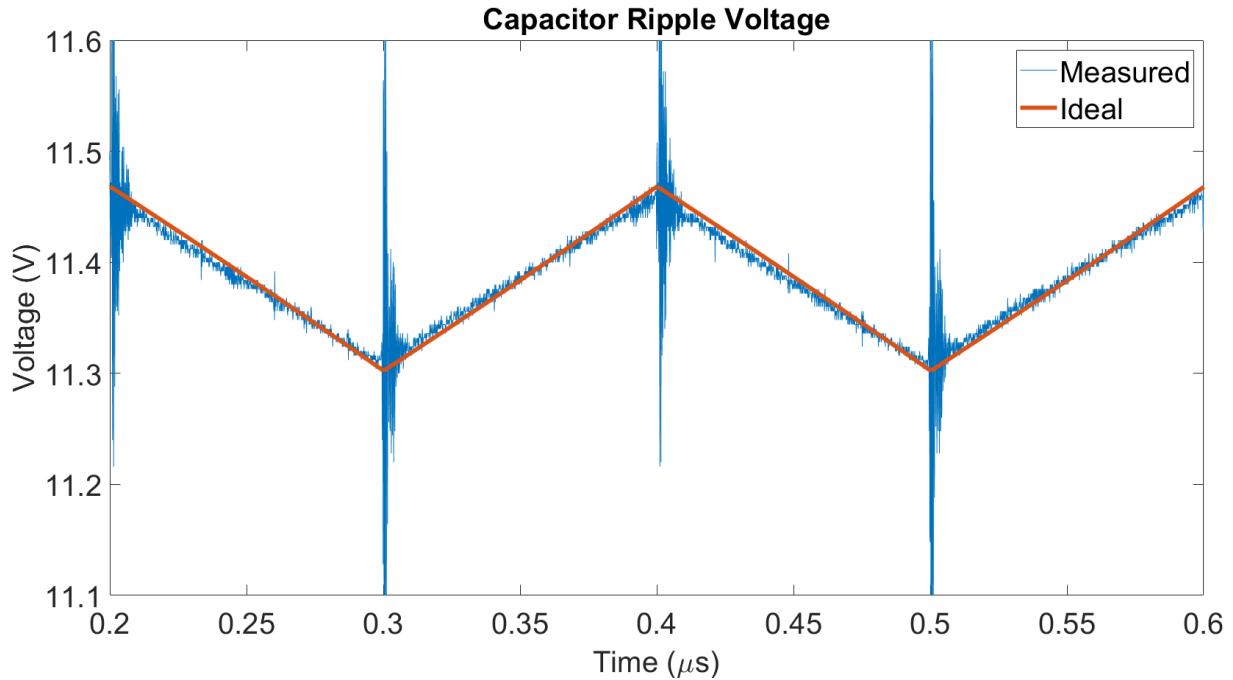


Fig. 7: Comparison of Simulated and Measured Buck Converter Data

In addition to modeling the ideal performance of the buck converter, we additionally found that changes to capacitor properties internal resistance  $R_c$ , and capacitance  $C$  correctly reflect the changes that would take place in the real-world capacitor degradation. We tested the data at increases of ESR between 20 and 40% and decreases of capacitance between 5 and 20% based on the claim that these are reasonable percentages of failure as stated in [3].

Figures 8 and 9 below show the simulated results of the capacitor ripple response from increasing the equivalent series resistance and decreasing the capacitance values of the capacitor. As the capacitor ripple was modeled from its ideal values to a 20% increase of  $R_c$  the peak capacitor ripple voltage increased and the ripple became very distinct from its ideal waveform. This change was clear using the lowest value of the ESR percentage increase range, however, the change in the waveform due to capacitance decreases was less noticeable graphically in the 5-15% range which is why Figure 9 shows the results for a 90% decrease in capacitance. At this degradation value, there is a noticeable change in the shape of the simulated data compared to

the ideal simulation.

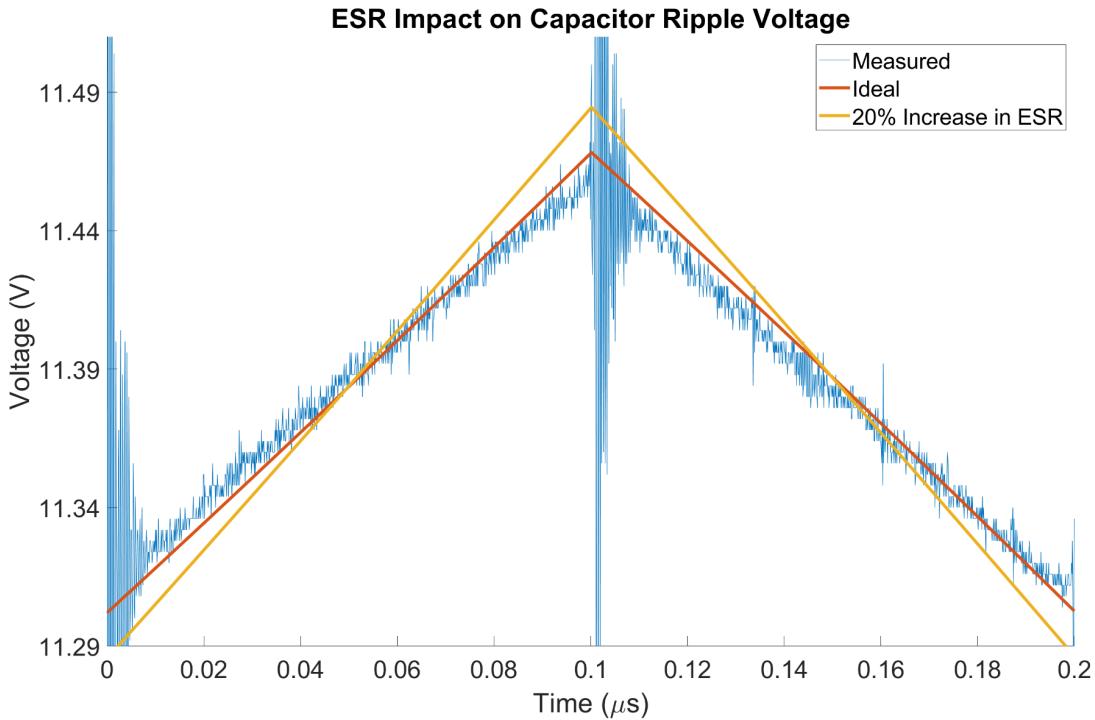


Fig. 8: Impact of ESR on Capacitor Ripple Voltage

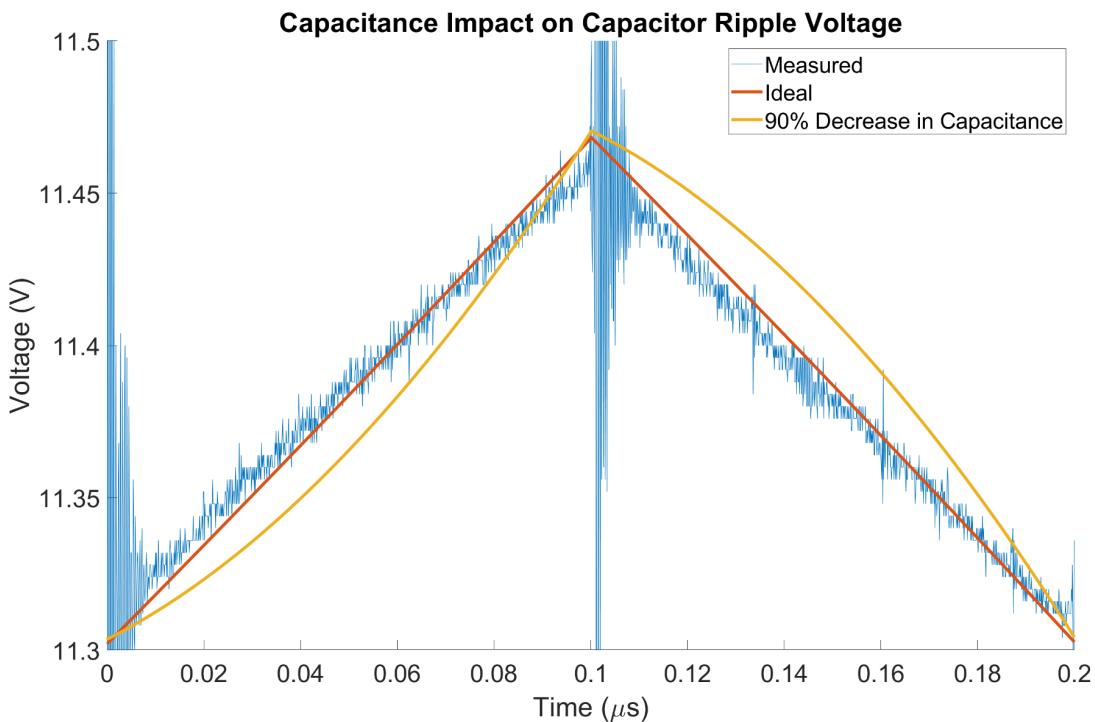


Fig. 9: Impact of Capacitance on Capacitor Ripple Voltage

 These results indicate that our state space construction of a digital twin at the given parameters will be accurate enough to the real-world capacitor ripple voltage for our purposes of identifying capacitor degradation. As a capacitor degrades over time, changes in its ripple shape and more critically its peak value data can be collected with our selected ADC and embedded system and compared with the results of our digital twin to identify and predict failure.

## Future Work

With this basis of understanding of the problem presented and given the work completed up to this point, our future goals to complete the project can be defined in two parts. ~~The first goal will be to construct the selected sampling circuit to sample the data in real time using the microcontroller on the black-pill board to collect, store, and transmit data from the processed capacitor voltage signal output of the buck converter. As discussed in the section about the sampling circuit, we plan to use the STM32 microcontroller on the black pill board to~~ to accomplish this goal and transmit data via USB to be compared.

Secondly, we plan to compare the waveform to its digital counterpart and quantifiably assign the possibility of failure for the capacitor based on the statistical similarity of the waveforms. ~~Several distance metric algorithms~~ exist to assign the similarity of two waveforms such as the Euclidean, Manhattan, and Minkowski distance metrics. We plan to study these and possibly other methods to identify failure. We plan to especially focus on the relationship between the peak values of the capacitor ripple to identify failure due to increasing ESR as this seems to be a very clear indicator with a relationship to the likelihood a capacitor will fail.

Other minor ~~work that we plan to complete consists of~~ bettering our signal processing design by transferring it to a perf board to increase the reliability of the circuit as well as continuing to organize our research for our presentation and report at the end of the spring semester. In these ways, failure can be accurately monitored and predicted for our buck converter circuit.

## Reflection

The research and implementation of our virtual twin project took us through multiple paths over the course of the semester. It was evident that for an involved and complex project such as this and the many projects in our futures', it is necessary that we engage in lifelong learning. To assume that our current knowledge is sufficient introduces limitations and inhibits a project's natural ability to progress. We must be mindful of this so that we don't just create products that work, but rather that we design ones that efficiently utilize resources to better meet the diverse needs of the people in our world. This is the benefit of our liberal education: to broaden our horizons to comprehend the diverse facets of our world so that we can design solutions that meet the changing needs of our world. While our engineering education was imperative to the progress accomplished, it could be argued that the skills we've gained in our

other studies motivated us to see this project through, by understanding the universal benefits of finding a simple, scalable, and inexpensive solution to this problem that can benefit society and save lives.

## Conclusion

In this report, we highlight the benefits of a virtual twin health monitoring approach to predict circuit failure by monitoring the performance of the capacitor of a buck converter circuit. We compiled significant findings about the literature surrounding this subject and built the foundation of our approach including our supporting research and assumptions made during the process. We then gave detailed explanations about the theorized ADC and embedded systems solutions to test our virtual twin and gave sufficient support as to why we settled on the STM32 microcontroller on the black pill board as meeting our requirements. Additionally, results for the simulated digital twin were produced and utilized to support the conclusions that our digital twin successfully modeled the performance of a buck converter's capacitor and that this model will be accurate enough to predict failure in the future. We concluded with descriptions of the future work to be performed for this project and reflected on the importance of this project to our present and future careers as engineers.

## Appendix

### References

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### Code

Link to our Project GitHub: <https://github.com/agrosjean0/ECE448-VirtualTwinning>