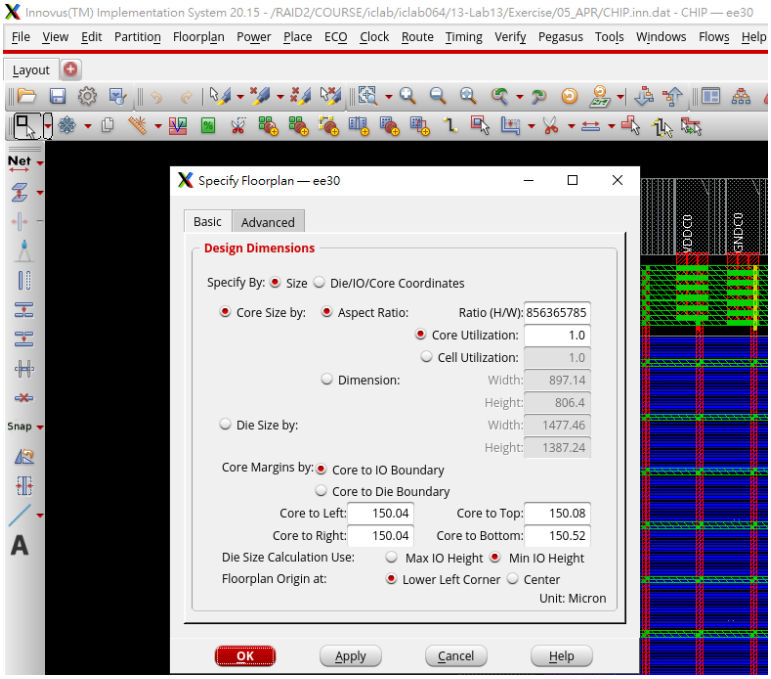
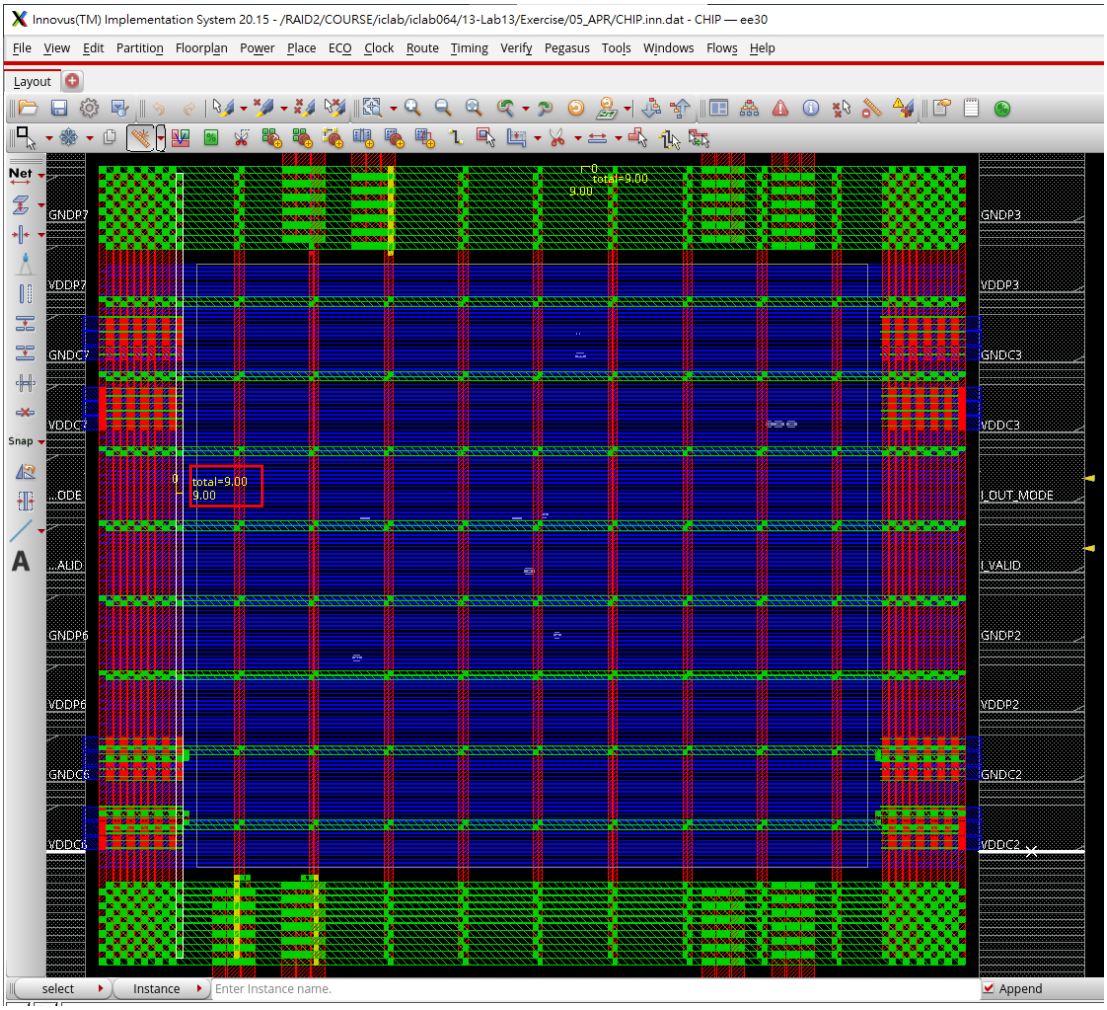
Report

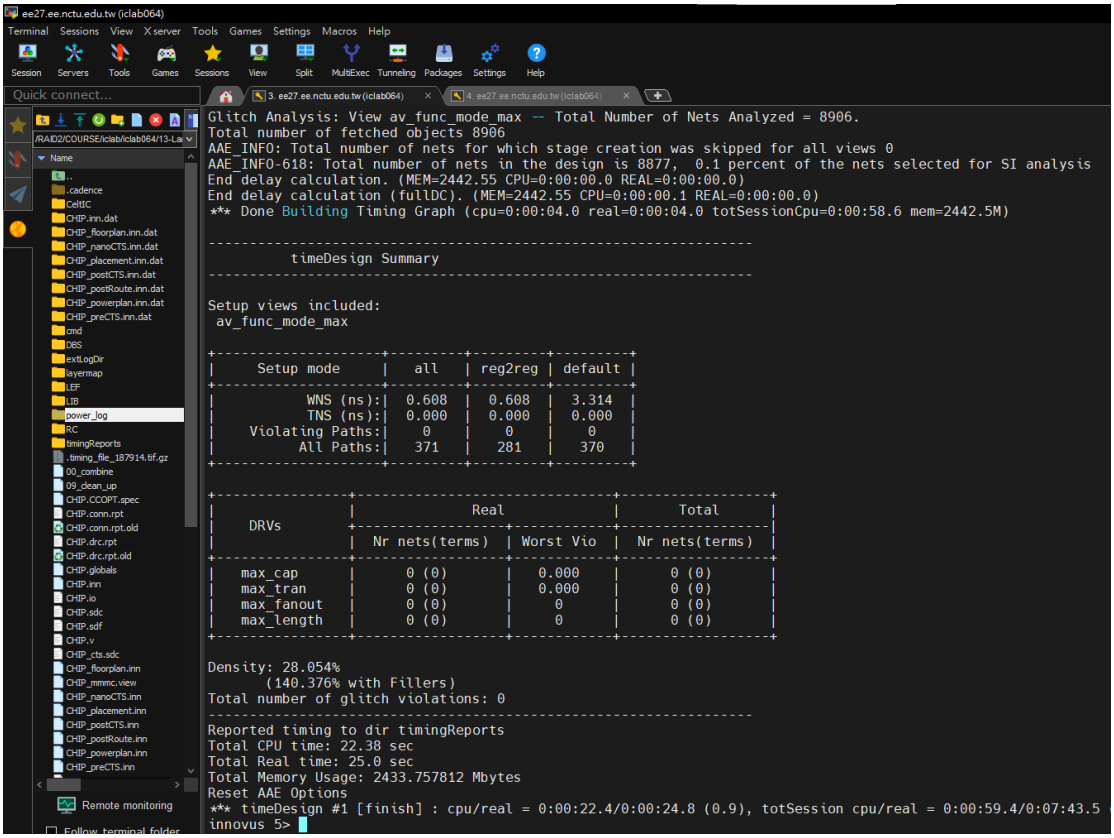
1. Core to IO boundary :



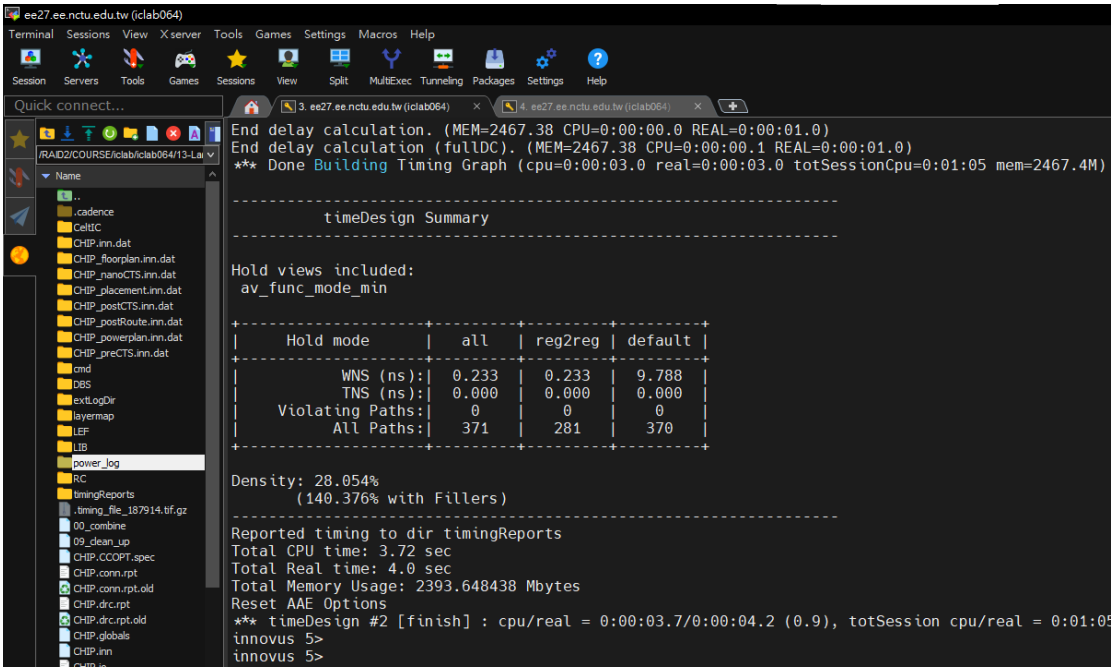
2. Core Ring :



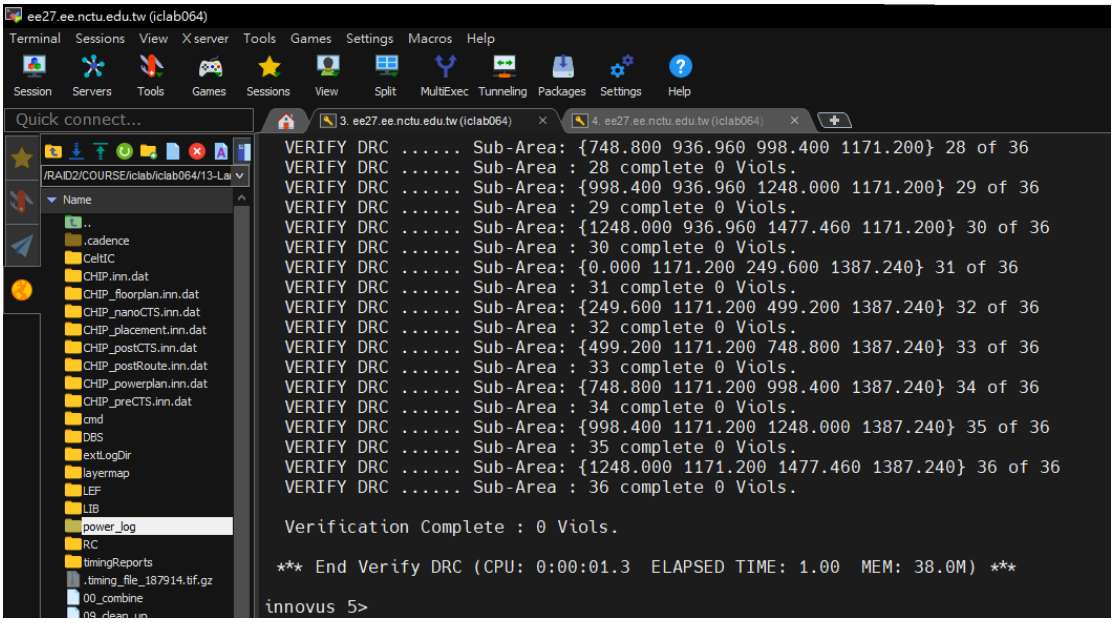
3. Post-Route setup time analysis :



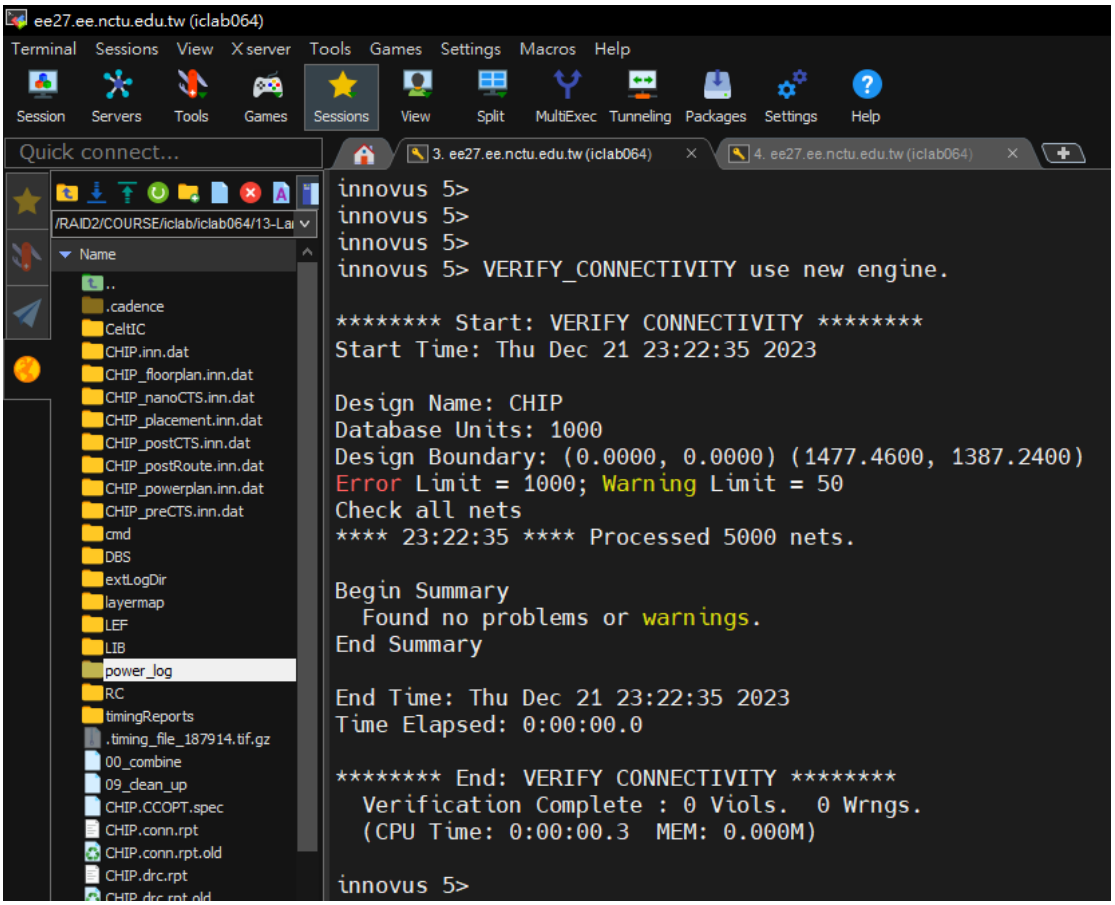
4. Post-Route hold time analysis :



5. DRC result :



6. LVS result :



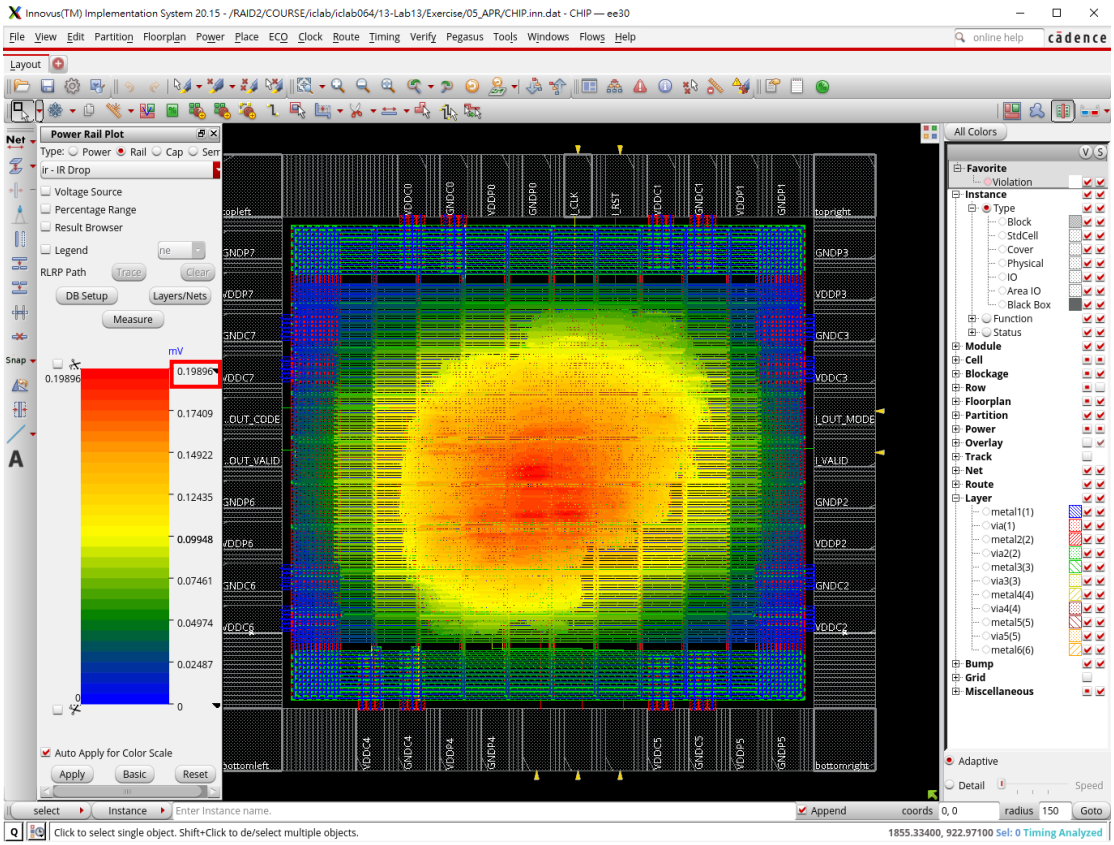
7. Post Layout simulation result :

```
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999
--------------------------------------------------------------------
                    Congratulations!
                You have passed all patterns!
                Your execution cycles = 32000 cycles
                Your clock period = 20.0 ns
                Total Latency = 640000.0 ns
--------------------------------------------------------------------
$finish called from file "PATTERN.v", line 36.
$finish at simulation time          1819630000
           V C S   S i m u l a t i o n   R e p o r t
Time: 1819630000 ps
CPU Time:     27.080 seconds;       Data structure size:   2.2Mb
Fri Dec 22 15:33:30 2023
CPU time: 2.039 seconds to compile + .427 seconds to elab + .658 seconds to link + 27.158 seconds in simulation
15:33 iclab064@ee30[~/13-Lab13/Exercise/06_POST]$
```

8. Power result :

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:        1.42444066            52.4954%
Total Switching Power:       1.28023186            47.1808%
Total Leakage Power:         0.00878706             0.3238%
Total Power:                 2.71345958
--------------------------------------------------------------------------------
```

9. IR Drop Results :



i. 增加IO power、core power的pair數量

ii. 在IO pin的設計上盡量讓core各個位置距離這些pin都不要太遠

iii. Power ring增加為6 pairs

iv. Power stripe的線寬設計的比較寬