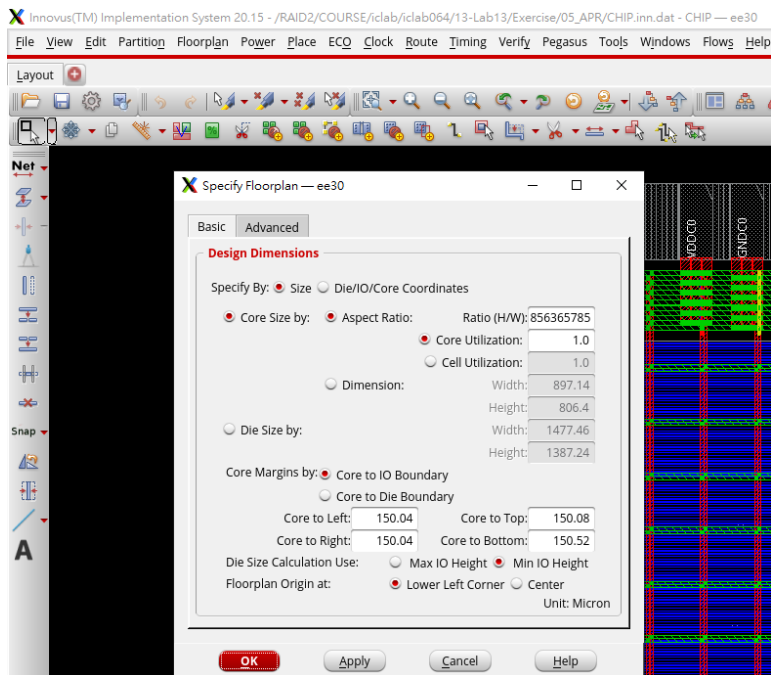
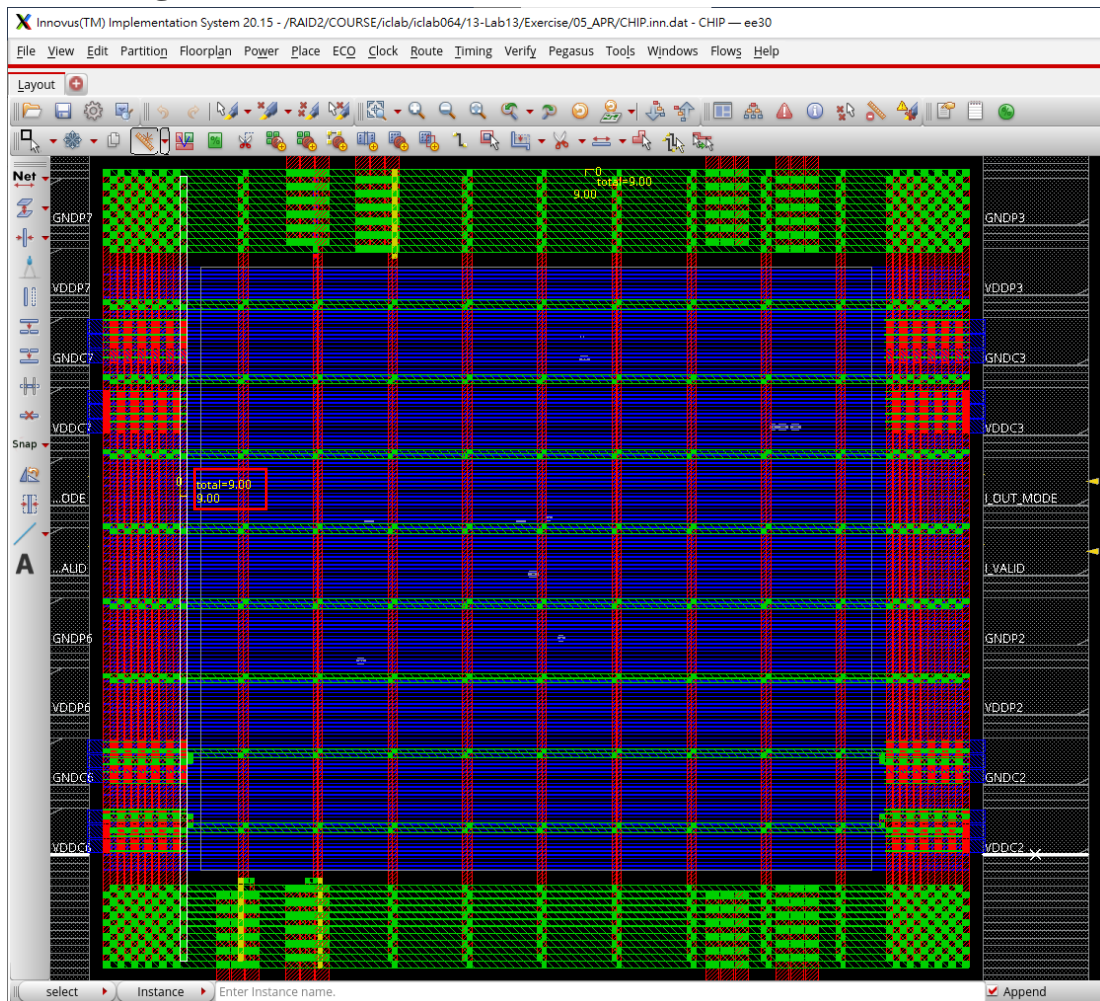


Report

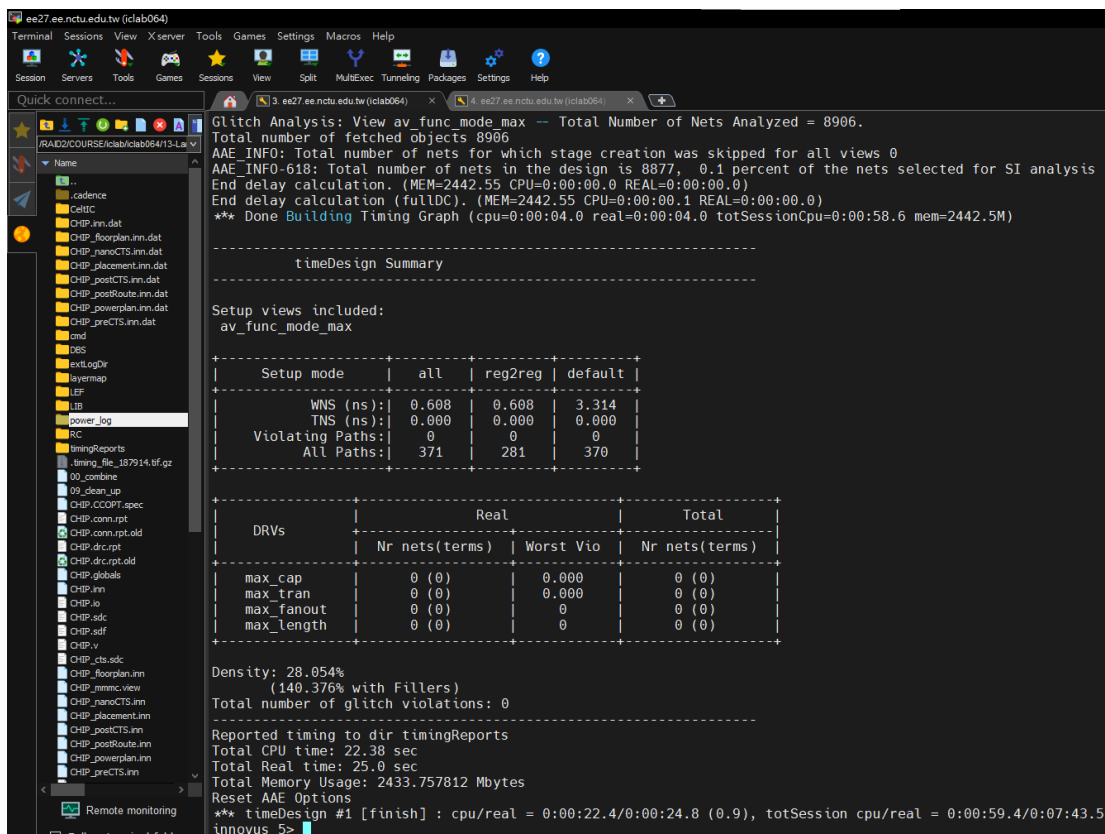
1. Core to IO boundary :



2. Core Ring :



3. Post-Route setup time analysis :



```
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 8906.
Total number of fetched Objects 8906
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 8877, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=2442.55 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2442.55 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:04.0 real=0:00:04.0 totSessionCpu=0:00:58.6 mem=2442.5M)

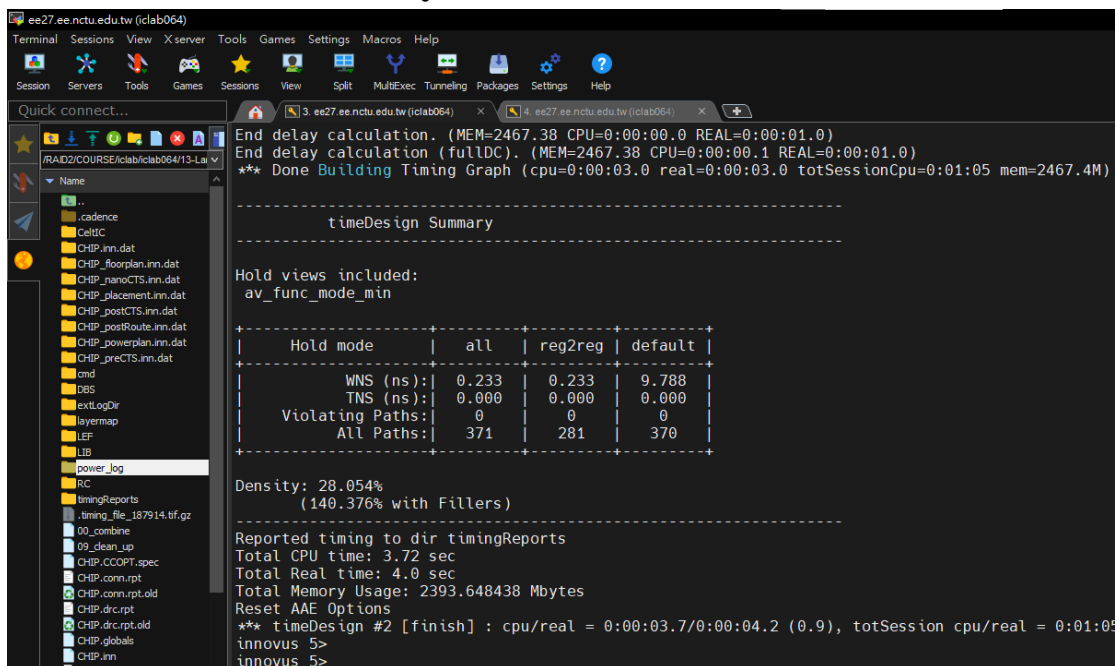
-----
timeDesign Summary
-----
Setup views included:
av_func_mode_max

-----
Setup mode | all | reg2reg | default |
-----
WNS (ns): | 0.608 | 0.608 | 3.314 |
TNS (ns): | 0.000 | 0.000 | 0.000 |
Violating Paths: | 0 | 0 | 0 |
All Paths: | 371 | 281 | 370 |
-----

-----
DRVs | Real | Total |
-----
Nr nets(terms) | Worst Vio | Nr nets(terms) |
-----
max_cap | 0 (0) | 0.000 | 0 (0) |
max_tran | 0 (0) | 0.000 | 0 (0) |
max_fanout | 0 (0) | 0 | 0 (0) |
max_length | 0 (0) | 0 | 0 (0) |
-----

Density: 28.054%
(140.376% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 22.38 sec
Total Real time: 25.0 sec
Total Memory Usage: 2433.757812 Mbytes
Reset AAE Options
*** timeDesign #1 [finish] : cpu/real = 0:00:22.4/0:00:24.8 (0.9), totSession cpu/real = 0:00:59.4/0:07:43.5
innovus 5>
```

4. Post-Route hold time analysis :



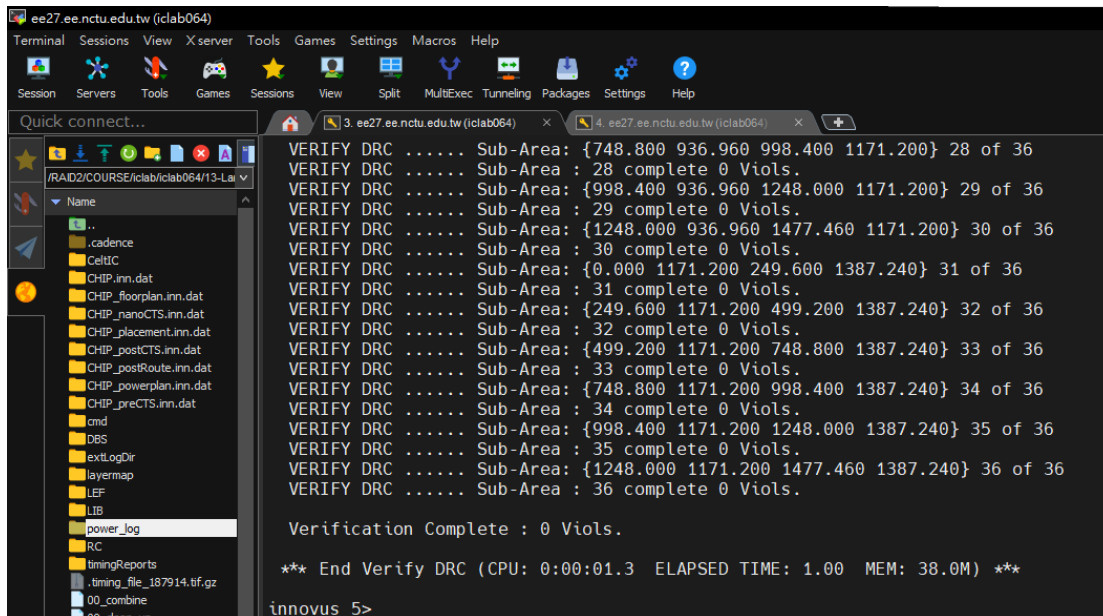
```
End delay calculation. (MEM=2467.38 CPU=0:00:00.0 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=2467.38 CPU=0:00:00.1 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:03.0 real=0:00:03.0 totSessionCpu=0:01:05 mem=2467.4M)

-----
timeDesign Summary
-----
Hold views included:
av_func_mode_min

-----
Hold mode | all | reg2reg | default |
-----
WNS (ns): | 0.233 | 0.233 | 9.788 |
TNS (ns): | 0.000 | 0.000 | 0.000 |
Violating Paths: | 0 | 0 | 0 |
All Paths: | 371 | 281 | 370 |
-----

Density: 28.054%
(140.376% with Fillers)
Reported timing to dir timingReports
Total CPU time: 3.72 sec
Total Real time: 4.0 sec
Total Memory Usage: 2393.648438 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:03.7/0:00:04.2 (0.9), totSession cpu/real = 0:01:05.4/0:07:43.5
innovus 5>
innovus 5>
```

5. DRC result :



The screenshot shows a terminal window with a menu bar (Terminal, Sessions, View, X server, Tools, Games, Settings, Macros, Help) and a toolbar. The left sidebar shows a file tree under the path /RAID2/COURSE/iclab/iclab064/13-Lab. The main terminal area displays the output of a DRC verification process. It lists 36 sub-areas, each with a 'VERIFY DRC' status, a list of coordinates, and a count of violations (all are 0). The process concludes with 'Verification Complete : 0 Viols.' and a summary line: '** End Verify DRC (CPU: 0:00:01.3 ELAPSED TIME: 1.00 MEM: 38.0M) **'. The prompt 'innovus 5>' is visible at the bottom.

```
ee27.ee.nctu.edu.tw (iclab064)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

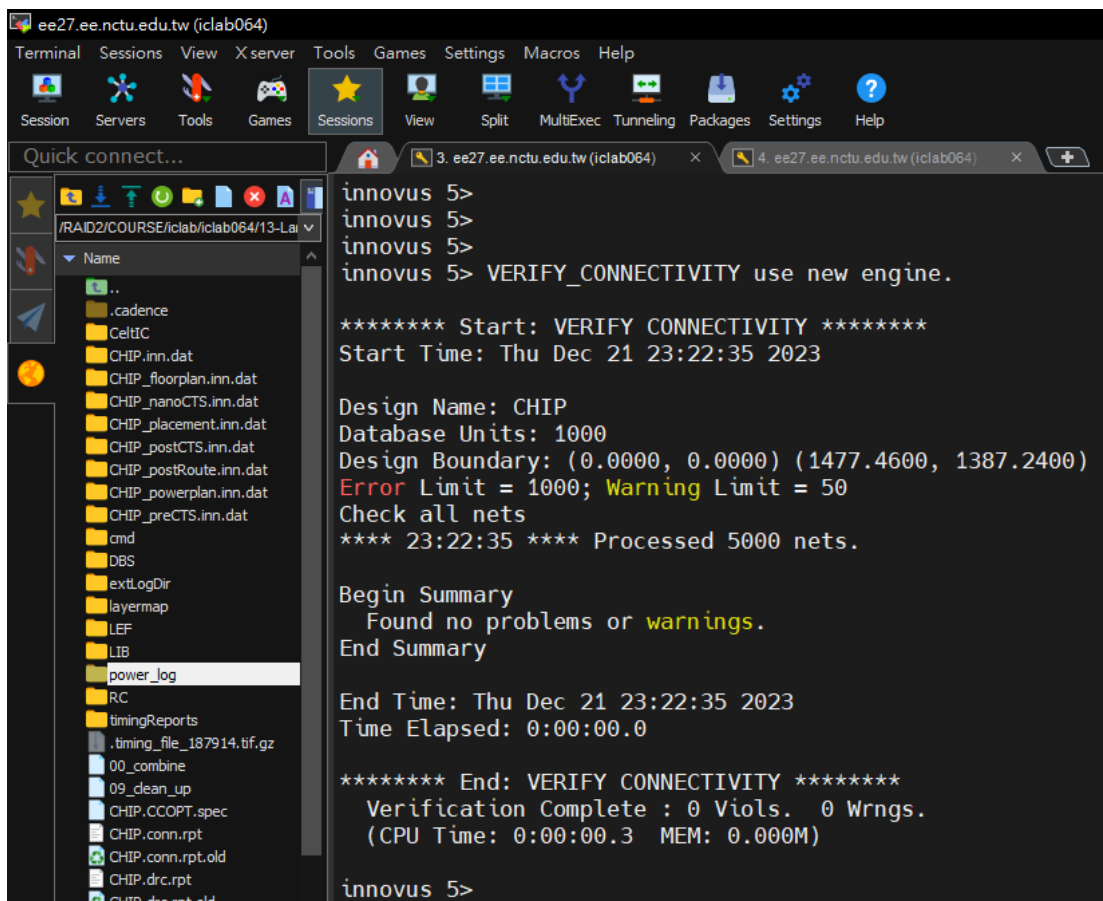
Quick connect...
/RAID2/COURSE/iclab/iclab064/13-Lab
Name
..
.cadence
CeltiC
CHIP.inn.dat
CHIP_floorplan.inn.dat
CHIP_nanoCTS.inn.dat
CHIP_placement.inn.dat
CHIP_postCTS.inn.dat
CHIP_postRoute.inn.dat
CHIP_powerplan.inn.dat
CHIP_preCTS.inn.dat
cmd
DBS
extLogDir
layermap
LEF
LIB
power_log
RC
timingReports
.timing_file_187914.tif.gz
00_combine
09_clean_up

VERIFY DRC ..... Sub-Area: {748.800 936.960 998.400 1171.200} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 936.960 1248.000 1171.200} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1248.000 936.960 1477.460 1171.200} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1171.200 249.600 1387.240} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {249.600 1171.200 499.200 1387.240} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {499.200 1171.200 748.800 1387.240} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {748.800 1171.200 998.400 1387.240} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {998.400 1171.200 1248.000 1387.240} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1248.000 1171.200 1477.460 1387.240} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

Verification Complete : 0 Viols.

** End Verify DRC (CPU: 0:00:01.3 ELAPSED TIME: 1.00 MEM: 38.0M) **
innovus 5>
```

6. LVS result :



The screenshot shows the same terminal window as in the previous image, but now displaying the output of an LVS (Logic Verification) process. The prompt 'innovus 5>' is repeated several times. The main output includes: 'Start: VERIFY CONNECTIVITY', 'Design Name: CHIP', 'Database Units: 1000', 'Design Boundary: (0.0000, 0.0000) (1477.4600, 1387.2400)', 'Error Limit = 1000; Warning Limit = 50', 'Check all nets', '***** Start: VERIFY CONNECTIVITY *****', 'Start Time: Thu Dec 21 23:22:35 2023', 'Design Name: CHIP', 'Database Units: 1000', 'Design Boundary: (0.0000, 0.0000) (1477.4600, 1387.2400)', 'Error Limit = 1000; Warning Limit = 50', 'Check all nets', '**** 23:22:35 **** Processed 5000 nets.', 'Begin Summary', 'Found no problems or warnings.', 'End Summary', 'End Time: Thu Dec 21 23:22:35 2023', 'Time Elapsed: 0:00:00.0', '***** End: VERIFY CONNECTIVITY *****', 'Verification Complete : 0 Viols. 0 Wrngs.', '(CPU Time: 0:00:00.3 MEM: 0.000M)'. The prompt 'innovus 5>' is visible at the bottom.

```
ee27.ee.nctu.edu.tw (iclab064)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/RAID2/COURSE/iclab/iclab064/13-Lab
Name
..
.cadence
CeltiC
CHIP.inn.dat
CHIP_floorplan.inn.dat
CHIP_nanoCTS.inn.dat
CHIP_placement.inn.dat
CHIP_postCTS.inn.dat
CHIP_postRoute.inn.dat
CHIP_powerplan.inn.dat
CHIP_preCTS.inn.dat
cmd
DBS
extLogDir
layermap
LEF
LIB
power_log
RC
timingReports
.timing_file_187914.tif.gz
00_combine
09_clean_up
CHIP.CCOPT.spec
CHIP.conn.rpt
CHIP.conn.rpt.old
CHIP.drc.rpt
CHIP.drc.rpt.old

innovus 5>
innovus 5>
innovus 5>
innovus 5> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 21 23:22:35 2023

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1477.4600, 1387.2400)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 23:22:35 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu Dec 21 23:22:35 2023
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.3 MEM: 0.000M)

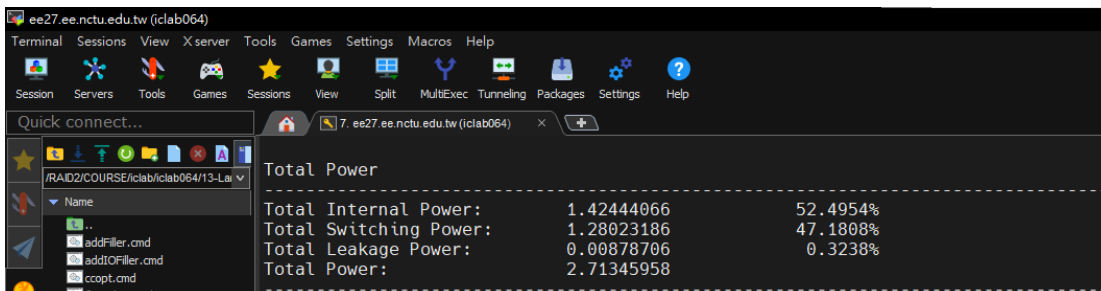
innovus 5>
```

7. Post Layout simulation result :

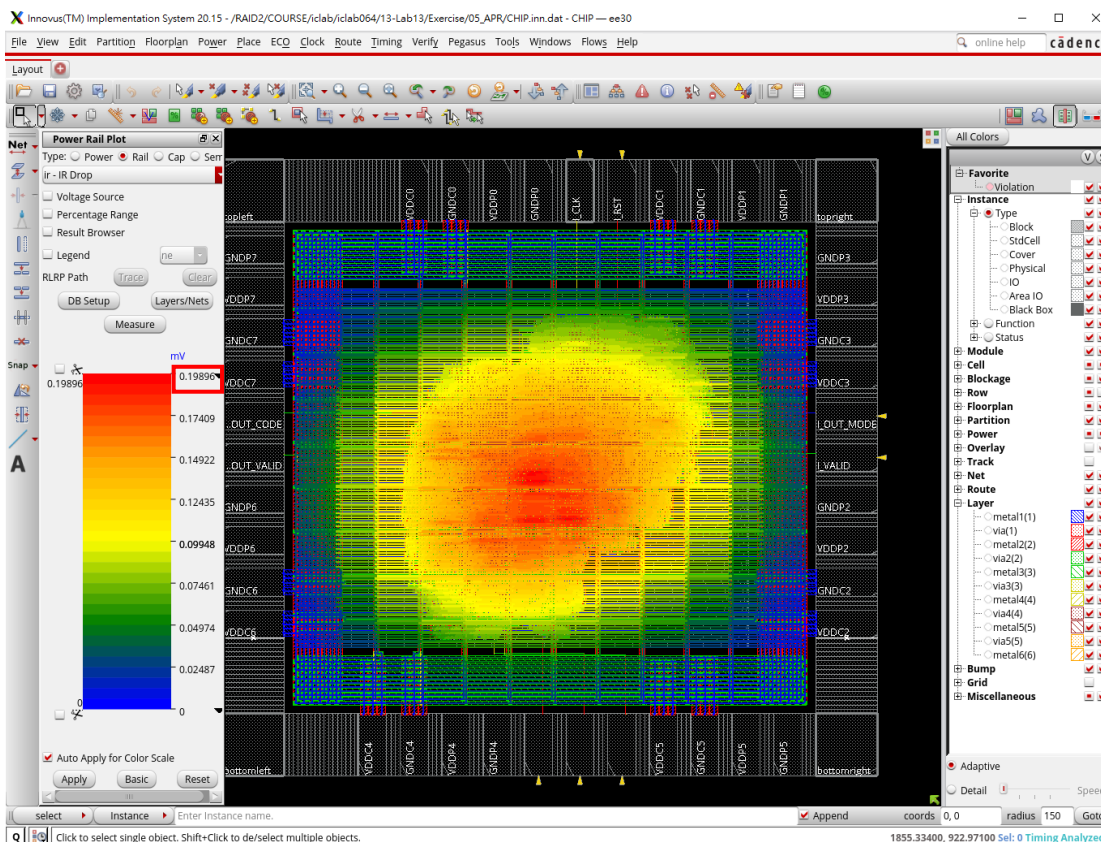
```
5. ee27.ee.nctu.edu.tw (iclab064) x 5. ee27.ee.nctu.edu.tw (iclab064) x
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----
$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1819630000
VCS Simulation Report
Time: 1819630000 ps
CPU Time: 27.080 seconds; Data structure size: 2.2Mb
Fri Dec 22 15:33:30 2023
CPU time: 2.039 seconds to compile + .427 seconds to elab + .658 seconds to link + 27.158 seconds in simulation
15:33 iclab064@ee30[~13-Lab13/Exercise/06_POST]$
```

8. Power result :



9. IR Drop Results :



- 增加IO power、core power的pair數量
- 在IO pin的設計上盡量讓core各個位置距離這些pin都不要太遠
- Power ring增加為6 pairs
- Power stripe的線寬設計的比較寬