CS 061 – Computer Organization — Fall - 2013

Quiz 7 – Thursday 11/14 — solution

Construction of an LC-3 instruction (Instruction Register fields):
opcode: [15:12]
Destination register/Source register/condition code test (nzp): [11:9]
Source Register 1/Base Register: [8:6]
Source Register 2: [2:0]
PCoffset9: [8:0] PCoffset11: [10:0] Offset6: [5:0] Imm5: [4:0] trapvec8: [7:0]
Mode flags: [11], [5]

1. Given that the opcode for the ADD instruction is **b0001**, and that the addressing mode flag (bit 5) for the *immediate mode* add instruction is **1**:
What does the instruction **`ADD R6, R5, #-10`** assemble to? *(Note the sign!!)*

a. x1566 **c.** x1D6A **e.** x1BB6
b. x1BBA **d.** **x1D76** **f.** x1656

2. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction is loaded):

```
x3025       loop1    ADD  R4, R5, R6
                     .....
x30EB                BRn loop1
```

Given that the BR opcode is **b0000**, what does the instruction at x30EB assemble to? *(Note the direction of the branch!)*

a. **x0939** **c.** x093B **e.** x0B3A
b. x093A **d.** x0B39 **f.** x0B3B

3. What are the "micro-instructions" that comprise the Fetch phase of the Instruction cycle?

a. `IR <- (PC); MAR <- (IR); PC <- Mem[MDR]; PC <- (PC) + 1;`
b. `PC <- (MDR) + 1; MAR <- Mem[PC]; IR <- (MDR)`
c. `MAR <- (PC) + 1; MDR <- Mem[IR]; IR <- (MAR);`
d. **`MAR <- (PC); PC <- (PC) + 1; MDR <- Mem[MAR]; IR <- (MDR)`**
e. `MDR <- (PC); PC <- (PC) + 1; MAR <- Mem[MDR]; IR <- (PC)`

4. In the ***Direct mode*** of memory addressing in the LC-3 (e.g. the instructions LD & ST), the Effective Address is calculated by:

a. `(BaseReg) + SEXT(IR[5:0])`
b. `Mem[ (BaseReg) + SEXT(PC[5:0]) ]`
c. **`(PC) + SEXT(IR[8:0])`**
d. `Mem[(PC) + SEXT(IR[8:0]) ]`
e. `(IR) + SEXT(PC[8:0])`
f. `Mem[(IR) + SEXT(PC[8:0]) ]`

5. In the ***Relative*** or ***Base + Offset mode*** of memory addressing in the LC-3 (e.g. the instructions LDR & STR), the Effective Address is calculated by:

a. **`(BaseReg) + SEXT(IR[5:0])`**
b. `Mem[ (BaseReg) + SEXT(PC[5:0]) ]`
c. `(PC) + SEXT(IR[8:0])`
d. `Mem[ (PC) + SEXT(IR[8:0]) ]`
e. `(IR) + SEXT(PC[8:0])`
f. `Mem[ (IR) + SEXT(PC[8:0]) ]`

6. All control instructions in the LC-3 (e.g. BR, JMP, TRAP, etc.) have one main step in common:
   - **a.** They all reconstruct the required memory address in the same way
   - **b.** They all use the ALU in reconstructing the required memory address
   - **c.** They all write to the IR in the execution phase of the instruction cycle
   - **d.** **They all write to the PC in the execution phase of the instruction cycle**
   - **e.** They all write to the MDR in the execution phase of the instruction cycle
   - **f.** They all write to the GPR bank in the execution phase of the instruction cycle

7. The DR decoder input comes from the DRMUX. What are two of the inputs to the DRMUX? *(Hint: think about the JSR/R and TRAP instructions)*
   - **a.** `IR[8:6] and IR[11:9]`
   - **b.** **`[111] and IR[11:9]`**
   - **c.** `[000] and IR[11:9]`
   - **d.** `IR[2:0] and IR[11:9]`
   - **e.** `The system bus and IR[11:9]`
   - **f.** `(PC) and IR[11:9]`

8. The SR1 decoder input comes from the SR1MUX. What are two of the inputs to the SR1MUX?
   (Hint: think about the Store instructions)
   - **a.** **`IR[8:6] and IR[11:9]`**
   - **b.** `[111] and IR[8:6]`
   - **c.** `[000] and IR[8:6]`
   - **d.** `IR[2:0] and IR[8:6]`
   - **e.** `The system bus and IR[8:6]`
   - **f.** `(PC) and IR[8:6]`

9. One of the four values of ALUK, the control signal to the LC-3 ALU, instructs the ALU to "pass-through input A" - i.e. input A is connected directly to the output.
   Which of the following instructions would use this control signal?
   - **a.** NOT
   - **b.** LD, LDI & LDI
   - **c.** **ST, STI & STR**
   - **d.** BR & JMP
   - **e.** JSR/JSRR
   - **f.** TRAP

10. In the LC-3 data path, the output of the address adder goes to both the MARMUX and the PCMUX, potentially causing two very different register transfers to take place. Why does this not happen?
    - **a.** Another multiplexer routes the adder output to the desired target
    - **b.** **Only one of the two control signals (Marmux.Gate and LD.PC) will be asserted.**
    - **c.** Only one of the two control signals (MDR.Gate and addressAdder1MUX=select PC) will be asserted
    - **d.** Both register transfers actually do take place, but one of them is ignored
    - **e.** The MARMUX and the PCMUX can each be caused (via a selector signal) to have no ouput when the other mux is the desired target.