CS 061 – Computer Organization **Fall - 2013**

Quiz 6 – Thursday 11/7 solution

1. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would ***toggle*** the character stored in R0 between *upper* case and *lower* case - i.e. convert a *lower* case character into *upper* case, and convert an *upper* case character to *lower* case (so 'a' would become 'A', and 'A' would become 'a').
   Note: the LC-3 stores ASCII characters in the lower ("right-hand") byte of a 16-bit word, with the upper byte set to zero.
   a. and R0 with x0020
   b. or R0 with x0020
   c. xor R0 with x0020
   d. and R0 with x005F
   e. or R0 with x005F
   f. and R0 with x004F

2. You are given a box of **16k by 8-bit** memory chips, and asked to construct from them a **256k by 1-byte** memory module, utilising the Chip Select (CS) input on each of the chips. This will require "two levels" of addressing – i.e. a portion of the address will be input to the address pins of the individual chips, and a portion will be input to a module-level decoder connected to the chips' CS pins. How many bits will be input to this module-level decoder?
   a. 2
   b. 3
   c. 4
   d. 5
   e. 6
   f. 7

3. An ISA specifies a *word size* of 4 bytes; *word addressability*; and an *address space* of 16M; it uses single-word instructions (i.e. each instruction is a single 4 byte word). What are the sizes of the PC and the IR?
   a. both 16 bits
   b. both 24 bits
   c. both 32 bits
   d. PC: 16 bits; IR: 32 bits
   e. PC: 24 bits; IR: 32 bits
   f. PC: 32 bits; IR: 24 bits

4. For the system in the previous question: What are the sizes of the MDR and the MAR?
   a. both 16 bits
   b. both 24 bits
   c. both 32 bits
   d. MDR: 16 bits; MAR: 32 bits
   e. MDR: 24 bits; MAR: 32 bits
   f. MDR: 32 bits; MAR: 24 bits

The next two questions refer to the following system:
A certain ISA has a 32-bit word size, uses single word instructions, has 120 opcodes, 32 registers, and 4Gbyte of byte-addressable memory.

One group of instructions in this ISA takes the form:

```
OPCODE | DESTINATION REGISTER | SOURCE REGISTER | FLAG | IMMEDIATE VALUE
```

Or

```
OPCODE | DESTINATION REGISTER | SOURCE REGISTER 1 | FLAG | SOURCE REGISTER 2
```

A one-bit flag distinguishes between these two addressing modes.

Another group of instructions takes the form

```
OPCODE | SOURCE/DESTINATION REGISTER | PC OFFSET
```

Where PC Offset is the 2's complement "distance" from the current PC to the labelled location.

5. What is the range of values that can be stored in the "Immediate" field (as a 2's complement value, to within +/- 1)?

a. +/- 16 **c.** **+/- 8k** **e.** +/- 32k
b. +/- 2k **d.** +/-16k **f.** +/- 2M

6. How far (in memory locations) can a labelled location be from an instruction using the PC-relative addressing mode? (to within +/- 1)

a. +/- 256k **c.** +/- 1M **e.** +/- 4M
b. **+/- 512k** **d.** +/- 2M **f.** +/- 4G

7. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction is loaded):

```
xB829                    LEA  R5, data_ptr
                           ......
xB860        data_ptr    .FILL   x6000
                           ......
```

Given: the LEA opcode is 1110
What does the instruction at xB829 assemble to (i.e. what is the Machine Language encoding of the instruction)? *(Remember, `9+1 = A`, **not** `10`!)*

a. xE531 **b.** xE650 **c.** xE651 **d.** **xEA36** **e.** xEA37
f. assemble error (no ML translation)

8. In the LC-3, the input to the first "arm" of the ALU is always the contents of SR1 (Source Register 1, one of the 8 General Purpose Registers);
the second input is *either* the contents of SR2 (another GPR) *or*:

a. the 5-bit "immediate" value embedded in the instruction
b. **the 16-bit word formed from SEXT(IR[4:0])**
c. the contents of a memory location
d. the contents of the "immediate" register
e. the 9-bit offset embedded in the instruction
f. none of the above

9. How does the control unit decide which of the two possible inputs (described in the previous question) to use for the second operand in an ADD instruction?

a. The two possible inputs occupy different positions in the IR
b. If the IR contains a 5-bit embedded value, that is used; if it doesn't, SR2 is used
c. The two versions of the ADD instruction have different op-codes
d. The immediate input is contained in a separate register
e. By the value of a flag bit in the ADD instruction
f. The control unit is omniscient

10. The purpose of a "gate" circuit between data "suppliers" and the global bus is:

a. to prepare the bus to carry the data
b. to separate the 16 individual bits of data to be carried by the bus
c. to prevent the contents of the bus being written back to the "supplier" device
d. **to allow a single "supplier" device to control the state of the bus at any one time**
e. to inform the bus regarding the destination of the data