CS 061 – Computer Organization **Fall - 2013**

Quiz 4 – Thursday 10/24 solution

1. What is the decimal equivalent of the IEEE-754 floating point number
   `1 10000001 00010000000000000000000`
   a. -17.0 **c.** **-4.25** **e.** -1.06125
   b. -8.5 **d.** -2.125

2. The LC-3 does not have the operation "OR". Which of the following combinations of LC-3 instructions would be the equivalent of `OR R3, R1, R2` (i.e. bitwise OR the contents of R1 and R2 and store the result into R3)?

   a.
   ```
   AND R3, R1, R2
   NOT R3, R3
   ```
   b.
   ```
   NOT R1, R1
   NOT R2, R2
   AND R3, R1, R2
   NOT R3, R3
   ```
   c.
   ```
   NOT R1, R1
   ADD R1, R1, #1
   ADD R3, R1, R2
   NOT R3, R3
   ```
   d.
   ```
   AND R1, R1, #1
   AND R3, R1, R2
   NOT R3, R3
   ```
   e.
   ```
   AND R3, R1, R2
   NOT R1, R1
   AND R3, R3, R1
   ```
   f.
   ```
   NOT R1, R1
   NOT R2, R2
   AND R3, R1, R2
   ```

3. What is the logic expression corresponding to the following truth table, in the form Out = f(A, B, C)

   a. `Out = A.B + A.C`
   b. `Out = A.B' + A.C`
   c. `Out = A.B' + B.C`
   d. `Out = A.B.C + A'.C`
   e. `Out = A.B.C + A'.B'.C'`
   f. **`Out = A.B + A.C + B.C`**

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

4. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would force the character stored in R0 to *lower* case - i.e. convert a character stored in R0 from *upper* case into *lower* case, or *preserve* the case if it was lower case already.(so 'A' would become 'a', and 'a' would remain unchanged).
   Note: the LC-3 stores ASCII characters in the lower ("right-hand") byte of a 16-bit word, with the upper byte set to zero.
   a. and R0 with x0020 **c.** xor R0 with x0020 **e.** or R0 with x005F
   b. **or R0 with x0020** **d.** and R0 with x005F **f.** and R0 with x004F

5. How many *select* lines does an 8 input multiplexer have?
   a. 1 **b.** **3** **c.** 8 **d.** 64 **e.** 256

6. How many *inputs* does a full adder have?
   a. 1 **b.** 2 **c.** **3** **d.** 4
   e. It depends on the number of bits in the numbers being added

7. In order to overcome the gate delay problem of the simple ripple-adder circuit, we can design an adder with the following design improvement:
   a. Make each full-adder smaller so as to reduce the gate delay of each.
   b. Recursively pre-calculate the carry bit for each digit.
   c. Add an n-bit register to hold intermediate results, where n is the number of digits being added.
   d. Use a multiplexer to distribute the carry bits to subsequent columns

8. How many memory locations can be addressed by a microprocessor that uses 24 bit addressing?
   a. 16 M **b.** 1024 **c.** 2 G **d.** 512 k
   e. none of the above

9. What is one purpose of the extra gates of a gated D-latch with respect to a simple R-S latch?
   a. to provide a feedback circuit in order to store the output.
   b. to allow the output to be read.
   c. to decrease the propagation delay of the circuit.
   d. to prevent the R and S lines from transitioning to 0 simultaneously.
   e. to prevent the R and S lines from transitioning to 1 simultaneously.

10. What data types are implemented natively in the LC-3?
   a. integer, double, character and boolean
   b. twos complement integer
   c. twos complement integer and floating point
   d. ASCII and twos complement integer
   e. twos complement integer and Hexadecimal