CS 061 – Computer Organization — Fall - 2013

Quiz 8 – Thursday 11/21 — solution

Construction of an LC-3 instruction (Instruction Register fields):
opcode: [15:12]
Destination register/Source register/condition code test (nzp): [11:9]
Source Register 1/Base Register: [8:6]
Source Register 2: [2:0]
PCoffset9: [8:0] PCoffset11: [10:0] Offset6: [5:0] Imm5: [4:0] trapvec8: [7:0]
Mode flags: [11], [5]

1. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction or label is loaded):

```
x30BC        loop1     ADD  R4, R5, R6
                       .....
x3148                  BRzp loop1
```

Given that the BR opcode is **b0000**, what is the Machine Languabe translation of the instruction at x3148? *(Note the direction of the branch!)*

a. x0939 **c.** **x0773** **e.** x068B
b. x093B **d.** x0775 **f.** x068D

2. One of the four values of ALUK, the control signal to the LC-3 ALU, instructs the ALU to "pass-through input A" - i.e. input A is connected directly to the output.
Which of the following instructions would use this control signal?

a. NOT **c.** **ST, STI & STR** **e.** JSR/JSRR
b. LD, LDI & LDI **d.** BR & JMP **f.** TRAP

3. In the LC-3 data path, the output of the address adder goes to both the MARMUX and the PCMUX, potentially causing two very different register transfers to take place. Why does this not happen?

a. Another multiplexer routes the adder output to the desired target
b. **Only one of the two control signals (Marmux.Gate and LD.PC) will be asserted.**
c. Only one of the two control signals (MDR.Gate and addressAdder1MUX=select PC) will be asserted
d. Both register transfers actually do take place, but one of them is ignored
e. The MARMUX and the PCMUX can each be caused (via a selector signal) to have no ouput when the other mux is the desired target.

4. In the LC-3 (and most ISAs), the Trap Vector Table contains

a. the Trap Service Routines
b. the 9-bit PC offsets of the Trap Service Routine addresses
c. the 8-bit Trap Vector
d. **the starting addresses of the Trap Service Routines**
e. the return addresses to be used after returning from a Trap Service Routine

5. How many trap service routines could theoretically be created for the LC-3, given the format of the TRAP instruction? *(hint: how many bits are used for the trap vector?)*

a. 16 **b.** 64 **c.** **256** **d.** 512 **e.** 1024

6. What does the pseudo-op .EXTERNAL do?
   a. It invokes an external compiler – e.g. for handling embedded code written in a different programming language like C++
   b. It invokes an external subroutine – e.g. a pre-assembled library
   c. It allows external data to be input at run-time
   d. It allows a library to be dynamically linked, rather than statically linked
   e. It will cause the program to be suspended while waiting for an external input.
   f. **It defers resolution of a label to link time**

7. What is the main purpose of the first pass of a two-pass assembler?
   a. **to build a symbol table relating labels to memory addresses**
   b. to determine if the code will fit into available memory
   c. to produce the machine language equivalent of the assembly language instructions
   d. to link other possible object files in order to create the executable image
   e. to remove all pseudo-ops from the code before it is assembled

8. The purpose of the linker program is:
   a. **To produce a single executable image from multiple object files**
   b. To produce a single object file from multiple source files
   c. To implement pseudo-ops in the source file
   d. To build a symbol table from the source file

9. In a processor that uses the technique of memory mapping to address ports *(registers that interface between the cpu and peripherals)*, how are the ports actually accessed *(i.e. written to/read from)*?
   a. via dedicated i/o instructions.
   b. via interrupts
   c. via polling
   d. **via standard Load/Store instructions**
   e. via a status register

10. Memory mapping of ports is achieved by:
   a. A BIOS routine (i.e. software) that checks for the mapped address and re-routes the data to the register.
   b. The register is directly connected to the memory circuit decoder output of the mapped address.
   c. **An Address Control Logic circuit decodes the requested address and determines whether the main memory or the register is to be enabled.**
   d. A separate address bus carries the address to the external registers.