CS 061 – Computer Organization **Fall - 2013**

Quiz 5 – Thursday 10/31 solution

1. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would force the character stored in R0 to *upper* case - i.e. convert a character stored in R0 from *lower* case into *upper* case, or *preserve* the case if it was upper case already.(so 'a' would become 'A', and 'A' would remain unchanged).
   Note: the LC-3 stores ASCII characters in the lower ("right-hand") byte of a 16-bit word, with the upper byte set to zero.

   a. and R0 with x0020 **c.** xor R0 with x0020 **e.** or R0 with x005F
   b. or R0 with x0020 **d. and R0 with x005F** **f.** and R0 with x004F

2. You are given a box of **4k by 4-bit** memory chips, and asked to construct from them a 128k by 1-byte memory module, utilising the Chip Select (CS) input on each of the chips. This will require "two levels" of addressing -- i.e. a portion of the address will be input to the address pins of the individual chips, and a portion will be input to a module-level decoder driving the chips' CS pins. How many bits will be input to this module-level decoder?

   a. 2 **b.** 3 **c.** 4 **d. 5** **e.** 6 **f.** 8

The following two questions concern an ISA that has *word addressable* memory; you also know that the system can perform addition of 32-bit two's complement integers, and it uses 24-bit addressing.

3. What is the address space (i.e. how many memory locations can be addressed)?

   a. 32 **c.** 64k **e.** 256M
   b. 24k **d. 16M** **f.** 4G

4. What is the total memory available in the system of the previous question?

   a. 64 kbytes **c.** 1 Mbytes **e.** 256 Mbytes
   b. 256 kbytes **d. 64 Mbytes** **f.** 16 Gbytes

The next two questions refer to the following scenario:

Consider an elevator that connects the 1st, 2nd, 3rd & 4th floors of a building, able to make "express" rides, e.g. it can.go from the 1st floor to the 3rd or 4th floor without stopping at imtermediate floors (and vice versa).
The controller for this system is an example of a **finite state machine (fsm)**, whose state space consists of the elevator stopped at each of the four floors, with the doors either closed or open (i.e. doors open & doors closed are separate states). The task of the fsm is to control the transitions between all possible states, according to external inputs from button pushes, sensors, etc (which we don't need to worry about here).
To answer the following questions, you will need to sketch the fsm diagram, identifying all possible states and all possible transitions between states. Think carefully about the open- & closed-door states.

5. How many bits would be needed to label all possible states?

   a. 1 **c. 3** **e.** 5
   b. 2 **d.** 4 **f.** 6

6. How many distinct transitions are there between states (*not* including "null transitions", i.e. transitions back to the current state)?

   a. 4 **c.** 8 **e. 20**
   b. 6 **d.** 12 **f.** 24

The following five questions refer to the von Neumann model of computing:

7. The key components of the Processing unit are:
   - **a. the arithmetic & logic unit (ALU) and the register bank**
   - **b.** the ALU and the instruction register
   - **c.** the instruction decoder and the ALU
   - **d.** the memory data register and the program counter
   - **e.** the register bank and the program counter

8. The main purpose of the control unit is:
   - **a.** to store the list of instructions
   - **b. to fetch the next instruction from memory & decode it**
   - **c.** to control the ALU
   - **d.** to control access to memory
   - **e.** to clock the transitions between states of the whole microprocessor

9. The Program Counter is:
   - **a.** a binary counter that keeps track of the number of instructions executed
   - **b.** a register that stores the instruction currently being executed
   - **c.** a control circuit that steps through a sequence of instructions
   - **d.** a register that stores the address of the next memory location to be written to
   - **e. a register that stores the memory address of the next instruction**

10. The Instruction Register is:
   - **a.** a binary counter that keeps track of the number of instructions executed
   - **b. a register that stores the instruction currently being executed**
   - **c.** a control circuit that steps through a sequence of instructions
   - **d.** a register that stores the address of the next memory location to be written to
   - **e.** a register that stores the memory address of the next instruction