Lab Assignment: MODELSIM

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CSc 34300 & CSc 34200

Due: 2/15/22

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Section 1: Objective

The goal of this project is to familiarize myself with ModelSim and to create a project that uses my 2-1 Mux where each bit is one signal VHDL file to generate waves and output. We then take the bits and compare them to the truth table to validate our result.

Section 2: Modelsim Simulation and intro

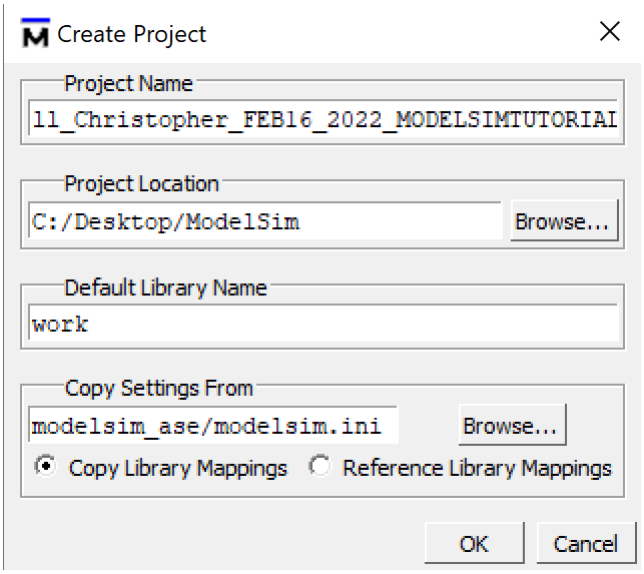

Figure 1. Creating new project

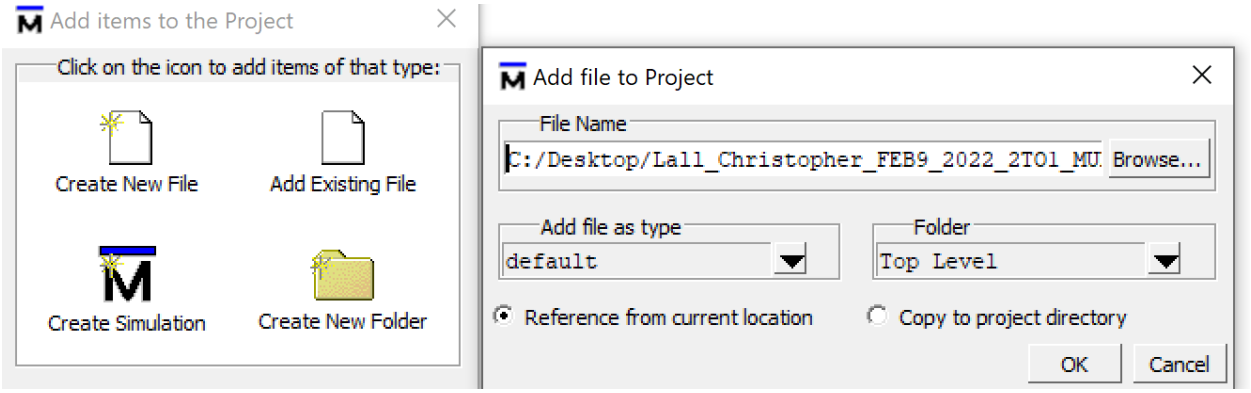

Figure 2. Adding existing item to project

Figure 3. Compiling file

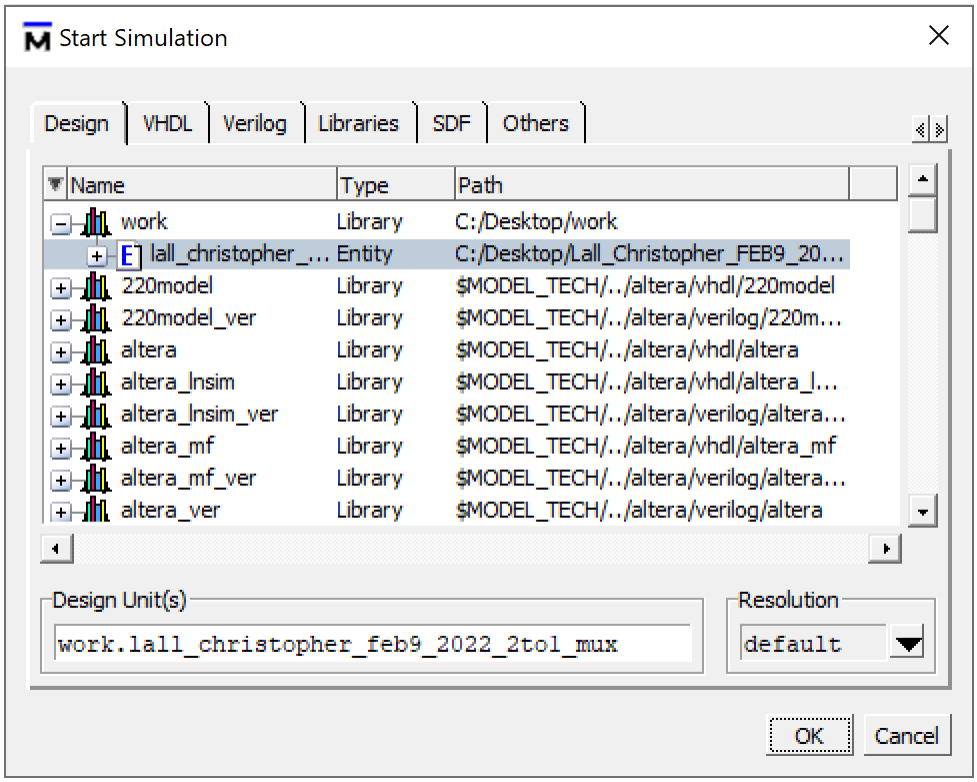

Figure 4. Simulating file

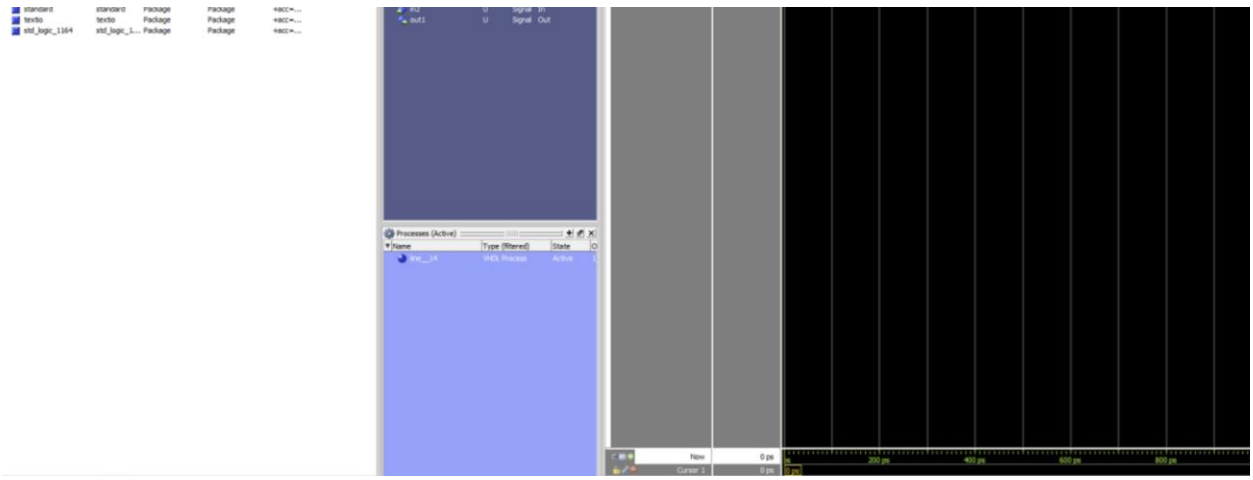

Figure 5. Window of project screen when opening simulation

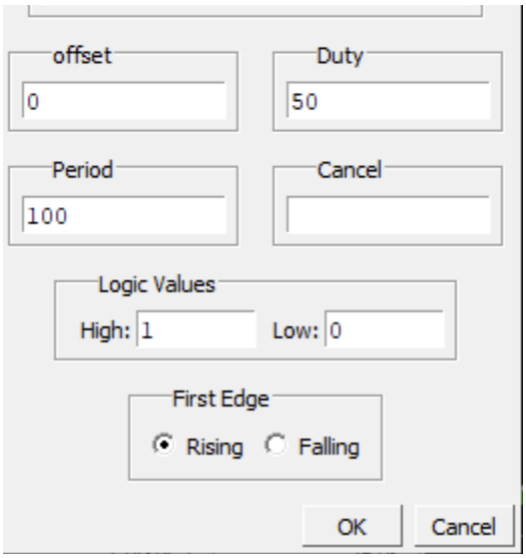

Figure 6. Changing period

Section 2.1: Simulation Results

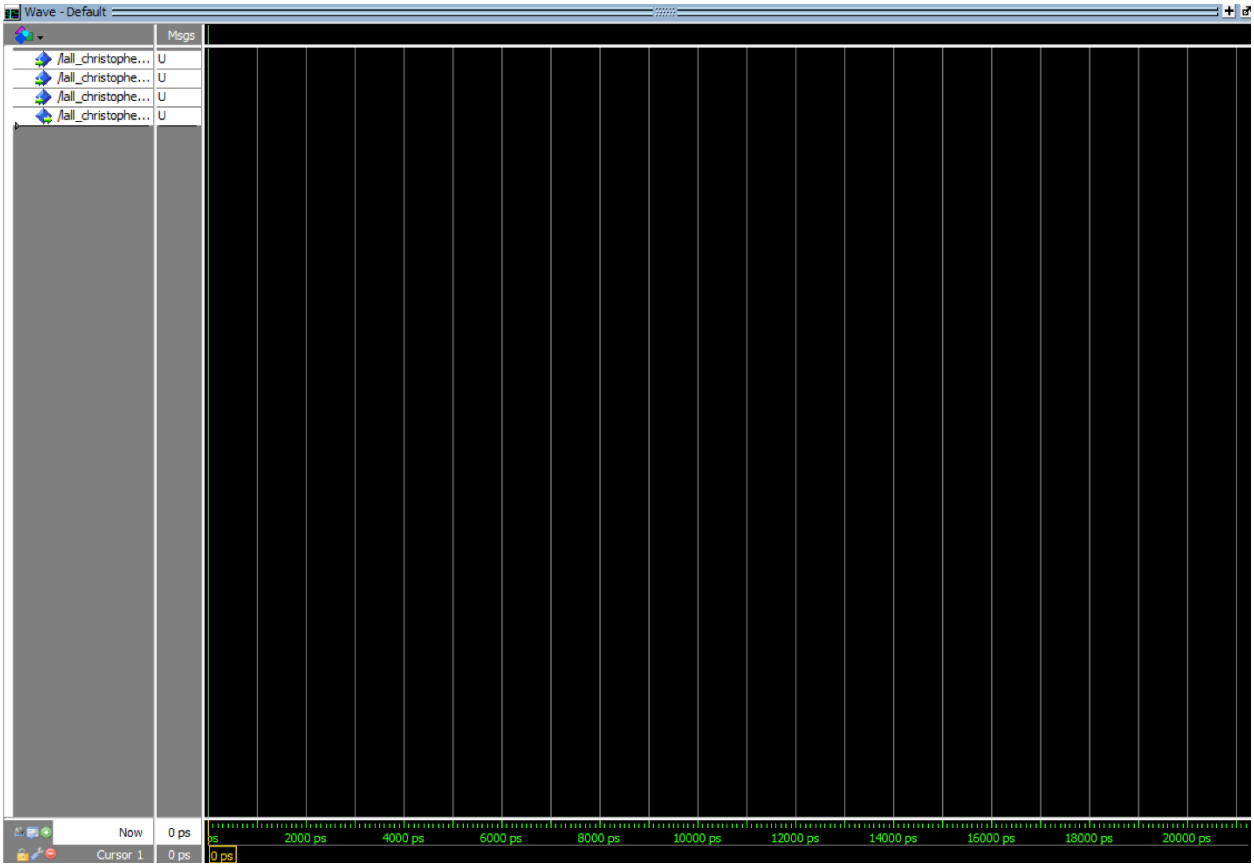

Figure 7. Simulation screen before running

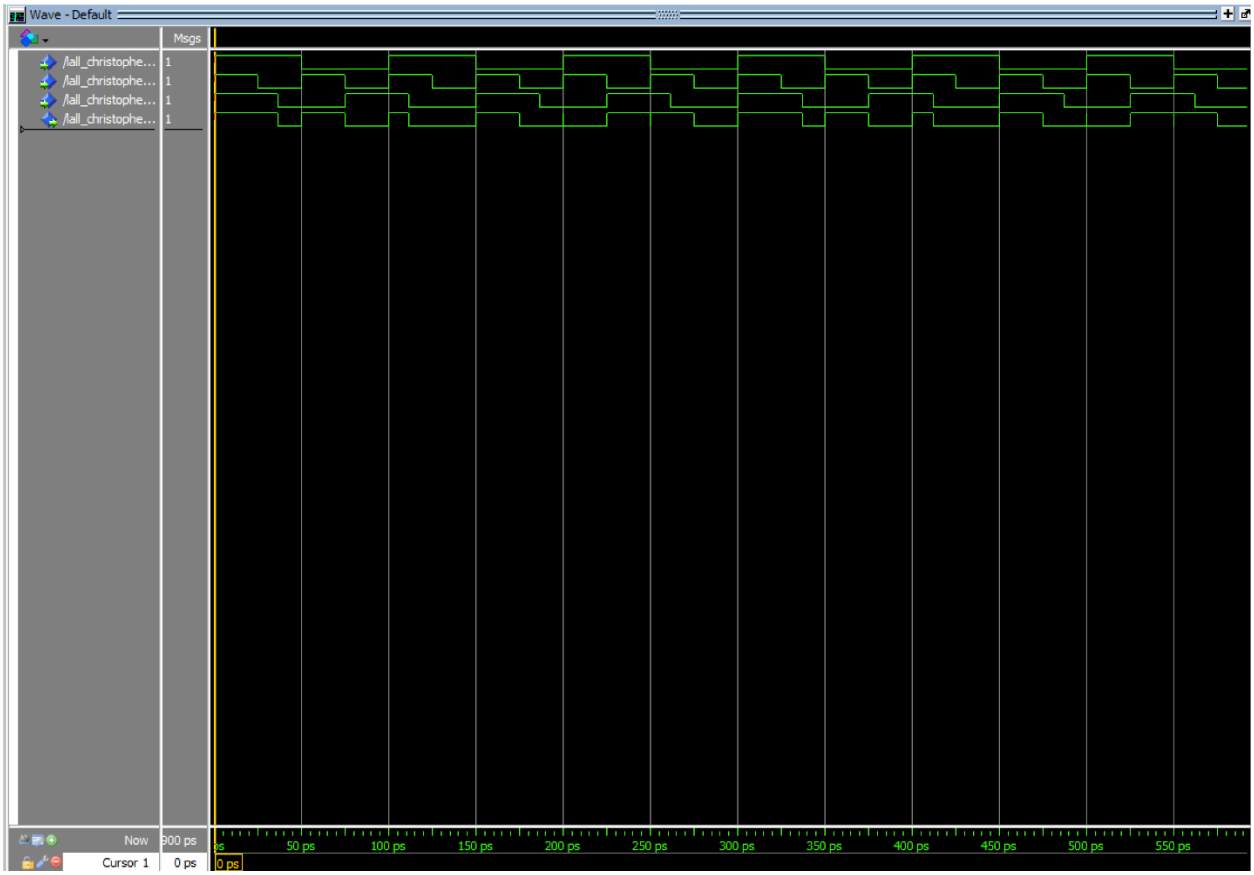

Figure 8. Example of all 1s in output

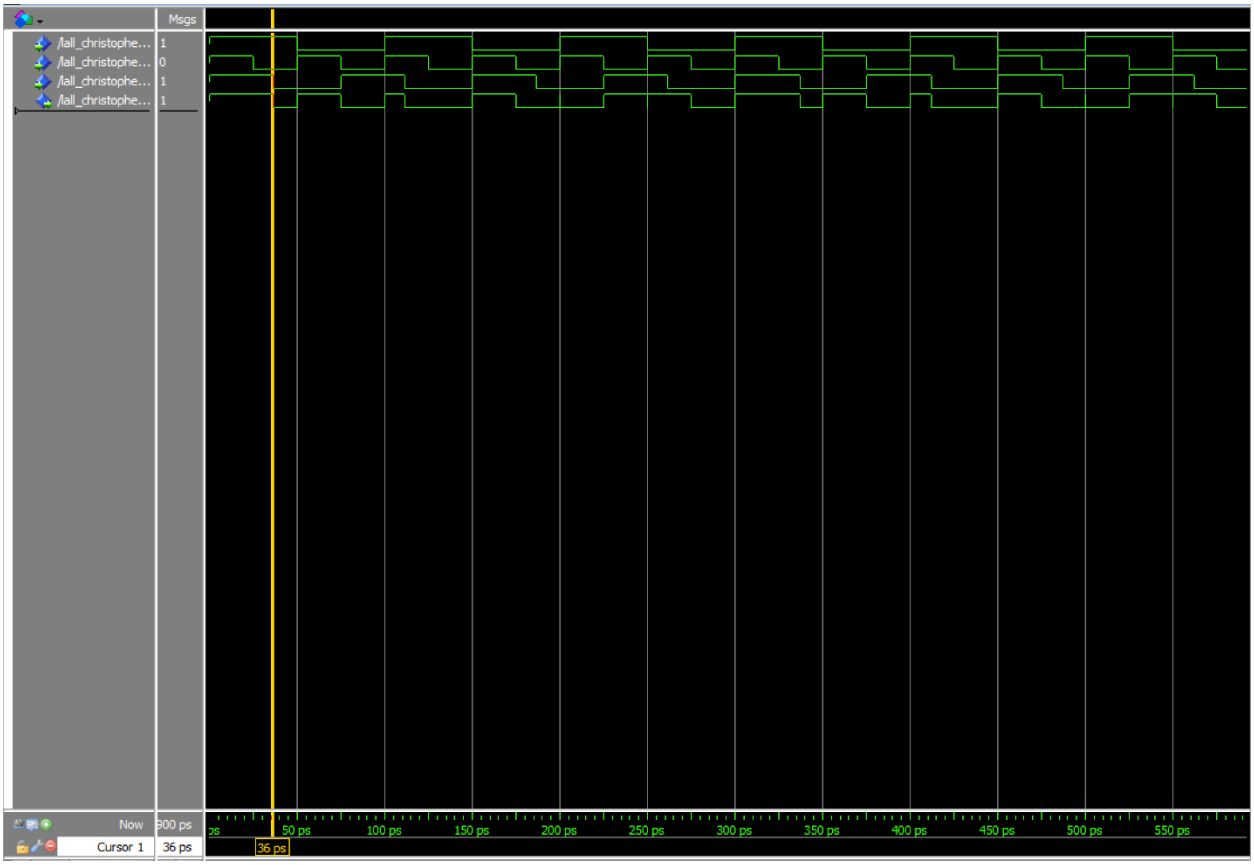

Figure 9. Example of 3 1's

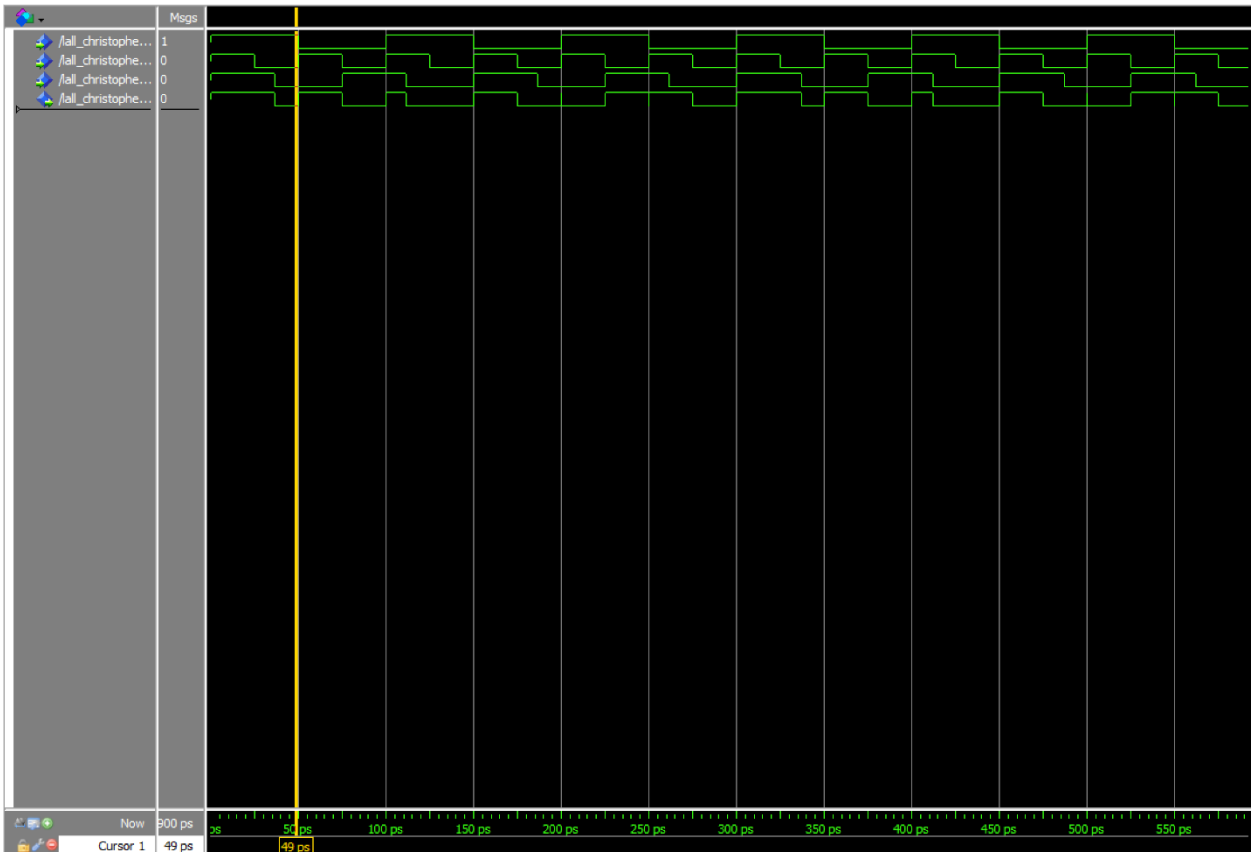

Figure 10. Example of 3 0's

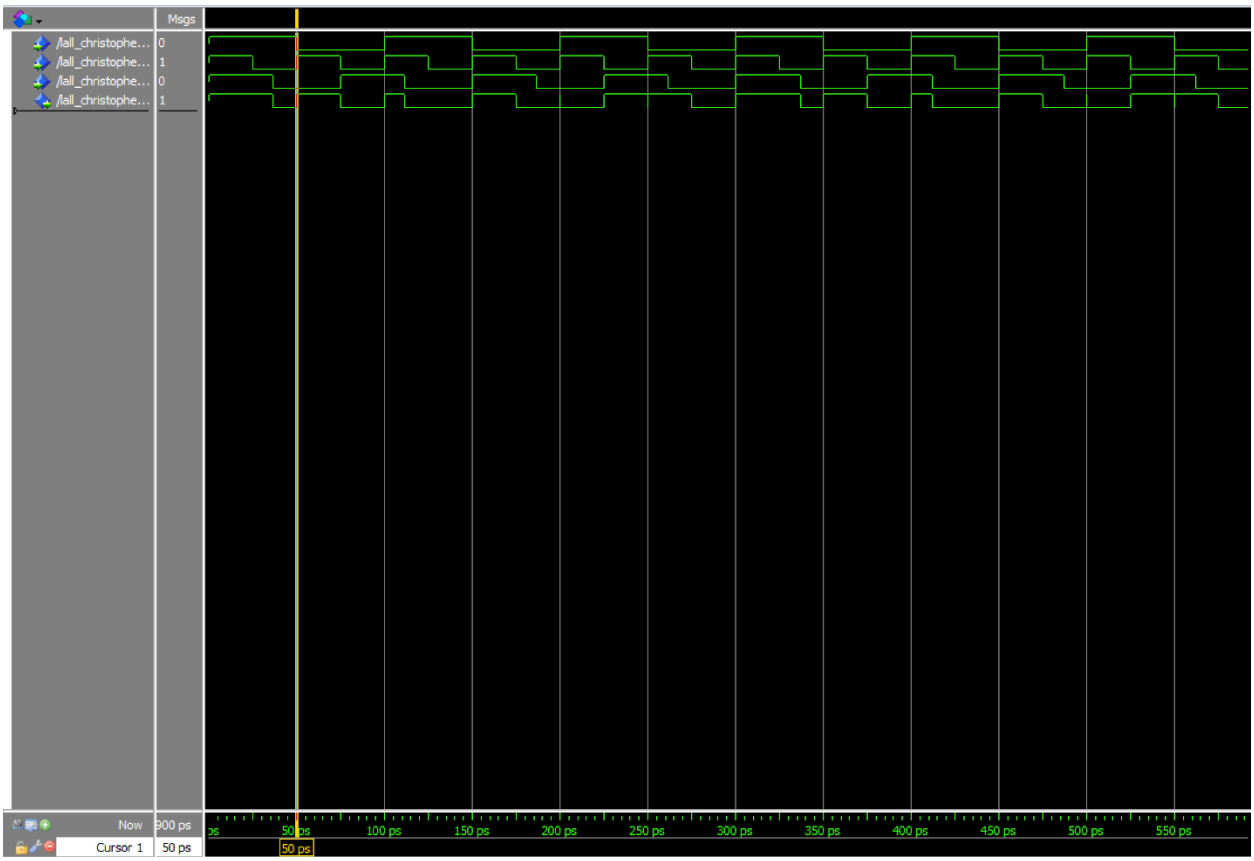

Figure 11. Example of 2 0's 2 1's

Section 3: Explanation and Analysis

Taking the 2-1 Mux VHDL file for the one-bit signals and putting it on Modelsim for waveforms we can see that the waveforms follow the truth table. Every input of the selector, input 1 and 2 we see that the output that is produced is correct. In the last few figures we can see that in the "MSGS" section the bits change so that we can compare it to the truth table respectively.

Section 4: Conclusion

I was able to familiarize myself with ModelSim and correctly match the 2-1 Mux file for the one-bit signal with the truth table. By looking at the waveform I can conclude that for the two inputs, the given output is correct.