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Lab #2 - Introduction to VHDL, ModelSim and Quartus using Comparators

CSc 342/343 – Professor Gertner

Due February 23, 2022

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Objective

This goal of this lab is to further understand Quartus, ModelSim, by using comparators. In this lab we will design 1-bit, 2-bit and 8-bit comparators.

Screenshots

1 Bit:

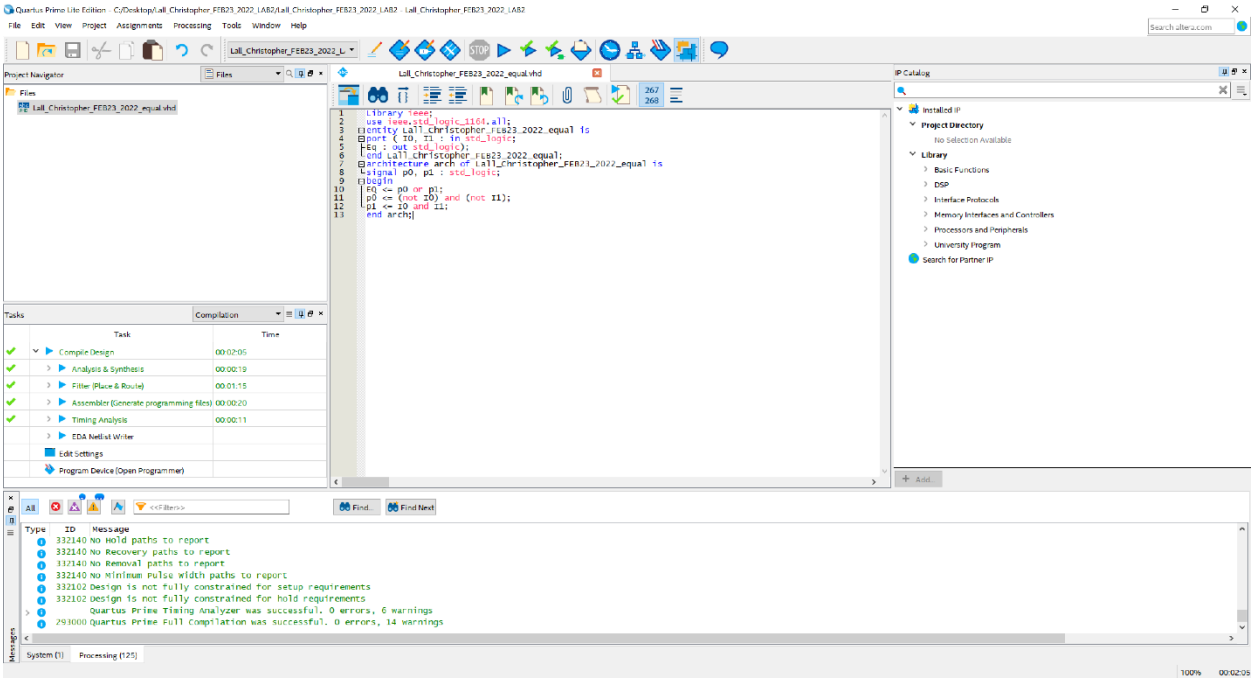


Figure 1. Compilation Report for 1 bit Quartus

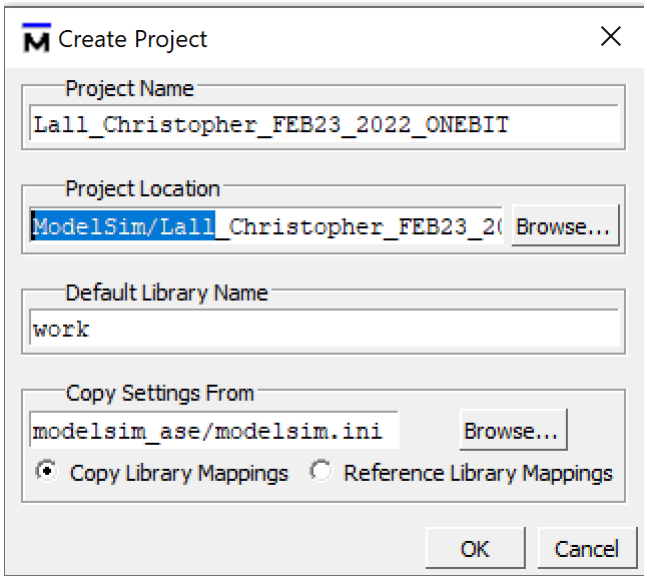


Figure 2. Create modelsim proj 1 bit

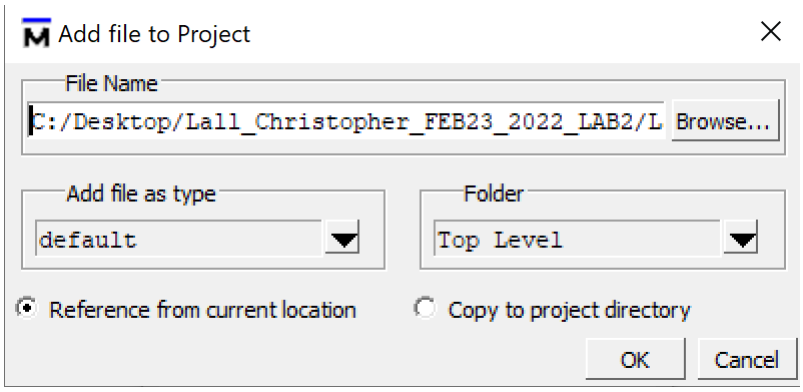


Figure 3. Adding File to Project

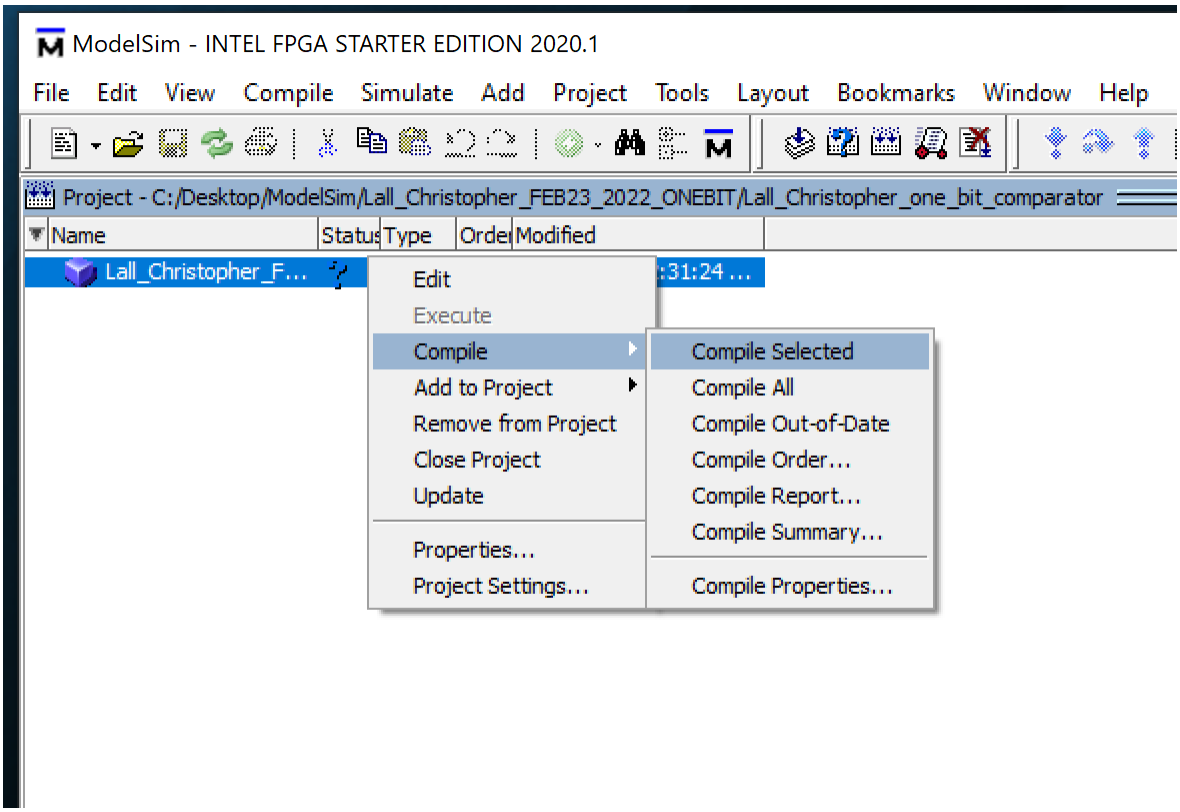


Figure 4. Compiling Project in Modelsim 1 bit

```
# reading C:/intelFPGA/20.1/modelsim_ase/win32aloem/../modelsim.ini
# Loading project Lall_Christopher_one_bit_comparator
# Compile of Lall_Christopher_FEB23_2022_equal.vhd was successful.
```

Figure 5. Successful Compile of 1 bit

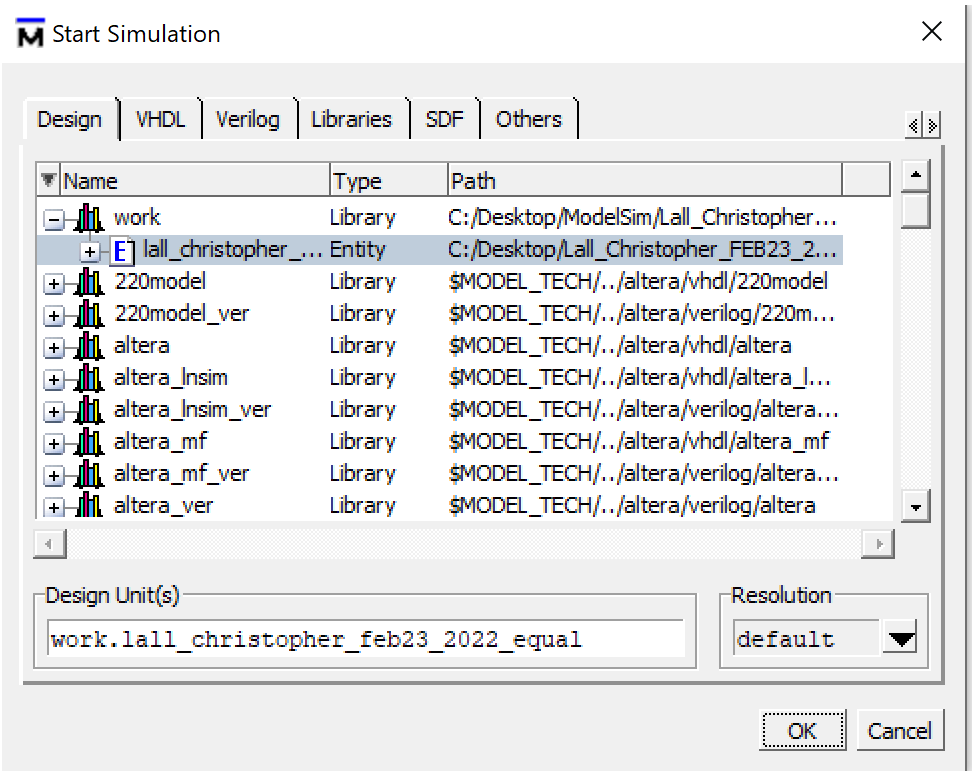


Figure 6. Starting Simulation 1 bit

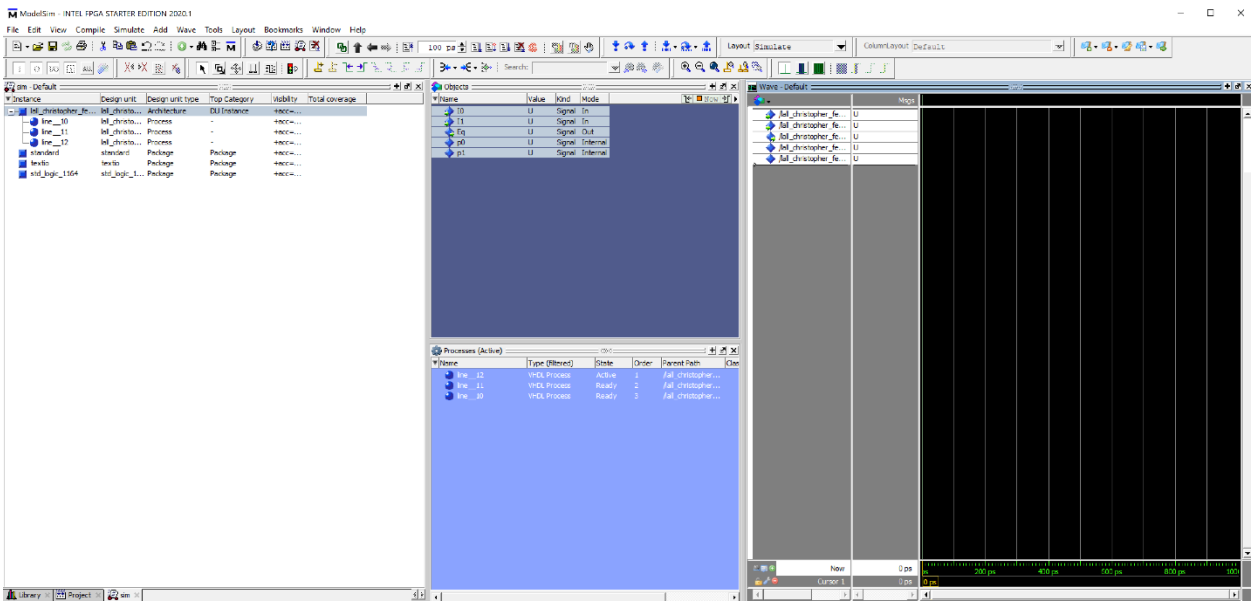


Figure 7. Dragging object for simulation 1 bit

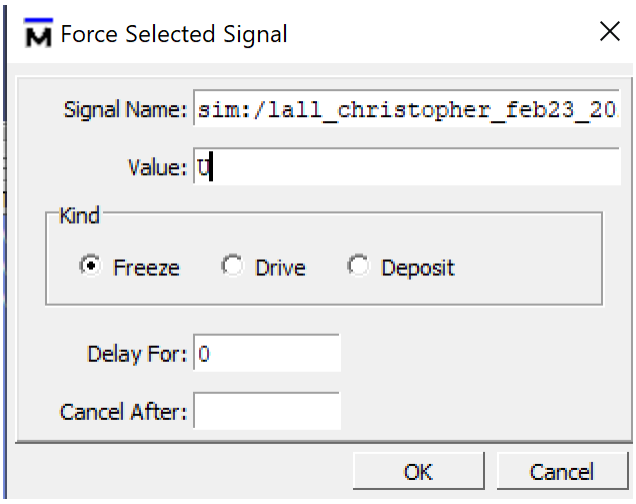


Figure 8. Force editing selected objects 1 bit

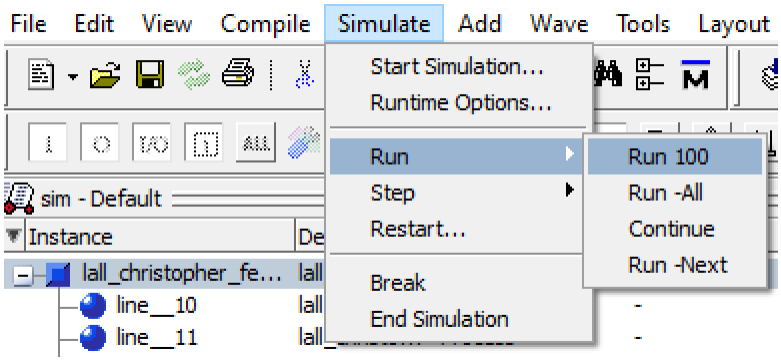


Figure 9. Running Project using run 100 for 1 bit

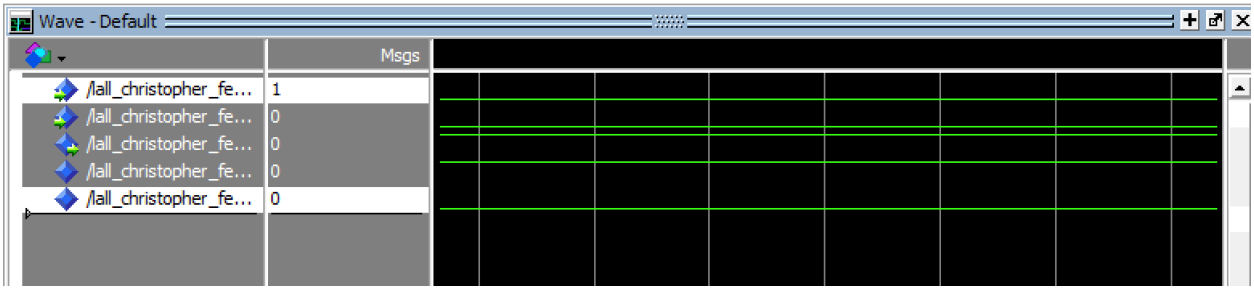


Figure 10. Waves for both forces as 0 for 1 bit

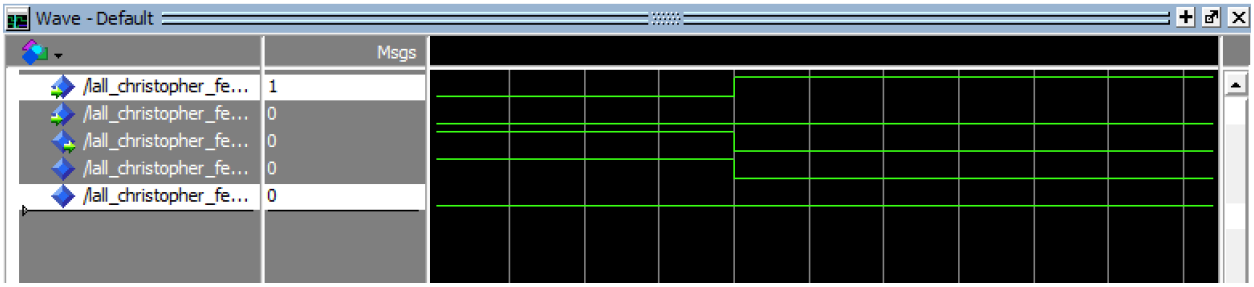


Figure 11. Waves for i0 as 1 force for 1 bit

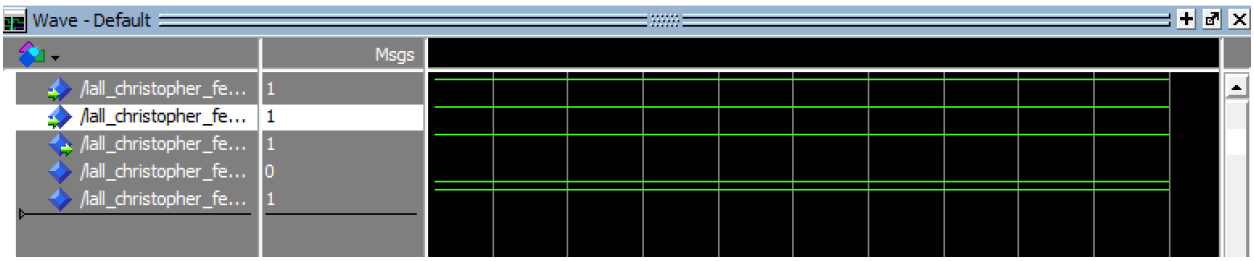


Figure 12. Waves for both 1 force for 1 bit

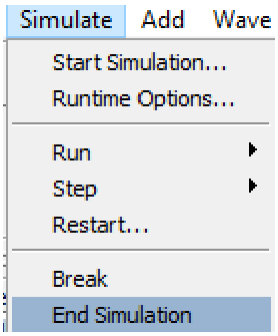


Figure 13. Ending the Simulation

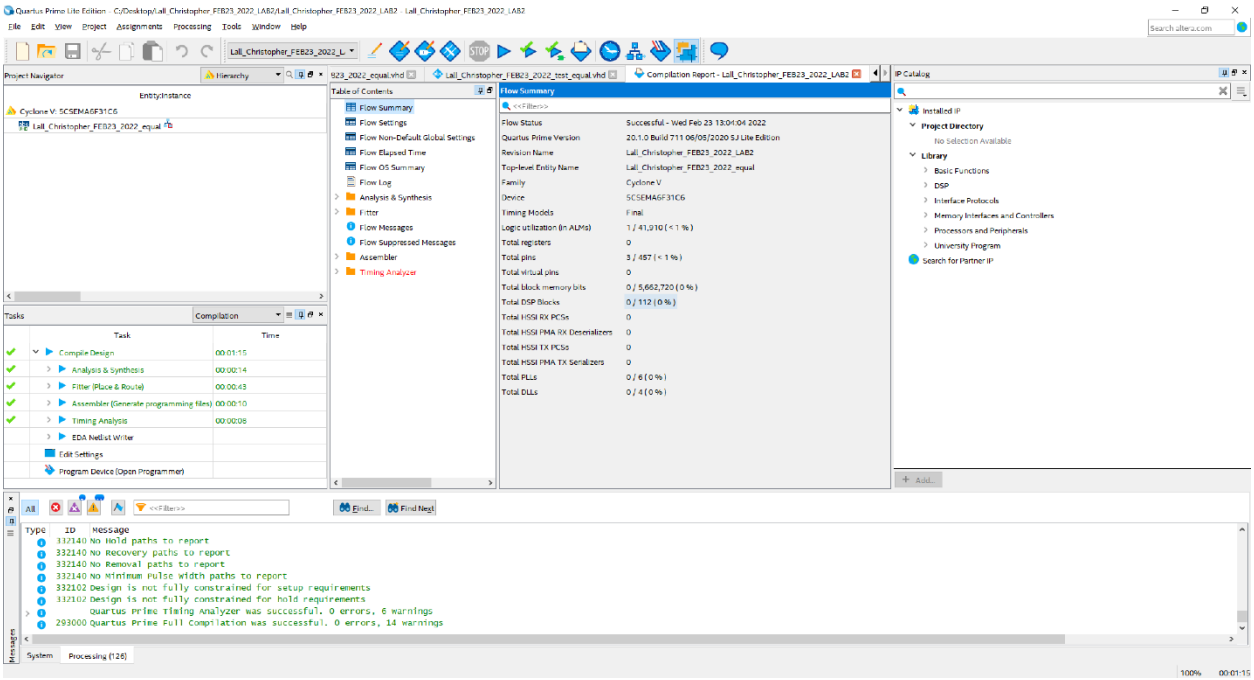


Figure 14. 1 bit test equal file in quartus, compilation report

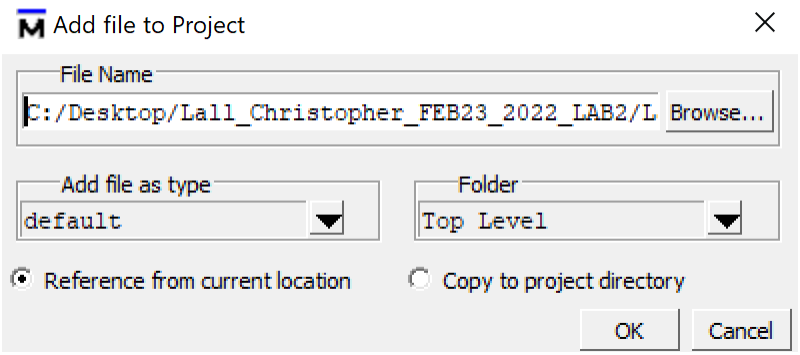


Figure 15. Adding Test Equal to modelsim proj for 1 bit

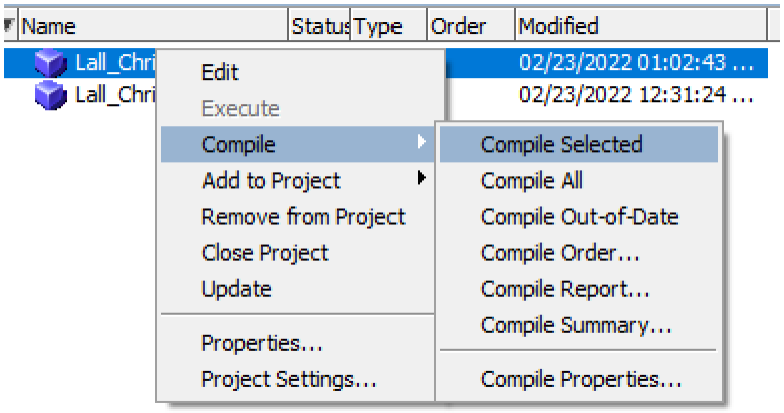


Figure 16. Compile test equal in modelsim

```
# Loading project Lall_Christopher_FEB23_2022_ONE_BIT_COMPARATOR
# Compile of Lall_Christopher_FEB23_2022_equal.vhd was successful.
# Compile of Lall_Christopher_FEB23_2022_test_equal.vhd was successful.
```

Figure 17. Successful compilation for 1 bit test equal

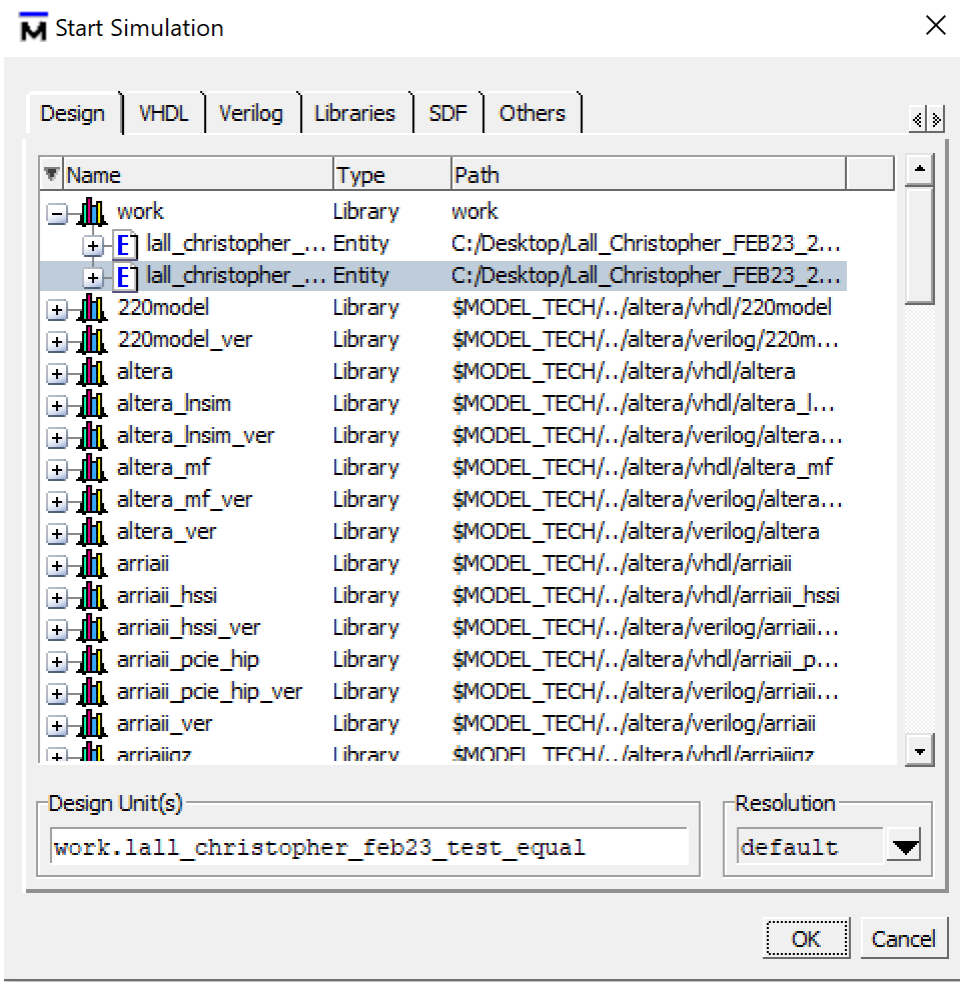


Figure 18. Starting Simulation for test equal 1 bit in modeslim

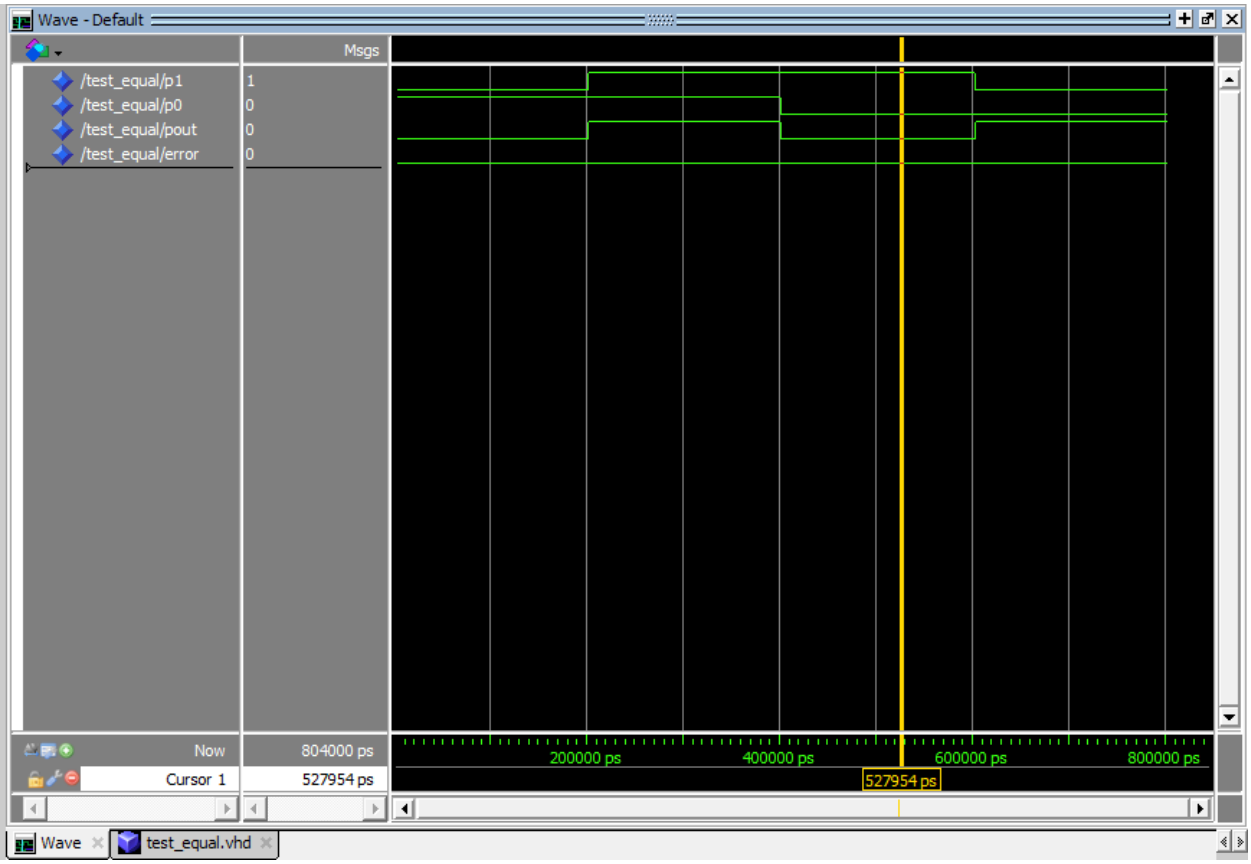


Figure 19. Waves for test equal in modelsim simulation

C:/Desktop/Lall_Christopher_FEB23_2022_LAB2/Lall_Christopher_FEB23_2022_test_equal.vhd (/lall_christopher_feb23_test_equal) - Default

```
Ln#
 9   port ( I0, I1 : in std_logic;
10   Eq : out std_logic );
11   end component;
12   signal p1, p0, pout : std_logic;
13   signal error : std_logic := '0';
14   begin
15   uut: Lall_Christopher_FEB23_equal port map (I0 => p0, I1 => p1, Eq => pout);
16   process
17   begin
18   p0 <= '1';
19   p1 <= '0';
20   wait for 1 ns;
21   if (pout = '1') then
22   error <= '1';
23   end if;
24   wait for 200 ns;
25   p0 <= '1';
26   p1 <= '1';
27   wait for 1 ns;
28   if (pout = '0') then
29   error <= '1';
30   end if;
31   wait for 200 ns;
32   p0 <= '0';
33   p1 <= '1';
34   wait for 1 ns;
35   if (pout = '1') then
36   error <= '1';
37   end if;
38   wait for 200 ns;
39   p0 <= '0';
40   p1 <= '0';
41   wait for 1 ns;
42   if (pout = '0') then
43   error <= '1';
44   end if;
45   wait for 200 ns;
46   if (error = '0') then
47   report "No errors detected. Simulation successful" severity
48   failure;
49   else
50   report "Error detected" severity failure;
51   end if;
52   end process;
53   end arch_test;
54
```

Figure 20. File Popup

```
# ** Failure: No errors detected. Simulation successful
```

Figure 21. No errors detected 1 bit test equal, 1 bit test

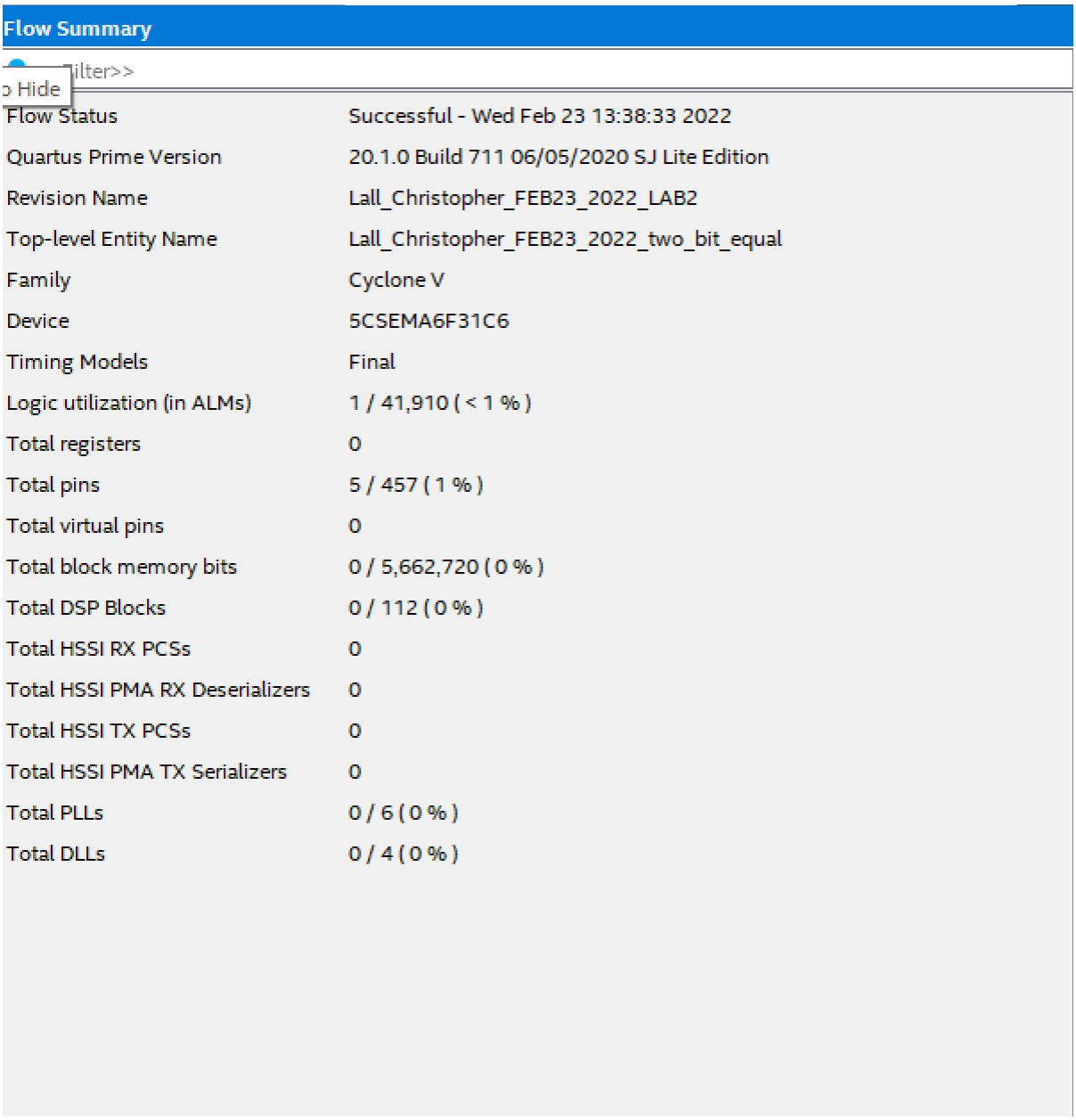
2 Bit:

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Feb 23 13:28:59 2022
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Lall_Christopher_FEB23_2022_LAB2
Top-level Entity Name	Lall_Christopher_FEB23_2022_two_bit_equal
Family	Cyclone V
Device	5CSEMA6F31C6
Timing Models	Final
Logic utilization (in ALMs)	1 / 41,910 (< 1 %)
Total registers	0
Total pins	5 / 457 (1 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Figure 22. Compilation Report 2 bit



Flow Summary

ilter>>

Hide

Flow Status	Successful - Wed Feb 23 13:38:33 2022
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Lall_Christopher_FEB23_2022_LAB2
Top-level Entity Name	Lall_Christopher_FEB23_2022_two_bit_equal
Family	Cyclone V
Device	5CSEMA6F31C6
Timing Models	Final
Logic utilization (in ALMs)	1 / 41,910 (< 1 %)
Total registers	0
Total pins	5 / 457 (1 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Figure 23. Compilation Report 2 bit test

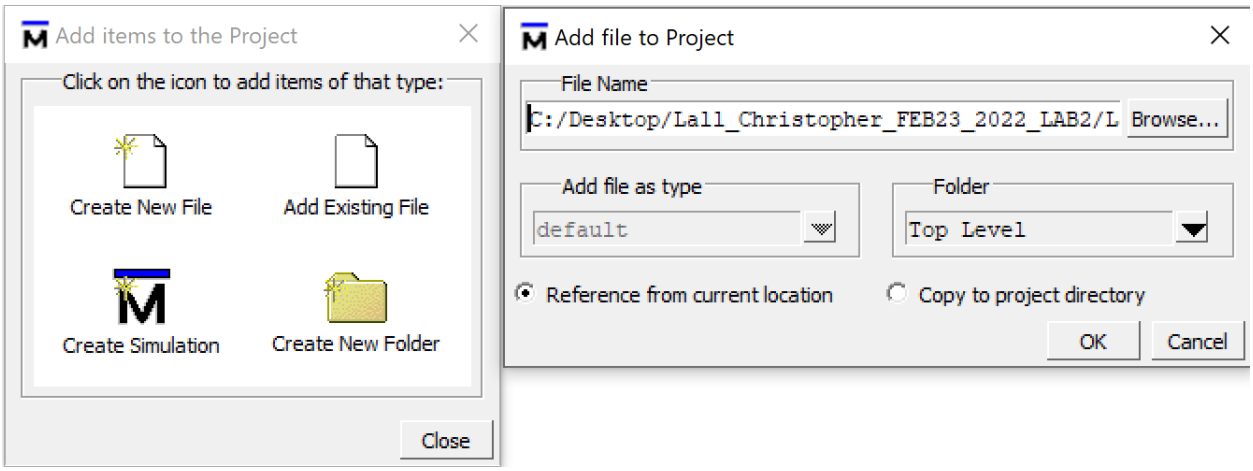


Figure 24. Adding Files to Project 2 bit

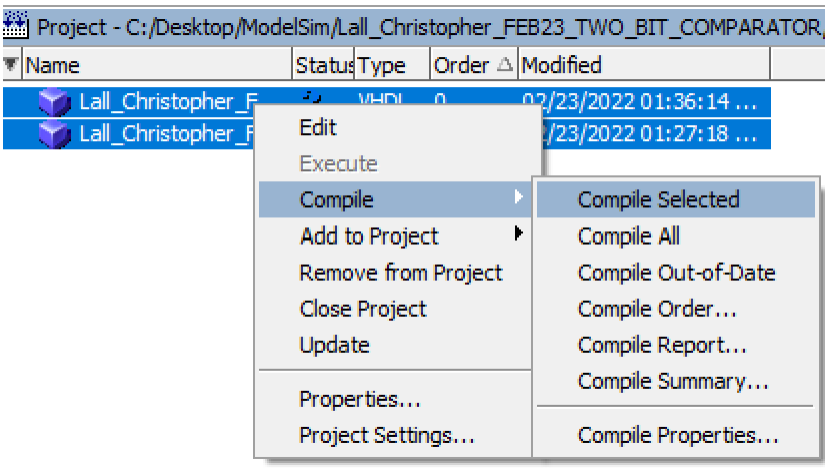


Figure 25. Compiling 2 bit files

```
# Compile of Lall_Christopher_FEB23_2022_test_two_bit_equal.vhd was successful.
# Compile of Lall_Christopher_FEB23_2022_two_bit_equal.vhd was successful.
```

Figure 26. Compilation

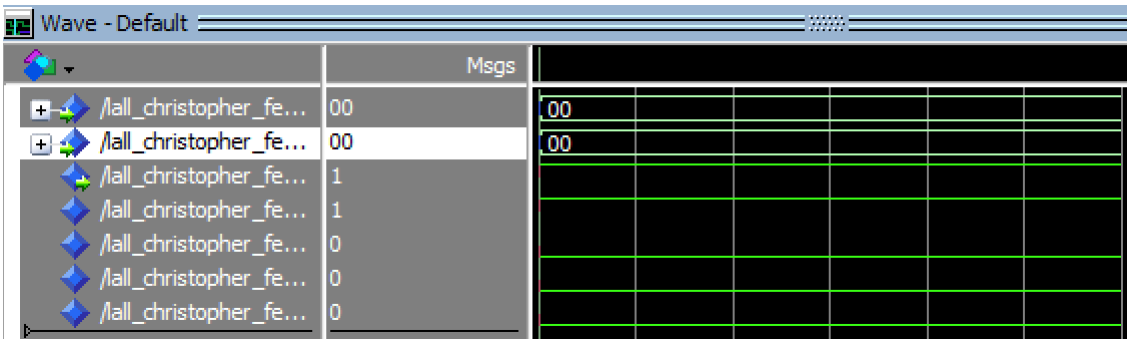


Figure 27. All 0's

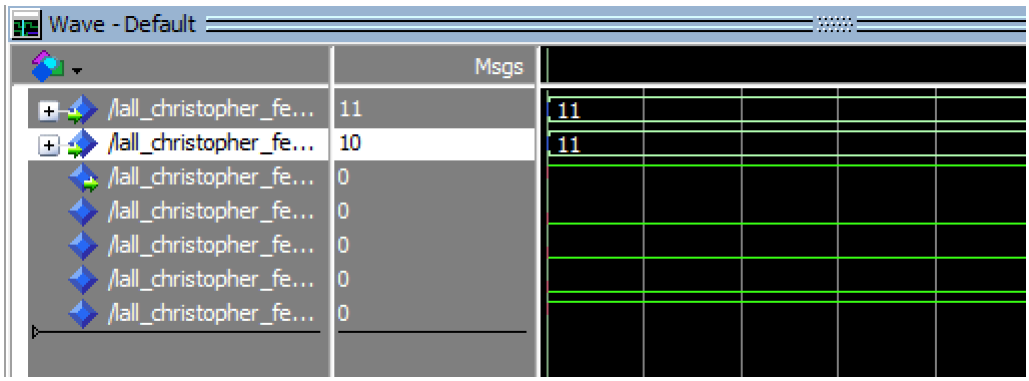


Figure 28. All 1's

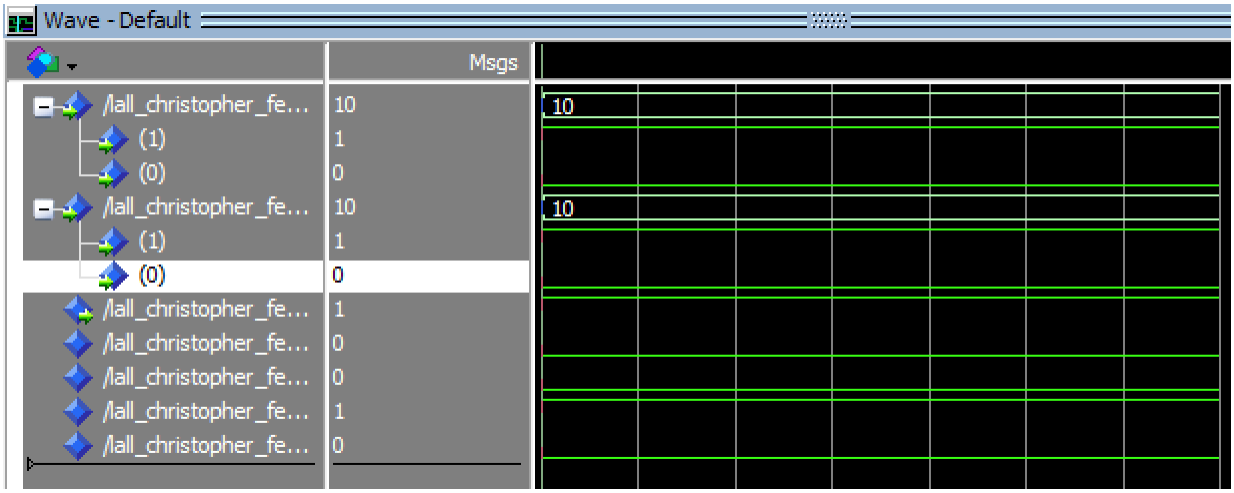


Figure 29. 10 10 2 bit

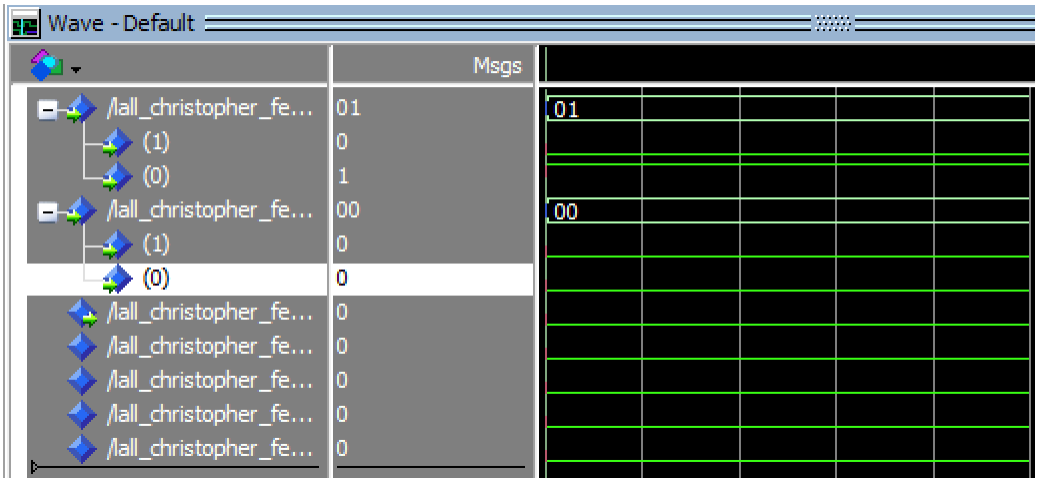


Figure 30. 01 00 1 bit

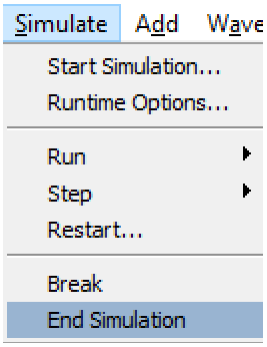


Figure 31. End 2 bit Sim

```
Ln#                                                                    Now
40    wait for 200 ns;
41    p0 <= "11";
42    p1 <= "00";
43    wait for 1 ns;
44    if (pout = '1') then
45                    error <= '1';
46    end if;
47    wait for 200 ns;
48    p0 <= "11";
49    p1 <= "11";
50    wait for 1 ns;
51    if (pout = '0') then
52                    error <= '1';
53    end if;
54    wait for 200 ns;
55    p0 <= "10";
56    p1 <= "11";
57    wait for 1 ns;
58    if (pout = '1') then
59                    error <= '1';
60    end if;
61    wait for 200 ns;
62    p0 <= "10";
63    p1 <= "10";
64    wait for 1 ns;
65    if (pout = '0') then
66                    error <= '1';
67    end if;
68    wait for 200 ns;
69    p0 <= "11";
70    p1 <= "01";
71    wait for 1 ns;
72    if (pout = '1') then
73                    error <= '1';
74    end if;
75    wait for 200 ns;
76
77    if (error = '0') then
78                                    report "No errors detected. Simulation successful" severity
79    failure;
80                    else
81                                            report "Error detected" severity failure;
82    end if;
83    end process;
84    end arch_test;
85
```

Figure 32. File Error

8 Bit:

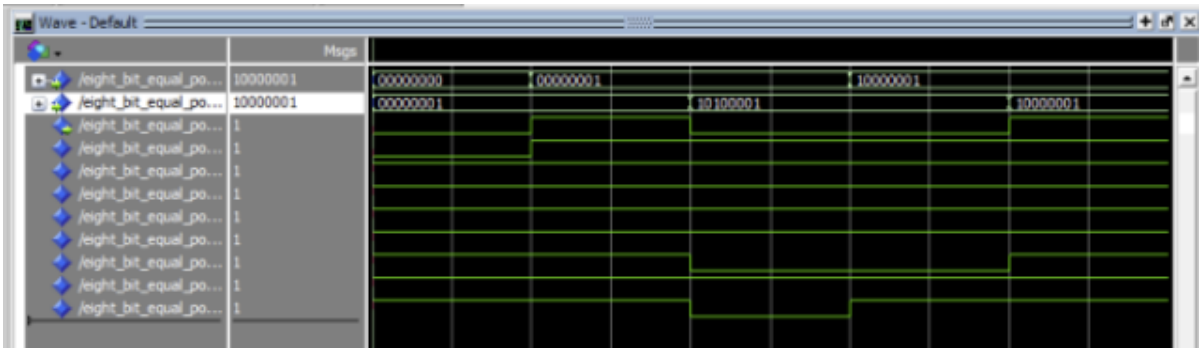


Figure 33. 8 bit waves

```
library ieee;
use ieee.std_logic_1164.all;
entity eight_bit_equal_port is
        port(a, b: in std_logic_vector(7 downto 0);
            aeqb : out std_logic);
end eight_bit_equal_port;

architecture arch of eight_bit_equal_port is
    component equal
    port (
            I0, I1: in std_logic;
            Eq : out std_logic);
    end component;
    signal e0,e1,e2,e3,e4,e5,e6,e7: std_logic;
    begin

    H1: equal port map(i0=>a(0), i1=>b(0), eq=>e0);
    H2: equal port map(i0=>a(1), i1=>b(1), eq=>e1);
    H3: equal port map(i0=>a(2), i1=>b(2), eq=>e2);
    H4: equal port map(i0=>a(3), i1=>b(3), eq=>e3);
    H5: equal port map(i0=>a(4), i1=>b(4), eq=>e4);
    H6: equal port map(i0=>a(5), i1=>b(5), eq=>e5);
    H7: equal port map(i0=>a(6), i1=>b(6), eq=>e6);
    H8: equal port map(i0=>a(7), i1=>b(7), eq=>e7);
    aeqb <= e0 and e1 and e3 and e4 and e5 and e6 and e7;

end arch;
```

Figure 34.8 bit file

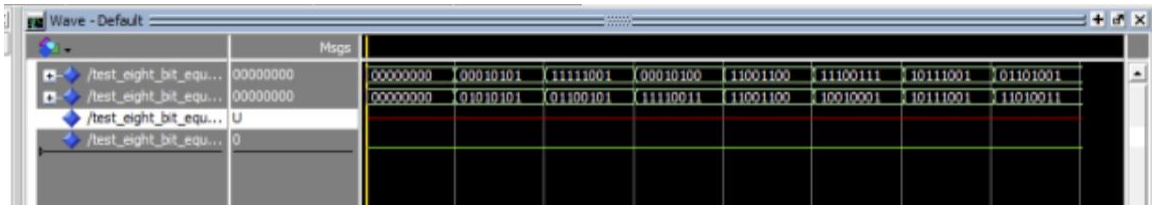


Figure 35. 8 bit test waves, unsure why redline

```
library ieee;
use ieee.std_logic_1164.all;

entity test_eight_bit_equal_port_map is
end test_eight_bit_equal_port_map;

architecture arch_test of test_eight_bit_equal_port_map is
component eight_bit_equal_port_map
    port( a, b : in std_logic_vector(7 downto 0);
          aeqb  : out std_logic);
end component;

signal p1, p0 : std_logic_vector(7 downto 0);
signal pout   : std_logic;
signal error  : std_logic:= '0';
begin
    uut: eight_bit_equal_port_map port map(a => p0, b => p1, aeqb => pout);
    process
     begin
        p0 <= "00000000";
        p1 <= "00000000";

        wait for 1 ns;
        if(pout = '0') then
            error <= '1';
        end if;

        wait for 200 ns;
        p0 <= "01010101";
        p1 <= "00010101";
        wait for 1 ns;

        if(pout = '1') then
            error <= '1';
        end if;

        wait for 200 ns;
        p0 <= "01100101";
        p1 <= "11111001";
        wait for 1 ns;
```

Figure 36. 8 bit test file

Explanation & analysis

In the above screenshots, you can see that I went through each 1 bit, 2 bit, and 8 bit comparator vhdl files. I then compiled each to make sure that there were no errors. After doing this, I then imported the files to modelsim to run simulations on them. The results above tell us that we were able to successfully get the right results for the most part. I was also introduced to the comparators and these created comparator files allowed us to visualize the waveforms in which we compared to the truth table. We then verify our results and conclude that it matches with the truth table.

Conclusion

In conclusion, I was able to created the 1 bit, 2 bit, and 8 bit comparator vhdl files by following the tutorial. Once it was simulated in modelsim, I was able to verify that the waves matched the truth table. With this being said I learned how to more familiarize myself with project creation and simulations.