ELECENG 3EJ4 - Electronic Devices and Circuits II

Lab 2 – Single-Stage Amplifiers

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06Oct2024

Questions for Part 1

Q1. Based on the simulation and graphs from step 1.2, $V_{O, min}$ = -3V and I_O = 0.000184825A. The measured data in Step 1.10 shows similar behavior as $V_{O, min}$ = -3V and I_O = 0.0001985A. In step 1.2, the range of R_O is between 4.07E+06 and -2.41E+06. In the measured step 1.10, R_O is within the range of 2.47E+07 and -1.23E+07.

The graph below shows the simulated results from Step 1.2.

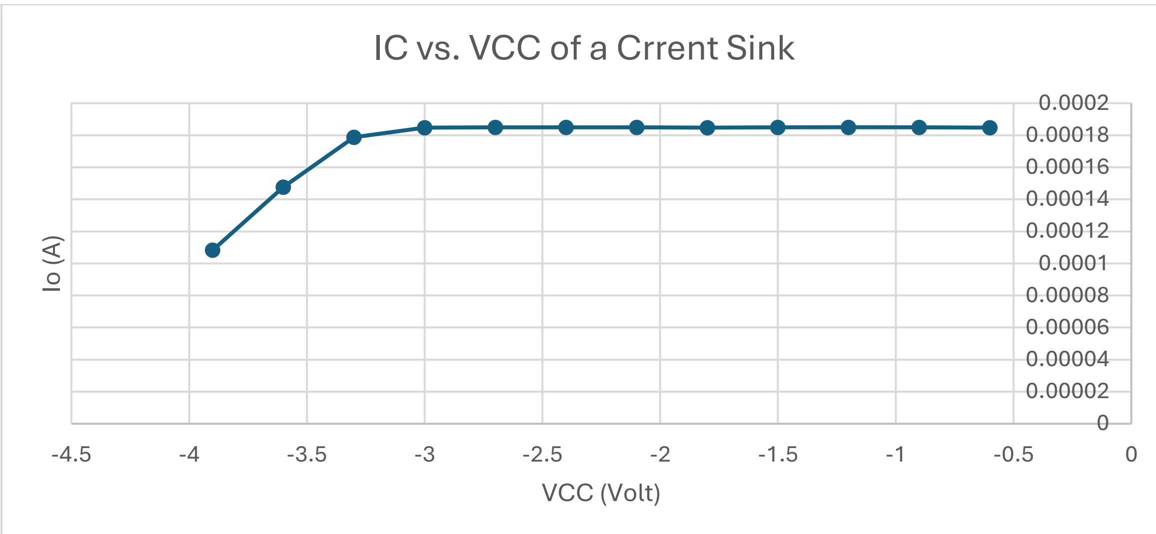


Figure 1 - Step 1.2 Simulation Results

The graph below shows the measured results from Step 1.10.

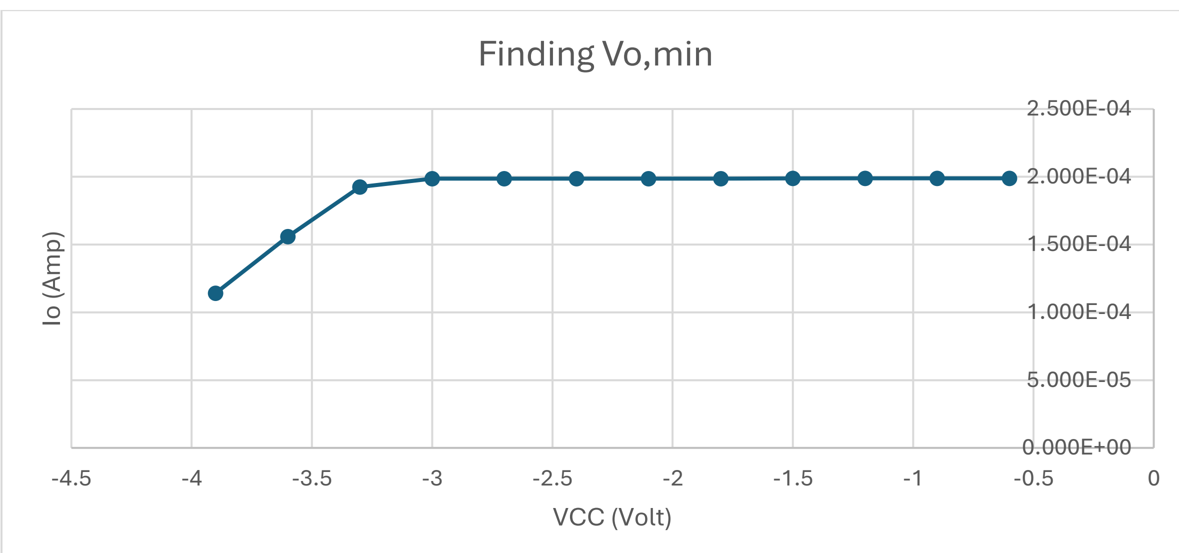


Figure 2 - Step 1.10 Measured results

Q2. In step 1.5, the value for V_{O1} = 4.9404V and V_{O2} = -3.5783V. In this case, the circuit is not functioning as an amplifier because Vsig is not within the required voltage range. Therefore, the obtained values are approximately the minimum and maximum values for the circuit outputs.

Q3. Plot of the simulated DC V_O vs. V_{sig}:

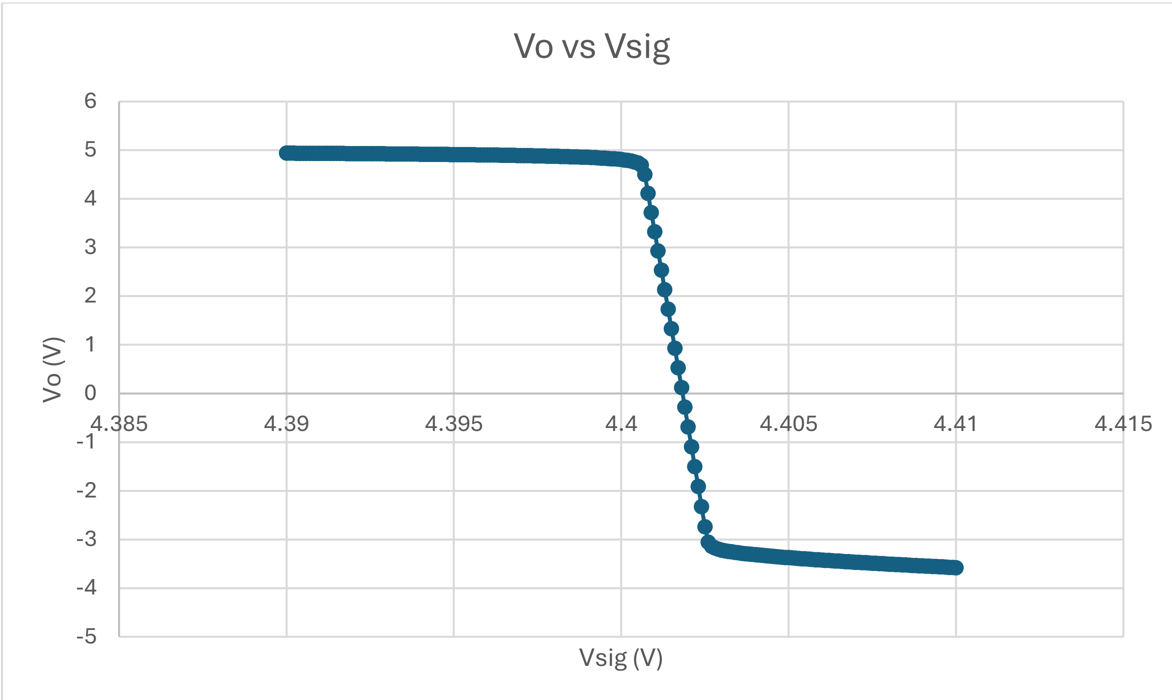


Figure 3 - Step 1.6 Simulated results

As shown in the graph above, V_O is initially positive and the BJT is on. During amplification, the graph is slanted downwards while the DC component of V_{sig} is between 4.4006V and 4.4027V. A this time the output voltage V_O is between 4.469 and -3.139V. When V_O = 0V, the value of V_{sig} = 4.4018V and current I_C of Q2 is 0.00018488A.

A plot was generated for the DC V_O vs. V_{sig} data measured in part 1.16, shown below

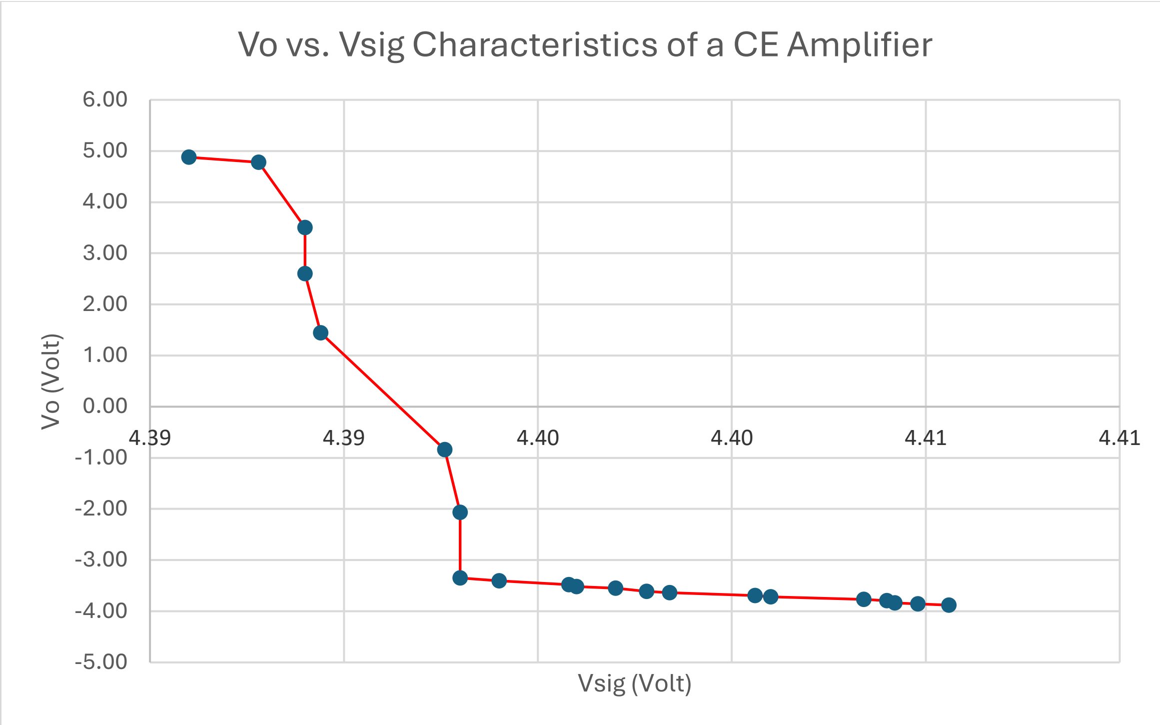


Figure 4 - Step 1.16 Measured results

Q4. To calculate the magnitude and phase of the intrinsic voltage gain A_{VO} at a low frequency,

A_{VO} = 20*log(V_O/V_i)

A_{VO} = 20*log(4.047106395/0.002)

A_{VO} = 66.86dB

Phase = 179.598 °

In the upper 3-dB range:

A_{VO} = 20*log(V_O/V_i)

A_{VO} = 20*log(2.8723/0.002)

A_{VO} = 63.14dB

Phase = 135.511°

Frequency = 14077.15 Hz

The Waveforms screenshot can be found below:

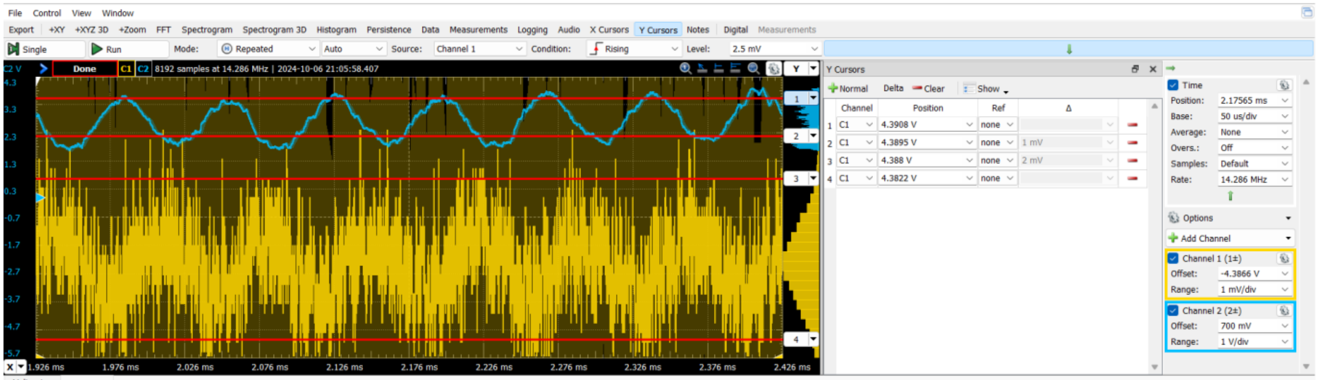


Figure 5 - Step 1.19 Waveform results

The gain was found to be 61dB, similar to the simulation results.

Questions for Part 2

Q5. Based on the simulation results in step 2.2, when VCM = 0V, VE = -0.525365259V, VO = 4.249991V, and IC2 = 9.10E-05A.

The input common-mode range is -2.7V and 4.5V, at which point the same output voltage is maintained. The bounds are determined by the required voltage for the BJT to act in the saturation region. The measured data can be used to confirm these findings.

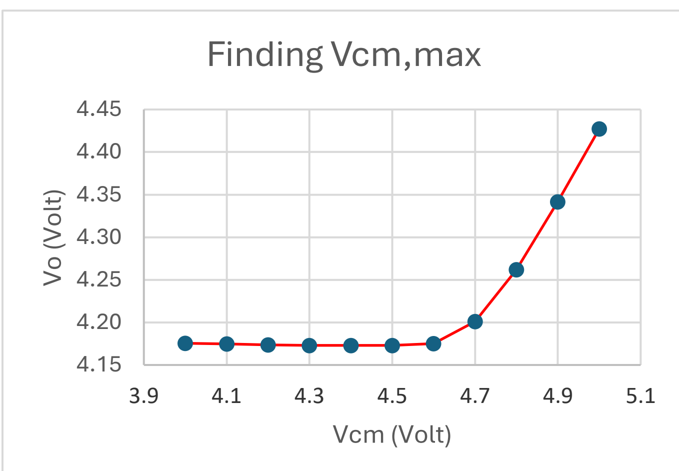


Figure 7 - Step 2.7 results

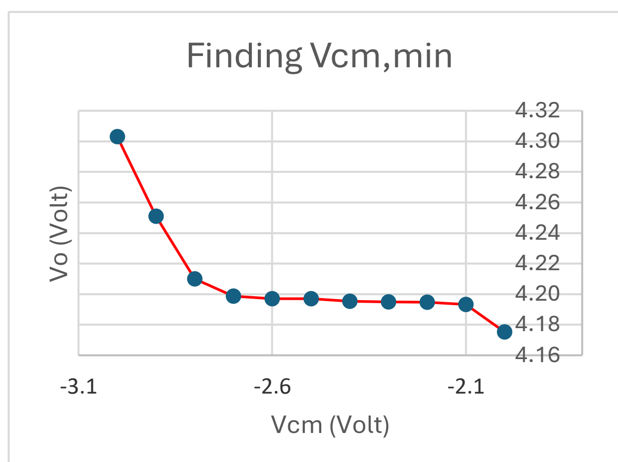


Figure 6 - Step 2.8 results

The graphs confirm that $V_{CM,max}$ is approximately 4.6V,and $V_{CM,min}$ is approximately -2.7V. These values represent the max and min when the voltage is constant.

Q6. Based on simulated data from Step 2.3, the low frequency volage gain A_{CM} at the lowest frequency of 0.1Hz is -86.90dB, and at 100Hz it is -86.24 dB.

Questions for part 3.

Q7. The simulated I_c vs V_{id} characteristics from Step 3.2 are shown in the graph below.

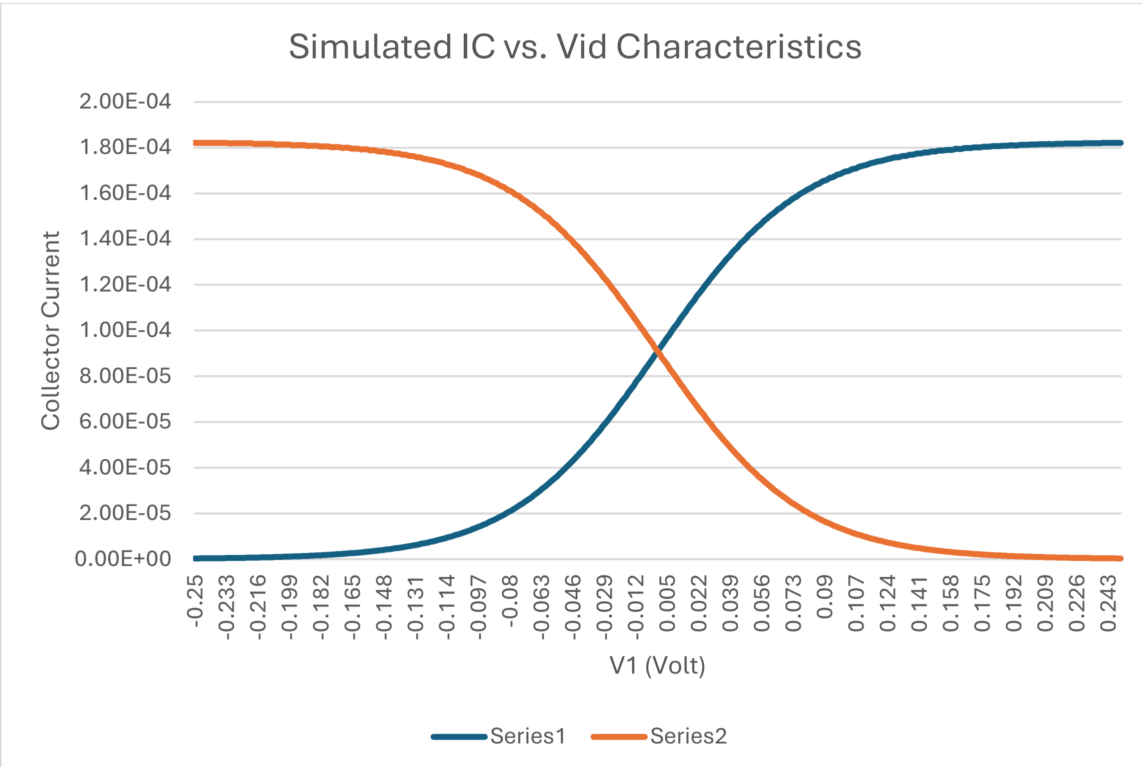


Figure 8 - Step 3.2 Results

V_T for a BJT is 0.025V. Using textbook section 9.2.3, the limitations for the differential input are $\pm V_T/2$ for AC, and $\pm 4V_T$ for DC. From the graph above, the intersection of series 1 and series 2 occurs at V1=0.003. Therefore, the AC range is -9.5mV to 15.5mV, and the DC range is -97mV to 103mV. The upper and lower bounds of these input differential-mode ranges are centered around the intersection of the series. Therefore, the circuit operates as a linear amplifier within the range $V_T/2$.

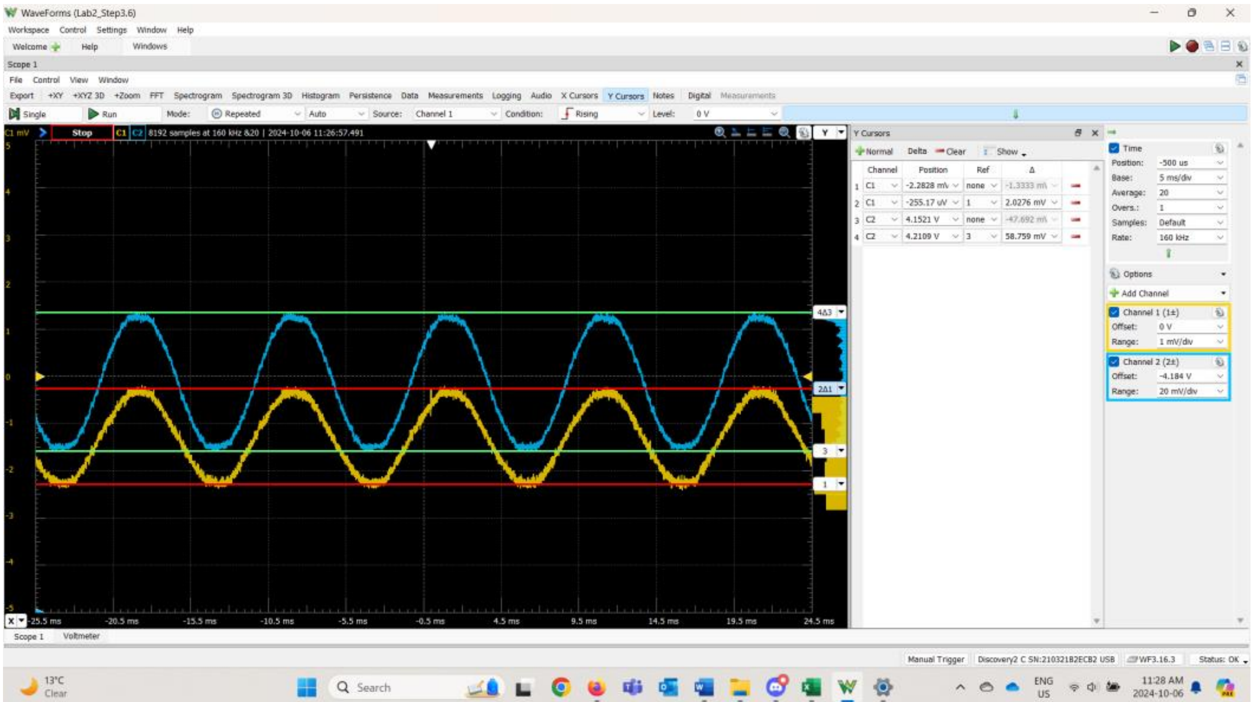
Q8. Based on the simulation data in step 3.3, the voltage gain A_d is 19.63dB for the differential-mode signal. The upper 3-dB frequency is 8145kHz which occurs at a phase of -44.7. To calculate the Gain-bandwidth product:

$19.63 = 20*\log(V_O/V_i)$

GB = (9.58297)(8145.282kHz) = 78088.54kHz

The upper 3-db frequency in Q4 was 14077.15 Hz. This is much smaller compared to the 8145kHz 3-db frequency derived in Q8.

Measurements were taken in Step 3.7 and the following waveform screenshot is provided.



The amplitudes for channel 1 and channel 2 were calculate, yielding a differential voltage gain A_v = 23.2dB.

Q9. The common-mode rejection ratio can be calculated as follows:

CMRR = $|A_d|$ / $|A_{CM}|$

CMRR = |19.63V| / |-86.9|

CMRR = 0.2269dB