ELECENG 3EJ4:Electronic Devices and Circuits II

Lab 3: Multistage Amplifiers

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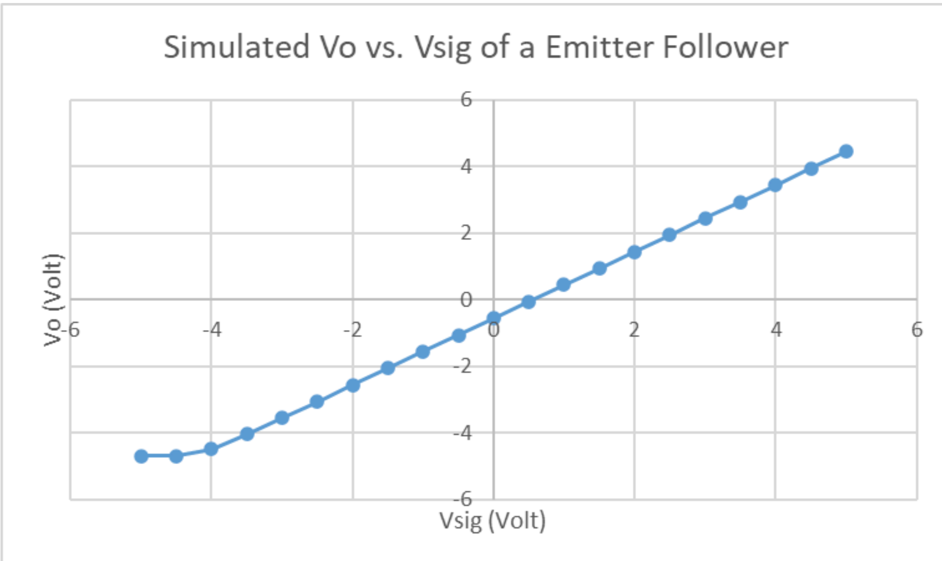
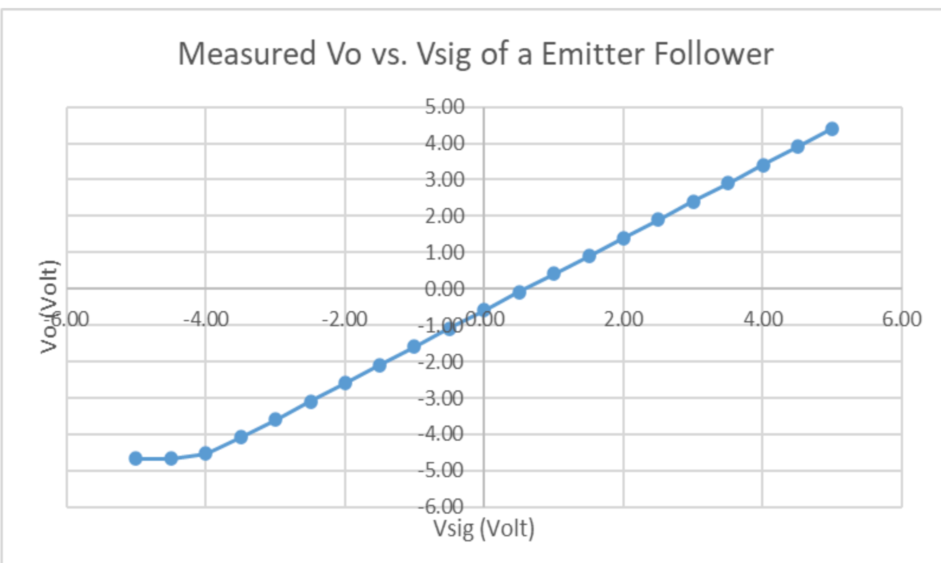
Questions for Part 1

1. a) The graphs for the simulated and measured Vo vs Vsig characteristics are shown in the graphs below.





The graphs demonstrate a linear relationship between Vo and Vsig, trending upwards. Both graphs portray the same overall shape and range of both Vo and Vsig values.

b) To ensure the circuit works as a common-collector (CC) amplifier, the DC input range for Vsig is between -4.5V and 5V. Based on collected data, the corresponding output Vo range is between -4.6 and 4.5V.

c) When Vsig = 0.5V, Vo ≈ 0.

2. In step 1.3, the simulated intrinsic voltage gain is 0.00dB with a phase of -8.47E-5°. In step 1.8, the measured intrinsic voltage gain is 0.8dB with a phase of -8.47E-5°.

Questions for Part 2

Q3. a) Based on the textbook section, if Q2 is matched to Q1 (when the EBJ area of Q2 is equal to the EBJ area of Q1), then Io = IREF.

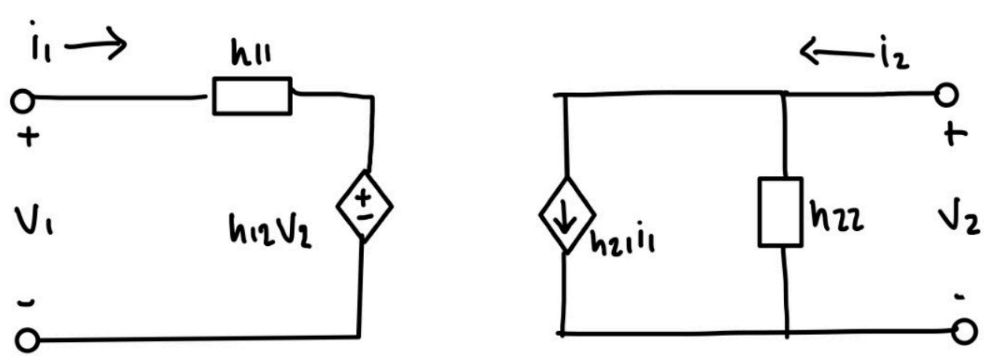
b) Based on the simulation data, when IREF = 0.0001A, Io = 0.000104A. When IREF = 0.001A, Io = 0.000975A.

3) Theoretically, IREF and Io should be equal values. However, when simulated, there was a small discrepancy between Io and IREF in each case. When IREF was 0.1mA, Io was different by 0.04A. When IREF was 1mA, Io was different by 0.025A. Therefore, the simulated values were very close to the theoretical values, and the differences can be attributed to simulation parameters and circumstances.

Q4. a) Based on the simulation data obtained in step 2.5, the output impedance
h11 = Rin = 389.12 Ω. The current gain h21 = Ai = 1.04 A/A.

b) Based on the simulation data obtained in step 2.6, the output impedance Ro = 1.58E6 Ω.

c) the linear two-port network for the current mirror using h-parameters is shown below:



With h parameters from the excel sheet:

h11 = Rin = 389.12 Ω
h12 = 7.05E-07 V/V (at 100Hz) to h12 = 1.41E-06 V/V (at 200Hz)
h21 = 1.04 A/A
h22 = 1.01E-04 S

Questions for Part 3

Q5. a) Based on the simulation data obtained in step 3.2, the voltage gain Ad = 70.07dB.

b) In step 3.6, there was a mismatch of 0.00725V observed. This value was used as the offset voltage applied at V2.

c) The measured gain in step 3.8 was observed as 58.9dB. This value is smaller than the gain recorded in step 3.2, which was 70.07dB. This discrepancy can be attributed to the noise from the AD2, and the fact that the exact placement of the Y cursors to perform the measurements are subjective based on the user.

Q6. At low frequencies, the Vo amplitude is 6.3786V. 70.7% of this low frequency value is (0.707)(6.3786V) = 4.5096V. In sheet 3.2, this magnitude corresponds to the frequency 11207.40201Hz.

Q7. In Q8 of Lab 2, the upper 3-dB frequency was determined to be 8145kHz. This is much greater than the 11KHz found in Q6 if lab 3. The differential amplifier with a current mirror load has this smaller 3dB frequency because of increased effective capacitance at the amplifier input. This is called the Miller effect, which reduces the direct gain of an amplifier at high frequencies.

Q8. With the resistive load in Lab 2, the GBW was 7.95E+07Hz. With the current mirror load in Lab 3, GBW was 3.57E+07Hz.