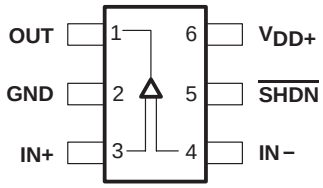
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS220J − JULY 1998 − REVISED FEBRUARY 2004

- **Rail-to-Rail Output Swing**
- **Gain Bandwidth Product . . . 6.4 MHz**
- **±80 mA Output Drive Capability**
- **Supply Current . . . 500 μA/channel**
- **Input Offset Voltage . . . 100 μV**
- **Input Noise Voltage . . . 11 nV/√Hz**
- **Slew Rate . . . 1.6 V/μs**
- **Micropower Shutdown Mode (TLV2460/3/5) . . . 0.3 μA/Channel**
- **Universal Operational Amplifier EVM**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards**

TLV2460
DBV PACKAGE
(TOP VIEW)



description

The TLV246x is a family of low-power rail-to-rail input/output operational amplifiers specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4 MHz of bandwidth and 1.6 V/μs of slew rate with only 500 μA of supply current, providing good ac performance with low power consumption. Three members of the family offer a shutdown terminal, which places the amplifier in an ultralow supply current mode (I_{DD} = 0.3 μA/ch). While in shutdown, the operational-amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 μV.

This family is available in the low-profile SOT23, MSOP, and TSSOP packages. The TLV2460 is the first rail-to-rail input/output operational amplifier with shutdown available in the 6-pin SOT23, making it perfect for high-density circuits. The family is specified over an expanded temperature range (T_A = −40°C to 125°C) for use in industrial control and automotive systems, and over the military temperature range (T_A = −55°C to 125°C) for use in military systems.

SELECTION GUIDE

DEVICE	V_{DD} [V]	V_{IO} [μV]	I_{DD}/ch [μA]	I_{IB} [pA]	GBW [MHz]	SLEW RATE [V/μs]	$V_{n,\ 1\ kHz}$ [nV/√Hz]	I_O [mA]	SHUTDOWN	RAIL-RAIL
TLV246x(A)	2.7−6	150	550	1300	6.4	1.6	11	25	Y	I/O
TLV277x(A)	2.5−5.5	360	1000	2	5.1	10.5	17	6	Y	O
TLV247x(A)	2.7−6	250	600	2.5	2.8	1.5	15	20	Y	I/O
TLV245x(A)	2.7−6	20	23	500	0.22	0.11	52	10	Y	I/O
TLV225x(A)	2.7−8	200	35	1	0.2	0.12	19	3	—	—
TLV226x(A)	2.7−8	300	200	1	0.71	0.55	12	3	—	—

TLV2460C/I/AI and TLV2461C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D)	SOT-23† (DBV)	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	2000 µV	TLV2460CD TLV2461CD	TLV2460CDBV TLV2461CDBV	VAOC VAPC	TLV2460CP TLV2461CP
−40°C to 125°C	2000 µV	TLV2460ID TLV2461ID	TLV2460IDBV TLV2461IDBV	VAOI VAPI	TLV2460IP TLV2461IP
	1500 µV	TLV2460AID TLV2461AID	— —	— —	TLV2460AIP TLV2461AIP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2460M/AM/Q/AQ and TLV2461M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (JG)	CERAMIC FLATPACK (U)	CHIP CARRIER (FK)
−40°C to 125°C	2000 µV	TLV2460QD TLV2461QD	TLV2460QPW TLV2461QPW	— —	— —	— —
	1500 µV	TLV2460AQD TLV2461AQD	TLV2460AQPW TLV2461AQPW	— —	— —	— —
−55°C to 125°C	2000 µV	— —	— —	TLV2460MJG TLV2461MJG	TLV2460MU TLV2461MU	TLV2460MFK TLV2461MFK
	1500 µV	— —	— —	TLV2460AMJG TLV2461AMJG	TLV2460AMU TLV2461AMU	TLV2460AMFK TLV2461AMFK

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460QDR).

TLV2462C/I/AI and TLV2463C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE† (D)	MSOP (DGK)	SYMBOL	MSOP† (DGS)	SYMBOL	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C to 70°C	2000 µV	TLV2462CD TLV2463CD	TLV2462CDGK —	xxTIAAI	— TLV2463CDGS	— xxTIAAK	— TLV2463CN	TLV2462CP —
−40°C to 125°C	2000 µV	TLV2462ID TLV2463ID	TLV2462IDGK —	xxTIAAJ	— TLV2463IDGS	— xxTIAAL	— TLV2463IN	TLV2462IP —
	1500 µV	TLV2462AID TLV2463AID	— —	— —	— —	— —	— TLV2463AIN	TLV2462AIP —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2462M/AM/Q/AQ and TLV2463M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (JG)	CERAMIC DIP (J)	CERAMIC FLATPACK (U)	CHIP CARRIER (FK)
−40°C to 125°C	2000 µV	TLV2462QD TLV2463QD	TLV2462QPW TLV2463QPW	— —	— —	— —	— —
	1500 µV	TLV2462AQD TLV2463AQD	TLV2462AQPW TLV2463AQPW	— —	— —	— —	— —
−55°C to 125°C	2000 µV	— —	— —	TLV2462MJG —	— TLV2463MJ	TLV2462MU	TLV2462MFK TLV2463MFK
	1500 µV	— —	— —	TLV2462AMJG —	— TLV2463AMJ	TLV2462AMU	TLV2462AMFK TLV2463AMFK

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462QDR).

TLV2464C/I/AI and TLV2465C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	2000 µV	TLV2464CD TLV2465CD	TLV2464CN TLV2465CN	TLV2464CPW TLV2465CPW
−40°C to 125°C	2000 µV	TLV2464ID TLV2465ID	TLV2464IN TLV2465IN	TLV2464IPW TLV2465IPW
	1500 µV	TLV2464AID TLV2465AID	TLV2464AIN TLV2465AIN	TLV2464AIPW TLV2465AIPW

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number(e.g., TLV2464CDR).

‡ Chip forms are tested at T_A = 25°C only.

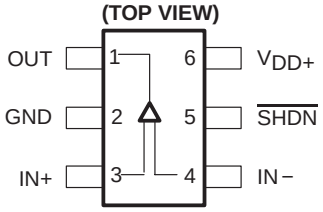
TLV2464M/AM/Q/AQ and TLV2465M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (J)	CHIP CARRIER (FK)
-40°C to 125°C	2000 µV	TLV2464QD TLV2465QD	TLV2464QPW TLV2465QPW	— —	— —
	1500 µV	TLV2464AQD TLV2465AQD	TLV2464AQPW TLV2465AQPW	— —	— —
−55°C to 125°C	2000 µV	— —	— —	TLV2464MJ TLV2465MJ	TLV2464MFK TLV2465MFK
	1500 µV	— —	— —	TLV2464AMJ TLV2465AMJ	TLV2464AMFK TLV2465AMFK

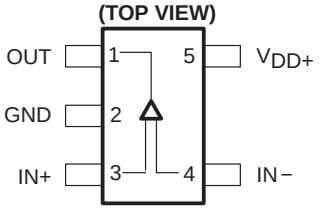
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2464QDR).

TLV246x PACKAGE PINOUTS(1)

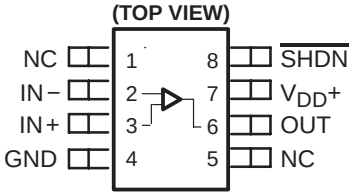
TLV2460
DBV PACKAGE
(TOP VIEW)



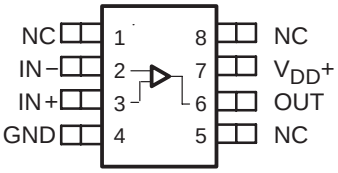
TLV2461
DBV PACKAGE
(TOP VIEW)



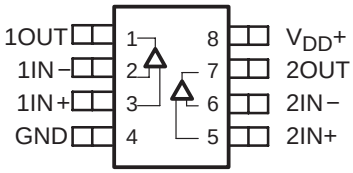
TLV2460
D, P, JG, OR PW PACKAGE
(TOP VIEW)



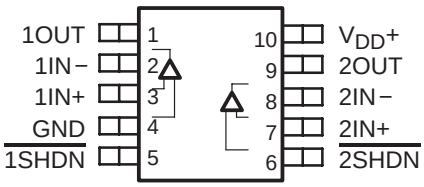
TLV2461
D, P, JG, OR PW PACKAGE
(TOP VIEW)



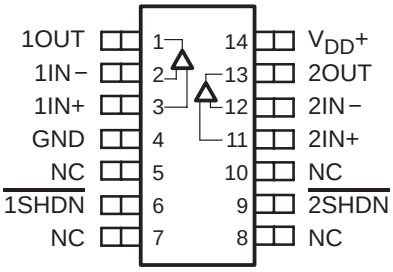
TLV2462
D, DGK, P, JG, OR PW PACKAGE
(TOP VIEW)



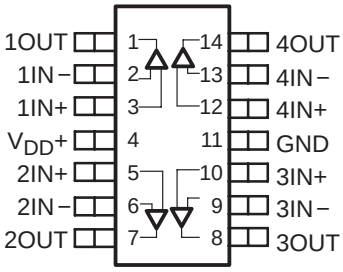
TLV2463
DGS PACKAGE
(TOP VIEW)



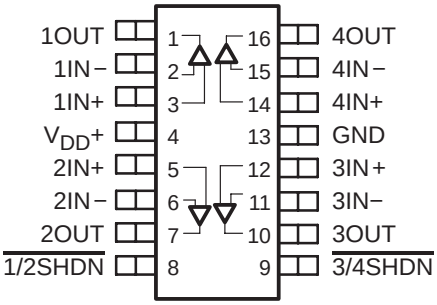
TLV2463
D, N, J, OR PW PACKAGE
(TOP VIEW)



TLV2464
D, N, PWP, J, OR PW PACKAGE
(TOP VIEW)

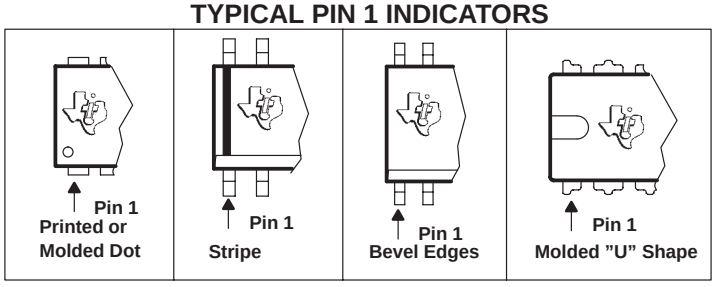


TLV2465
D, N, PWP, J, OR PW PACKAGE
(TOP VIEW)



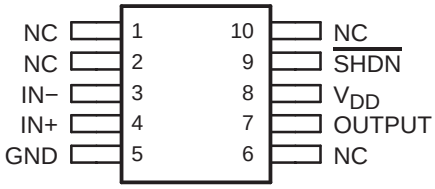
NC − No internal connection
(1) SOT−23 may or may not be indicated

TYPICAL PIN 1 INDICATORS

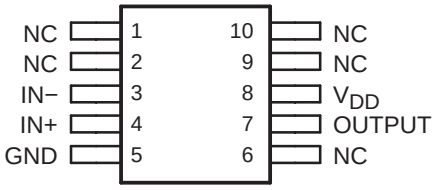


TLV246x PACKAGE PINOUTS (continued)(1)

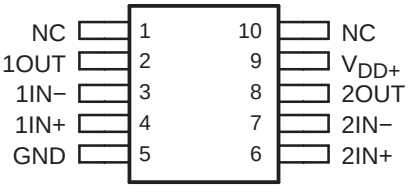
TLV2460
U PACKAGE
(TOP VIEW)



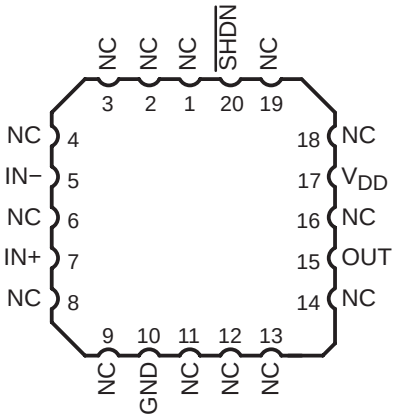
TLV2461
U PACKAGE
(TOP VIEW)



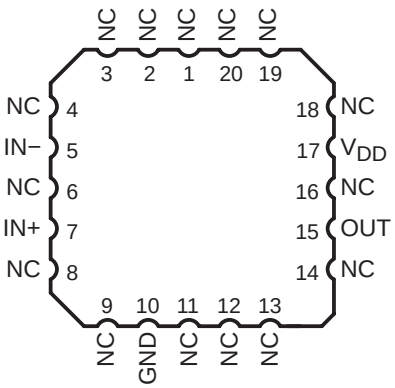
TLV2462
U PACKAGE
(TOP VIEW)



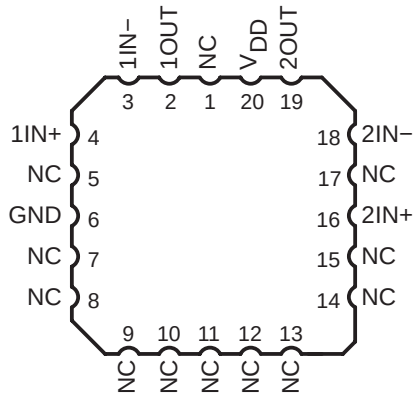
TLV2460
FK PACKAGE
(TOP VIEW)



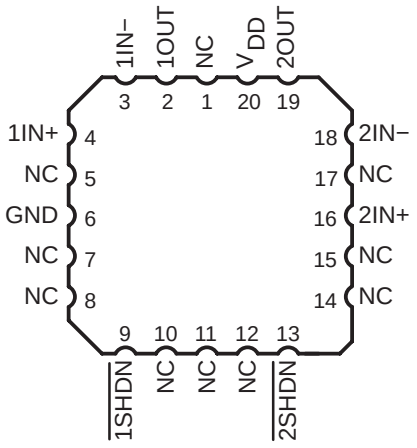
TLV2461
FK PACKAGE
(TOP VIEW)



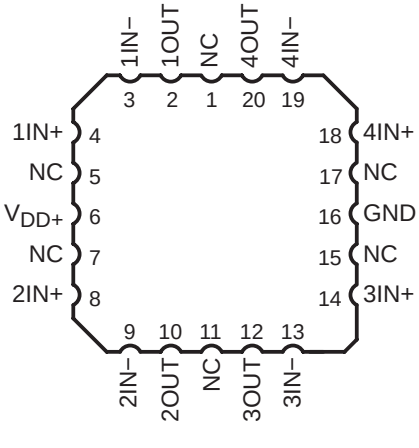
TLV2462
FK PACKAGE
(TOP VIEW)



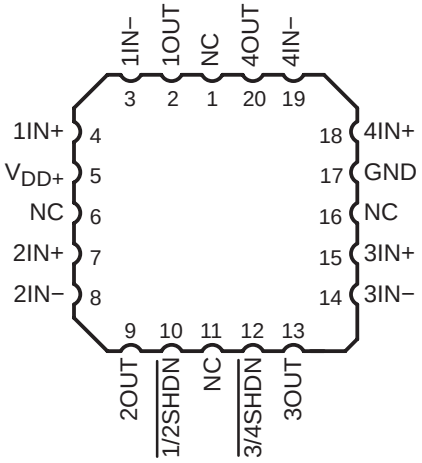
TLV2463
FK PACKAGE
(TOP VIEW)



TLV2464
FK PACKAGE
(TOP VIEW)



TLV2465
FK PACKAGE
(TOP VIEW)



NC − No internal connection
(1) SOT−23 may or may not be indicated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 6 V
Differential input voltage, V_{ID} . . . . . − 0.2 V to V_{DD} + 0.2 V
Input current, I_I (any input) . . . . . ± 200 mA
Output current, I_O . . . . . ± 175 mA
Total input current, I_I (into V_{DD+}) . . . . . 175 mA
Total output current, I_O (out of GND) . . . . . 175 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I and Q suffix . . . . . −40°C to 125°C
M suffix . . . . . −55°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE FOR C and I SUFFIX

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING	$T_A < 125°C$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
D (16)	25.7	114.7	1090 mW	218 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DBV (6)	55	294.3	425 mW	84.9 mW
DGK	54.2	259.9	481 mW	96.2 mW
DGS	54.1	257.7	485 mW	97 mW
N (14, 16)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW
PW (16)	28.7	161.4	774 mW	154.9 mW

NOTE: Thermal resistances are not production tested and are for informational purposes only.

DISSIPATION RATING TABLE FOR Q and M SUFFIX

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R\Theta_{JA}$). Thermal resistances are not production tested and are for informational purposes only.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix and Q-suffix	−40	125	
	M-suffix	−55	125	
Shutdown on/off voltage level‡	V_{IH}	2		V
	V_{IL}		0.7	

‡ Relative to voltage on the GND terminal of the device.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C		500	2000	µV
				Full range			2200	
			TLV246xA	25°C		500	1500	
			TLV246xA	Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage					2		µV/°C
I_{IO}	Input offset current	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C		2.8	7	nA
			TLV246xC	Full range			20	
			TLV246xI/Q/M	Full range			75	
I_{IB}	Input bias current			25°C		4.4	14	nA
			TLV246xC	Full range			25	
			TLV246xI/Q/M	Full range			75	
V_{OH}	High-level output voltage	I_{OH} = −2.5 mA		25°C		2.9		V
				Full range	2.8			
		I_{OH} = −10 mA		25°C		2.7		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 1.5 V,	I_{OL} = 10 mA	25°C		0.3		
				Full range			0.5	
I_{OS}	Short-circuit output current	Sourcing		25°C		50		mA
				Full range	20			
		Sinking		25°C		40		
				Full range	20			
I_O	Output current	Measured 1 V from rail		25°C		±40		mA
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ,	$V_{O(PP)}$ = 1 V	25°C	90	105		dB
				Full range	89			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω

† Full range is 0°C to 70°C for the C suffix, −40°C to 125°C for the I and Q suffixes, and −55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		33		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 to 3 V, R_S = 50 Ω		25°C	66	80		dB
			TLV246xC	Full range	64			
			TLV246xI/Q/M	Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channels)	V_O = 1.5 V,	No load	25°C		0.5	0.575	mA
				Full range			0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 0.7 V, Per channel in shutdown		25°C		0.3		µA
				Full range			2.5	

† Full range is 0°C to 70°C for the C suffix, −40°C to 125°C for the I and Q suffixes, and −55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	0.9	1.6		V/µs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		16		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.006%		
			A_V = 10			0.02%		
			A_V = 100			0.08%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		µs
			Channel 1 only, Channel 2 on			7.65		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.47		µs
			0.01%			1.78		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.77		
			0.01%			1.98		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		44°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix, −40°C to 125°C for the I and Q suffixes, and −55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5 V, R_S = 50 Ω		25°C		500	2000	µV
				Full range			2200	
			TLV246xA	25°C		500	1500	
			TLV246xA	Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		2		µV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		0.3	7	nA
			TLV246xC	Full range			15	
			TLV246xI/Q/M	Full range			60	
I_{IB}	Input bias current			25°C		1.3	14	nA
			TLV246xC	Full range			30	
			TLV246xI/Q/M	Full range			60	
V_{OH}	High-level output voltage	I_{OH} = −2.5 mA		25°C		4.9		V
				Full range	4.8			
		I_{OH} = −10 mA		25°C		4.8		
				Full range	4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 10 mA	25°C		0.2		
				Full range			0.3	
I_{OS}	Short-circuit output current	Sourcing		25°C		145		mA
				Full range	60			
		Sinking		25°C		100		
				Full range	60			
I_O	Output current	Measured at 1 V from rail		25°C		±80		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	92	109		dB
				Full range	90			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 5 V, R_S = 50 Ω		25°C	71	85		dB
			TLV246xC	Full range	69			
			TLV246xI/Q/M	Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	85	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load,	25°C		0.55	0.65	mA
				Full range			1	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 0.7 V, Per channels in shutdown		25°C		1		µA
				Full range			3	

† Full range is 0°C to 70°C for the C suffix, −40°C to 125°C for the I and Q suffixes, and −55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	0.9	1.6		V/µs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 10 kHz	A_V = 1	25°C		0.004%		
			A_V = 10			0.01%		
			A_V = 100			0.04%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		µs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		6.4		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.53		µs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		45°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix, −40°C to 125°C for the I and Q suffixes, and −55°C to 125°C for the M suffix.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

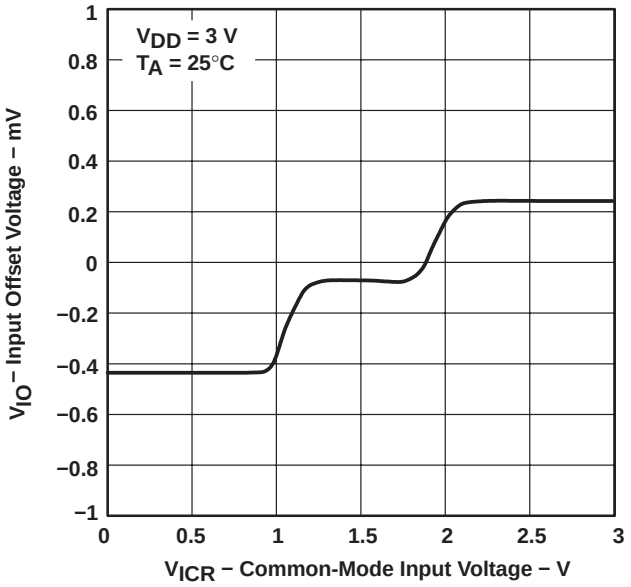


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

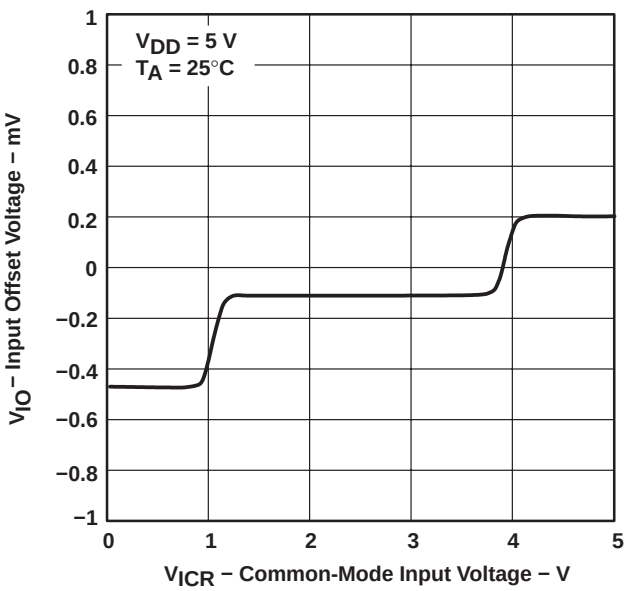


Figure 2

INPUT BIAS AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

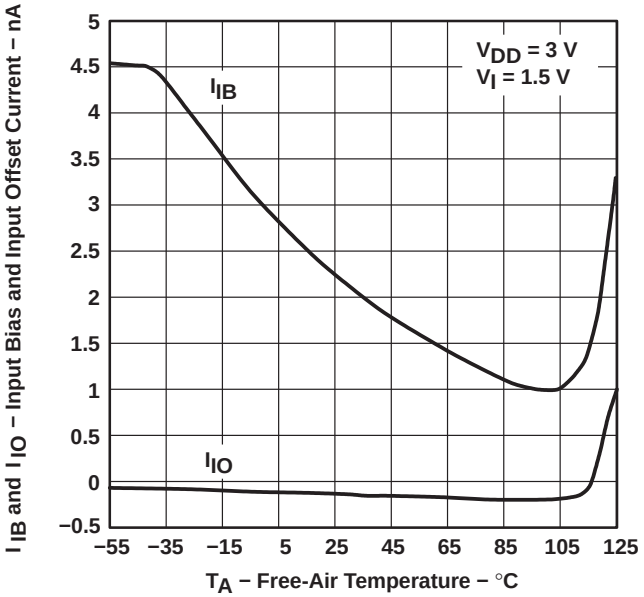


Figure 3

INPUT BIAS AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

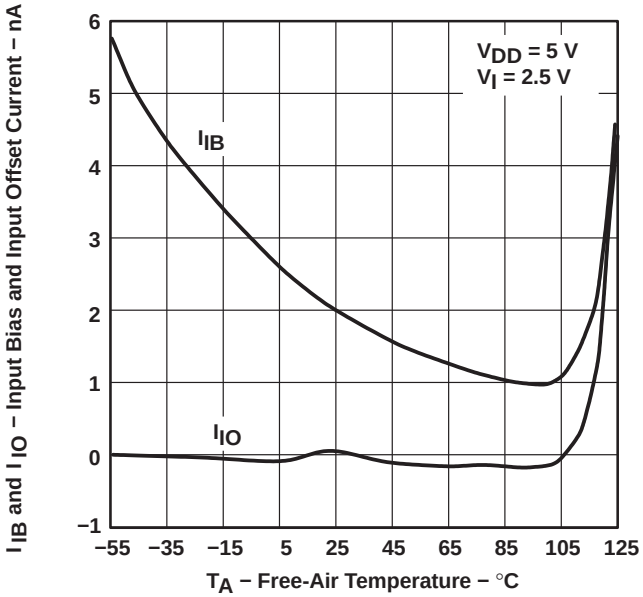


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

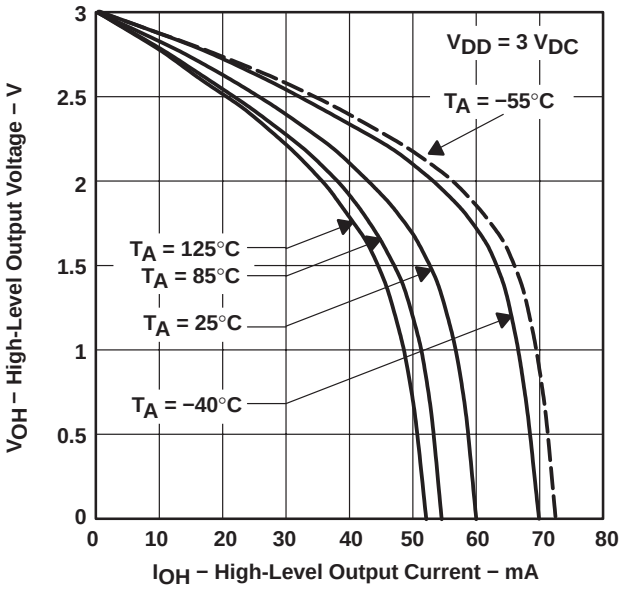


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

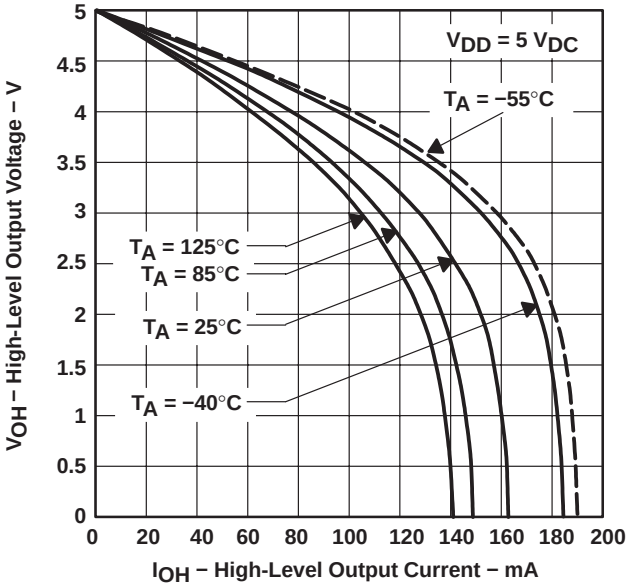


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

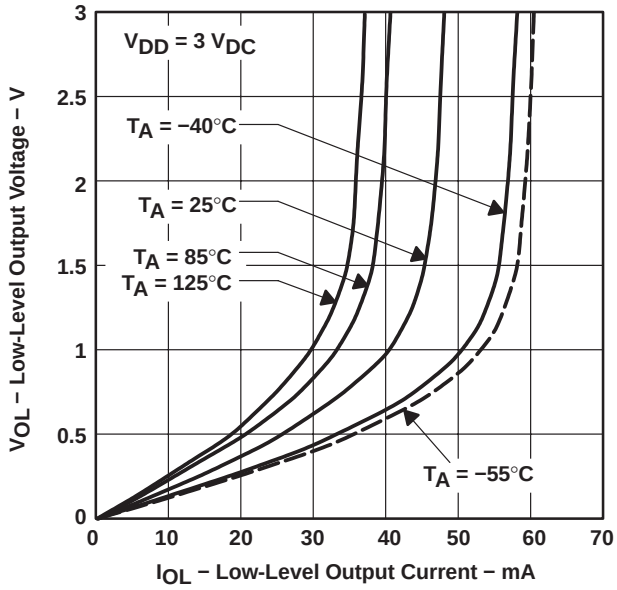


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

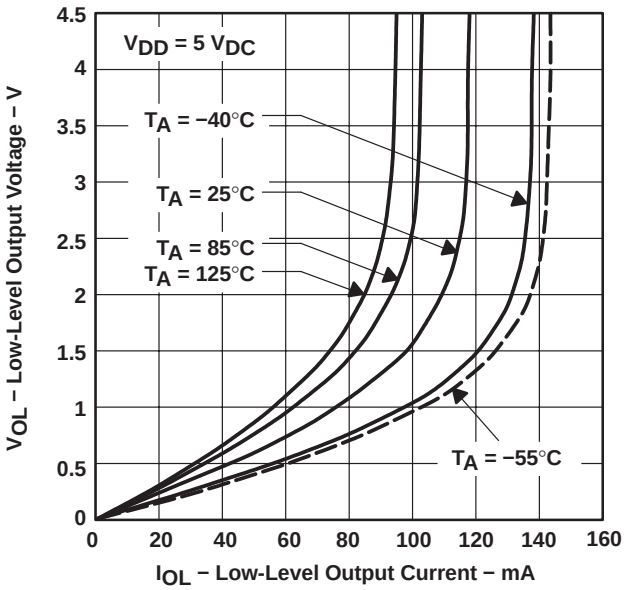


Figure 8

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

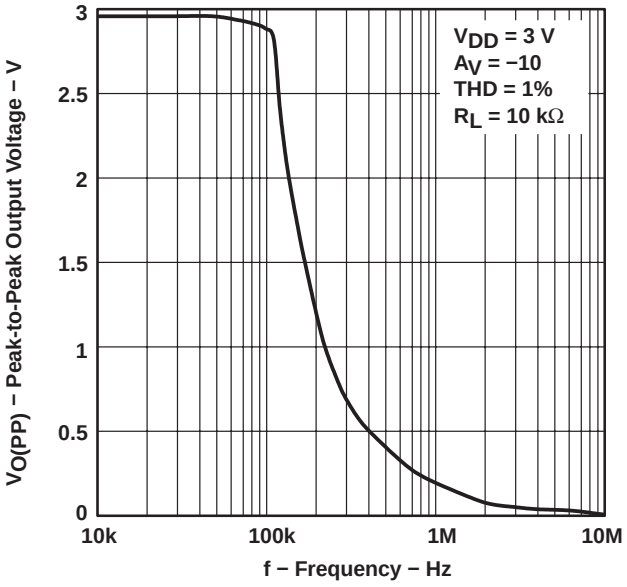


Figure 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

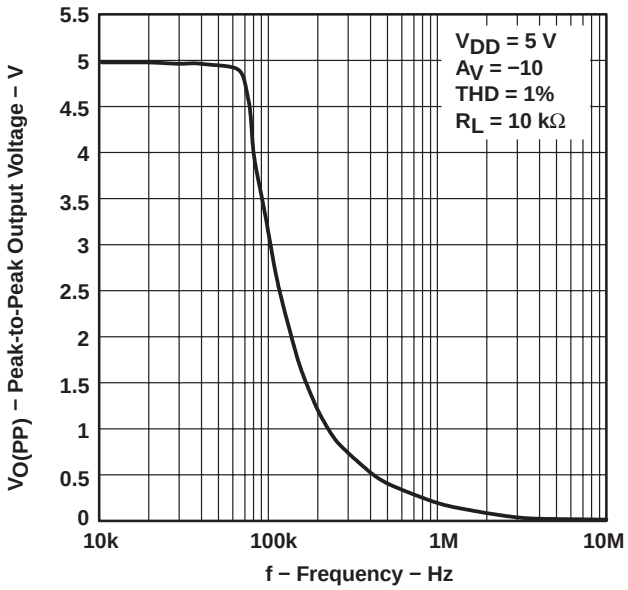


Figure 10

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

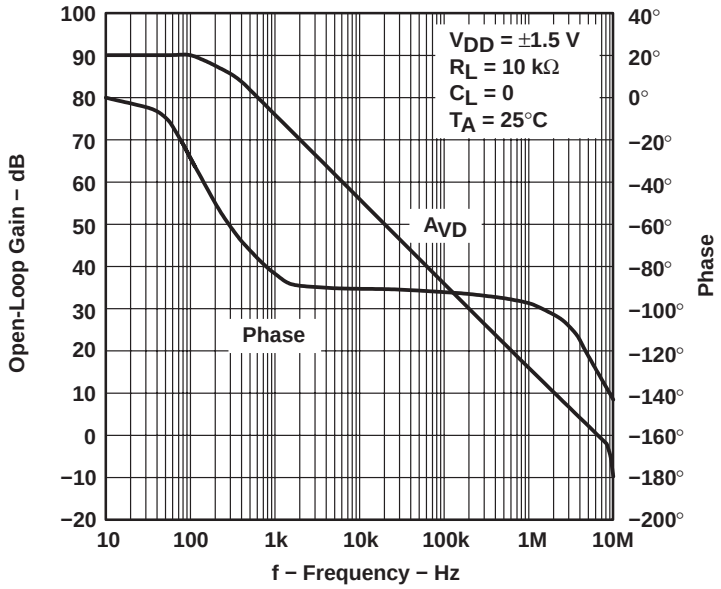


Figure 11

TYPICAL CHARACTERISTICS

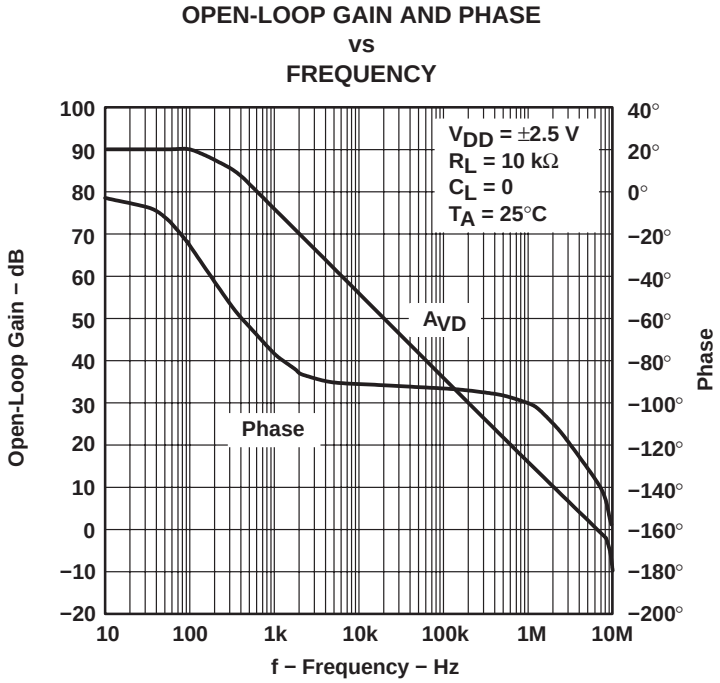


Figure 12

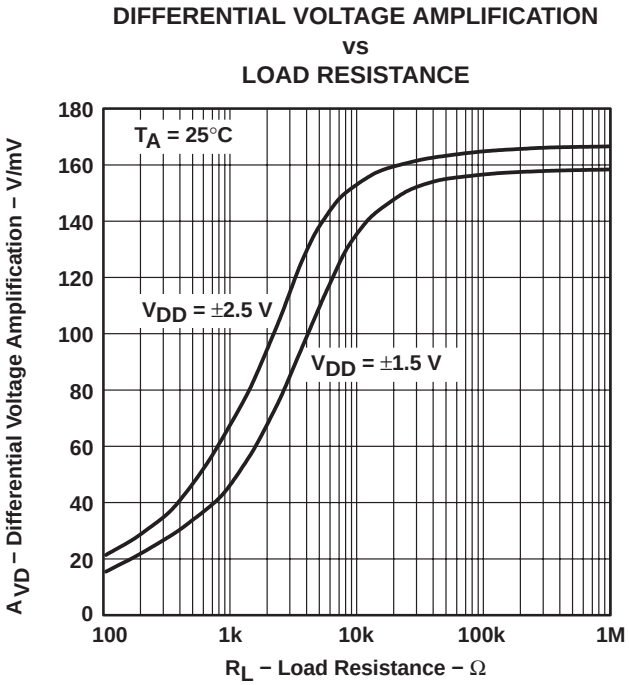


Figure 13

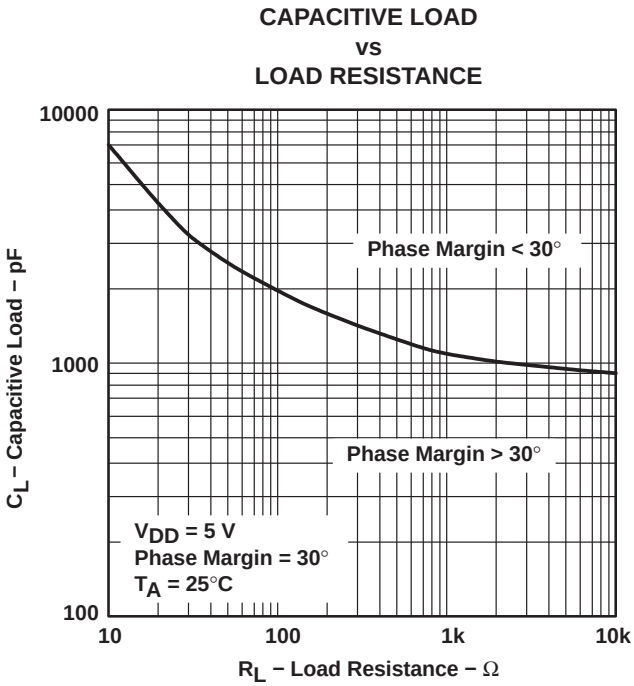


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

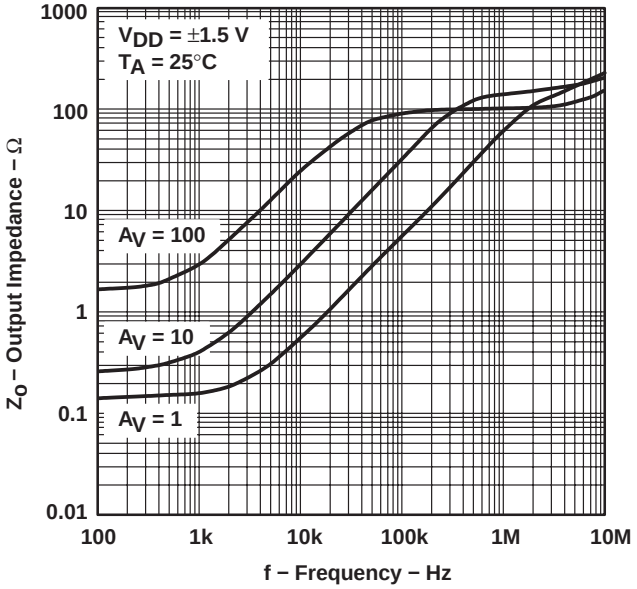


Figure 15

OUTPUT IMPEDANCE
vs
FREQUENCY

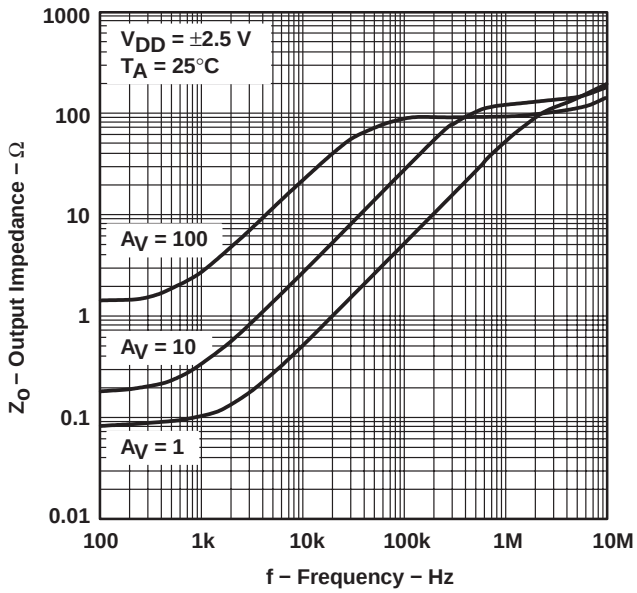


Figure 16

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

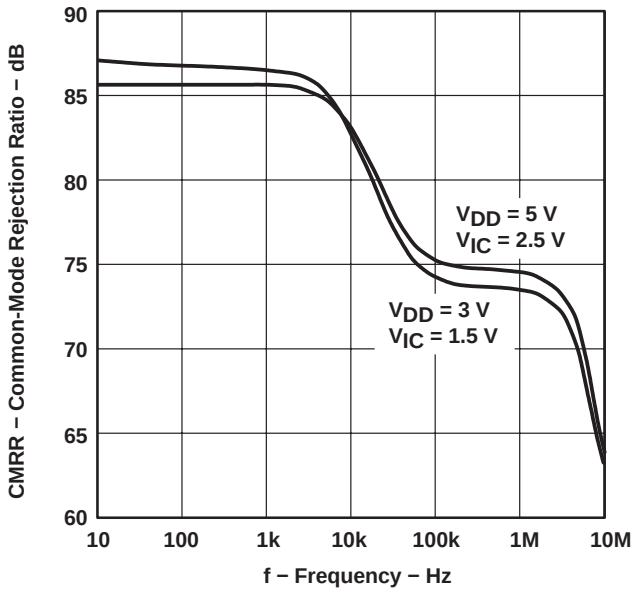


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

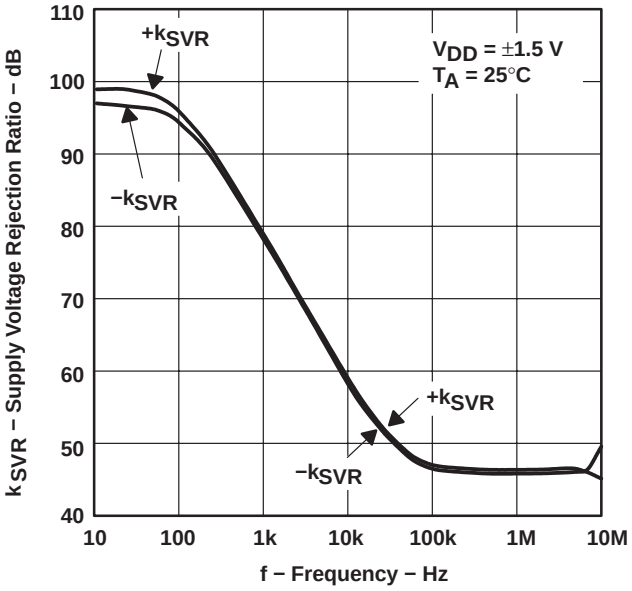


Figure 18

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

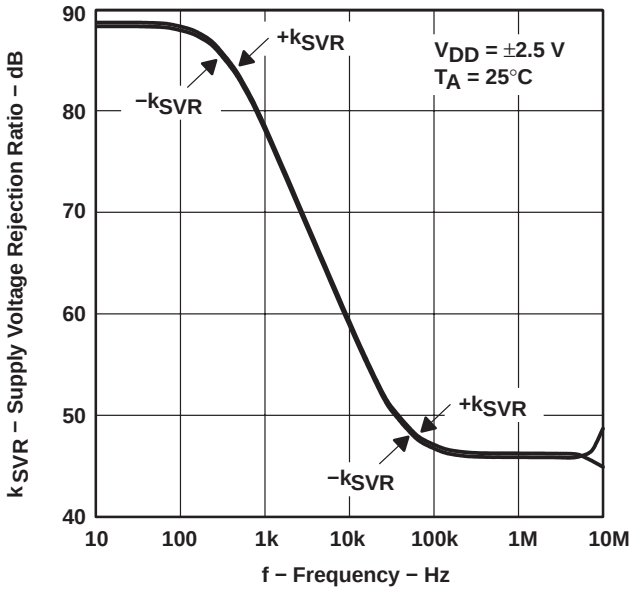


Figure 19

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

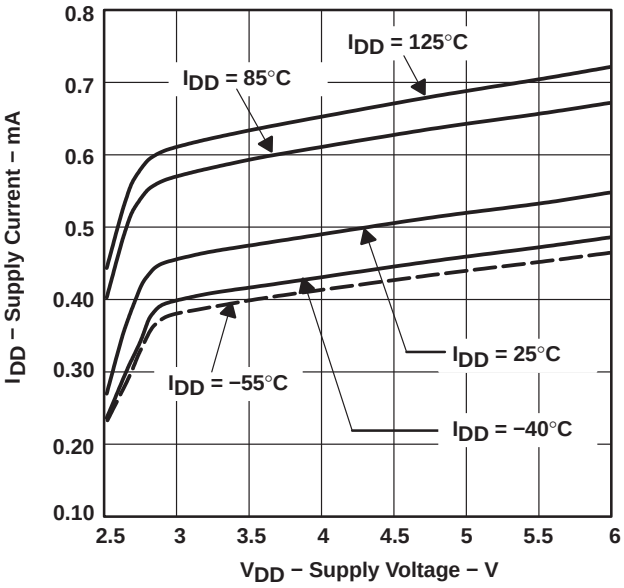


Figure 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

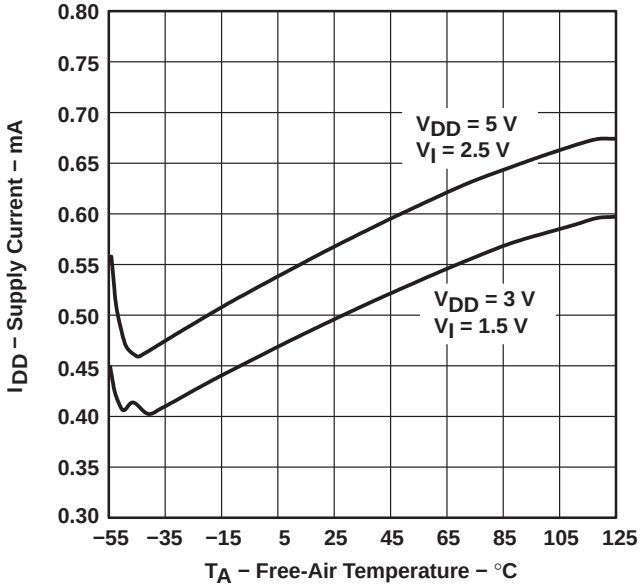


Figure 21

TYPICAL CHARACTERISTICS

AMPLIFIER WITH A SHUTDOWN PULSE
TURNON CHARACTERISTICS

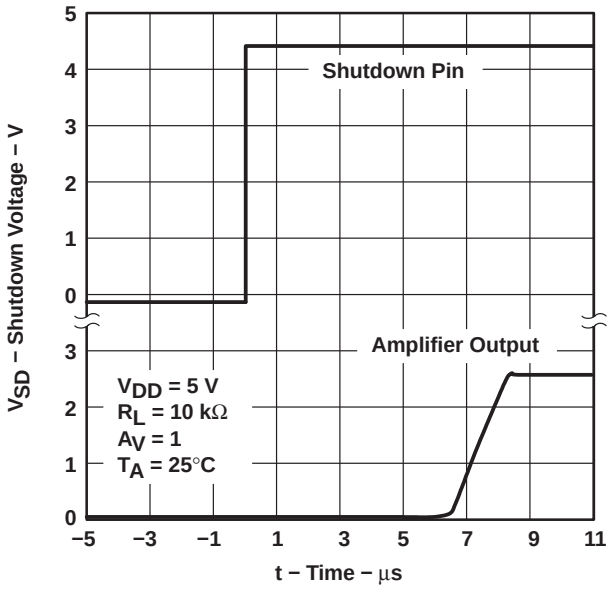


Figure 22

AMPLIFIER WITH A SHUTDOWN PULSE
TURNOFF CHARACTERISTICS

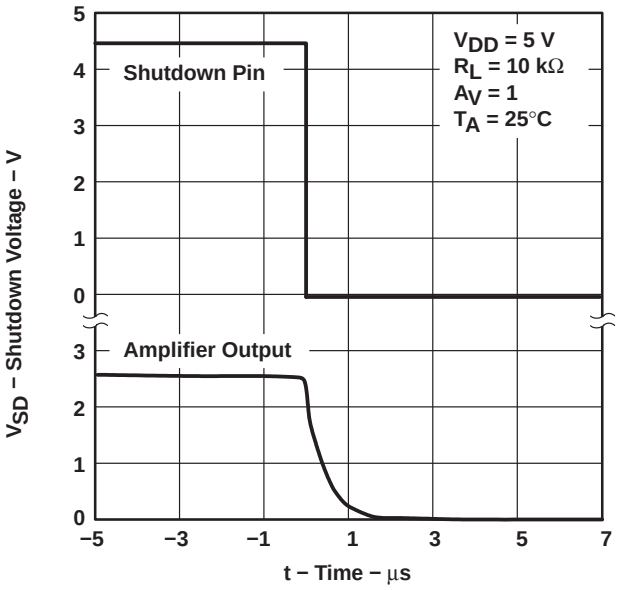


Figure 23

SUPPLY CURRENT WITH A SHUTDOWN PULSE
TURNON CHARACTERISTICS

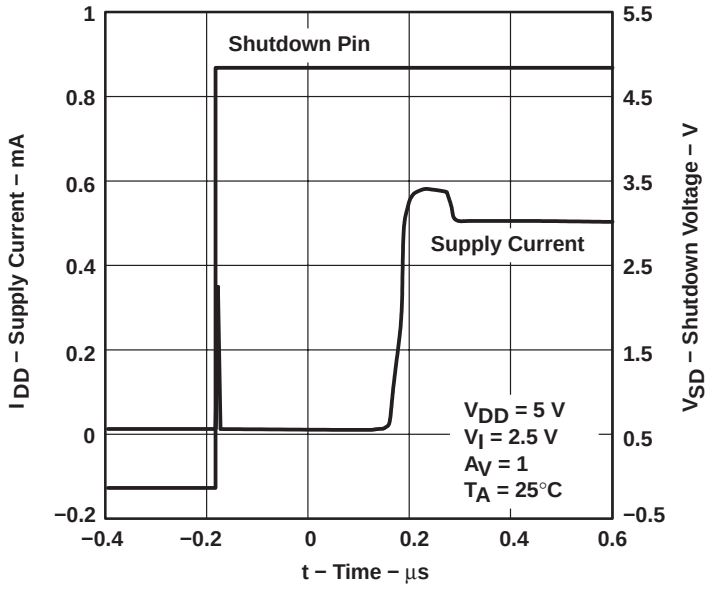


Figure 24

TYPICAL CHARACTERISTICS

TURNOFF SUPPLY CURRENT WITH A SHUTDOWN PULSE

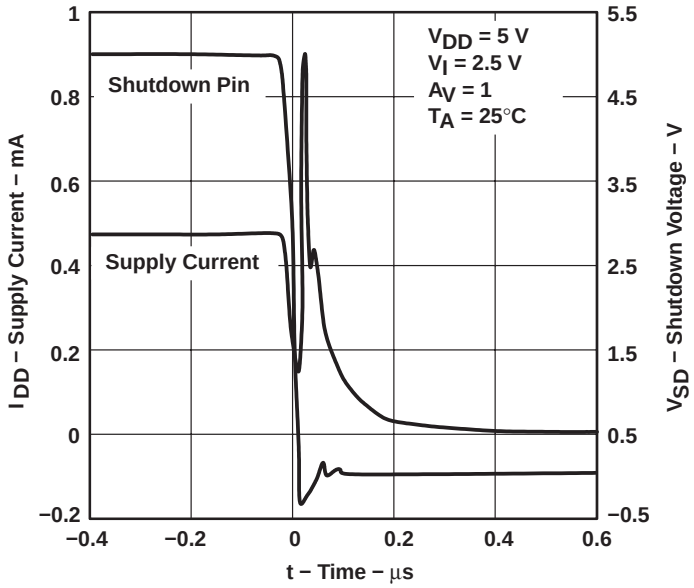


Figure 25

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

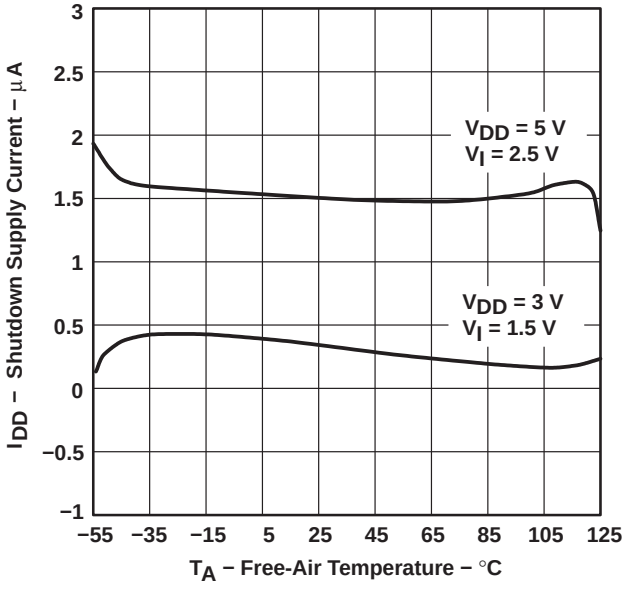


Figure 26

SLEW RATE vs SUPPLY VOLTAGE

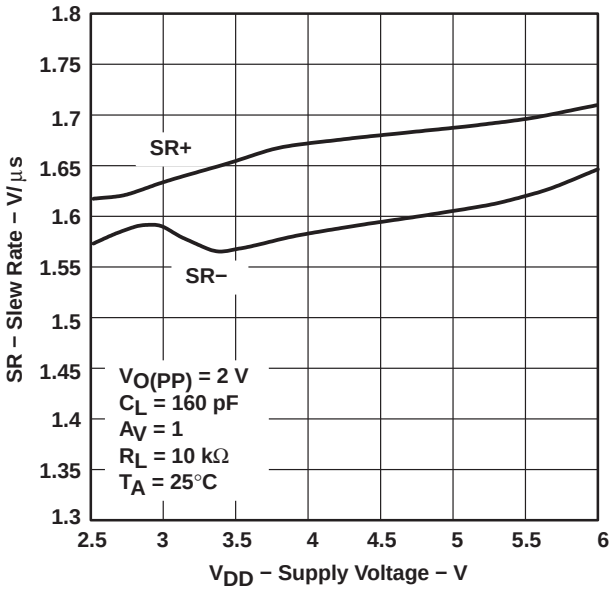


Figure 27

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

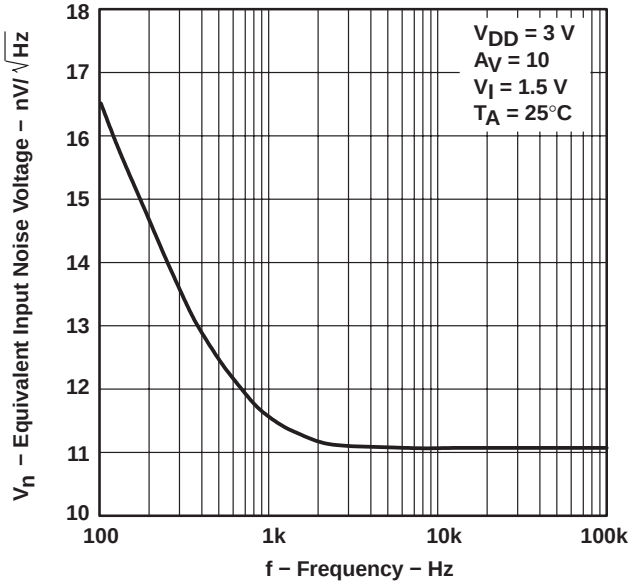


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

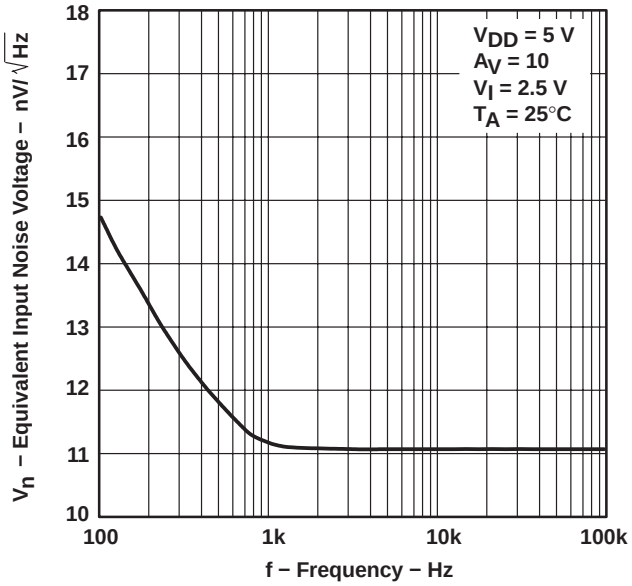


Figure 29

EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

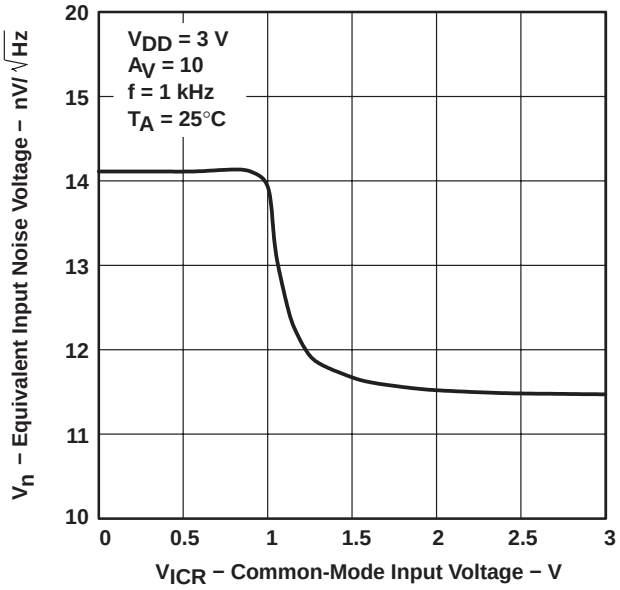


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

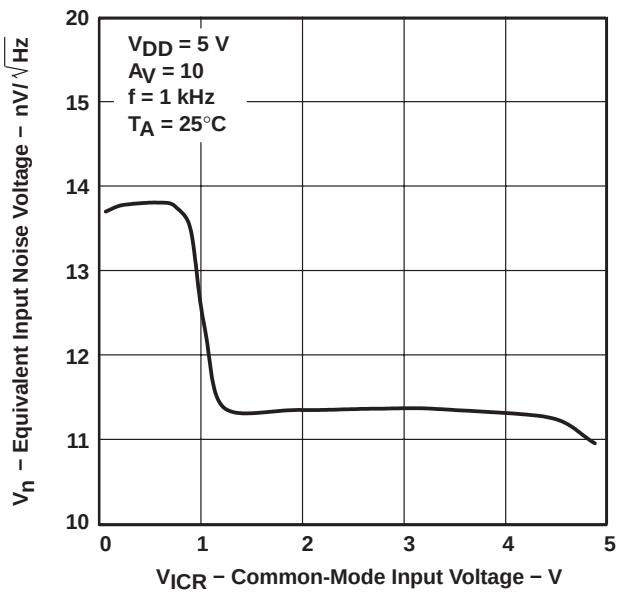


Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

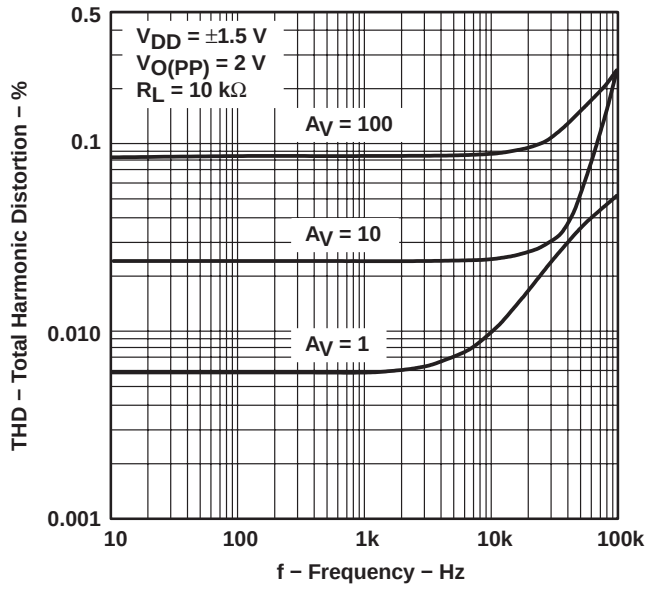


Figure 32

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

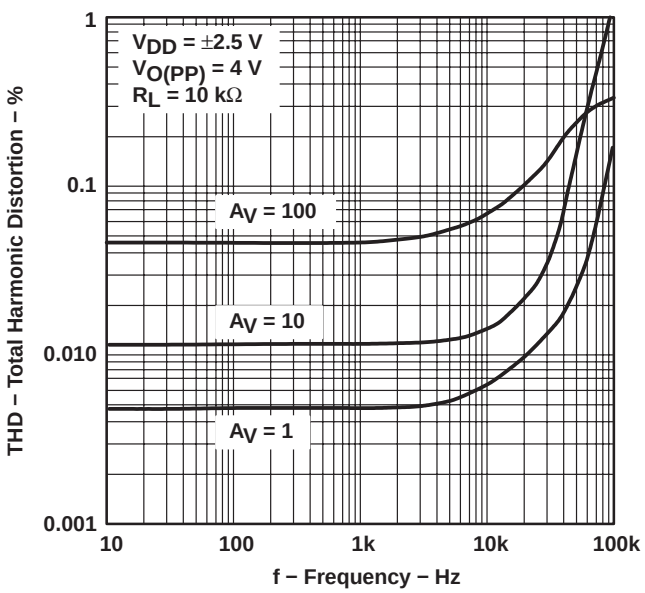


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
PEAK-TO-PEAK SIGNAL AMPLITUDE

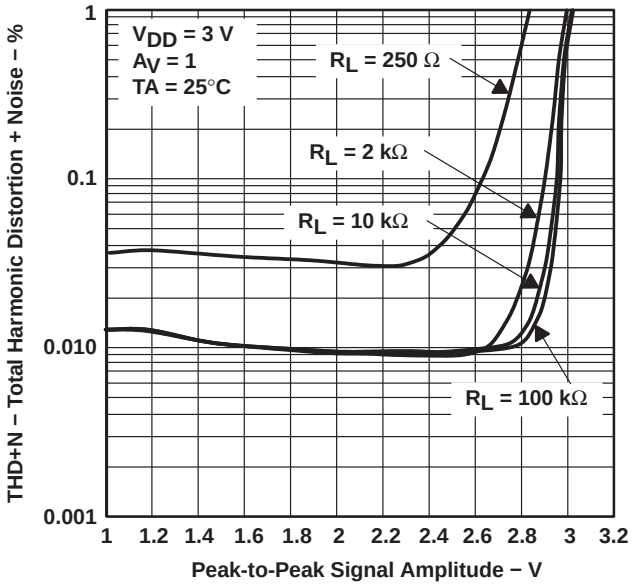


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
PEAK-TO-PEAK SIGNAL AMPLITUDE

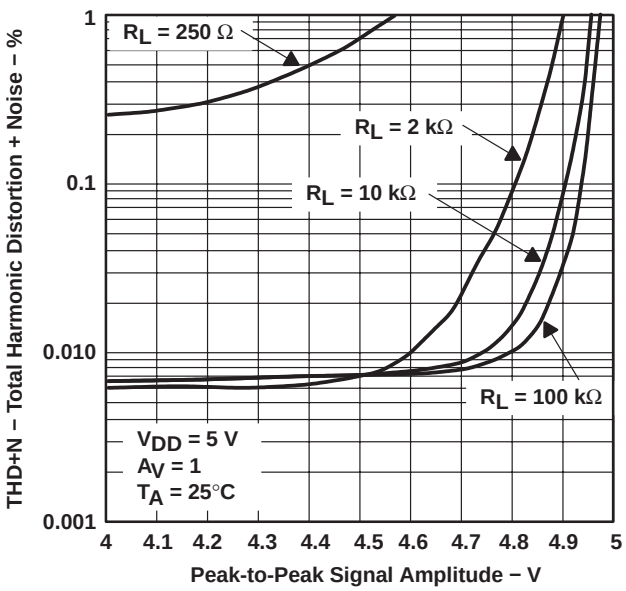


Figure 35

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

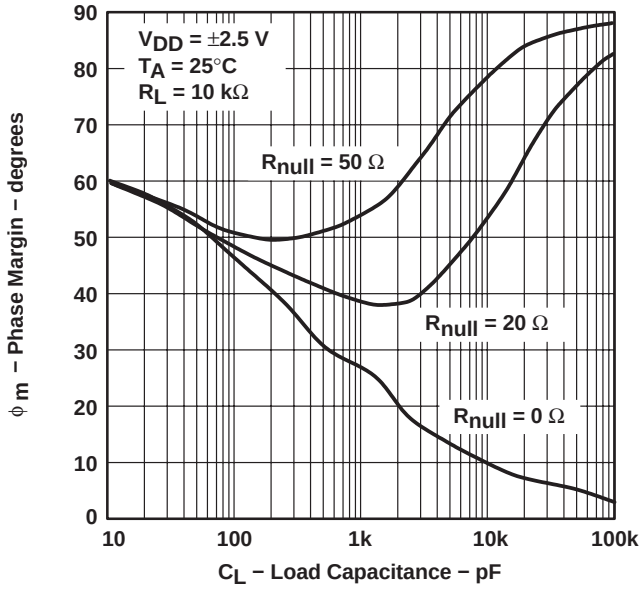


Figure 36

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

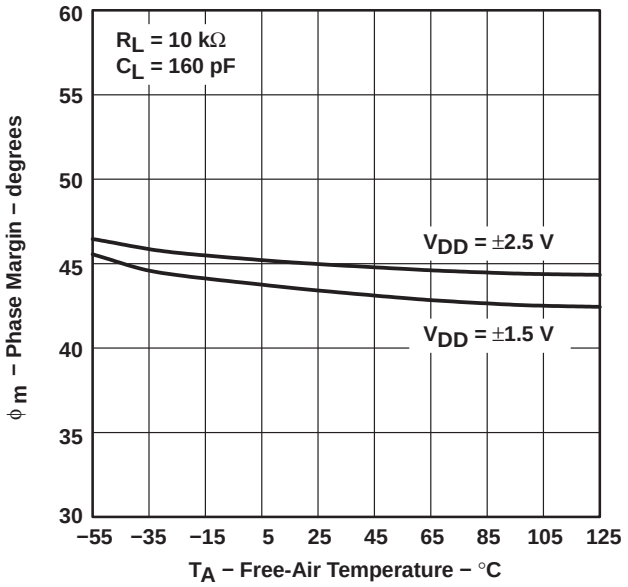


Figure 37

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

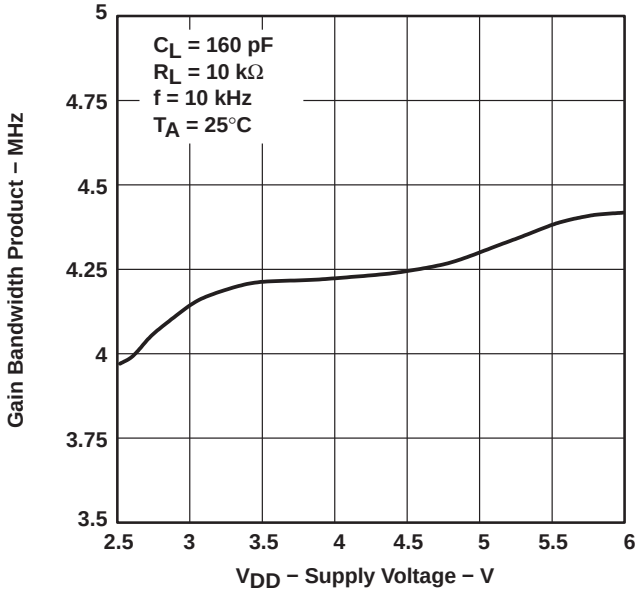


Figure 38

GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

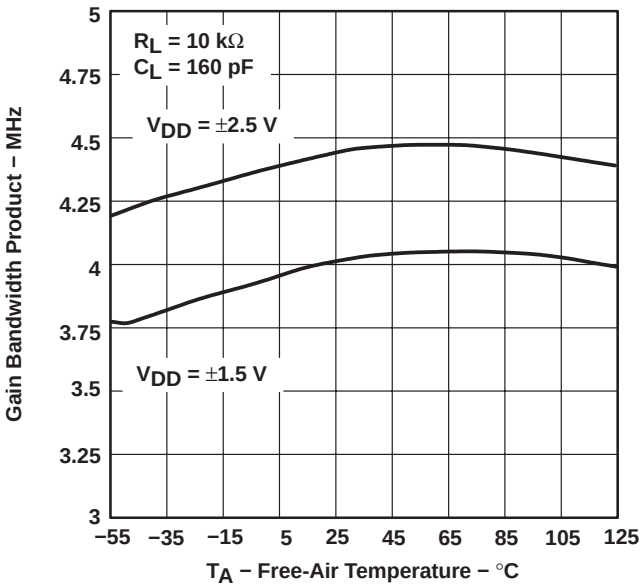


Figure 39

TYPICAL CHARACTERISTICS

LARGE SIGNAL FOLLOWER

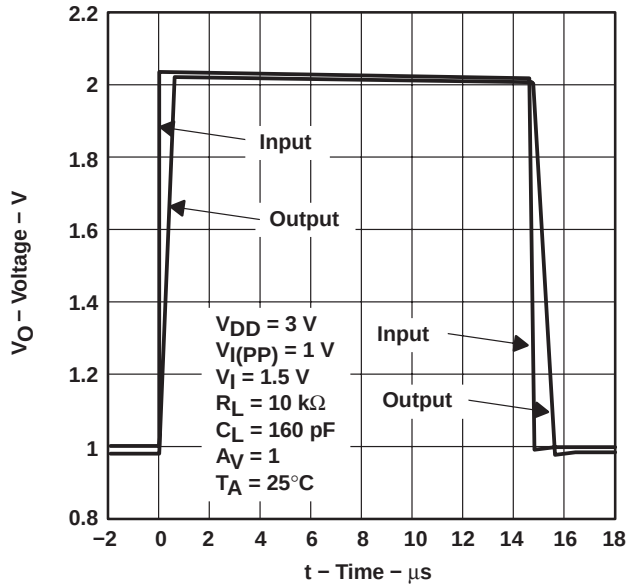


Figure 40

LARGE SIGNAL FOLLOWER

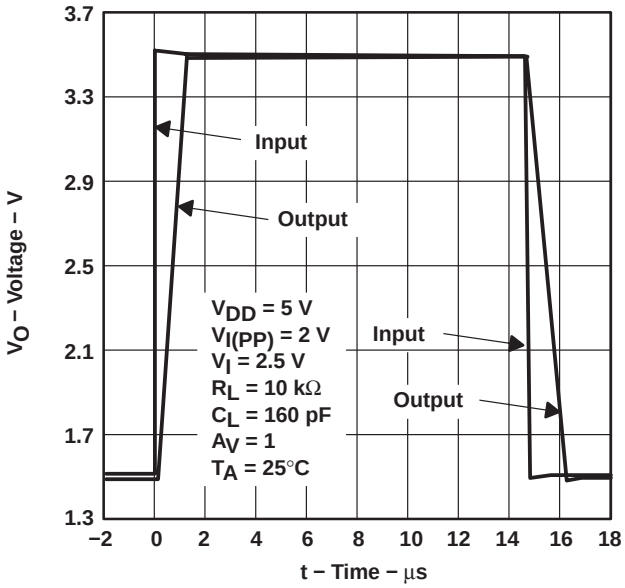


Figure 41

SMALL SIGNAL FOLLOWER

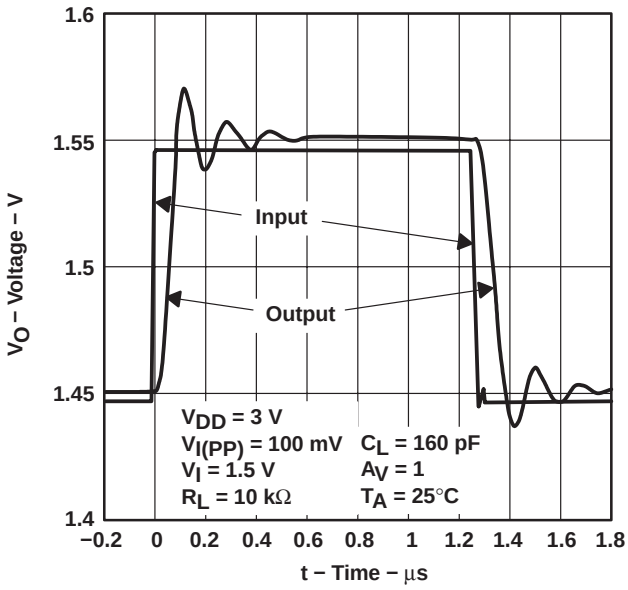


Figure 42

SMALL SIGNAL FOLLOWER

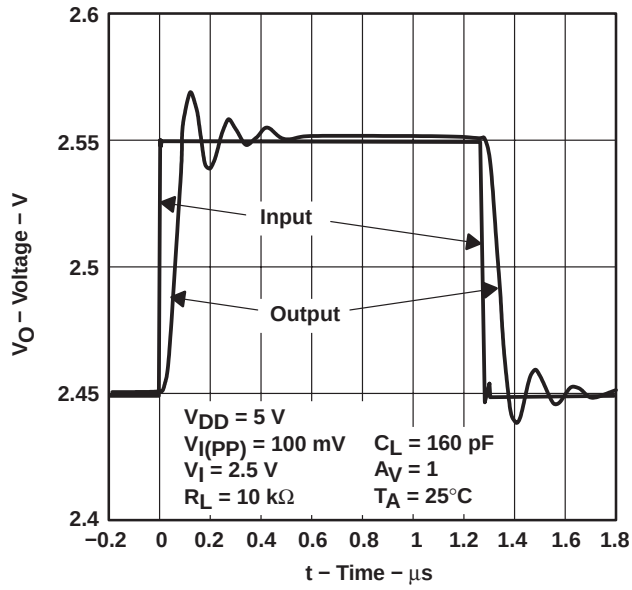


Figure 43

TYPICAL CHARACTERISTICS

INVERTING LARGE SIGNAL

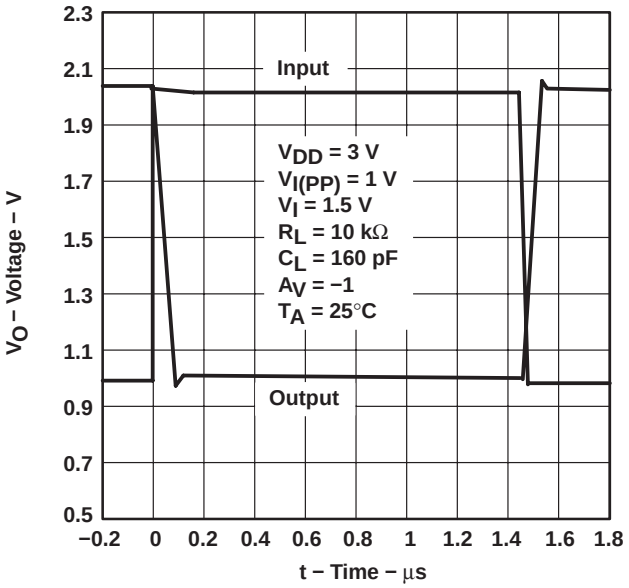


Figure 44

INVERTING LARGE SIGNAL

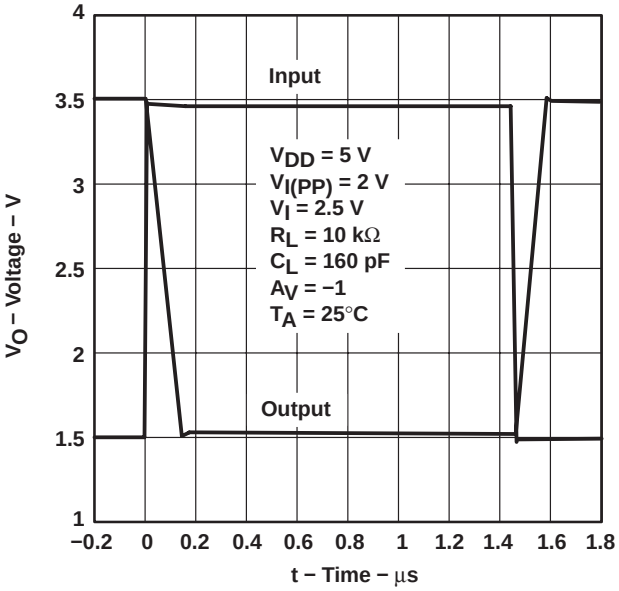


Figure 45

INVERTING SMALL SIGNAL

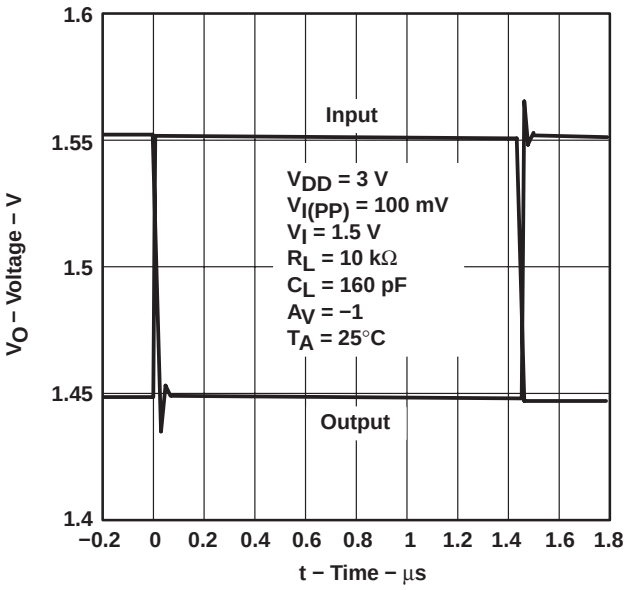


Figure 46

INVERTING SMALL SIGNAL

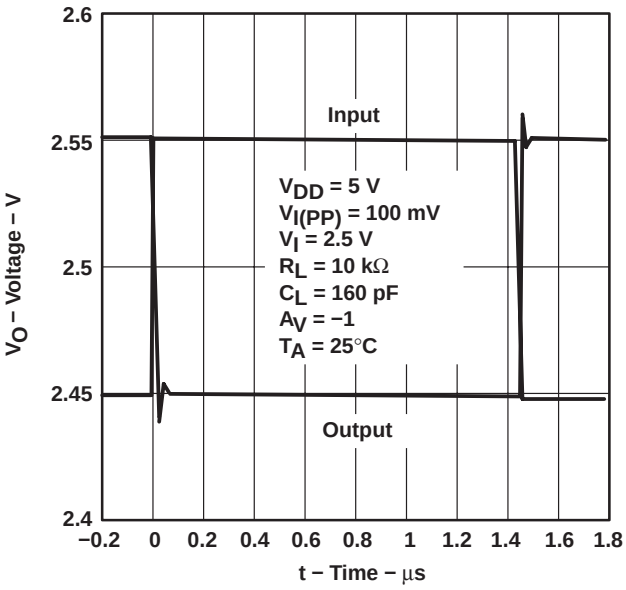


Figure 47

PARAMETER MEASUREMENT INFORMATION

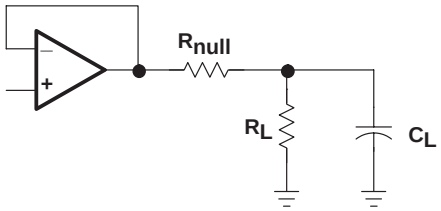


Figure 48

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

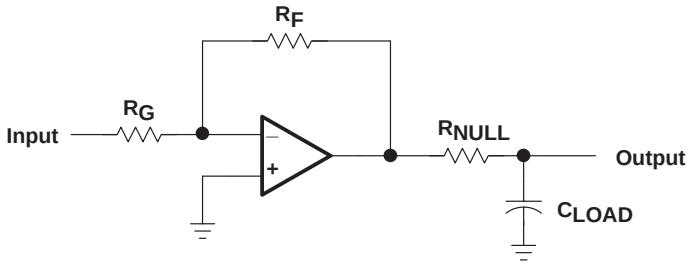
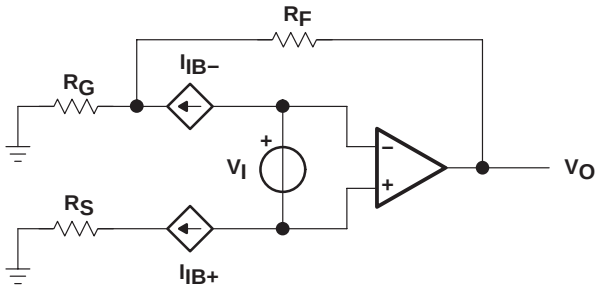


Figure 49. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 50. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

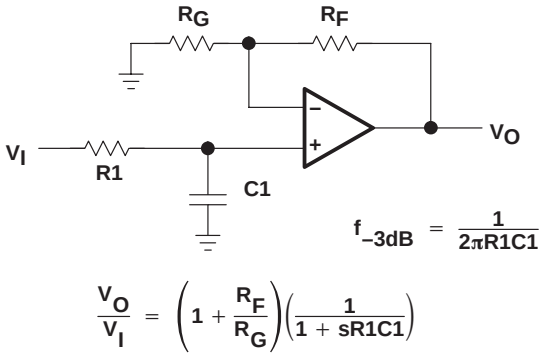


Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

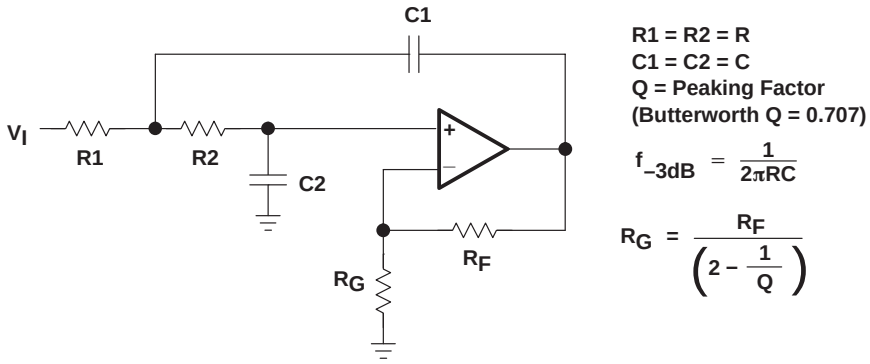


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

shutdown function

Three members of the TLV246x family (TLV2460/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

circuit layout considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

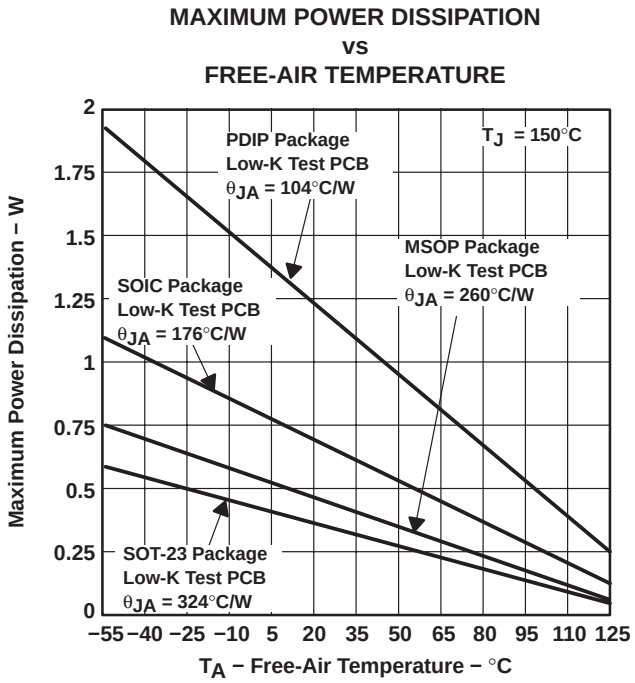
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS246x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

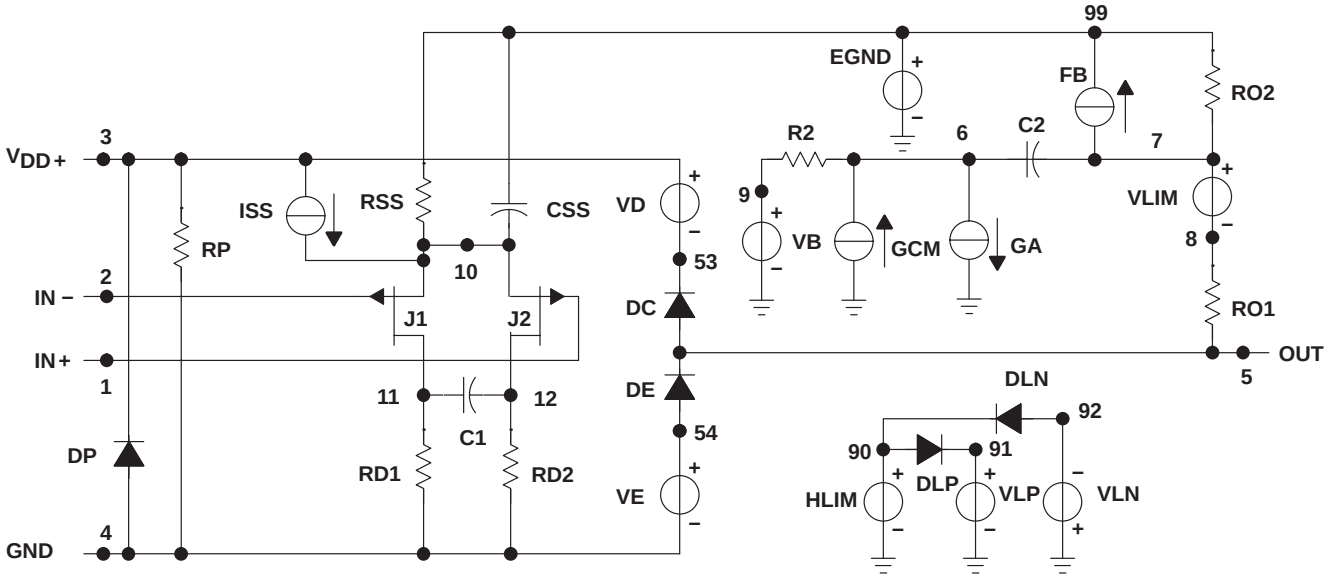
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 54 are generated using the TLV246x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV246X   1 2 3 4 5
C1          11      12      2.46034E−12
C2          6       7       10.0000E−12
CSS         10      99      443.21E−15
DC          5       53      DY
DE          54      5       DY
DLP         90      91      DX
DLN         92      90      DX
DP          4       3       DX
EGND        99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB          7       99      POLY (5) VB VC VE VLP
+ VLN 0 21.600E6 −1E3 1E3 22E6 −22E6
GA          6       0       11      12 345.26E−6
GCM         0       6       10      99 15.4226E−9
ISS         10      4       DC 18.850E−6
HLIM        90      0       VLIM 1K
J1          11      2       10 JX1
J2          12      1       10 JX2
R2          6       9       100.00E3
RD1         3       11      2.8964E3
RD2         3       12      2.8964E3
R01         8       5       5.6000
R02         7       99      6.2000
RP          3       4       8.9127
RSS         10      99      10.610E6
VB          9       0       DC 0
VC          3       53      DC .7836
VE          54      4       DC .7436
VLIM        7       8       DC 0
VLP         91      0       DC 117
VLN         0       92      DC 117
.MODEL DX D (IS=800.00E−18)
.MODEL DY D (IS=800.00E−18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E−12 BETA=6.3239E−3
+ VTO=−1)
.MODEL JX2 NJF (IS=1.0000E−12 BETA=6.3239E−3
+ VTO=−1)
.ENDS
```

Figure 54. Boyle Macromodels and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

macromodel information (continued)

```
.subckt TLV_246Y 1 2 3 4 5 6
c1      11   12   2.4603E−12
c2      72   7    10.000E−12
css     10   99   443.21E−15
dc      70   53   dy
de      54   70   dy
dlp     90   91   dx
dln     92   90   dx
dp      4    3    dx
egnd    99   0    poly(2) (3,0) (4,0) 0 .5 .5
fb      7    99   poly(5) vb vc ve vlp vln 0
21.600E6 −1E3 1E3 22E6 −22E6
ga      72   0    11 12 345.26E−6
gcm     0    72   10 99 15.422E−9
iss     74   4    dc 18.850E−6
hlim    90   0    vlim 1K
j1      11   2    10 jx1
j2      12   1    10 jx2
r2      72   9    100.00E3
rd1     3    11   2.8964E3
rd2     3    12   2.8964E3
ro1     8    70   5.6000
ro2     7    99   6.2000
rp      3    71   8.9127
rss     10   99   10.610E6
rs1     6    4    1G
rs2     6    4    1G
rs3     6    4    1G
rs4     6    4    1G
s1      71   4    6  4  s1x
s2      70   5    6  4  s1x
s3      10   74   6  4  s1x
s4      74   4    6  4  s2x
vb      9    0    dc 0
vc      3    53   dc .7836
ve      54   4    dc .7436
vlim    7    8    dc 0
vlp     91   0    dc 117
vln     0    92   dc 117
.model dx D(Is=800.00E−18)
.model dy D(Is=800.00E−18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E−12 Beta=6.3239E−3 Vto=−1)
.model jx2 NJF(Is=1.0000E−12 Beta=6.3239E−3 Vto=−1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x  VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodels and Subcircuit (Continued)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0051201QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051201QHA TLV2460M	Samples
5962-0051203QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051203QHA TLV2461M	Samples
5962-0051205QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051205QHA TLV2462M	Samples
5962-0051206Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-0051206Q2A TLV2462A MFKB	Samples
5962-0051206QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051206QHA TLV2462AM	Samples
5962-0051206QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051206QPA TLV2462AM	Samples
TLV2460AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2460AI	Samples
TLV2460AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2460AI	Samples
TLV2460CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2460C	Samples
TLV2460CDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAOC	Samples
TLV2460CDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAOC	Samples
TLV2460CDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAOC	Samples
TLV2460CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2460C	Samples
TLV2460CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2460C	Samples
TLV2460CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2460C	Samples
TLV2460ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2460I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2460IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAOI	Samples
TLV2460IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAOI	Samples
TLV2460IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAOI	Samples
TLV2460IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2460I	Samples
TLV2460IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2460I	Samples
TLV2460MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051201QHA TLV2460M	Samples
TLV2461AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461AI	Samples
TLV2461AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461AI	Samples
TLV2461AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2461AI	Samples
TLV2461CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2461C	Samples
TLV2461CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAPC	Samples
TLV2461CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAPC	Samples
TLV2461CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VAPC	Samples
TLV2461CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2461C	Samples
TLV2461CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2461C	Samples
TLV2461ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461I	Samples
TLV2461IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAPI	Samples
TLV2461IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAPI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2461IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAPI	Samples
TLV2461IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2461I	Samples
TLV2461IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2461I	Samples
TLV2461MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051203QHA TLV2461M	Samples
TLV2462AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AI	Samples
TLV2462AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AI	Samples
TLV2462AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AI	Samples
TLV2462AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2462AI	Samples
TLV2462AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-0051206Q2A TLV2462A MFKB	Samples
TLV2462AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLV2462AMJG	Samples
TLV2462AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051206QPA TLV2462AM	Samples
TLV2462AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051206QHA TLV2462AM	Samples
TLV2462AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2462A	Samples
TLV2462AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2462A	Samples
TLV2462AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2462A	Samples
TLV2462AQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2462A	Samples
TLV2462AQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2462A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2462CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2462C	Samples
TLV2462CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2462C	Samples
TLV2462CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAI	Samples
TLV2462CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAI	Samples
TLV2462CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAI	Samples
TLV2462CDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AAI	Samples
TLV2462CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2462C	Samples
TLV2462CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2462C	Samples
TLV2462CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2462CP	Samples
TLV2462CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2462CP	Samples
TLV2462ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462I	Samples
TLV2462IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462I	Samples
TLV2462IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAJ	Samples
TLV2462IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAJ	Samples
TLV2462IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAJ	Samples
TLV2462IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AAJ	Samples
TLV2462IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462I	Samples
TLV2462IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2462IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2462MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	0051205QHA TLV2462M	Samples
TLV2462QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2462Q	Samples
TLV2462QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2462Q	Samples
TLV2463AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2463AI	Samples
TLV2463AMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLV2463AMJ	Samples
TLV2463CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2463C	Samples
TLV2463CDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AAK	Samples
TLV2463CDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AAK	Samples
TLV2463CDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AAK	Samples
TLV2463CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2463C	Samples
TLV2463CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2463CN	Samples
TLV2463ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2463I	Samples
TLV2463IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAL	Samples
TLV2463IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAL	Samples
TLV2463IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2463IN	Samples
TLV2464AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2464AI	Samples
TLV2464AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2464AI	Samples
TLV2464AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2464AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2464AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2464AI	Samples
TLV2464AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2464AIN	Samples
TLV2464AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2464A	Samples
TLV2464AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2464A	Samples
TLV2464CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2464C	Samples
TLV2464CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2464C	Samples
TLV2464CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2464CN	Samples
TLV2464CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLV2464CN	Samples
TLV2464CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2464	Samples
TLV2464CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2464	Samples
TLV2464ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2464I	Samples
TLV2464IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2464I	Samples
TLV2464IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2464I	Samples
TLV2464IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2464IN	Samples
TLV2464IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2464	Samples
TLV2464IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2464	Samples
TLV2464IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2464	Samples
TLV2465CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2465C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2465CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2465C	Samples
TLV2465CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2465C	Samples
TLV2465ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2465I	Samples
TLV2465IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2465I	Samples
TLV2465IN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2465IN	Samples
TLV2465IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2465I	Samples
TLV2465IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2465I	Samples
TLV2465IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2465I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV2460, TLV2460A, TLV2460M, TLV2461, TLV2461A, TLV2461M, TLV2462, TLV2462A, TLV2462AM, TLV2462M, TLV2463, TLV2463A, TLV2463AM, TLV2464A :

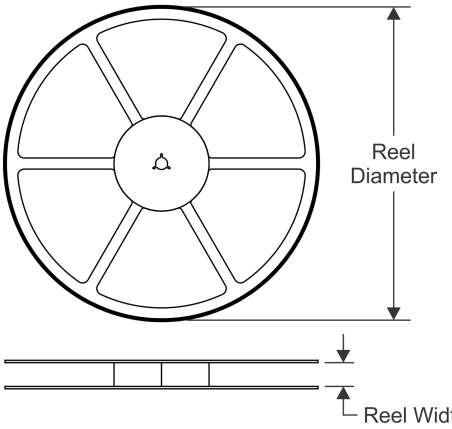
- Catalog: TLV2460, TLV2461, TLV2462A, TLV2462, TLV2463A
- Automotive: TLV2460-Q1, TLV2460A-Q1, TLV2460-Q1, TLV2461-Q1, TLV2461A-Q1, TLV2461-Q1, TLV2462-Q1, TLV2462A-Q1, TLV2462A-Q1, TLV2462-Q1, TLV2463-Q1, TLV2463A-Q1, TLV2463A-Q1, TLV2464A-Q1
- Enhanced Product: TLV2462A-EP, TLV2462A-EP, TLV2464A-EP
- Military: TLV2460M, TLV2461M, TLV2462M, TLV2462AM, TLV2463AM

NOTE: Qualified Version Definitions:

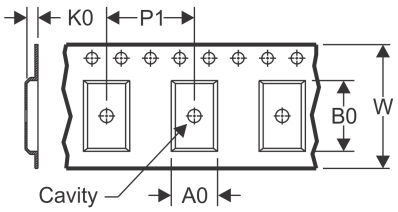
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

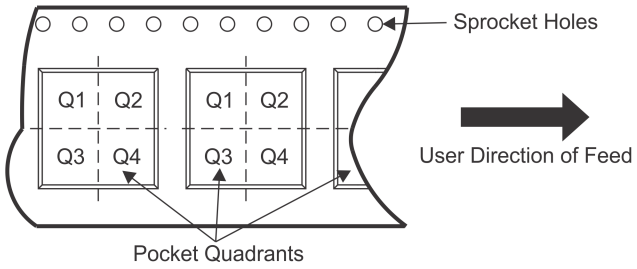


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

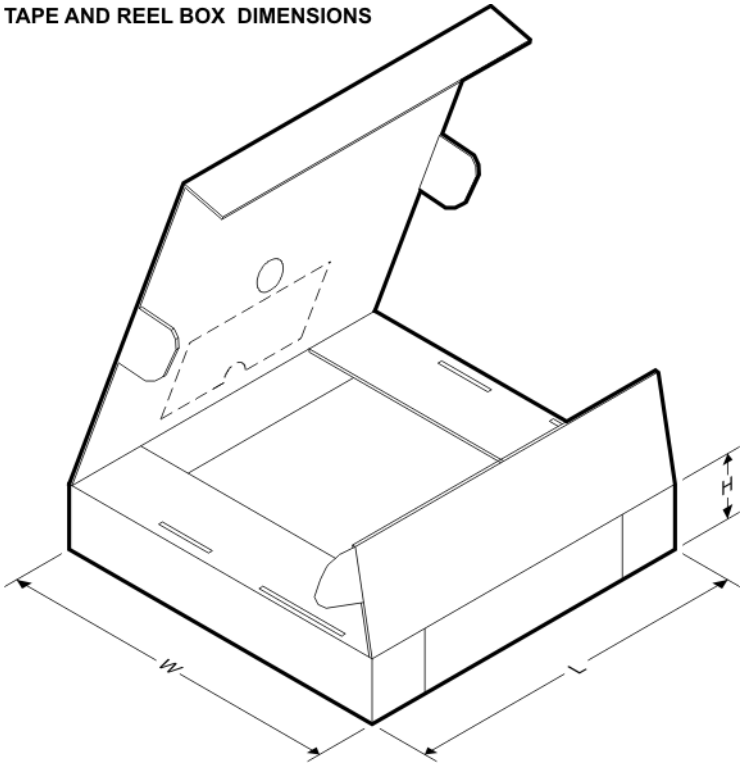


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2460AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2460CDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2460CDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2460CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2460IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2460IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2460IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2461AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2461CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2461CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2461CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2461IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2461IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2461IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2462AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2462AQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462AQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2462CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2462IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2462IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2462QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2462QPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2463AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2463CDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2463CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2463IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2464AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2464AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2464CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2464IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2464IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2465CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2465IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

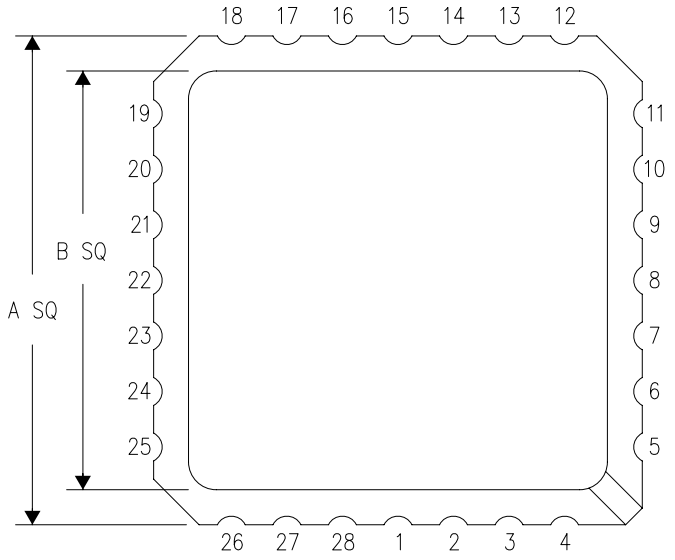


*All dimensions are nominal

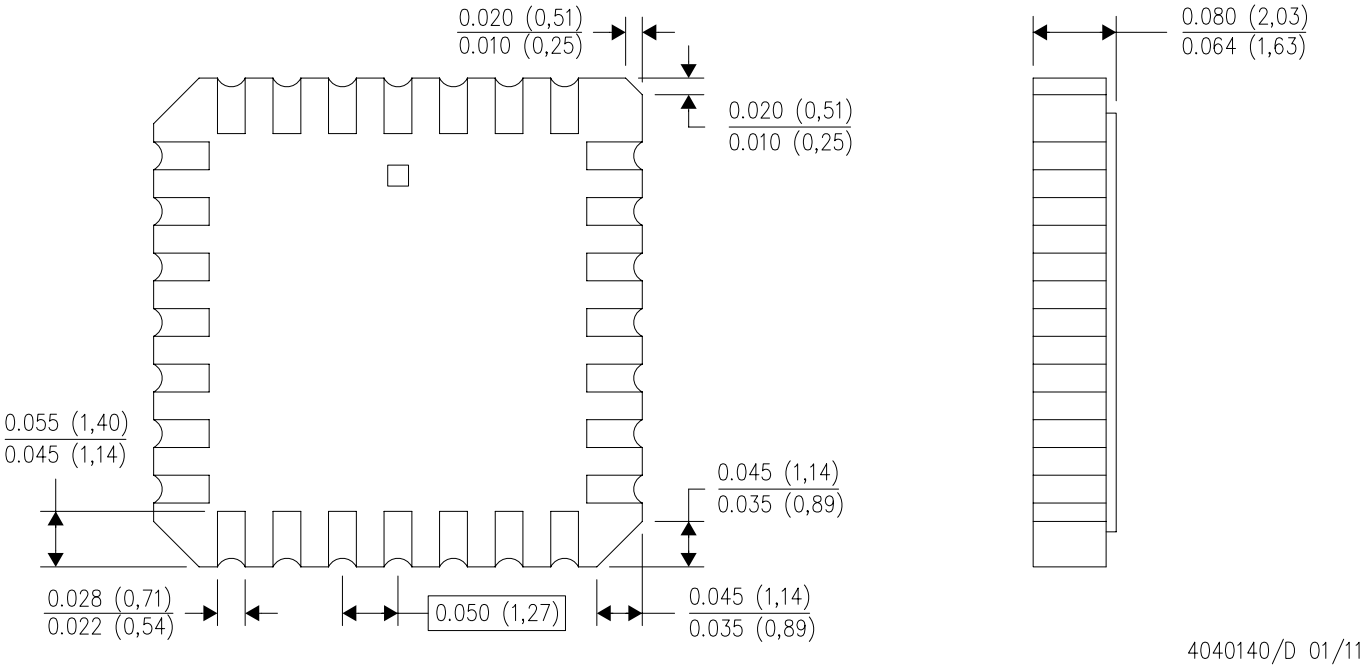
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2460AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2460CDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV2460CDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TLV2460CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2460IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV2460IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TLV2460IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2461AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2461CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2461CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2461CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2461IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2461IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2461IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2462AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2462AQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462AQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2462CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2462CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2462IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2462IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2462IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2462QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2462QPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2463AIDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2463CDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2463CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2463IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2464AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2464AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2464CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2464IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2464IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2465CDR	SOIC	D	16	2500	367.0	367.0	38.0
TLV2465IDR	SOIC	D	16	2500	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



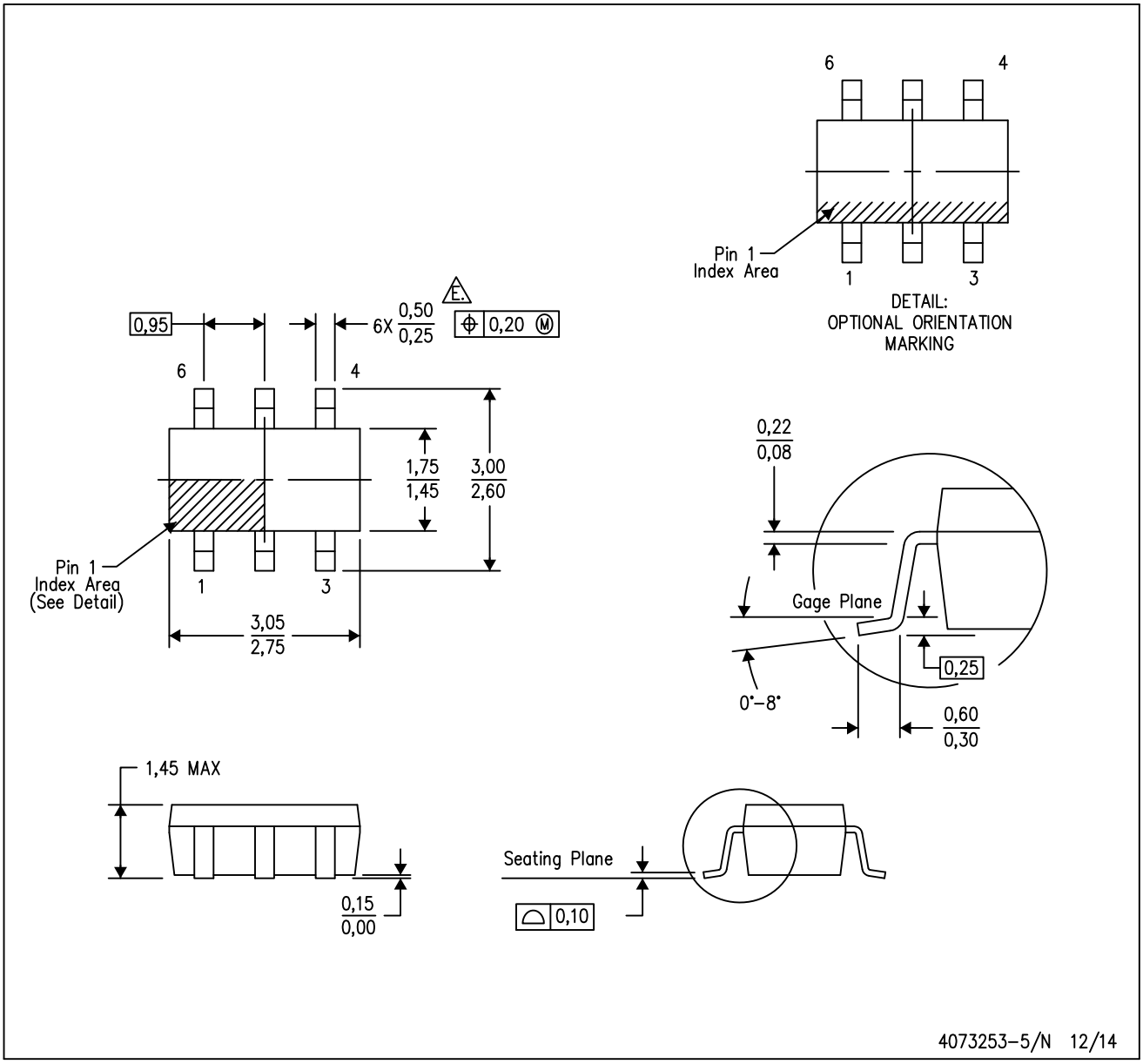
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

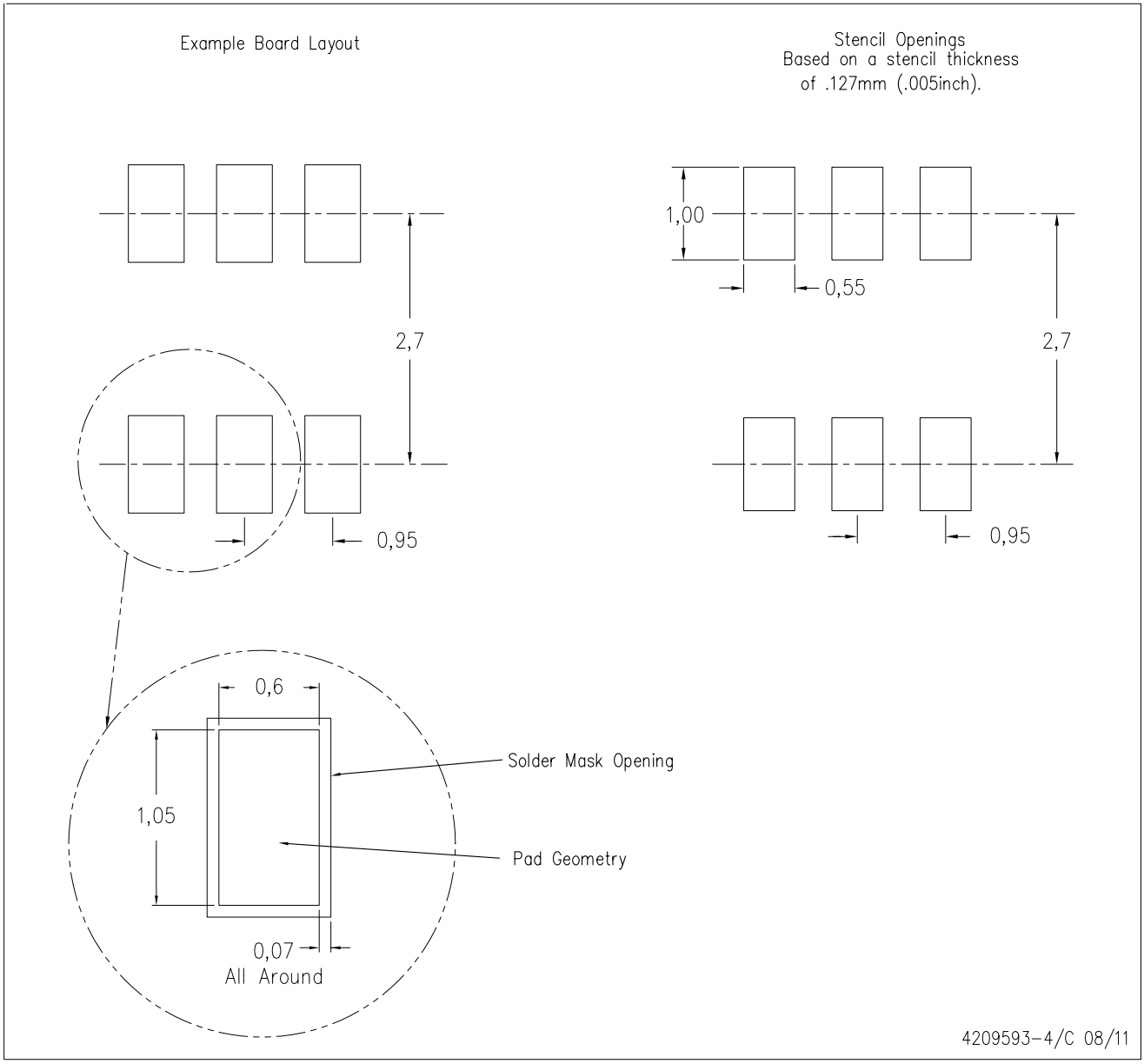
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



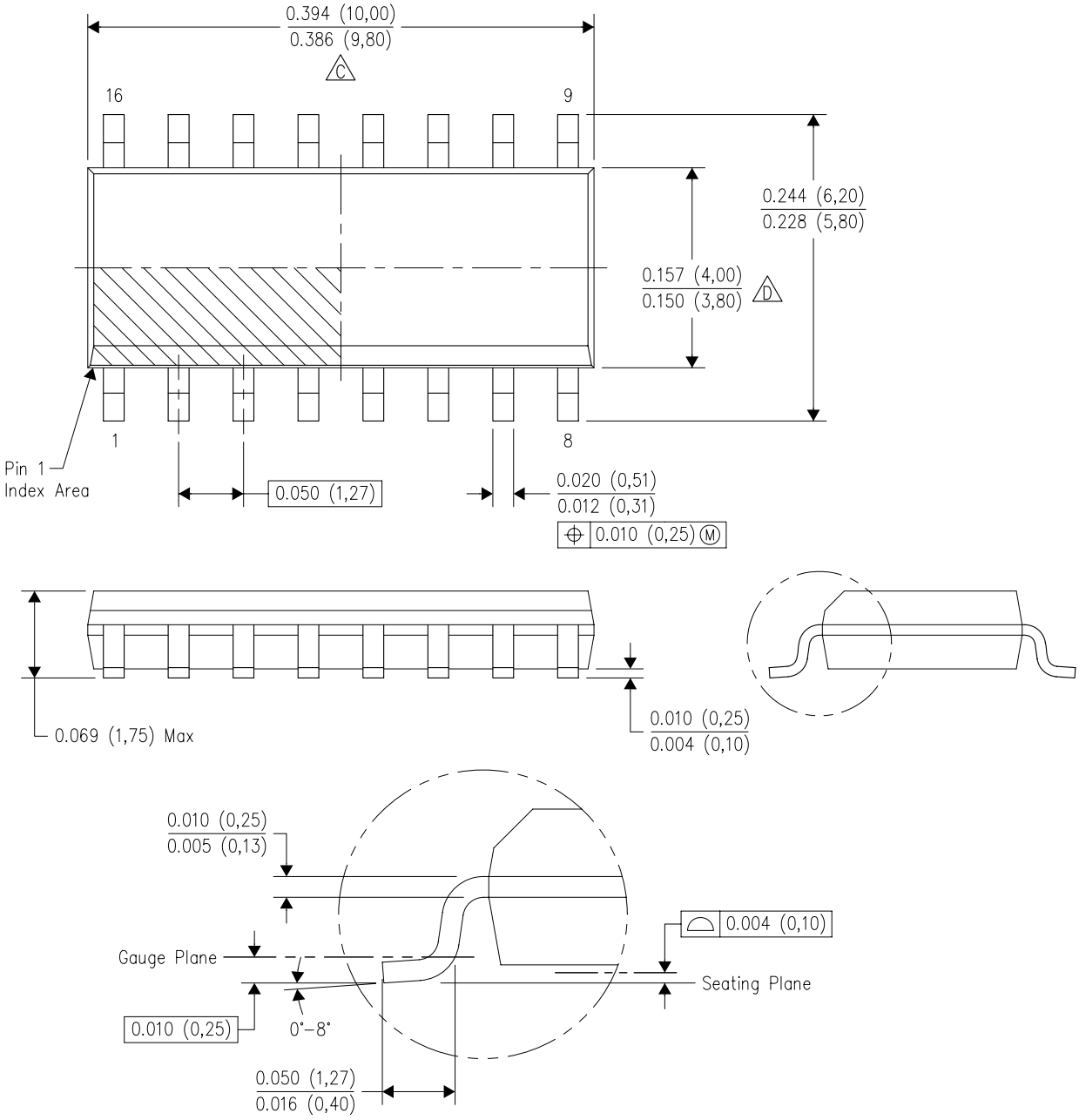
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



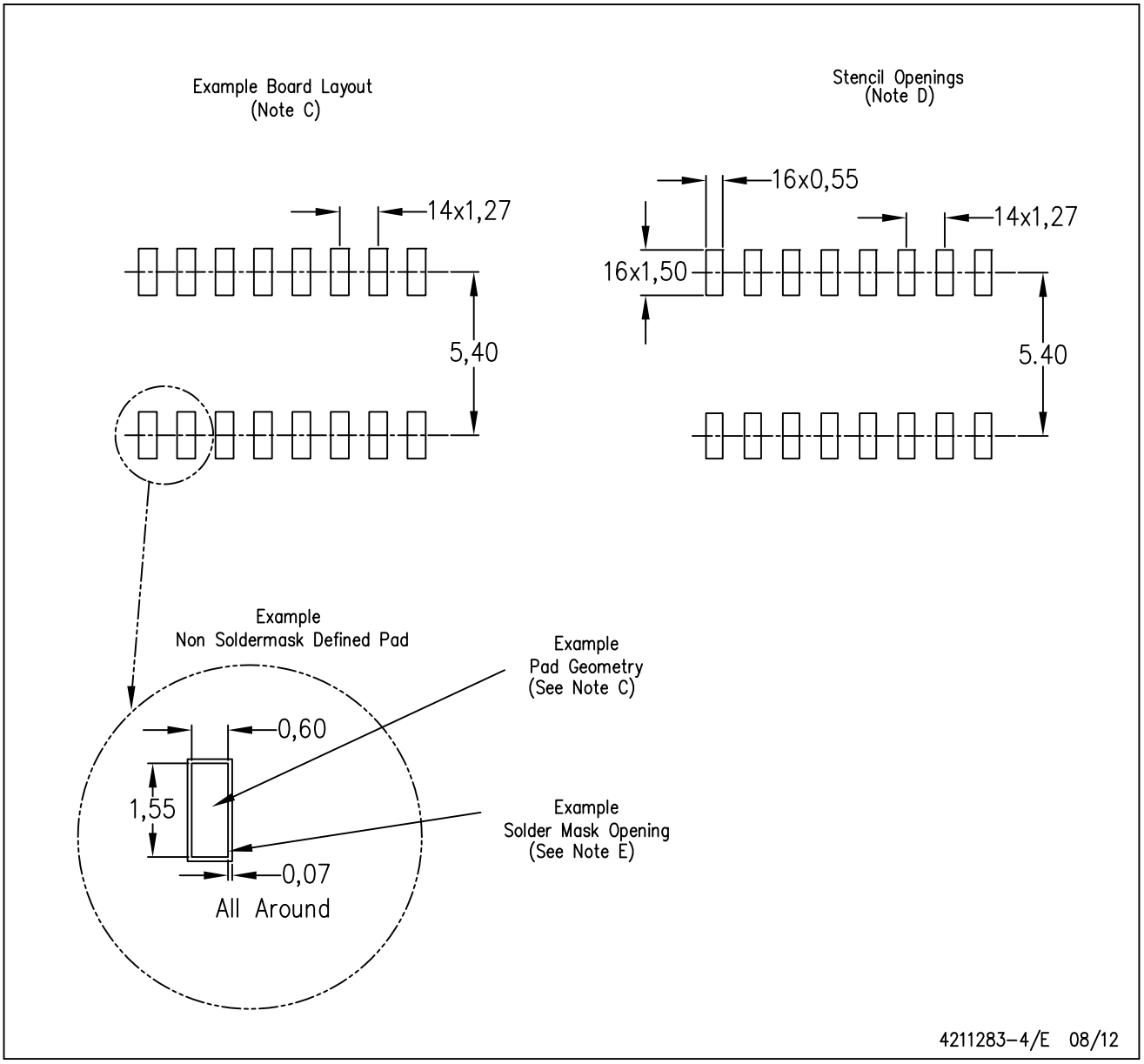
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



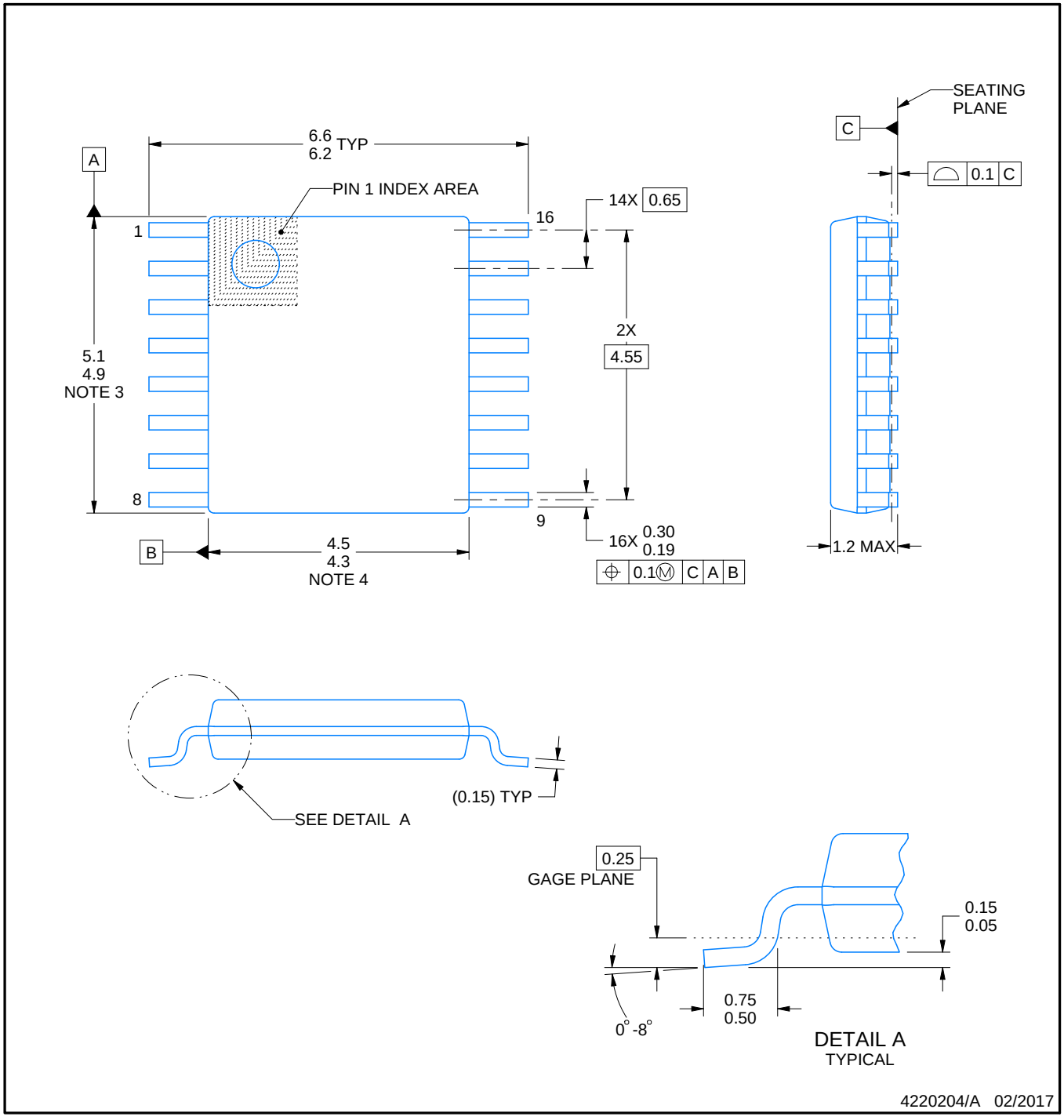
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

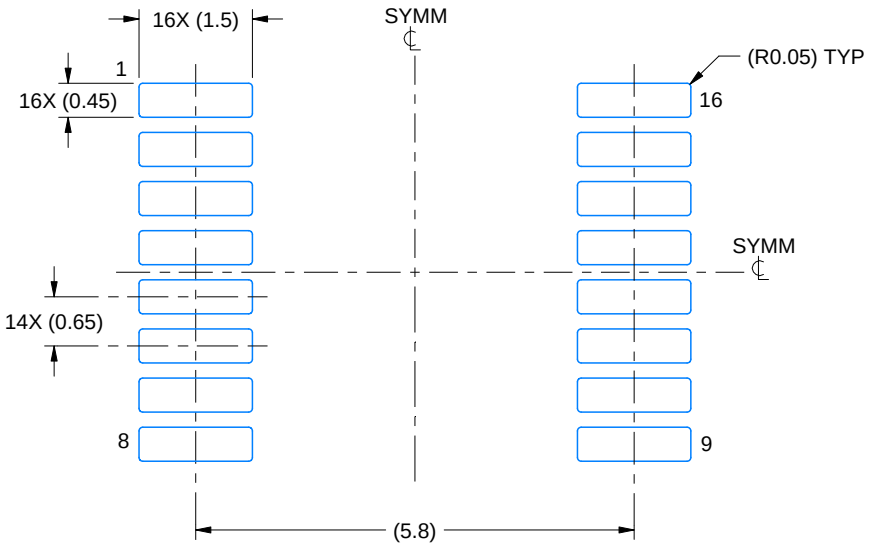
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

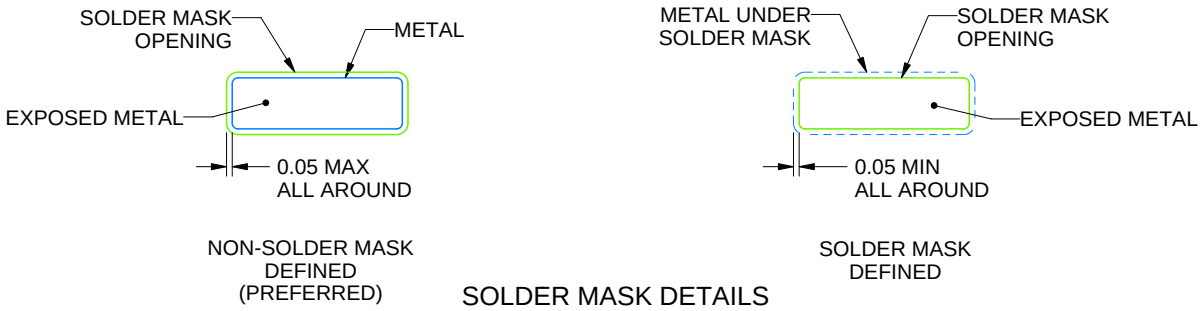


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

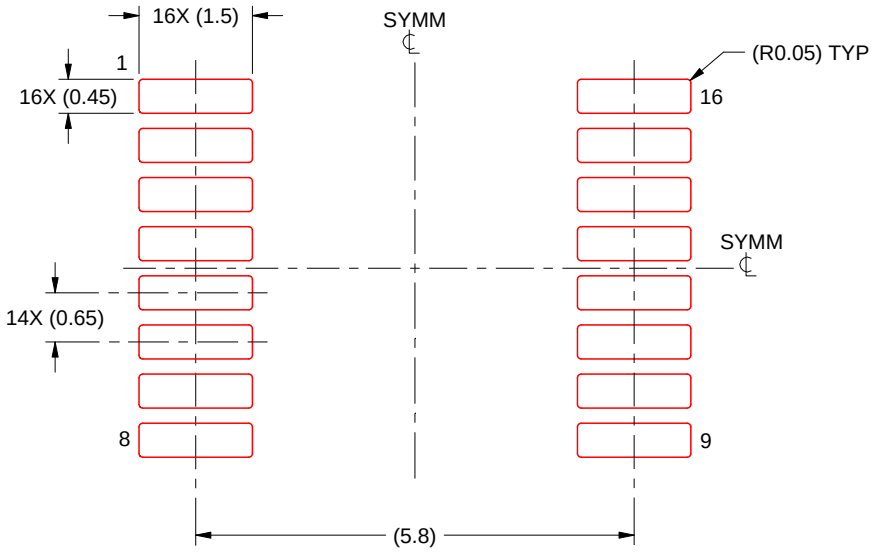


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



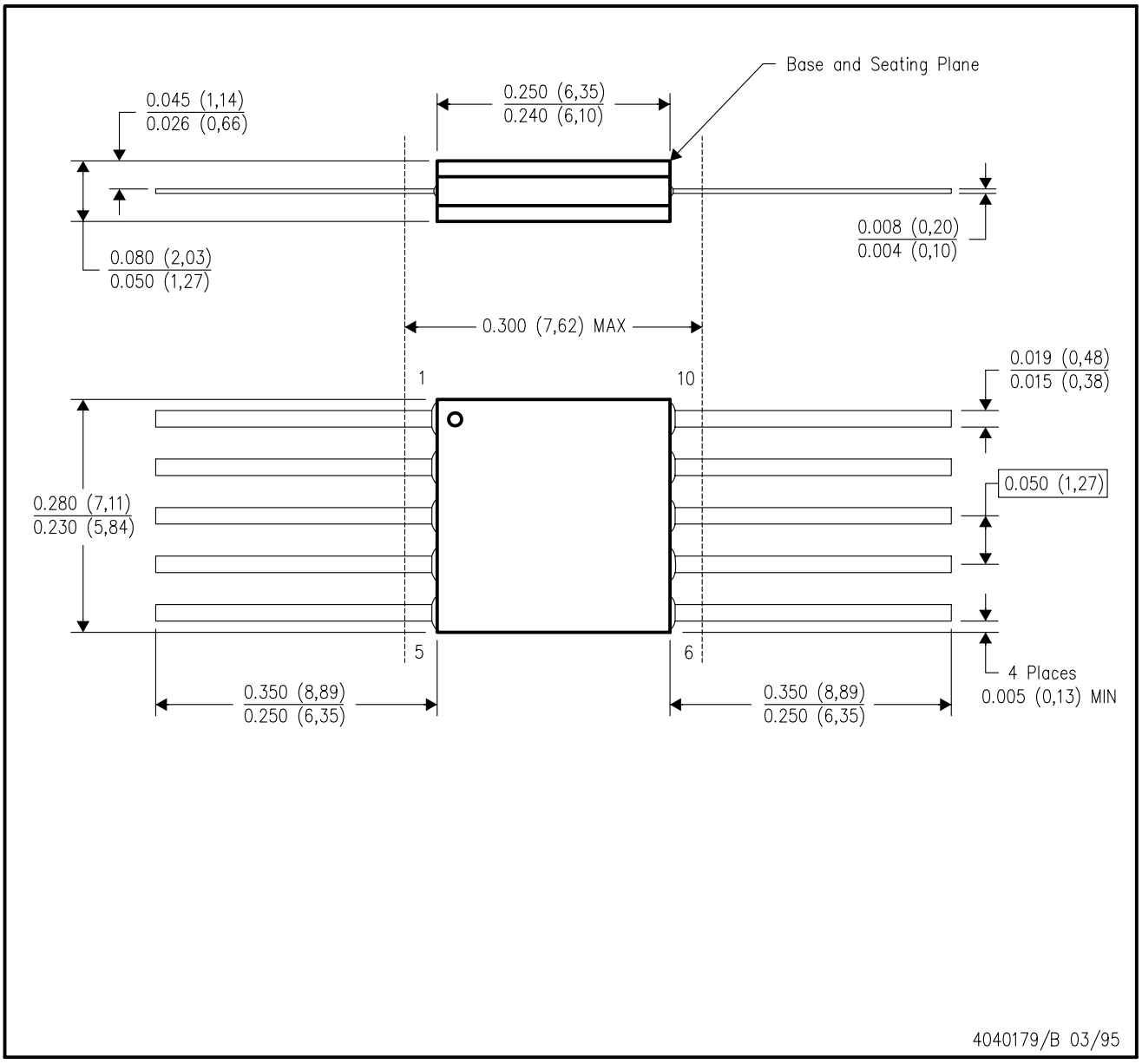
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK

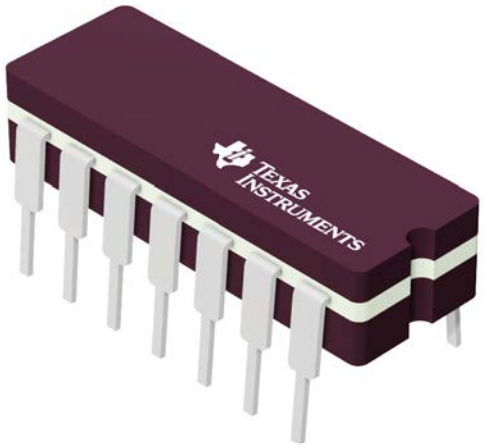


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

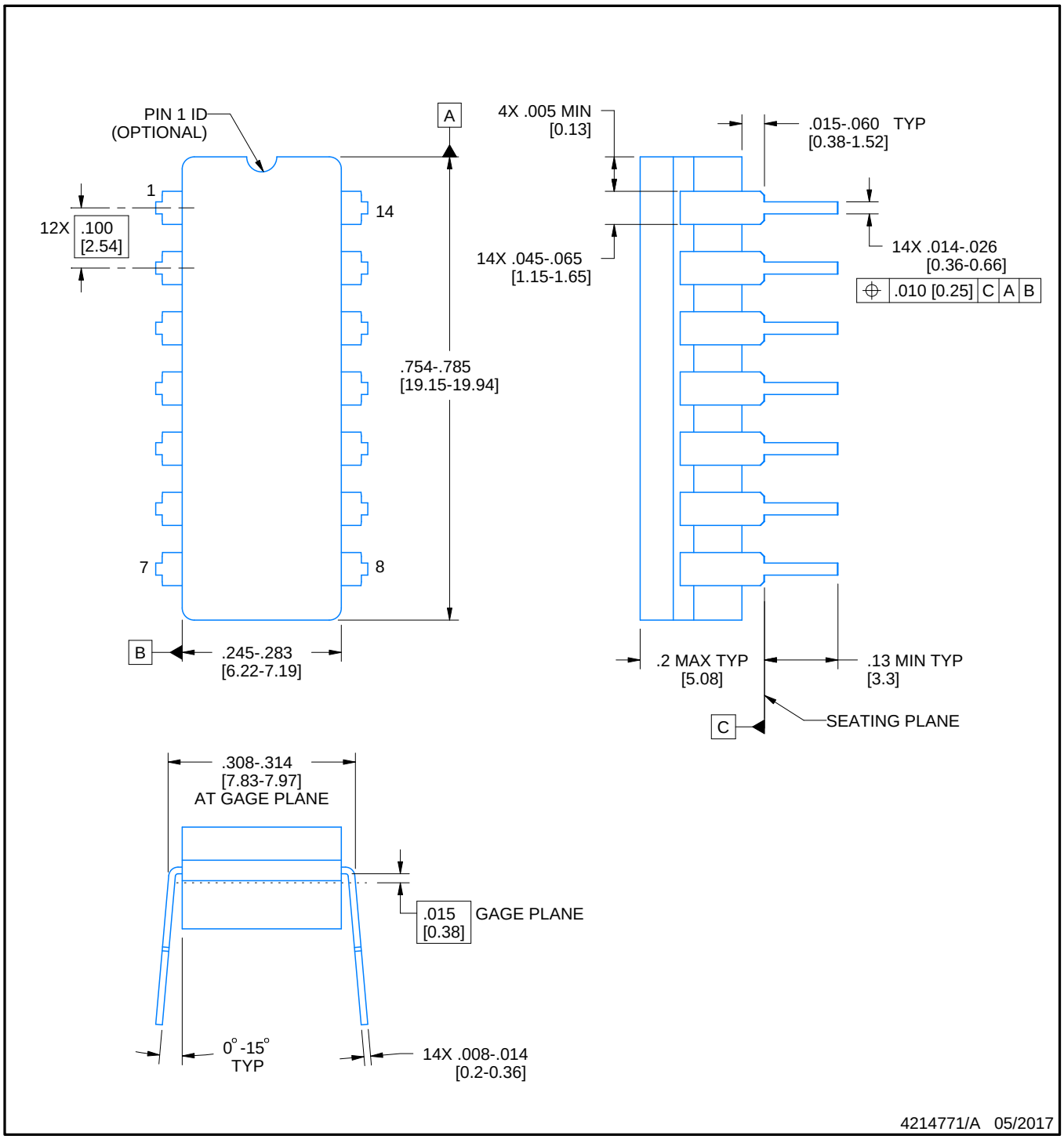
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

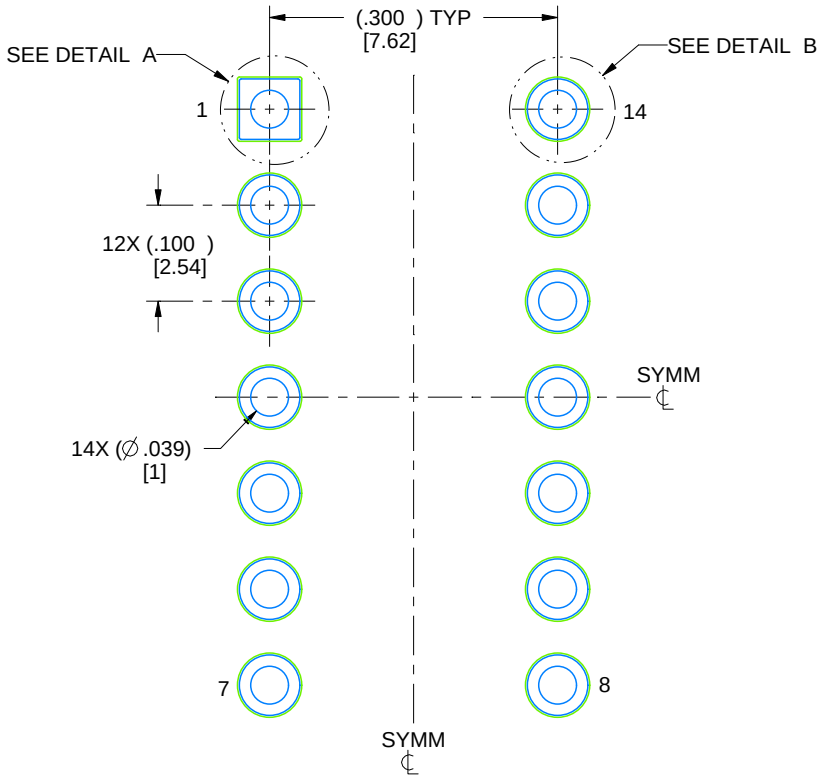
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

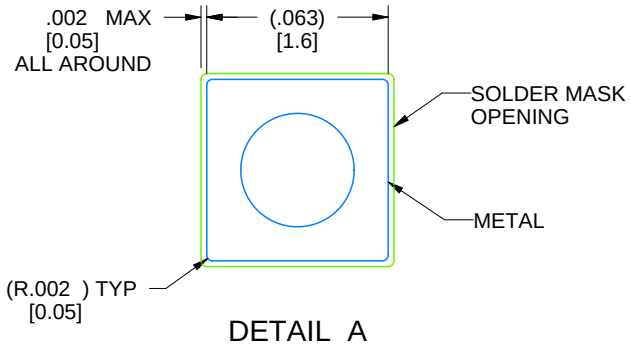
J0014A

CDIP - 5.08 mm max height

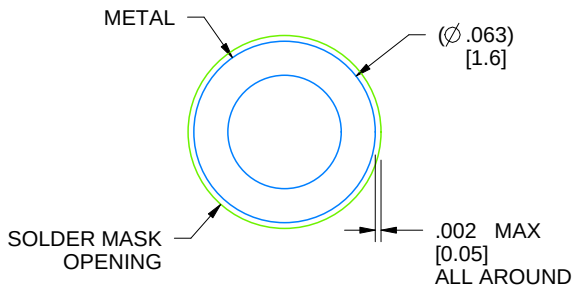
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

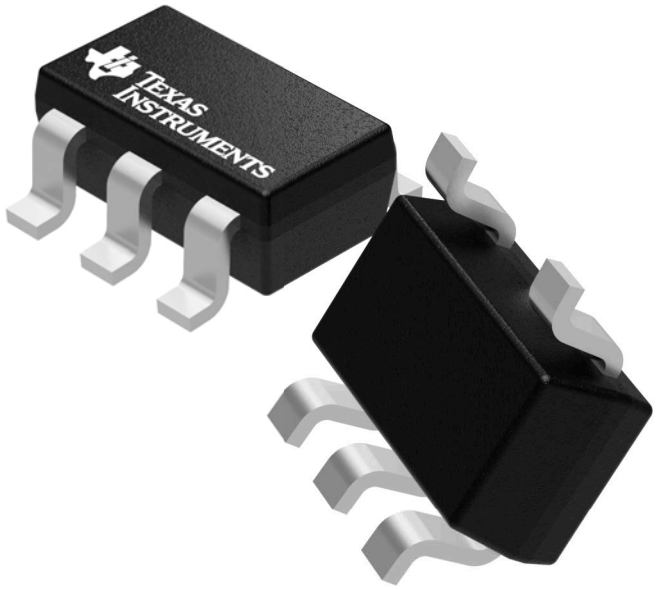


DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



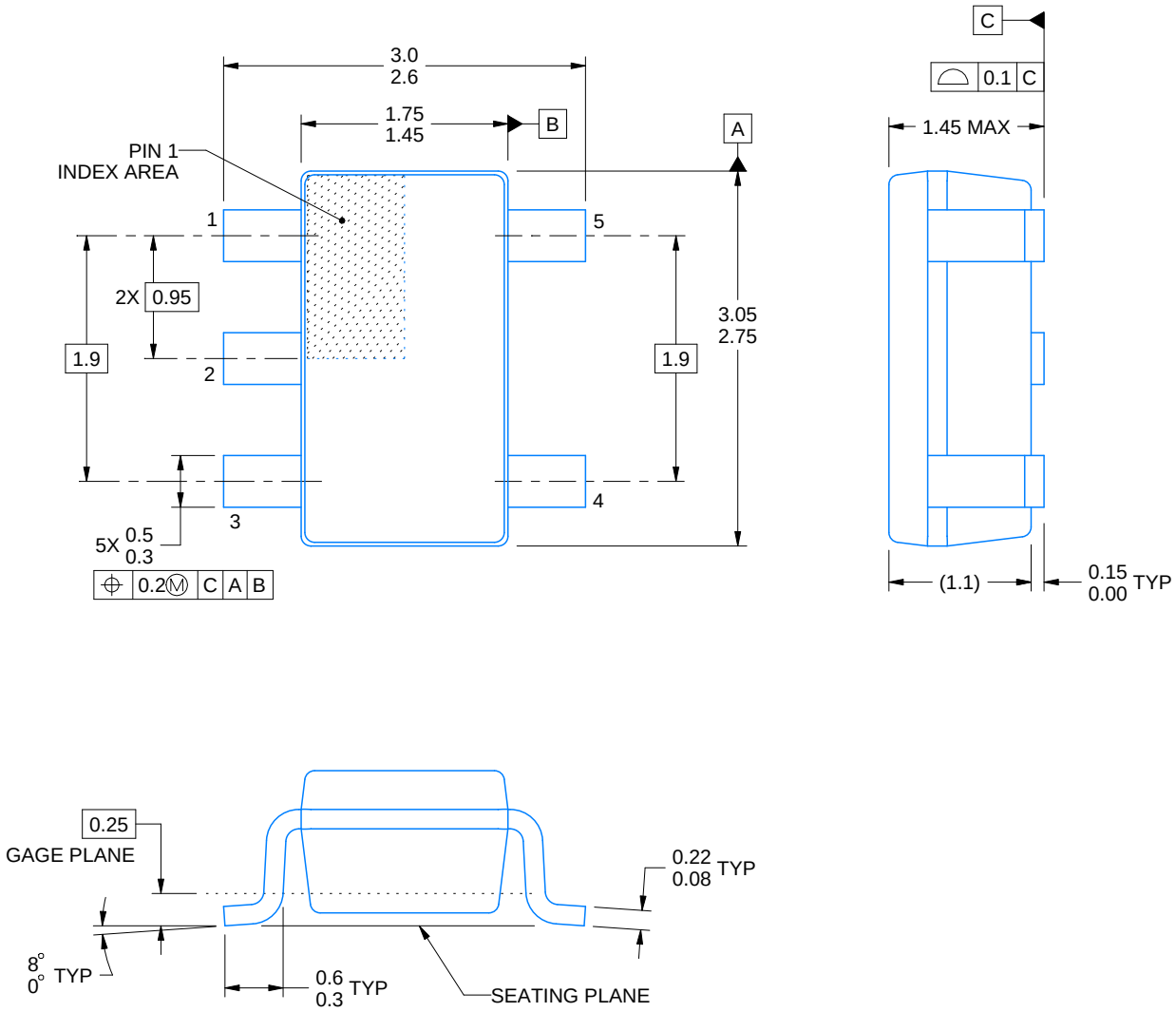
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

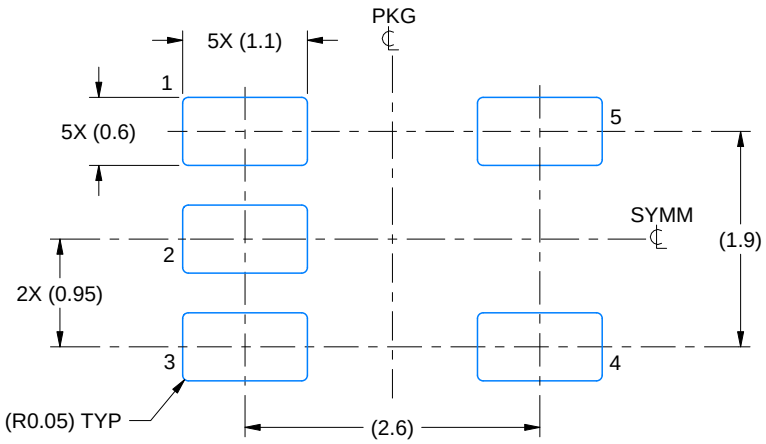
SMALL OUTLINE TRANSISTOR



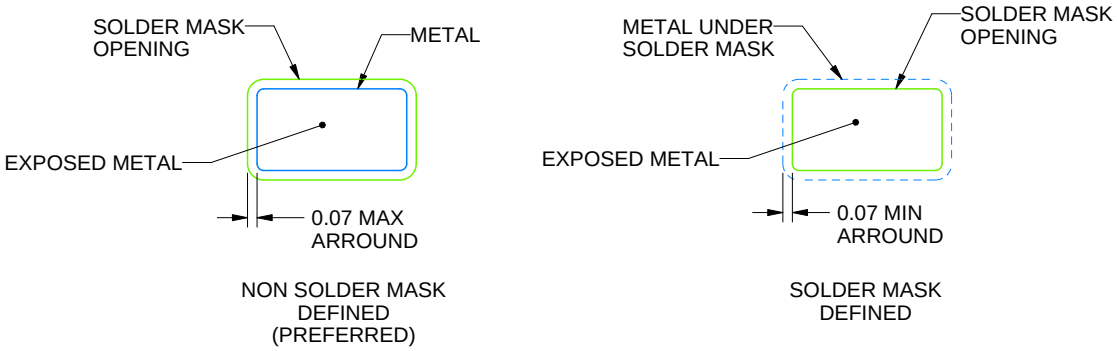
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

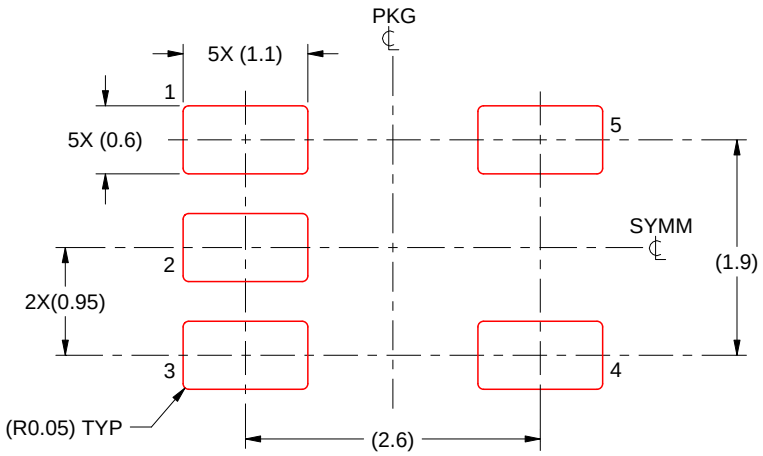


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

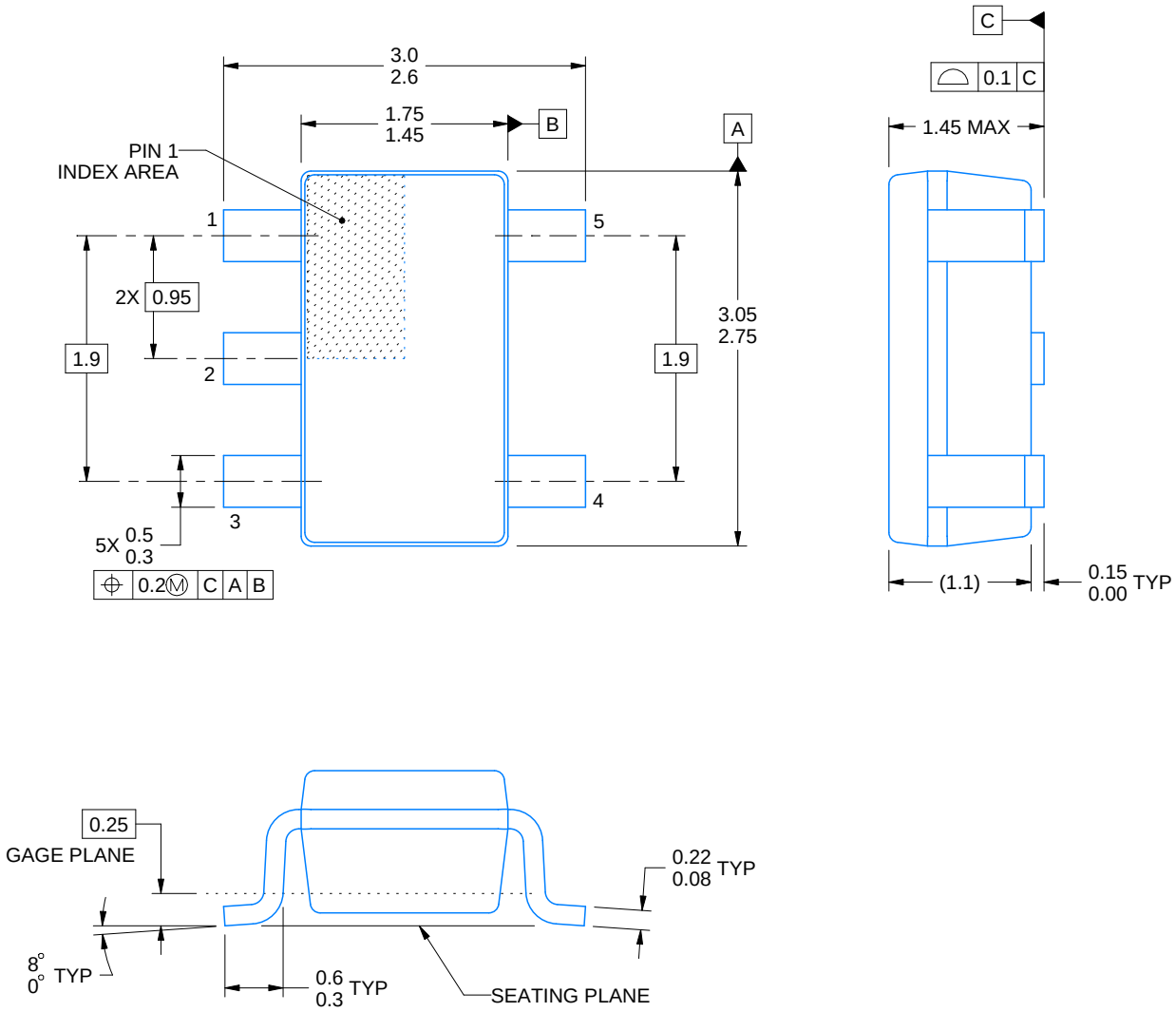
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

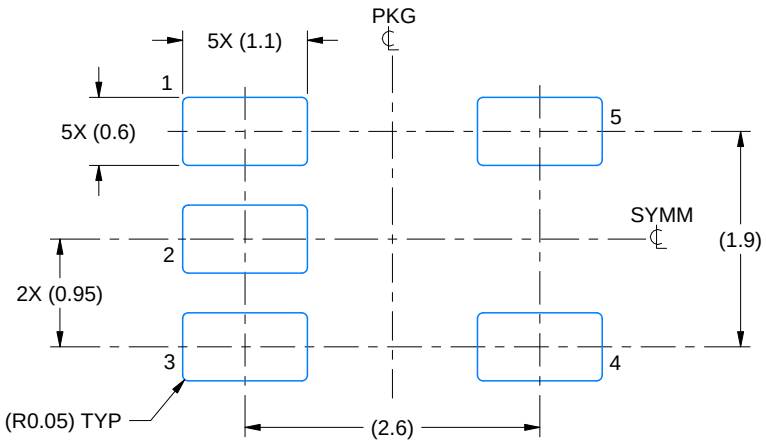
SMALL OUTLINE TRANSISTOR



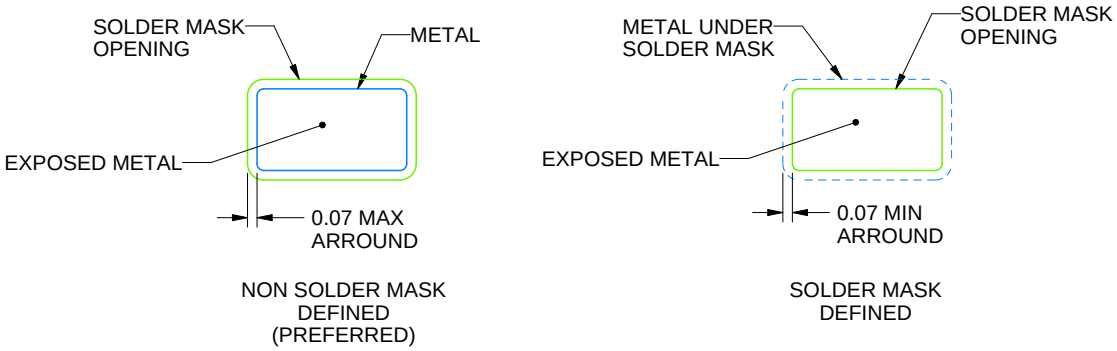
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

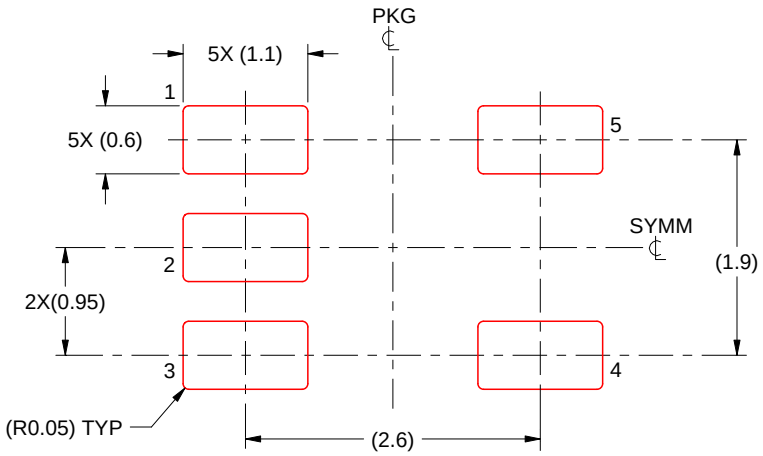


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



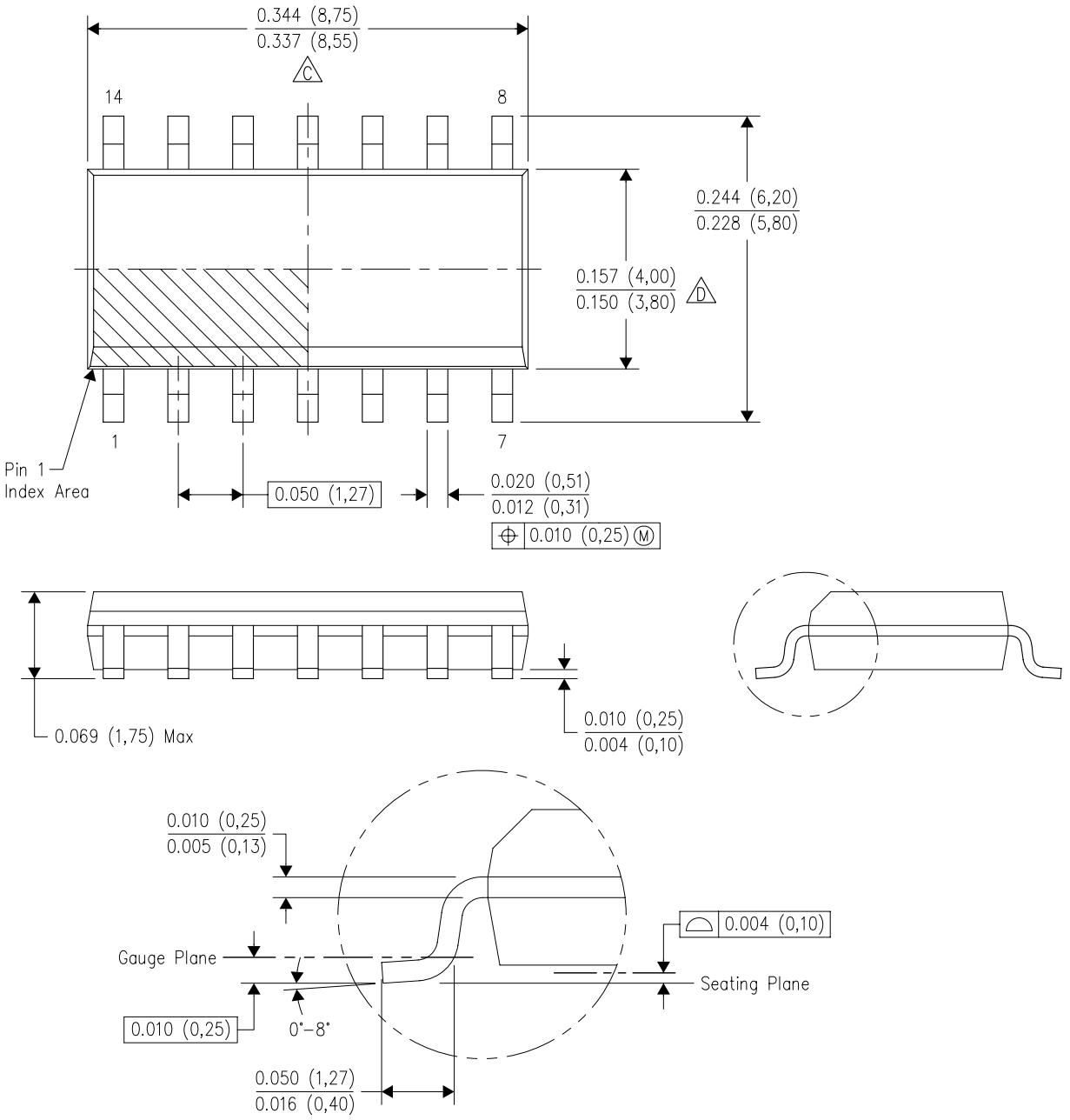
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

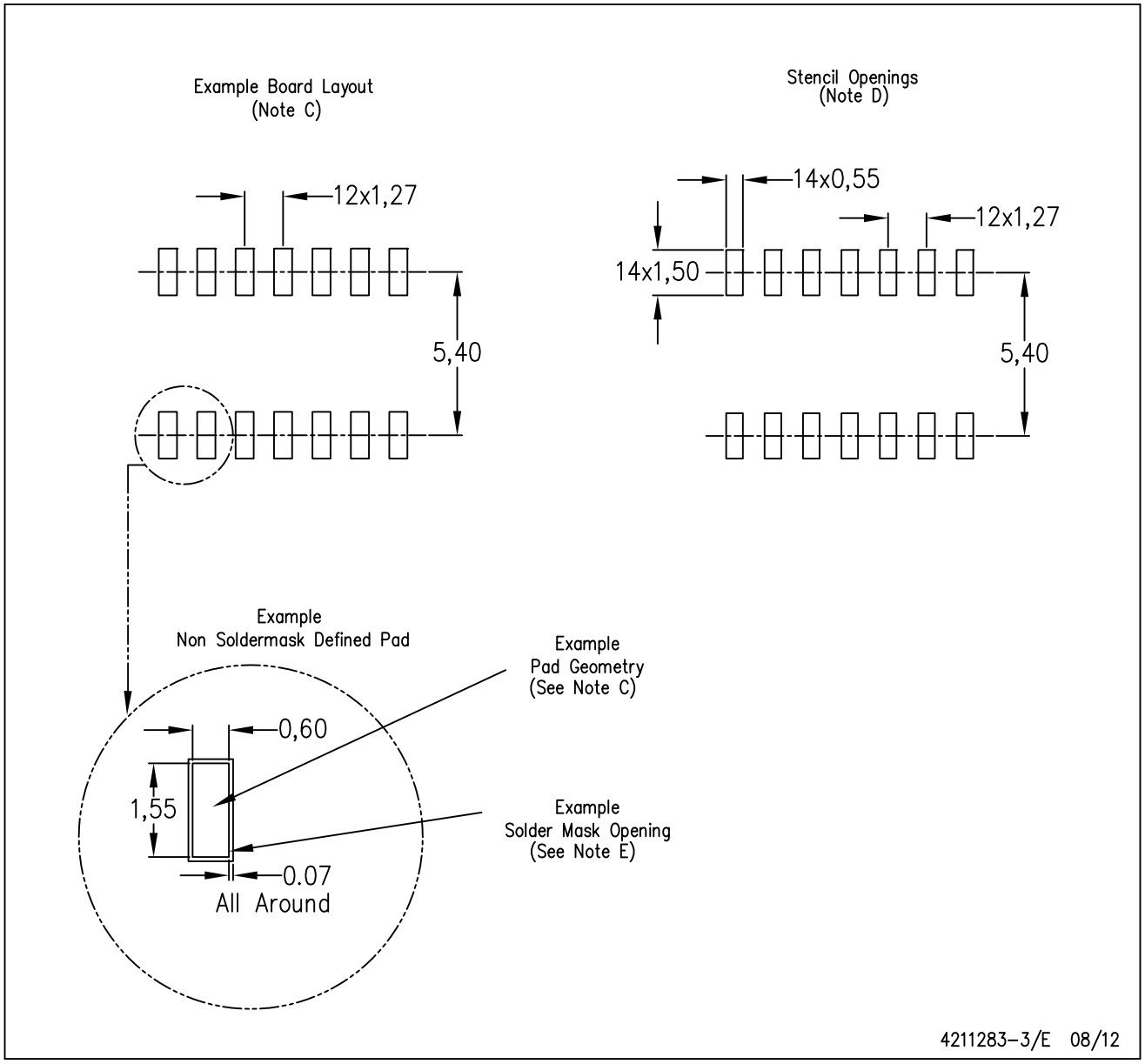
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

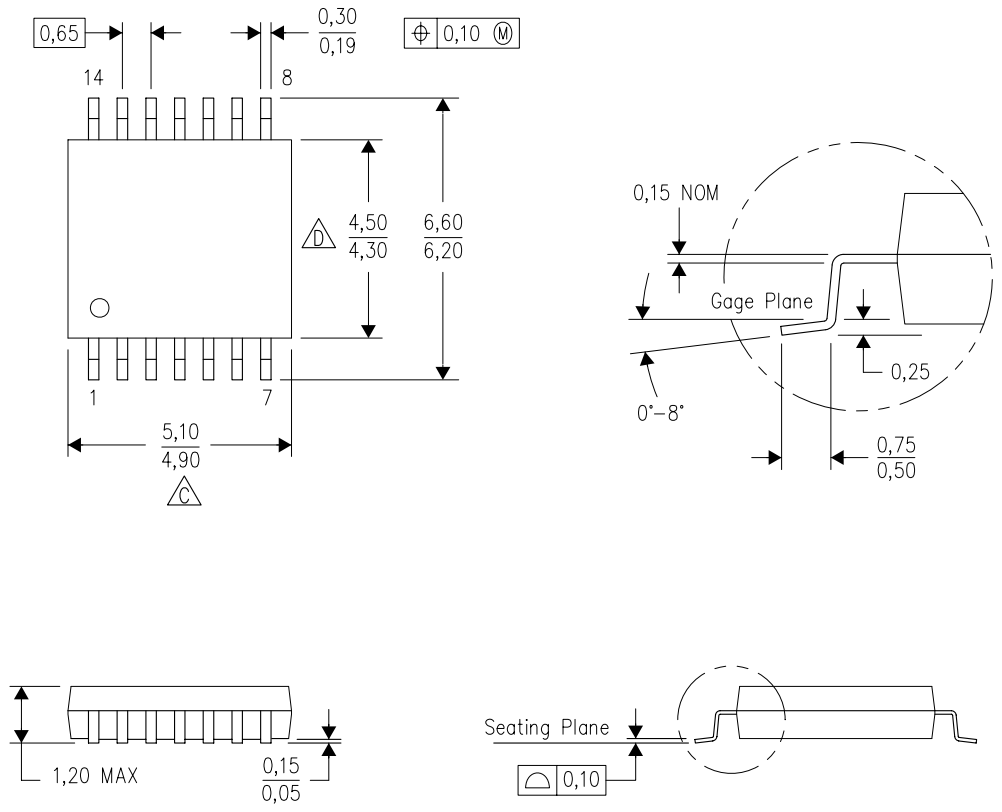
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

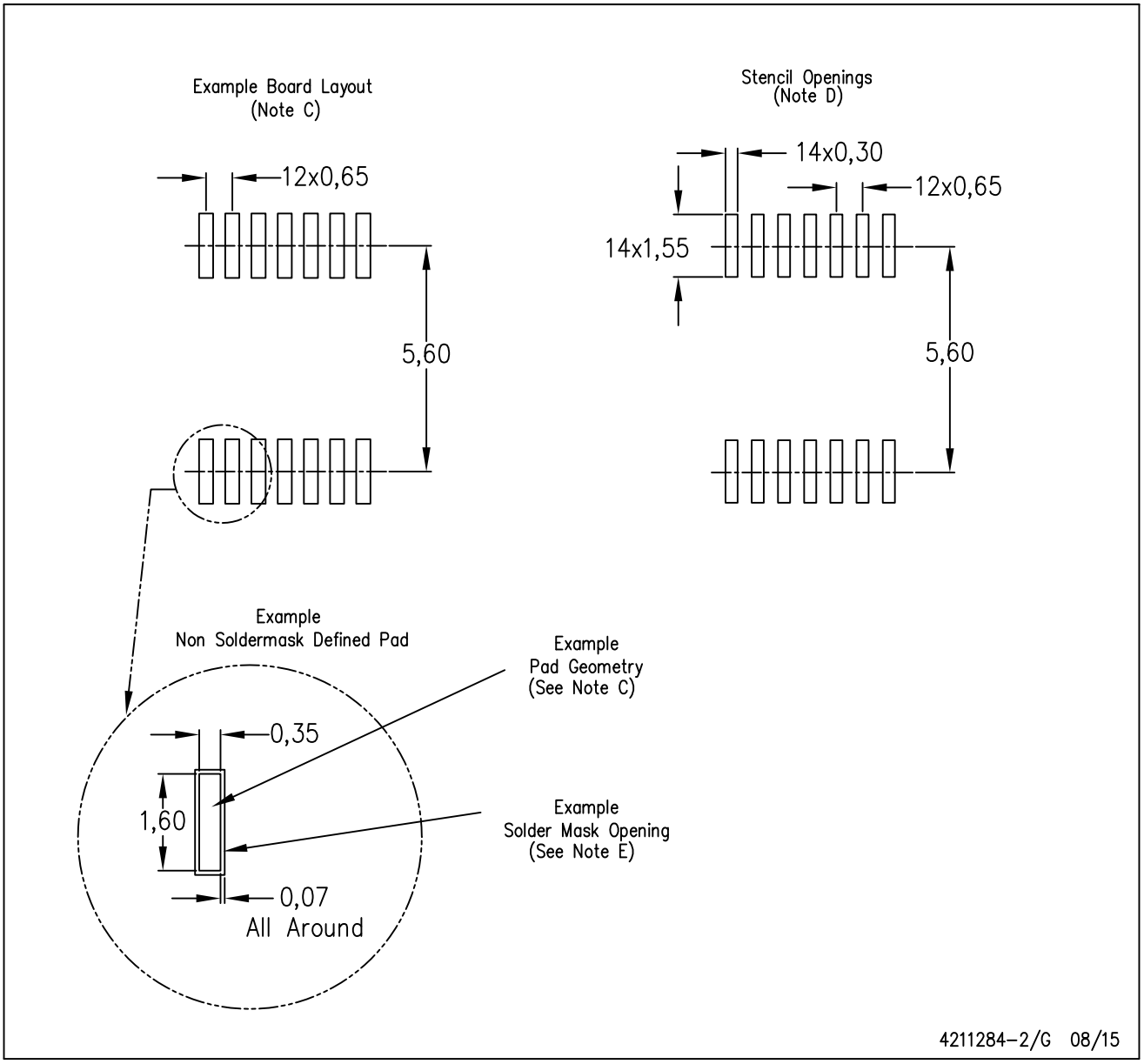
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

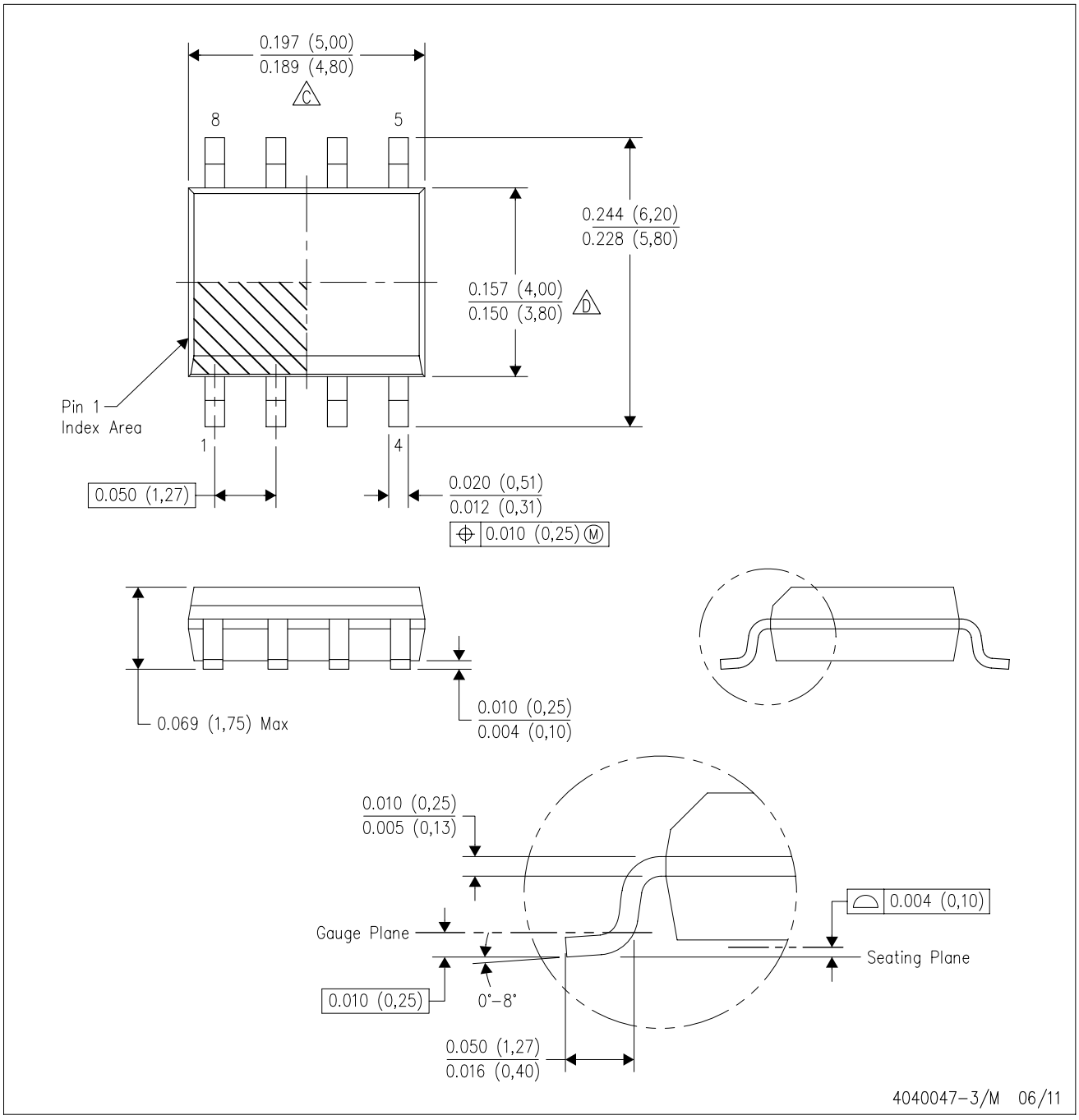
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



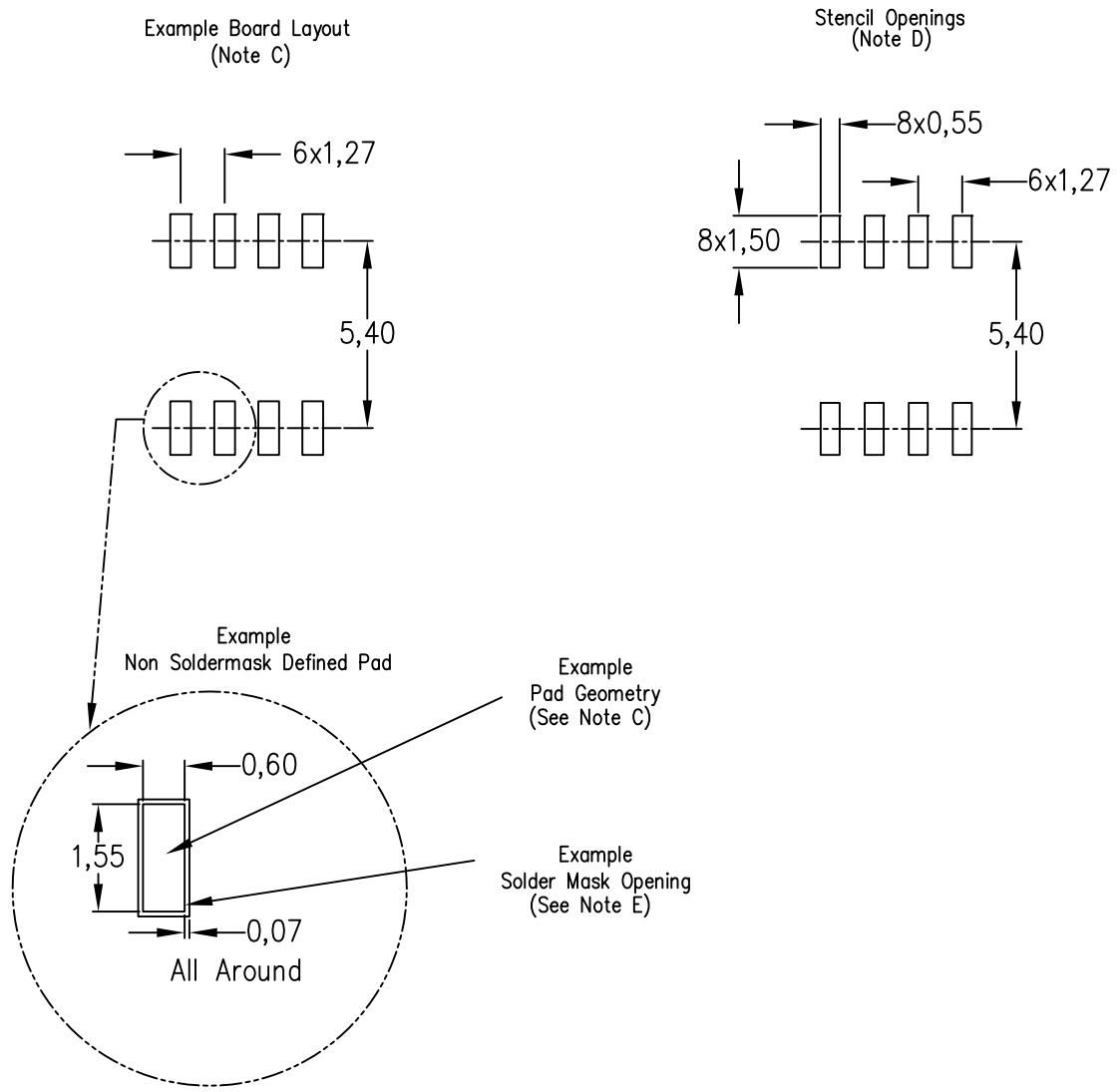
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

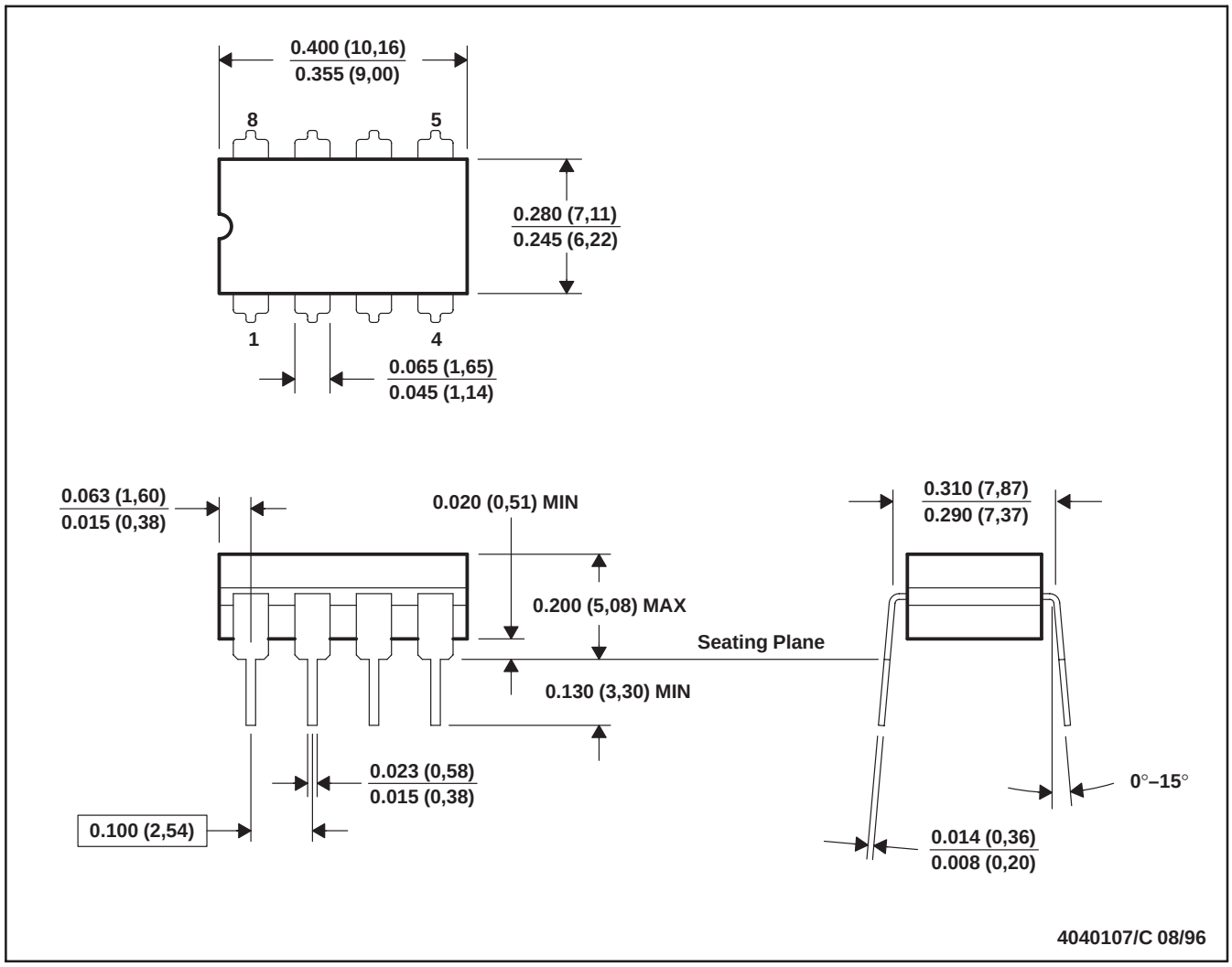
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

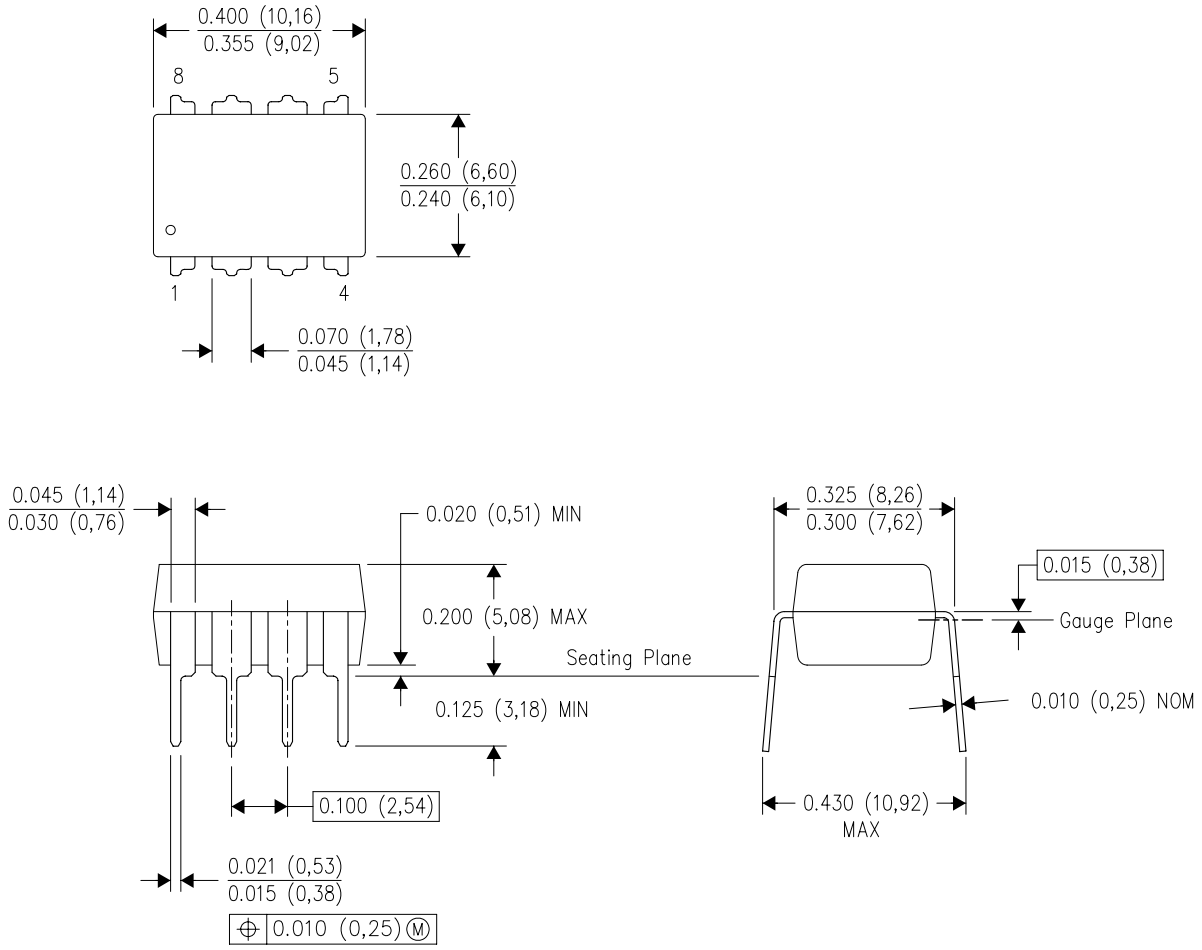
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

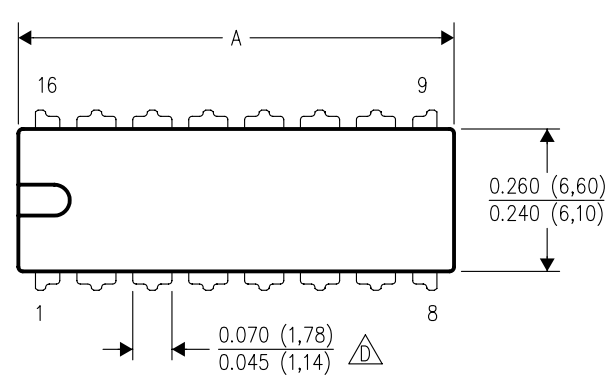


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

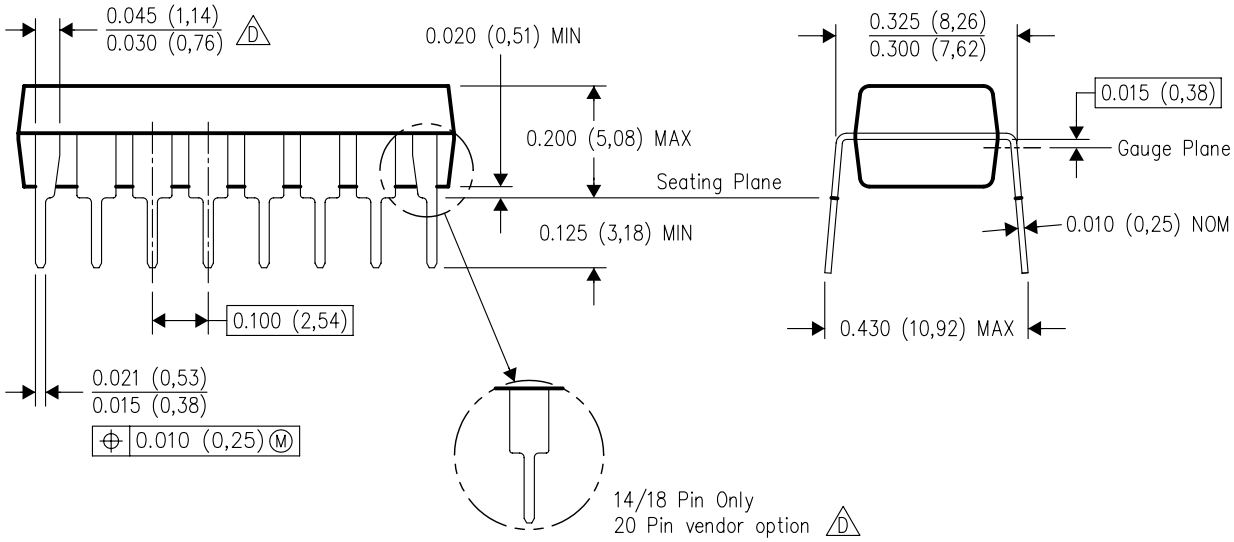
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



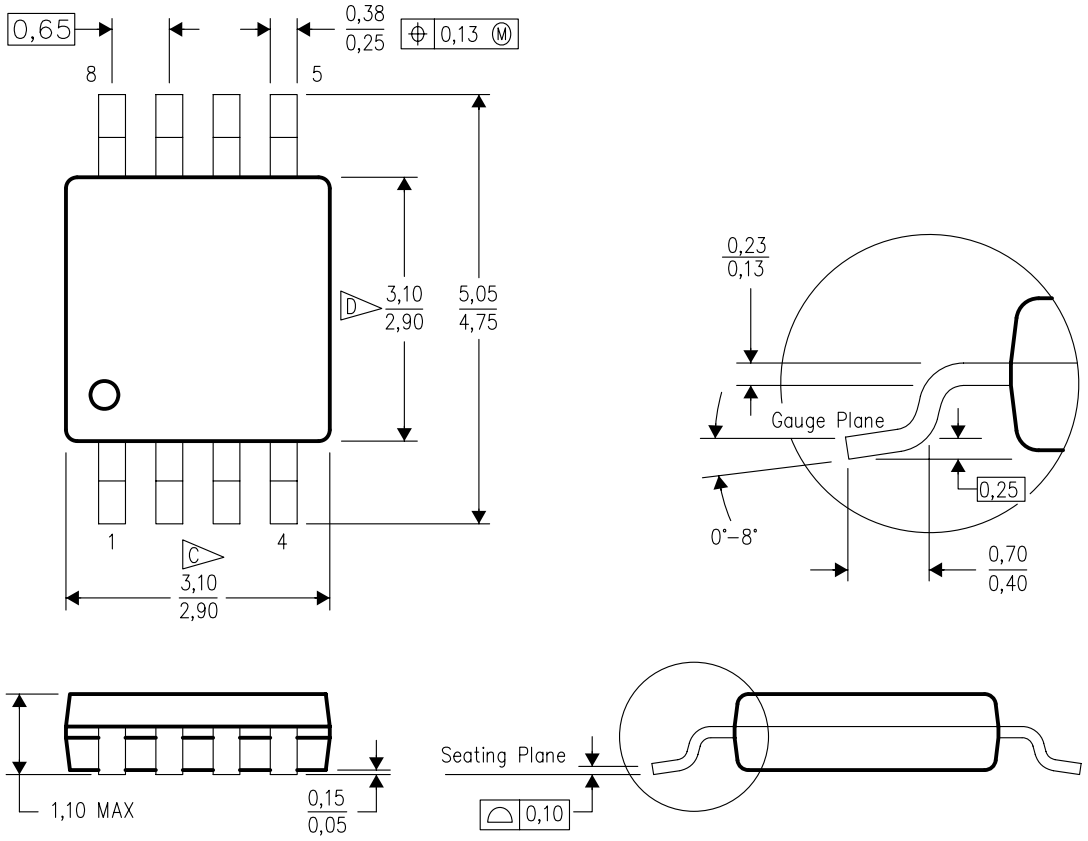
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

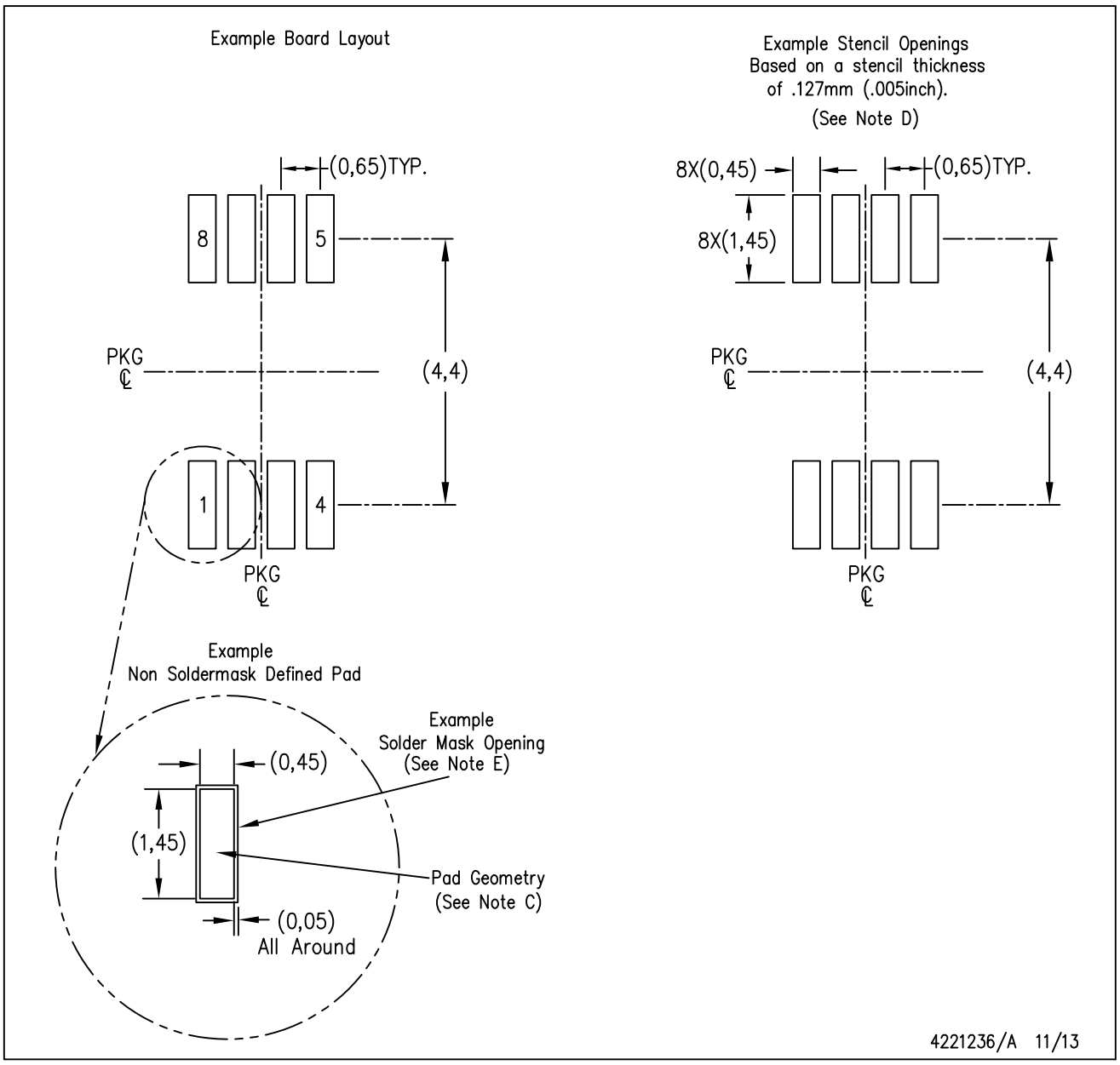
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

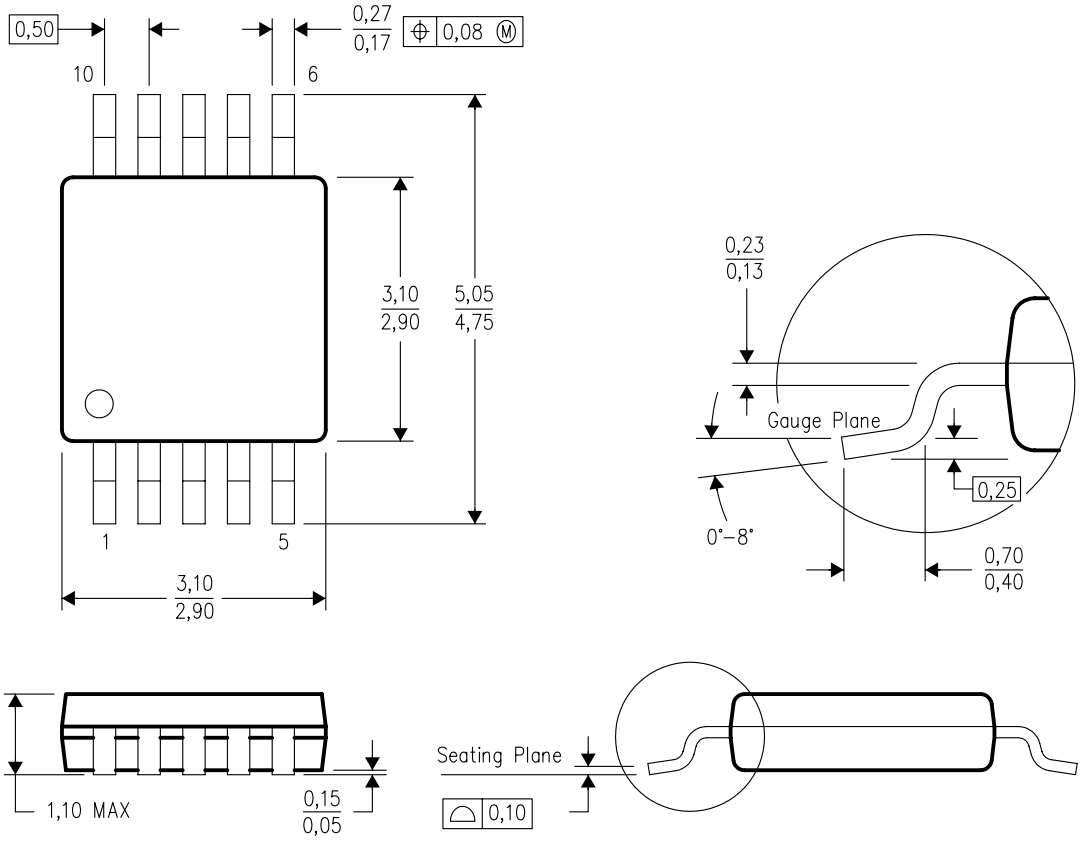
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

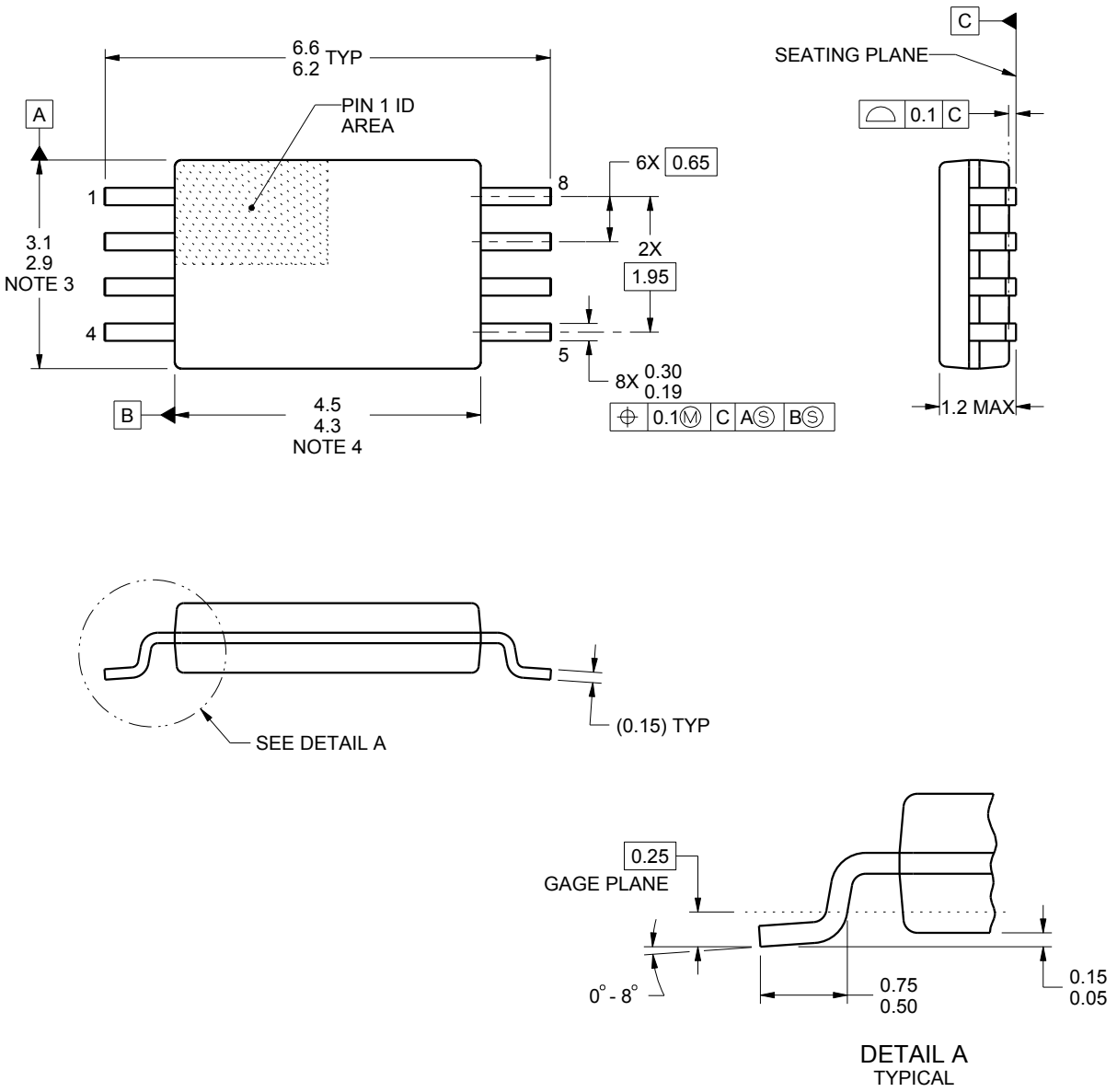
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

PACKAGE OUTLINE

PW0008A

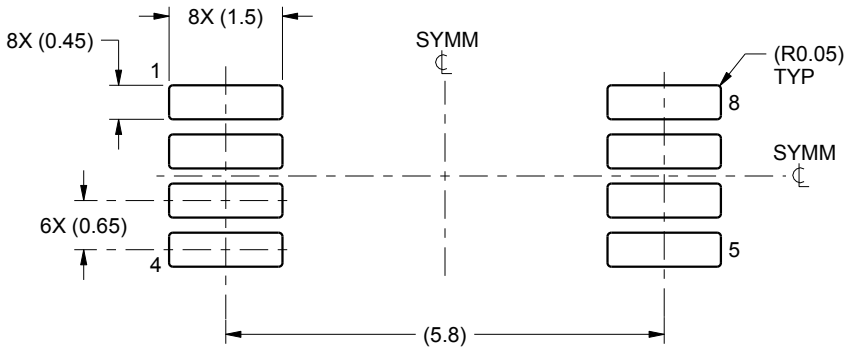
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

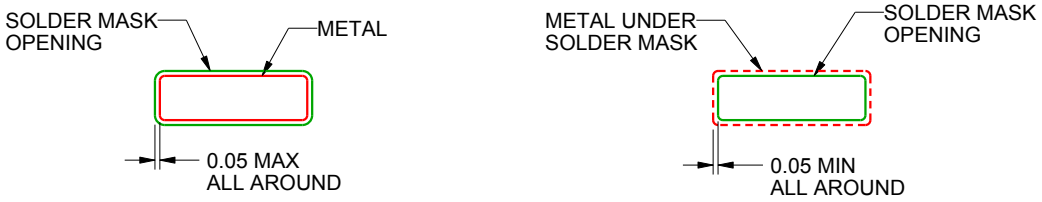


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

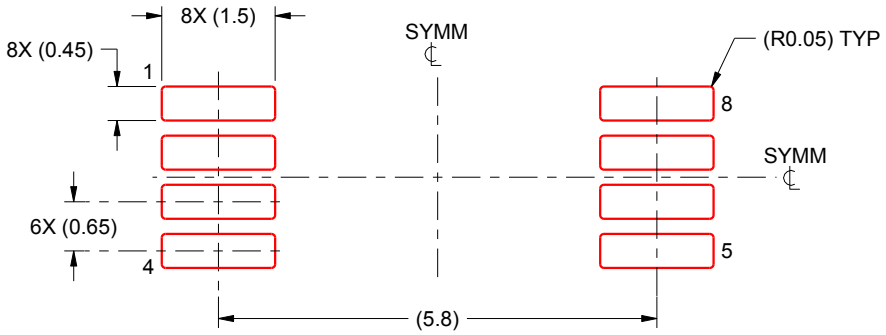


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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