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50/50
Sahar

•
Grade Breakdown•Points••
•
Build symmetrical CMOS inverter•4••
•
Show effect of charge sharing with 4 different clock per.•12••
•
Show effect of leakage with 4 different clock per.•12••
•
Back of the envelope calculation•5••
•
Min. Vout & the corresponding clk per. from SPICE•5••
•
Max Ileak for Vout to drop to 3V•6••
•
Verify the clk period•4••
•
Total(Part 1)•48••

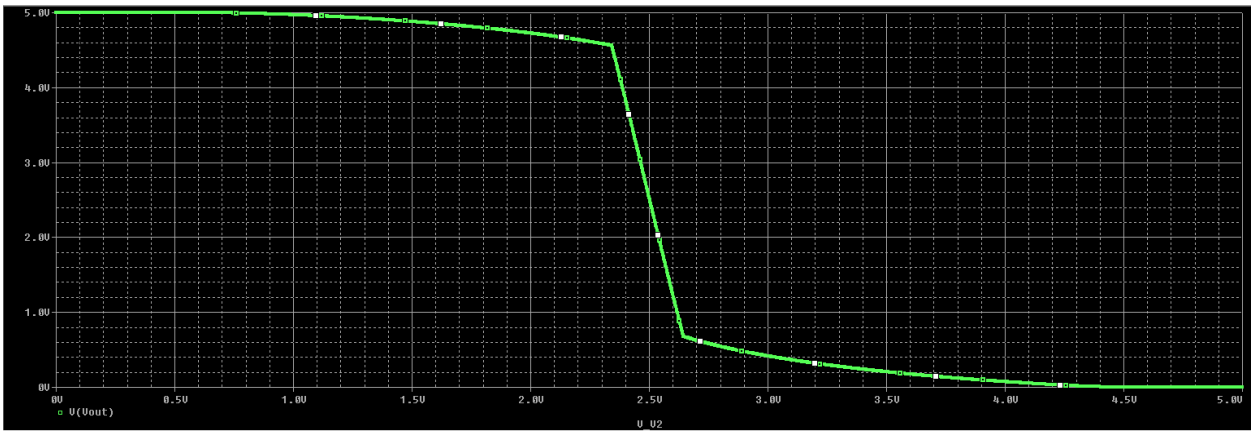
1) Dynamic CMOS NAND Gate

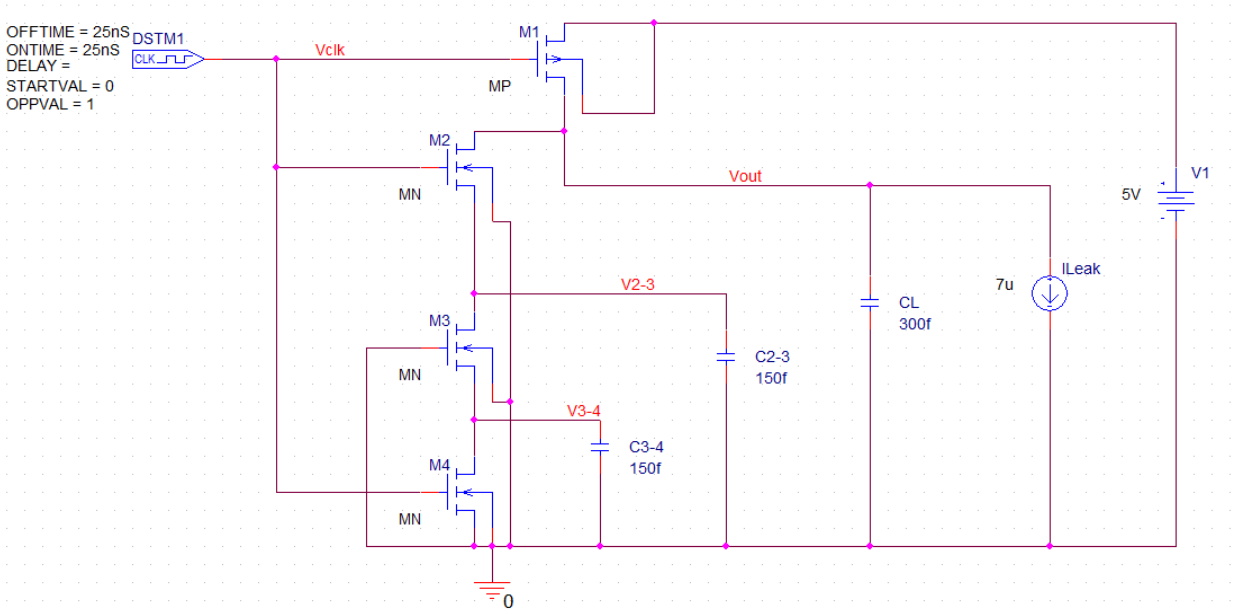
Below are the calculations for our symm

$9.0\ x\ 1$

$$\frac{9.0\ x\ 10^{-5}}{3 * 2.2\ x\ 10^{-5}} = \frac{W_p}{L_p} \rightarrow \frac{W_p}{L_p} = \frac{3}{2.2}$$

Experimentally, W_p =4.69um and L_p = 2.2um

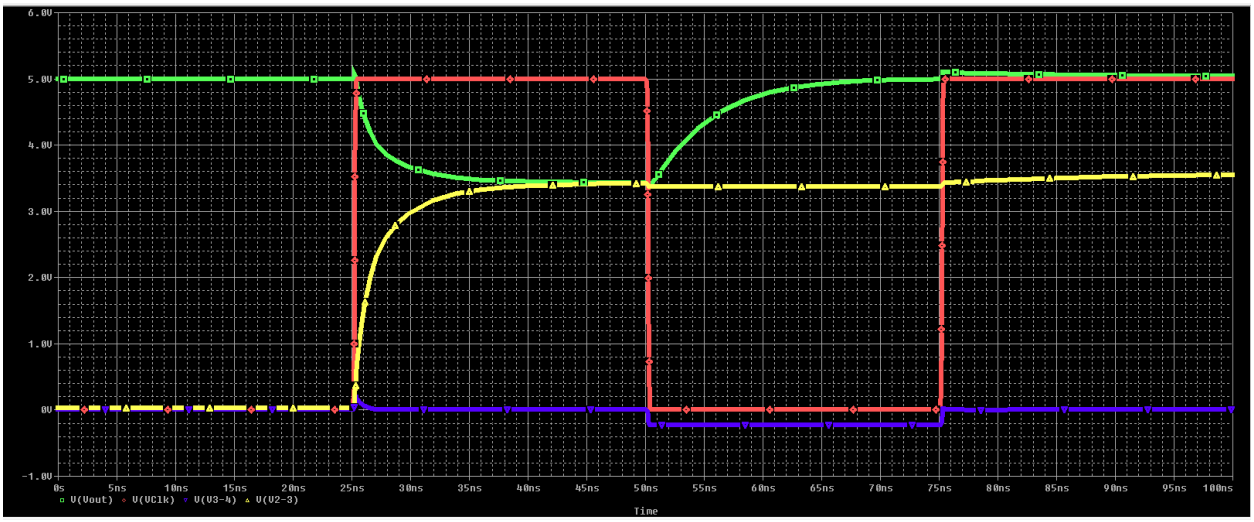




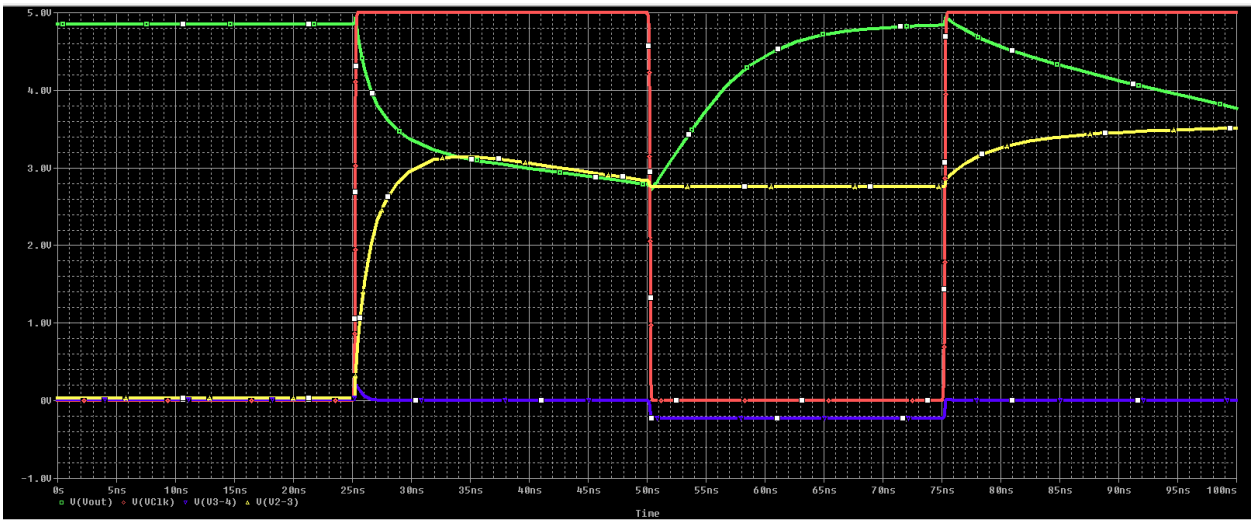
After replacing the pull down transistor with three pull down transistors in series, we ran our simulation of charge sharing and leakage current for 4 different clock periods: 25ns, 50ns, 100ns, and 200ns.

For 25ns:

Charge sharing

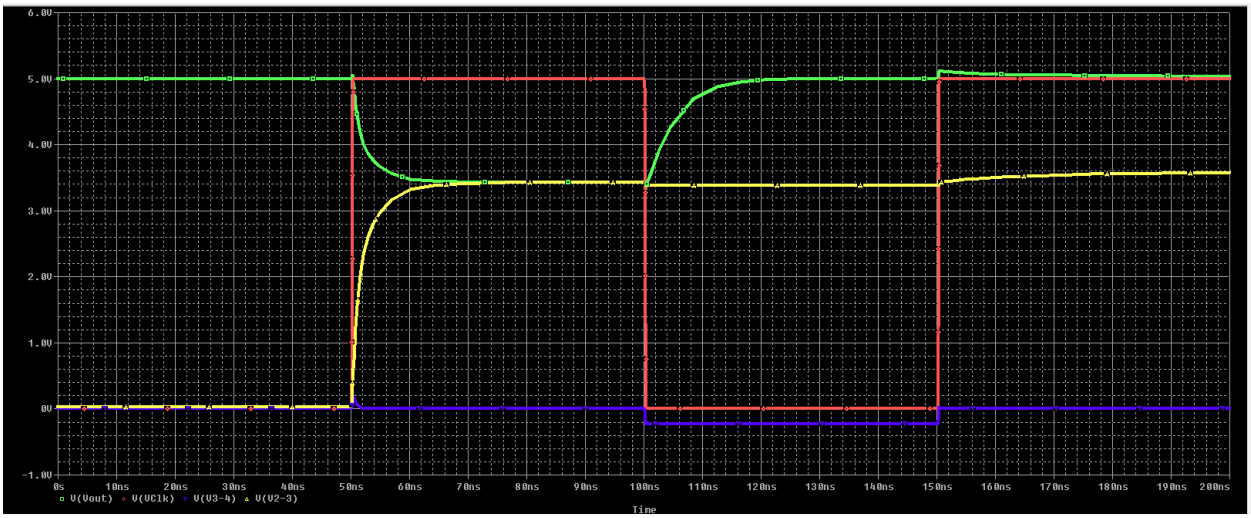


Leakage current

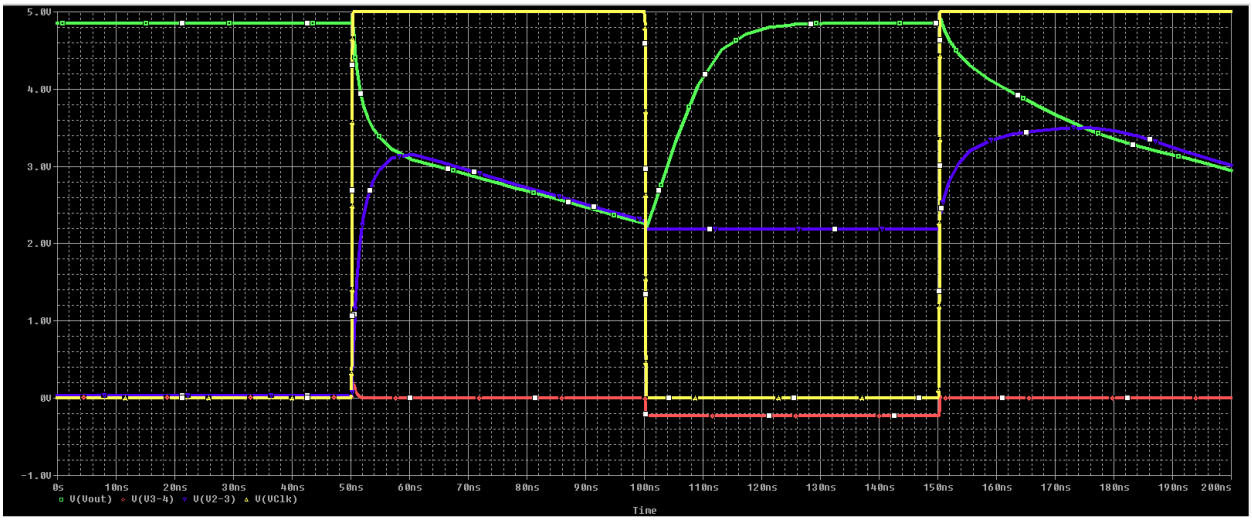


For 50ns:

Charge sharing

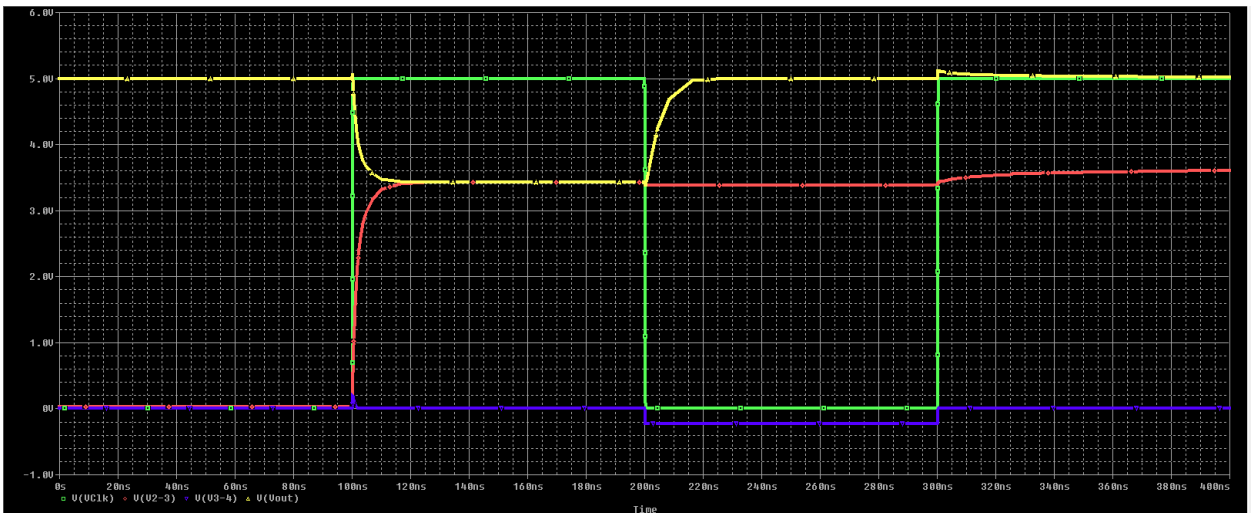


Leakage current



For 100ns:

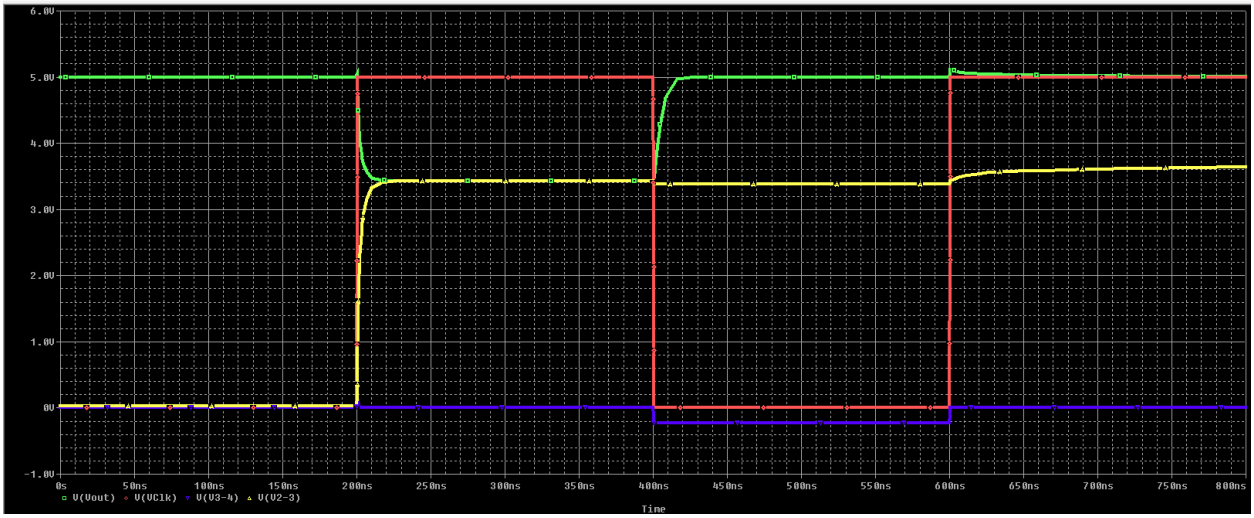
Charge sharing



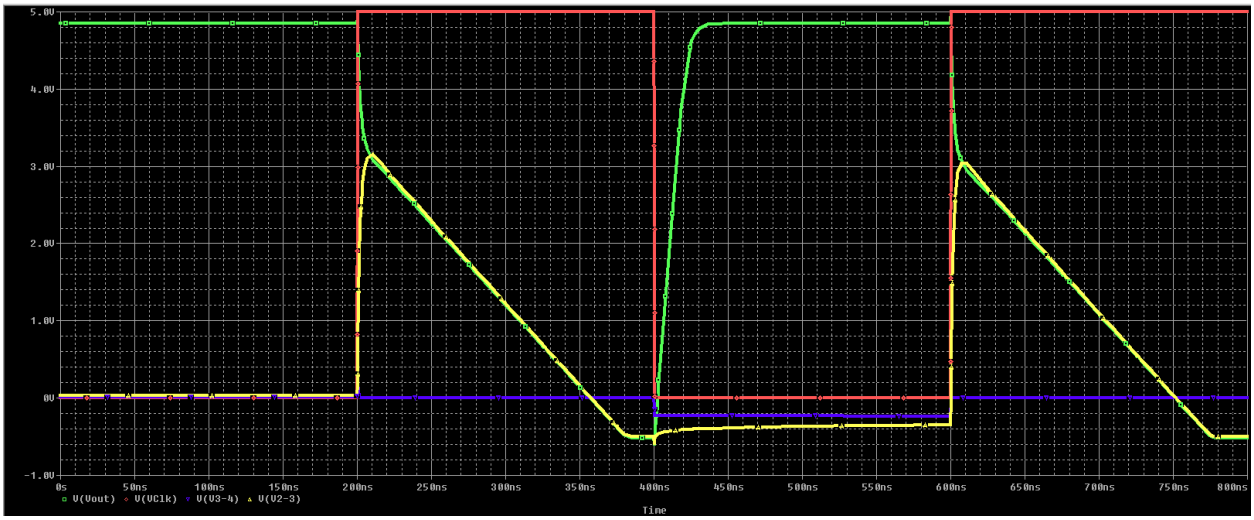
Leakage current

For 200ns:

Charge sharing



Leakage current



These are the calculations for the minimum output voltage.

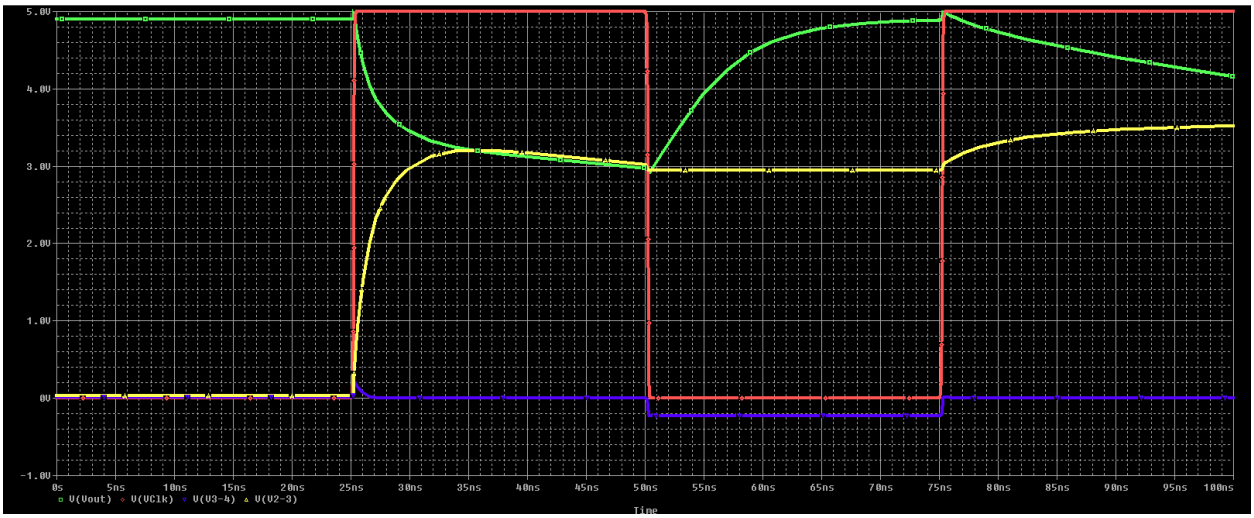
$$\Delta V_{out} = -V_{DD}\frac{C_a}{C_a + C_L}$$

$$= -5 * \frac{150}{150 + 300}$$

$$= -1.67\ Voltage\ drop$$

$$V_{min} = 3.33V$$

After adjusting the clock period to 50ns, we simulated the worst case minimum output voltage to be 3V.



Using this clock period, we simulated the maximum leakage current to be 7µA.

The calculations for leakage current are below.

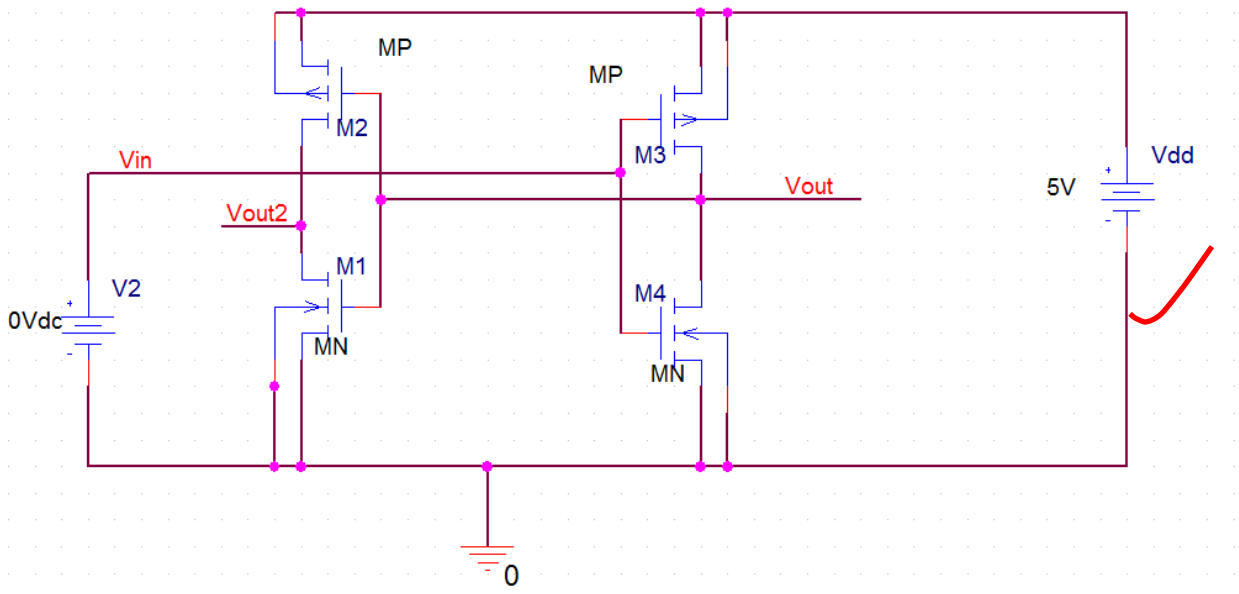
$$I_{leakage} = C\frac{\Delta V}{\Delta t} \rightarrow \Delta t = C\frac{\Delta V}{I_{leakage}}$$

$$= 300\ x\ 10^{-15} * \frac{2}{7 * 10^{-6}}$$

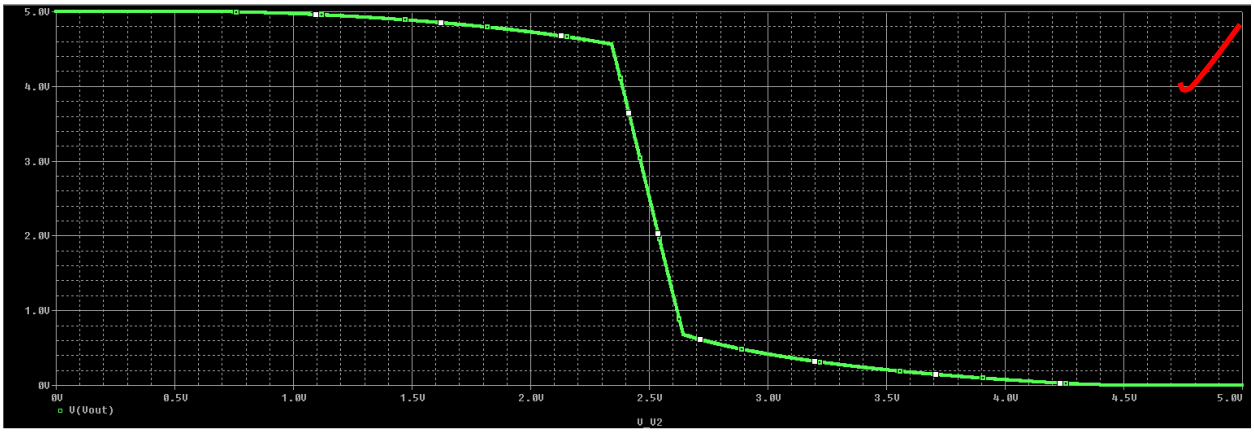
$$\Delta t = 71.14ns$$

As we can see from the calculations and the simulation, our results are off from the 50ns we expected.

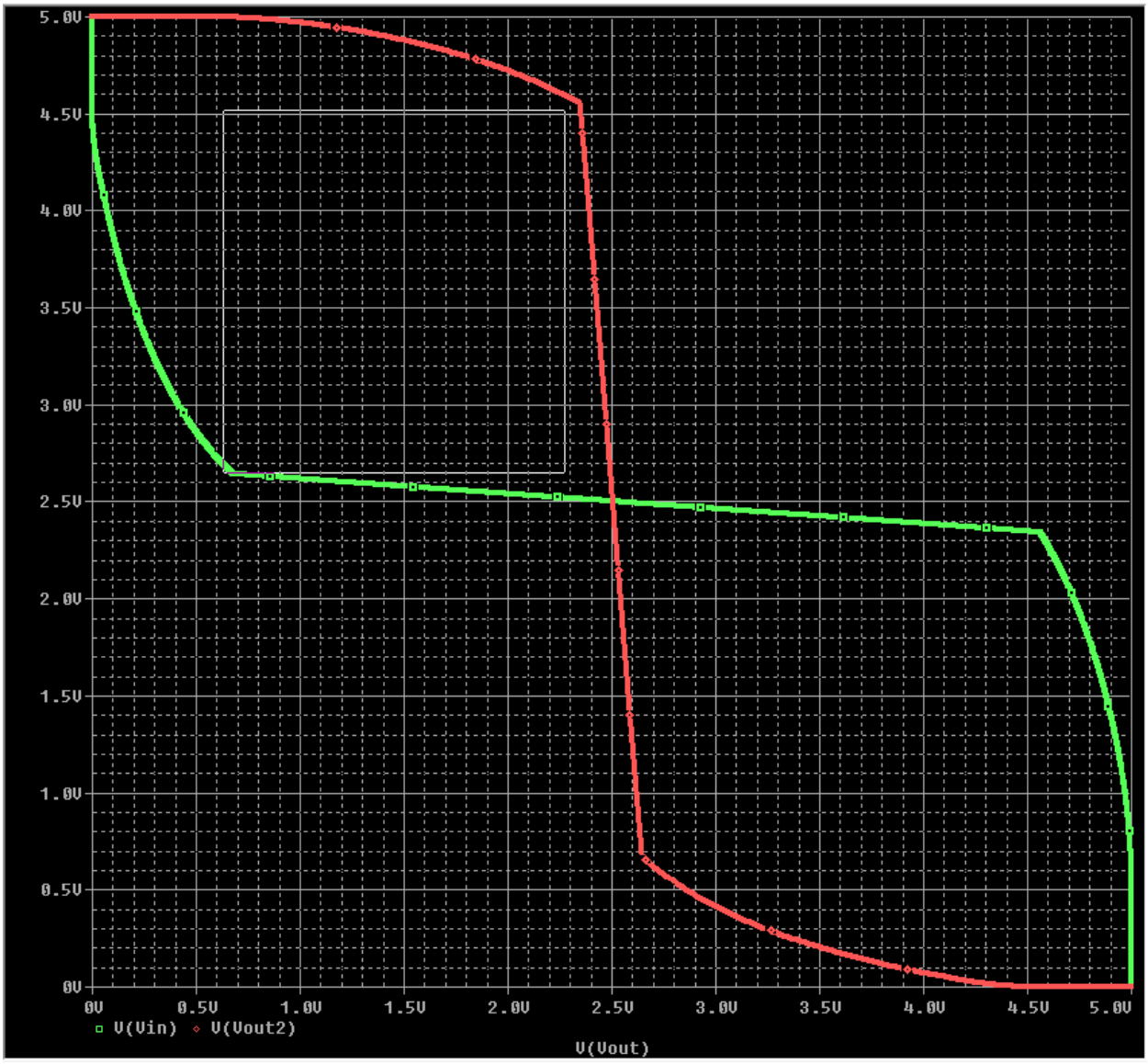
2) Design and Analysis of a CMOS RS Flip-Flop Based on Two CMOS NOR Gates



After designing two symmetric CMOS inverters, we obtained the following transfer characteristic.

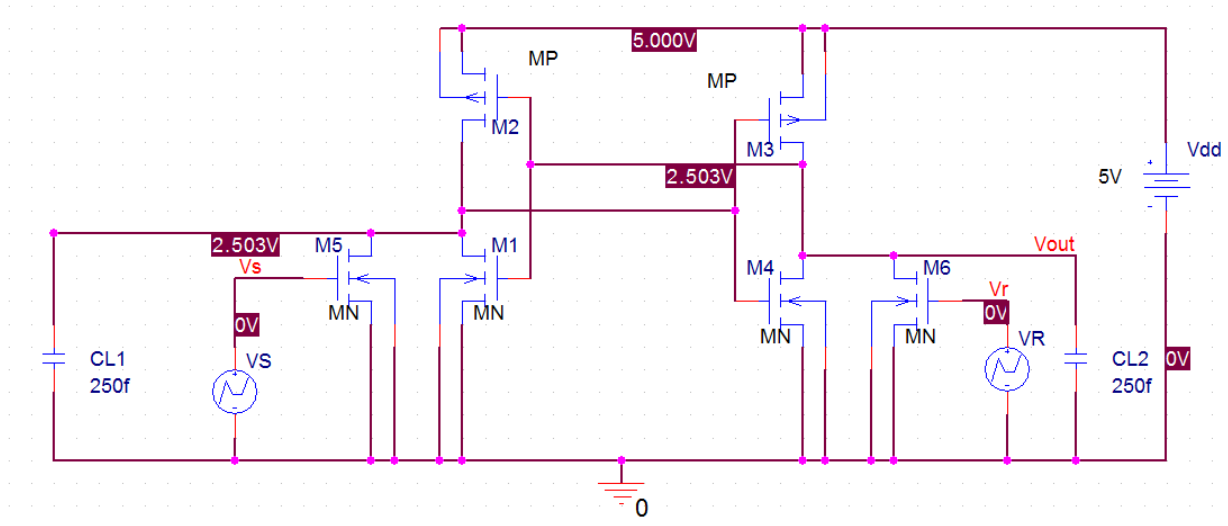


Using the butterfly curve for a latch circuit, we measured our static noise margins to be SNM = 1.63V

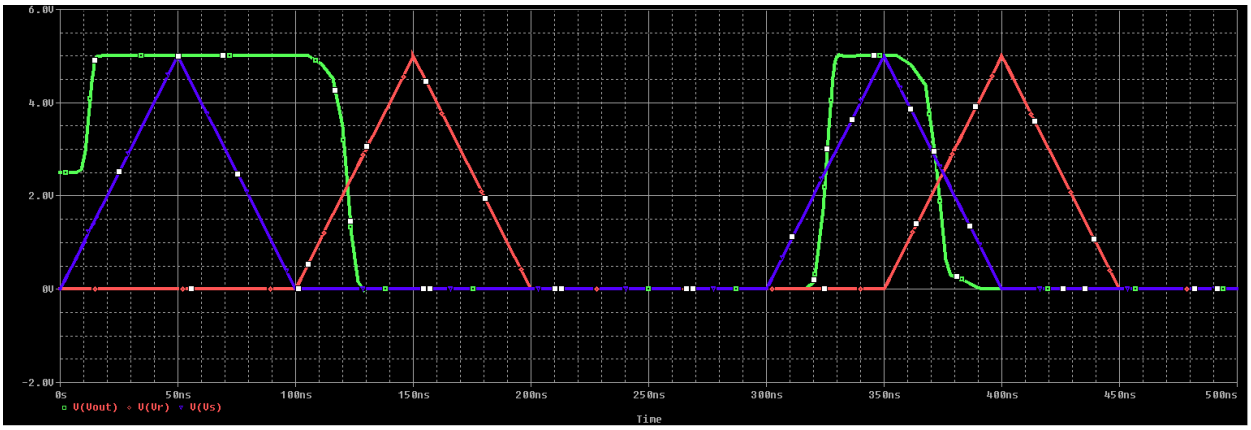


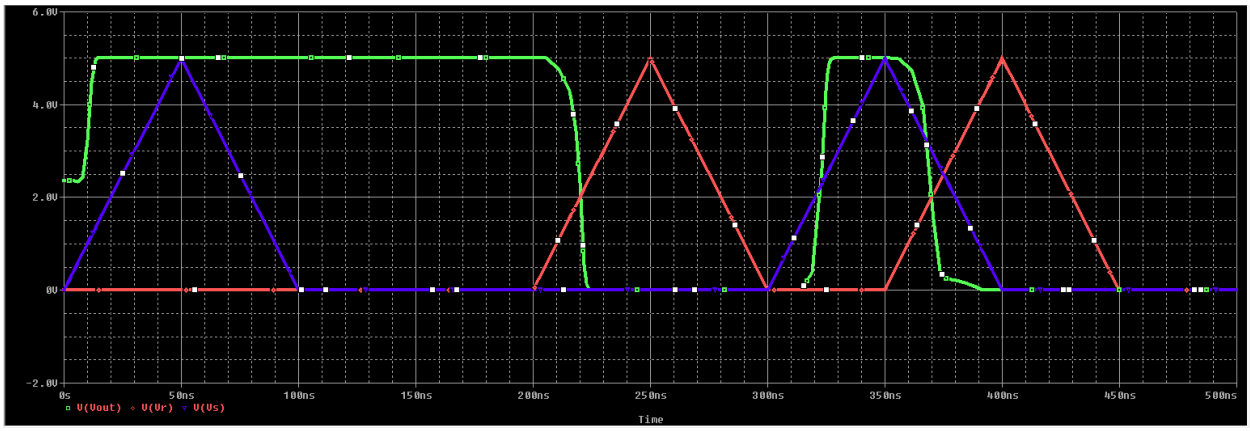
We can maximize our static noise margins by improving the CMOS inverter for speed. This will create a sharper transition and thus a higher SNR.

Below is our static CMOS RS flip-flop schematic



After forming a static CMOS RS flip-flop, we obtained the timing plots below.





With a load capacitance of 250fF, our speed is limited by the size of our M5 and M6 transistors. They control the capacitor discharge speed and therefore the fall times. The CMOS portion of the flip-flop is mainly responsible for capacitor charging. When increased in size, the PMOS will allow more current and charge the capacitor quickly, resulting in a quick rise time.

After sizing the MOS devices to, we increased the speed operation of our flip flop as shown below. Note the sharper rise and fall times in Vout, the green line.