99/100

Jennifer Delizo, A94013393

Clarence Lam, A08676105

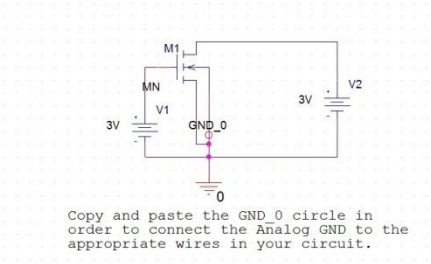
Arthur Robertson, A08280000

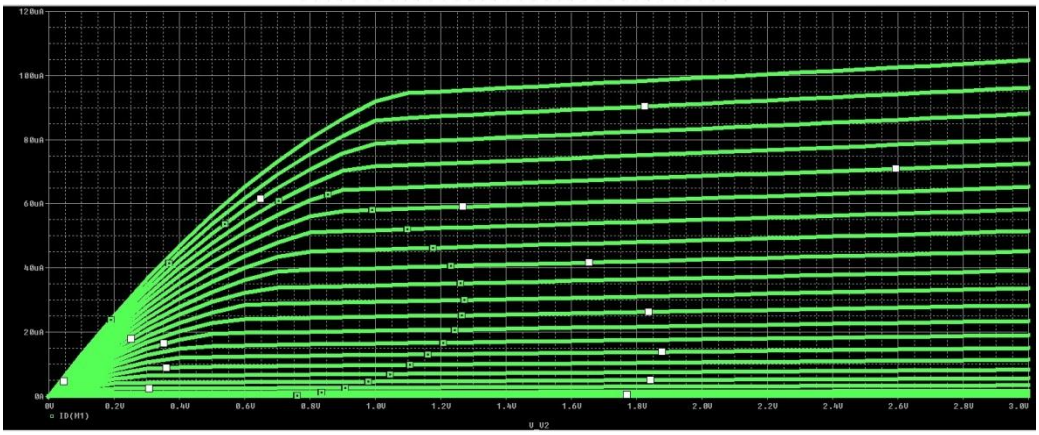
Matthew Borger, A08781527

ECE 108 Homework 1

Study of a Saturated pull-up NMOS

1)





2)

$$k_l = \mu C_{ox}\left(\frac{W}{L}\right) = \mu(\epsilon_{ox}/T_{ox})(W/L)$$

$$k_l = 31443.8 * \left(\frac{3.5x10^{-11}}{200x10^{-10}}\right) * \left(\frac{2x10^{-6}}{8x10^{-6}}\right)$$

$$k_l = 13.7567$$

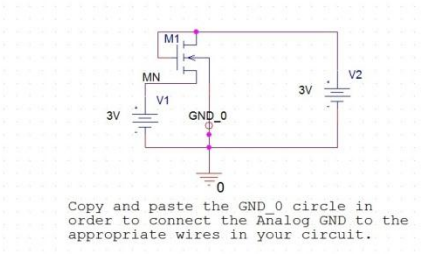
$$I_D = \frac{k}{2}(V_{DD} - V_{out} - V_T)^2$$

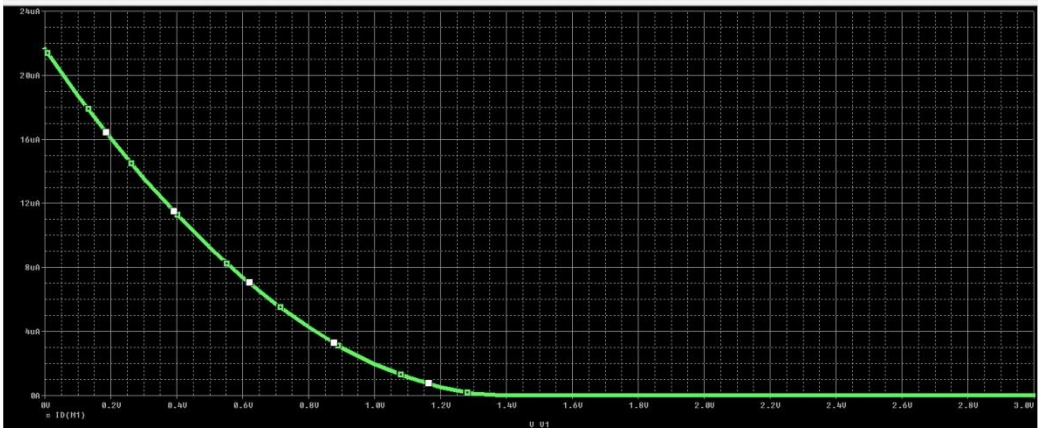
$$0 = \frac{k}{2}(V_{GS} - V_T)^2$$

$$0 = (V_{GS} - 1)^2$$

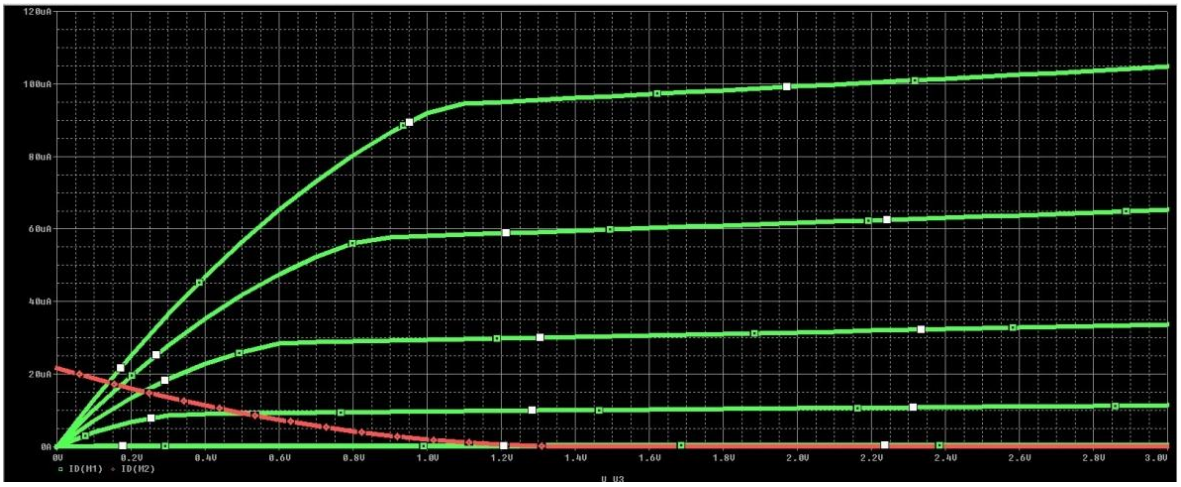
$$V_{GS} = 1V$$

3) As you can see in our graph, we obtained a result of 1.4V when our current ceases to flow. This small difference can be attributed.

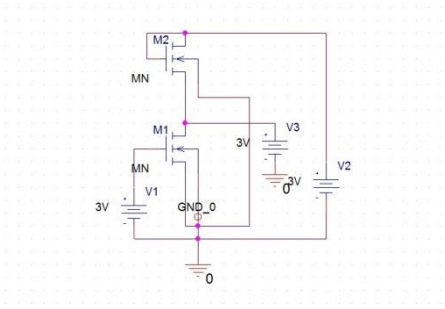


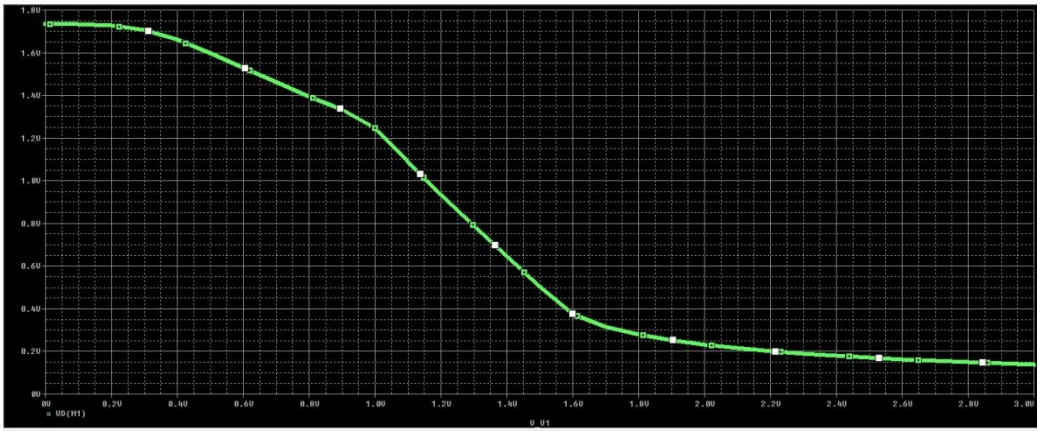


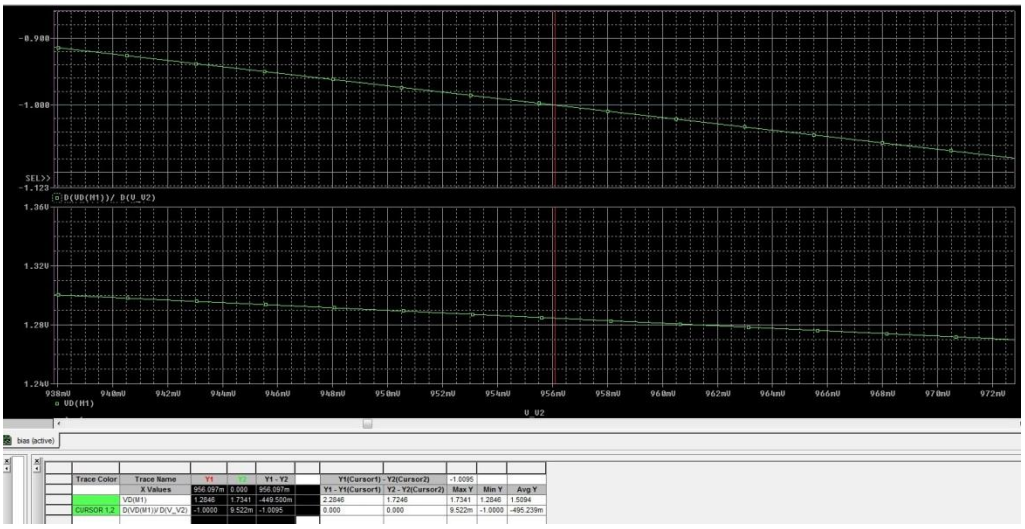
From the printout below, you can see that the input voltage where the pull-down is at the edge of saturation and linear is V_{GS}* = 0.24V.



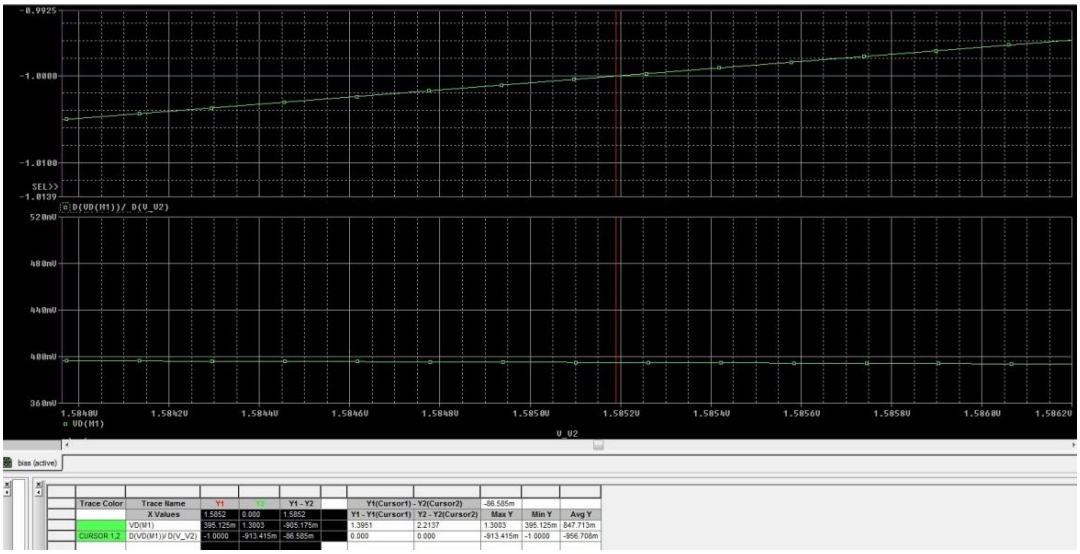
4) From the PSPICE drawings, we estimated our noise margins to be $NM_L = 0.560872$ and $NM_H = -0.3006$.



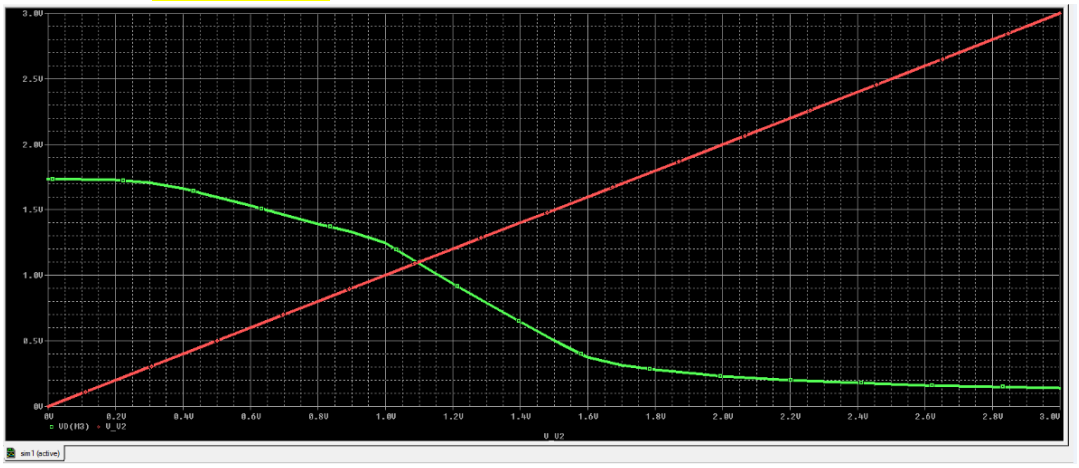




Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		-1.0095		
	X Values	956.097m	0.000	956.097m	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	VD(M1)	1.2846	1.7341	+449.500m	2.2846	1.7246	1.7341	1.2846	1.5094
CURSOR 1,2	D(VD(M1))/ D(V_V2)	-1.0000	9.522m	-1.0095	0.000	0.000	9.522m	-1.0000	-495.239m



The PSPICE graphs below shows how we graphically derived the inverter threshold voltage, found to be $V_{inv} = 1.0965V$.



5) As you can see from our calculations below, both our high and low noise margins differ significantly from our simulated noise margins. These discrepancies can be explained by the assumptions made in our calculations. In order for the noise margins to hold true, we assume that both inverters have similar VTC's. We see through simulations that this isn't always true which is why we have the slight discrepancies between our calculations and our simulations. The calculations for the noise margins, V_{inv} and V_{OL} are seen below.

$$k_D = \mu\left(\frac{\epsilon_{ox}}{T_{ox}}\right)\left(\frac{W}{L}\right) = 31442.8 * \left(\frac{3.5x10^{-11}}{200x10^{-10}}\right) * \left(\frac{2x10^{-6}}{2x10^{-6}}\right) = 55.0267$$

$$B = \frac{k_D}{k_L} = \frac{55.067}{13.7567} = 4$$

$$V_{IL} = V_T + \frac{1}{B} = 1 + \frac{1}{4} = 1.25V$$

$$V_{OL} = \frac{1}{3B}\left(\sqrt{1 + 6BV_{DD}} - 1\right) = \frac{1}{3 * 4}\left(\sqrt{1 + (6 * 4 * 3)} - 1\right) = 0.628667V$$

$$NM_L = V_{IL} - V_{OL} = 1.25 - 0.628667 = 0.62133 = NM_L$$

$$V_{OH} = V_{DD} - \frac{1}{2B} = 3 - \frac{1}{2*4} = 2.875V$$

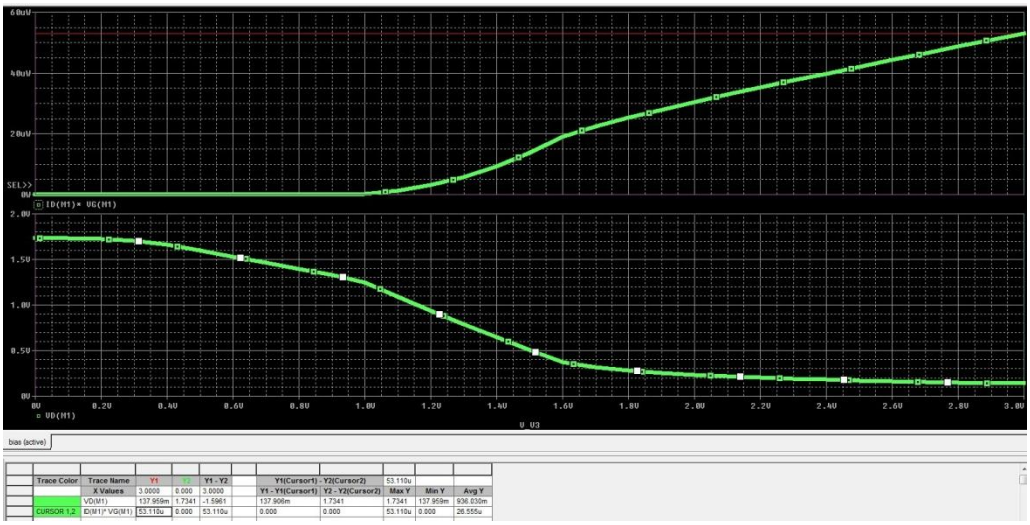
$$V_{IH} = \frac{2}{3B}\left(\sqrt{1+6BV_{DD}} - 1\right) + V_T = \frac{2}{3*4}\left(\sqrt{1+(6*4*3)} - 1\right) + 1 = 2.25733V$$

$$NM_H = V_{OH} - V_{IH} = 2.875 - 2.25733 = 0.61766 = NM_H$$

$$V_{inv} = V_T + \frac{1}{B}\left(1 \pm \sqrt{1+2B(V_{DD}-V_T)}\right) = 1 + \frac{1}{4}\left(1 \pm \sqrt{1+2*4(3-1)}\right) = 2.28V = V_{inv}$$

$$V_{OL} = \frac{V_{DD}}{1+B(V_{DD}-V_T)} = \frac{3}{1+4(3-2)} = .333V = V_{OL}$$

The PSPICE printout below show our power dissipation, which we simulated to be 53.11µW.



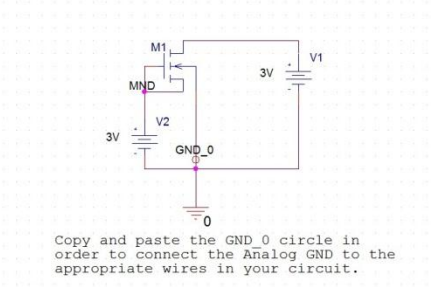
Study of a Depletion mode pull-up NMOS

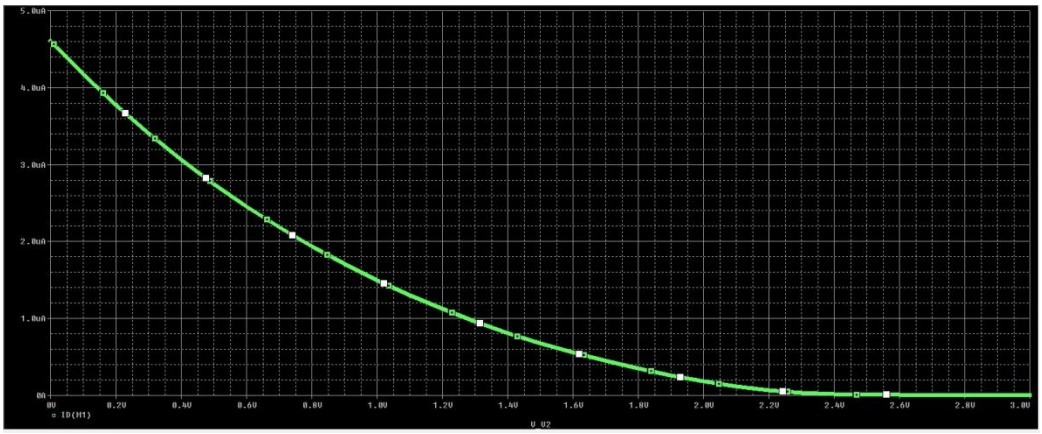
1)

$$k = \mu\left(\frac{\epsilon_{ox}}{T_{ox}}\right)\left(\frac{W}{L}\right) = 31442.8 * \left(\frac{3.5x10^{-11}}{200x10^{-10}}\right) * \left(\frac{2x10^{-6}}{10x10^{-6}}\right) = 11.0053$$

$$I_D = \frac{k}{2}(-V_T)^2 = \frac{11.0053}{2}(1^2) = 5.03\mu A$$

2) As you can see in the printouts below, we simulated a maximum current of 4.60µA, which means we have a 0.43 difference between our calculated value and our simulated value. This difference can be explained





3)

$$B = \frac{k_D}{k_L} = \frac{13.7567}{55.0267} = .25$$

$$V_{GS}* = V_T + \frac{1}{B}(\sqrt{1+2BV_{DD}} - 1 = -1 + \frac{1}{.25}\left(\sqrt{1+2(.25)(3)} - 1\right) = 1.32V = V_{GS}*$$

$$V_{inv} = V_T + \frac{1}{B}\left(1 \pm \sqrt{1+2B(V_{DD}-V_T)}\right) = -1 + \frac{1}{.25}\left(1 \pm \sqrt{1+2*.25(3+1)}\right) = 1.93V = V_{inv}$$

$$V_{IL} = V_T + \frac{1}{B} = -1 + \frac{1}{.25} = 3V$$

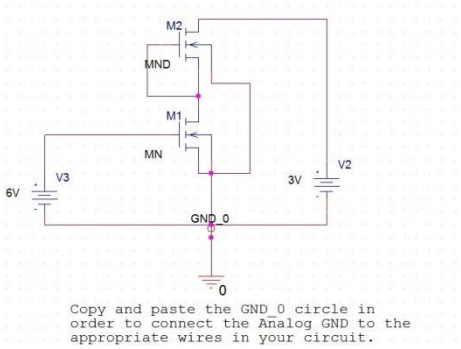
$$V_{OL} = \frac{1}{3B}\left(\sqrt{1+6BV_{DD}} - 1\right) = \frac{1}{3*.25}\left(\sqrt{1+(6*.25*3)} - 1\right) = 1.79V$$

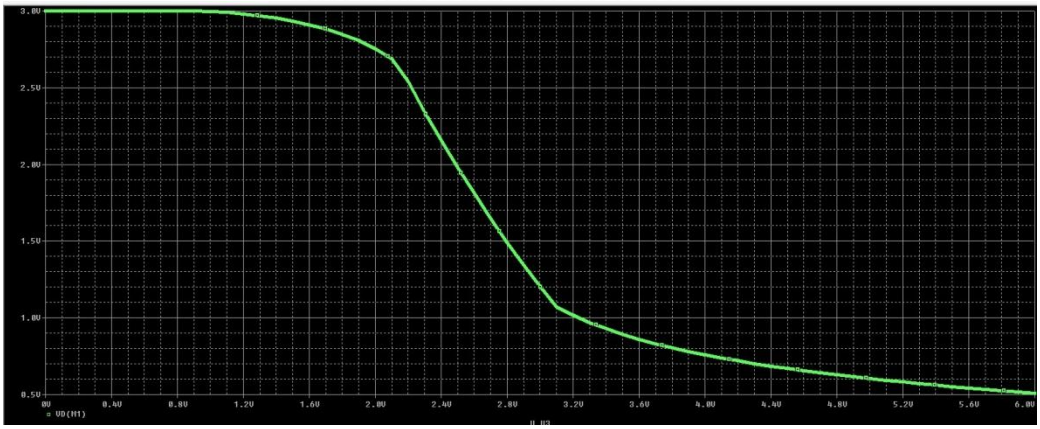
$$NM_L = V_{IL} - V_{OL} = 3 - 1.79 = 1.21 = NM_L$$

$$V_{OH} = V_{DD} - \frac{1}{2B} = 3 - \frac{1}{2*.25} = 1V$$

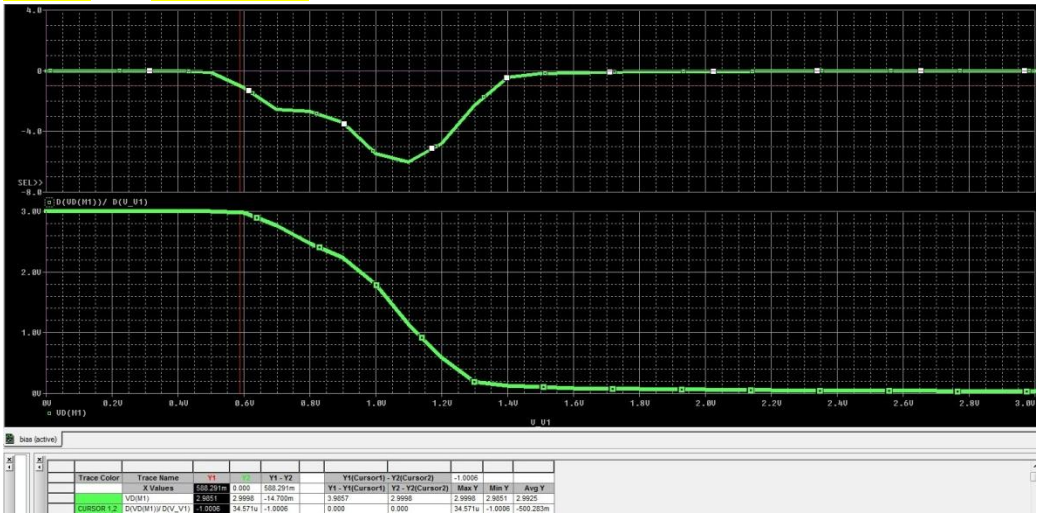
$$V_{IH} = \frac{2}{3B}\left(\sqrt{1+6BV_{DD}} - 1\right) + V_T = \frac{2}{3*.25}\left(\sqrt{1+(6*.25*3)} - 1\right) - 1 = 2.59V$$

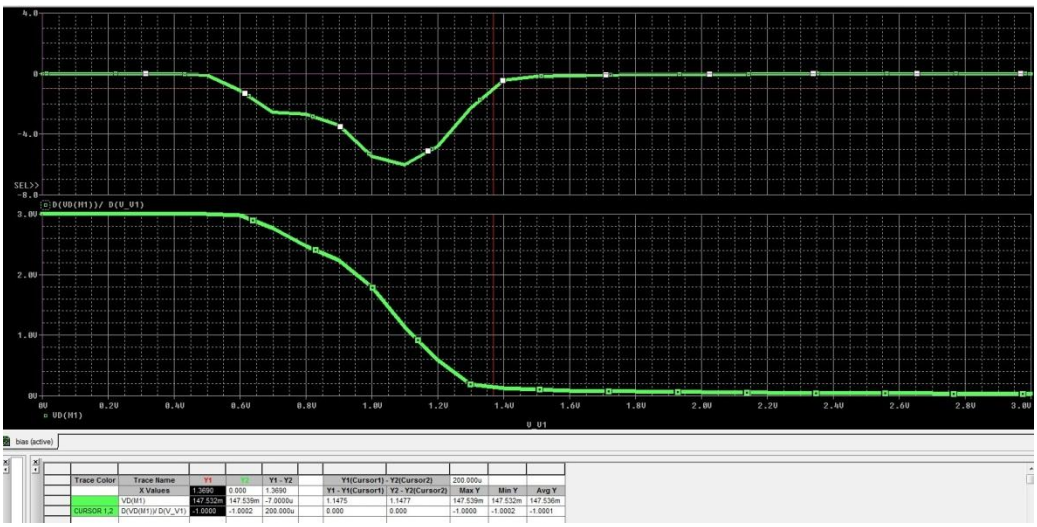
$$NM_H = V_{OH} - V_{IH} = 1 - 2.59 = -1.59 = NM_H$$



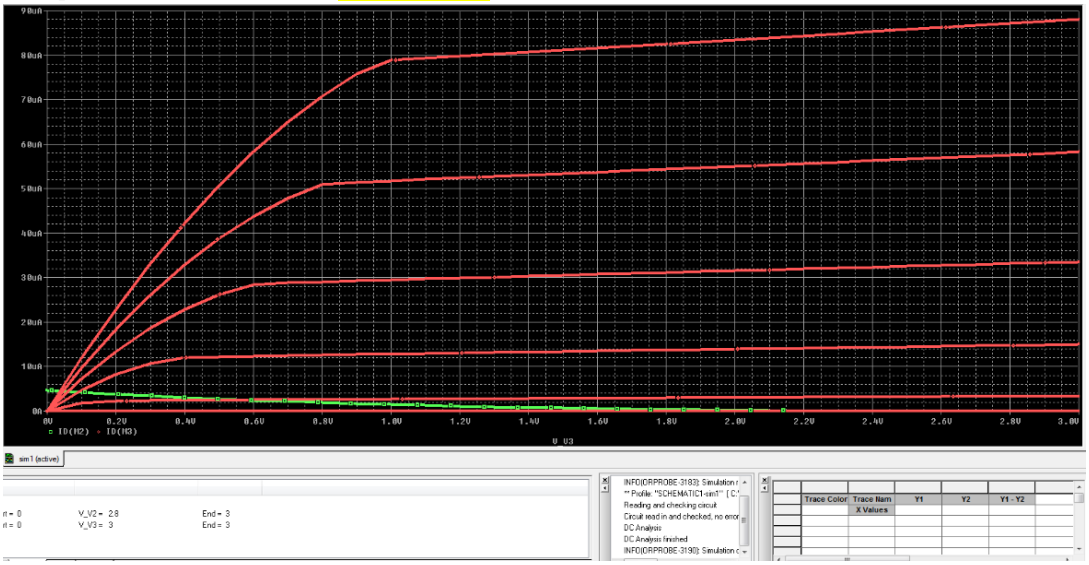


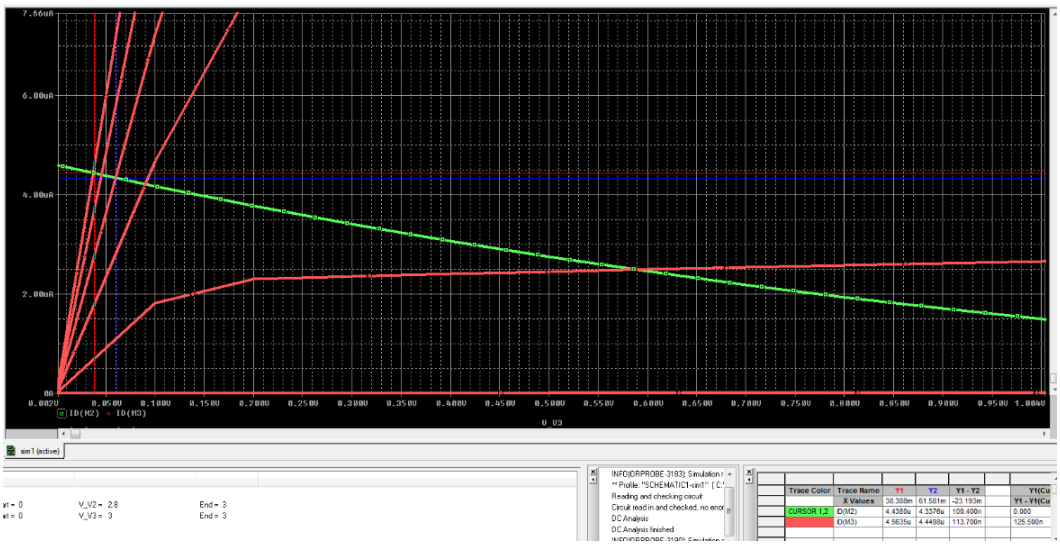
As you can see from the PSPICE drawings, we estimated our noise margins to be NM_L =0.441 and NM_H = 1.616.



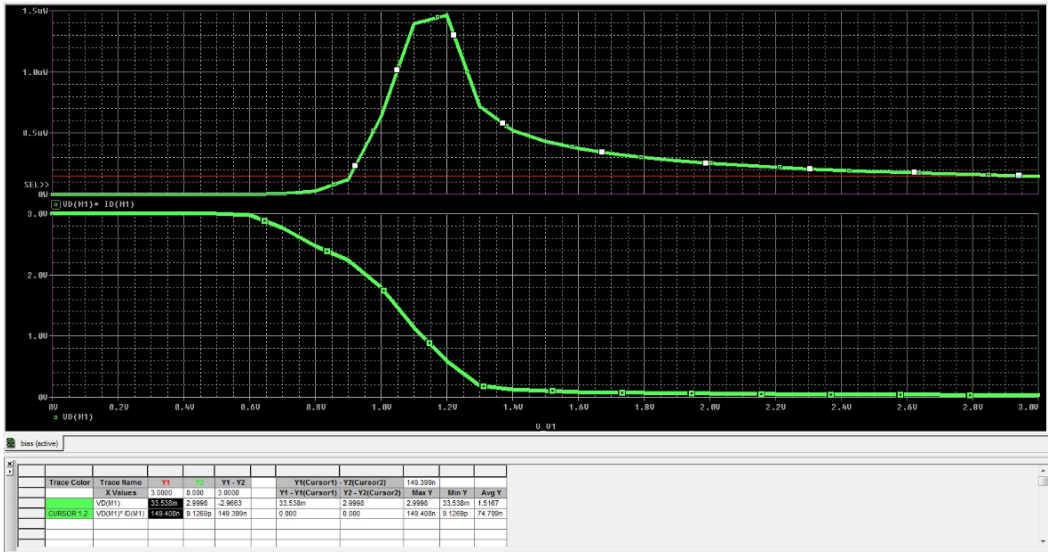


The printouts below show V_{GS}* = .570V



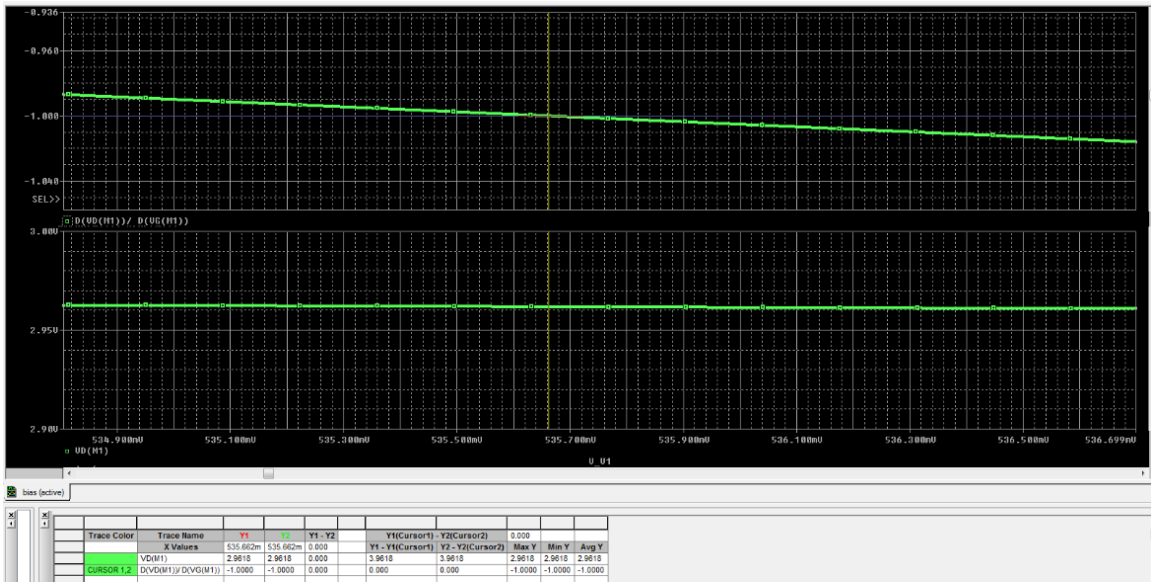


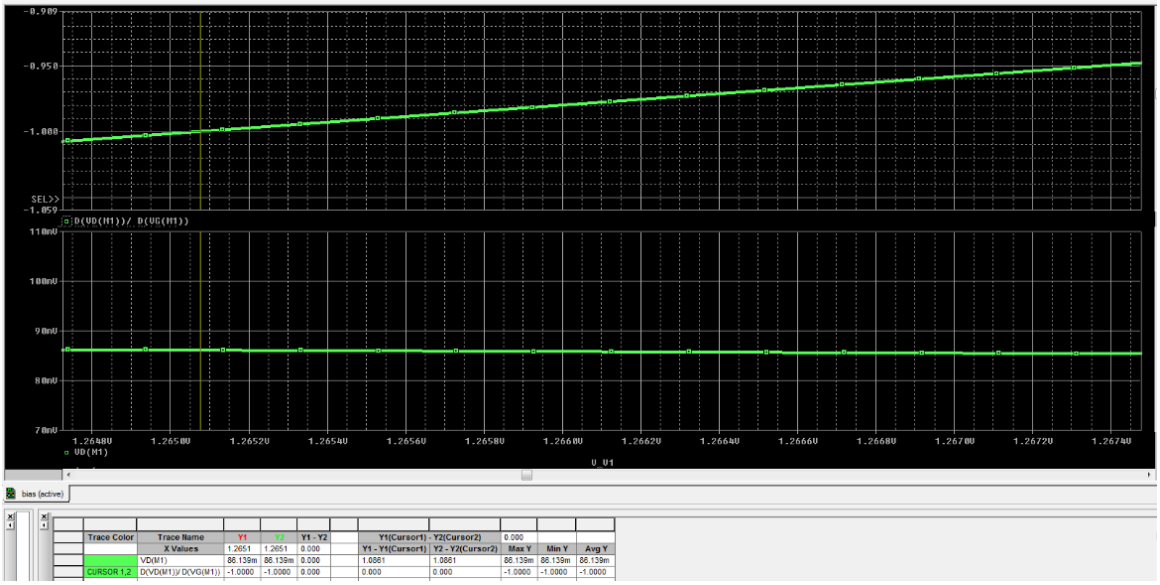
4) From the printout below, we find input high power dissipation to be 149.4nW



5) When we double the pull-down width of the MOSFET, we obtain the PSPICE transfer characteristics below.

<u>Double width</u>





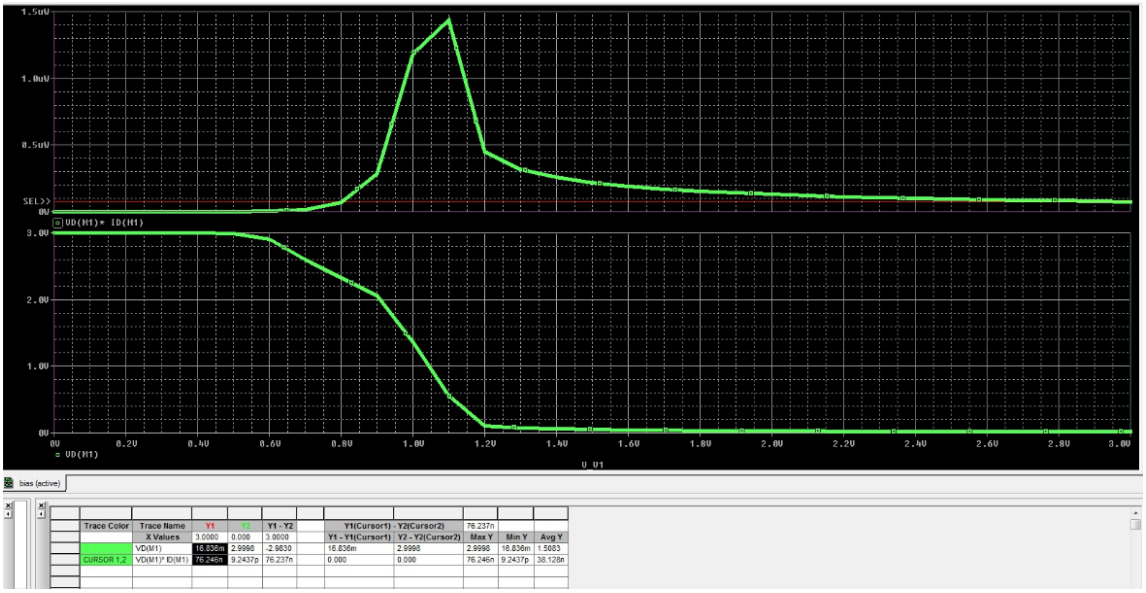
V_{OL} = .086V

NM_H = 1.696V

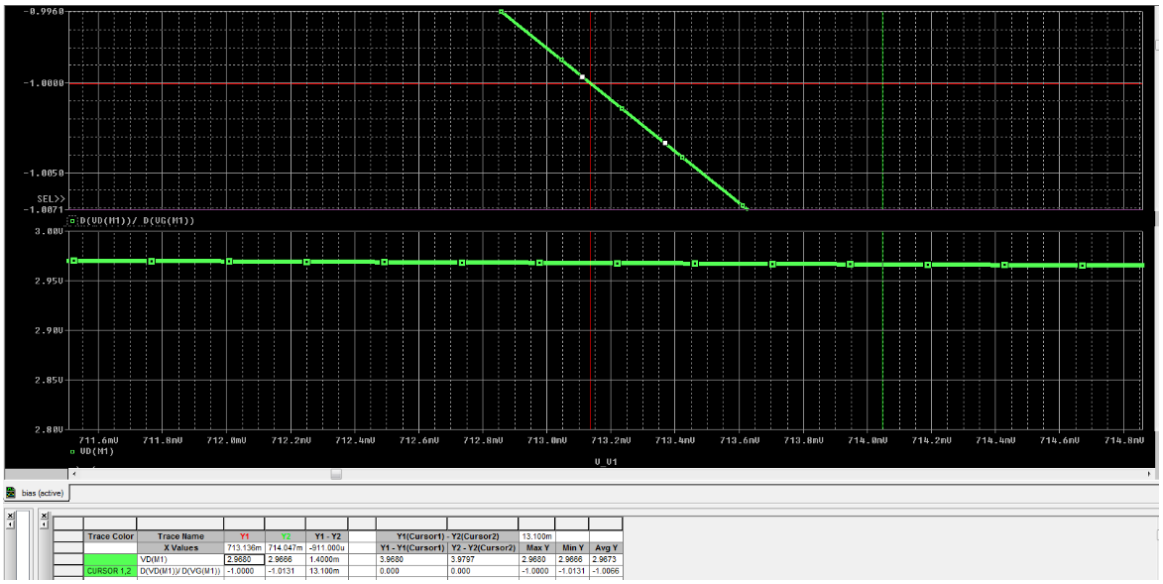
NM_L = .450V

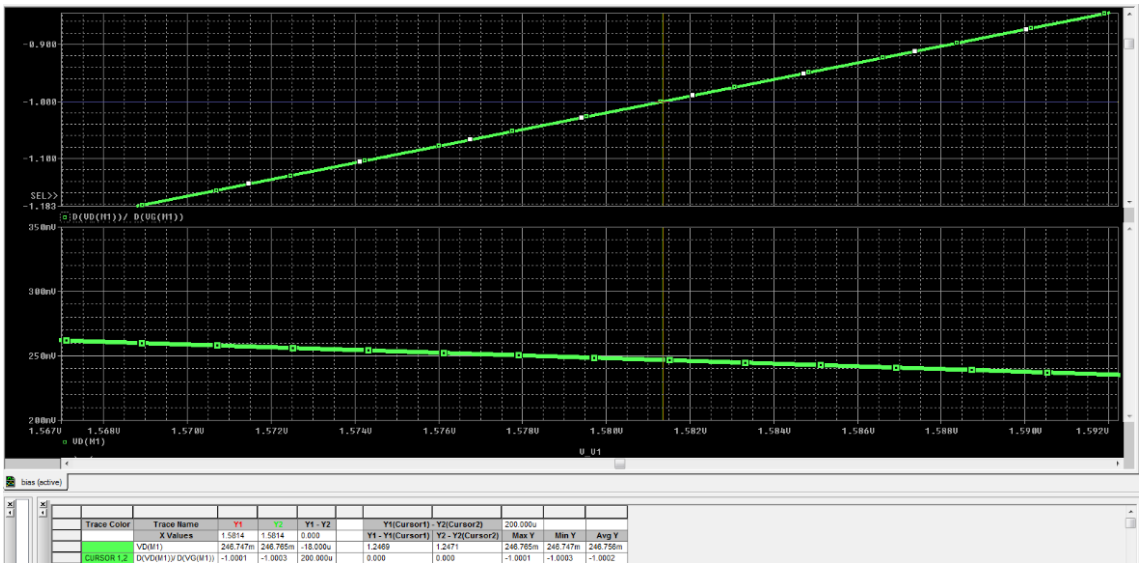
Power dissipation

After doubling width, we get input high power dissipation of 76.25nW



Double length





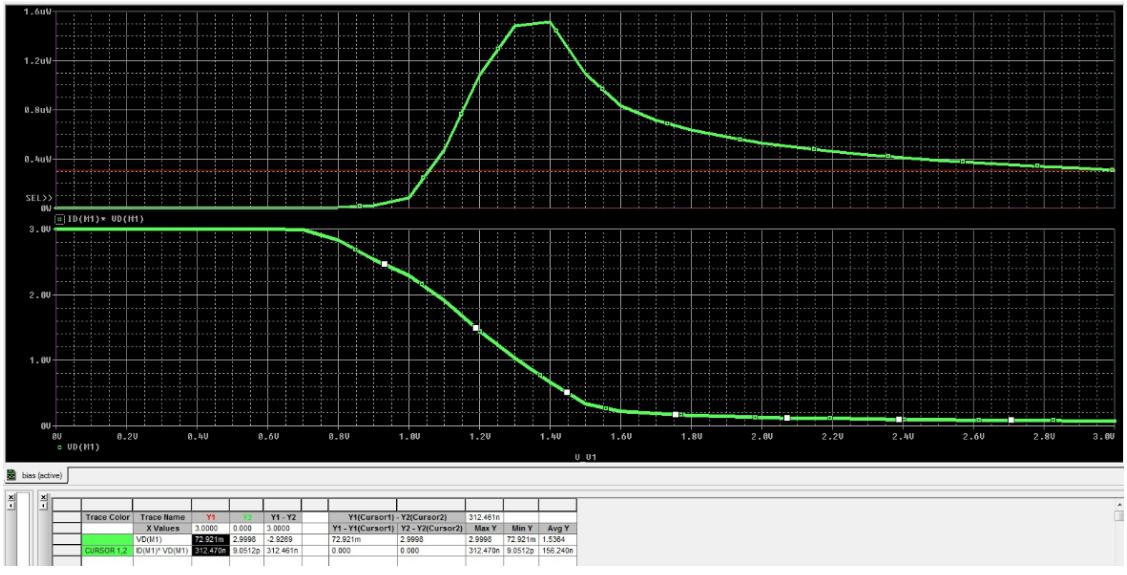
V_{OL} = .246V

NM_H = 1.399V

NM_L = .467V

Power dissipation

After doubling width, we get input high power dissipation of 312.47 nW



Discussion of above results in summary

Summary

Using a saturation load pull-up, we graphically derived good noise margins, but a relatively high V_{OL} of .38V. We saw better noise margins for the depletion load pull-up, and it achieved a lower V_{OL} of .2V. Additionally, V_{OH} for the saturation load pull-up did not reach even 2V, whereas V_{OH} of the depletion load pull-up was graphically derived to be 2.98V. Also, the transfer characteristic of the depletion load had a sharper curve than that of the saturation load pull-up. From this information, we infer that the depletion load pull-up has better performance in the inverter. This is shown by its high V_{OH}, low V_{OL}, and sharp transition (low Δt) in the transfer curve. With this transfer characteristic, we expect a greater tolerance to noise. Graphically calculated noise margins proved this.

Experimental results matched what we learned in lecture notes. As expected for an enhancement mode inverter, V_{OH} was offset from V_{DD} by more than V_t, and V_{OL} remained relatively high. For the depletion mode inverter, V_{OH} -> V_{DD} and V_{OH} was closer to zero.

For power dissipation, we see that an enhancement load inverter has a much higher input high power dissipation. For the depletion load inverter, we saw a small input high power dissipation. Due to the nature of a depletion load inverter, we would expect this, since we get high resistance from input high until transition. Only when resistance drops for output high do we see higher current flow through the depletion mode pull-up.

We also experimented with gate width and length. Doubled gate width halved input high power dissipation, while doubled length doubled it. This corresponds to optimal performance in inverters, where we would enhance the width of the pull-up and the length of the pull-down to get the best results. We did not experiment with the pull-down, but we did show how gate width enhances the gate channel, allowing for less power dissipation. Doubling gate width gave better transition and lowest V_{OL}. Doubling gate length, however slowed the transition and gave a significantly higher V_{OL}.

Calculations proved to be significantly off. This was because of back gate biasing, which was not accounted for in the calculations. By dropping the threshold voltage V_t, it threw off optimal calculated values, while PSPICE accounted for it. In any case, we found that graphical analysis proved best, especially for noise margins.