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49/50
Sahar
Part 1: 43/50

Grade Breakdown	Points
Build symmetrical CMOS inverter	5
Set Wp	5
VTC for different L's	5
Theoretical values for Vdsat, Id(unified), Id(suqare law)	16
Id from simulation and compare	5
Vdsat from SPICE	4
Discussion and compare the result	3
Total	43

ECE 108 L

1) Short Channel Inverter

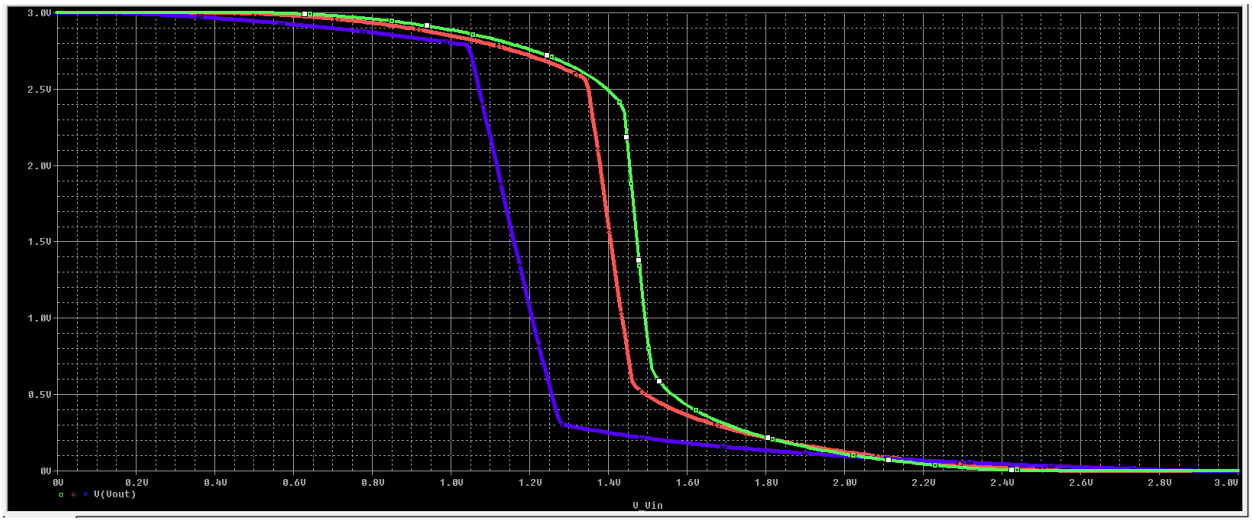
These are the calculations for obtaining W_P.

$$k_p = k_n$$

$$2.0\ x\ 10^{-5}\left(\frac{W_n}{L_n}\right.$$

$$\frac{(2.0)(1.5)}{0.8} = W$$

Below is our SPICE simulation when we step our gate length.



Below are the calculations for V_{DSSAT}, I_D(unified mod) and I_D(square mod) for L = 2.5µm, 1.2µm, and 0.6µm. As stated in the lecture notes, we assume $v_{sat} = 10^5$m/s.

For L_p = 2.5µm

NMOS (voltage high)

$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{2.5\ x\ 10^{-6} * 10^5}{655.881 * 10^{-2}}$$
$$= 38.12mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{2 * 10^{-5}}{2}(38.12 * 10^{-3})^2(1 + 0.0367072 * 38.12 * 10^{-3})$$
$$= 14.549nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{2.0x10^{-5}}{2}(38.12 * 10^{-3})^2$$
$$= 14.531nA$$

You have a unit problem in the calculations. the unit of mobility is cm2/V-s. I guess you used cm/V-s. So all the calculations are wrong.

Points: 16/20

PMOS (voltage low)

$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{2.5\ x\ 10^{-6} * 10^5}{261.977 * 10^{-2}}$$
$$= 95.43mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{0.8 * 10^{-5}}{2}(95.43 * 10^{-3})^2(1 + 0.0612279 * 95.43 * 10^{-3})$$
$$= 36.639nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{0.8 * 10^{-5}}{2}(95.43 * 10^{-3})^2$$
$$= 36.238nA$$

For L_p = 1.2µm

NMOS (voltage high)

$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{1.2\ x\ 10^{-6} * 10^5}{655.881 * 10^{-2}}$$
$$= 18.30mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{2 * 10^{-5}}{2}(18.30 * 10^{-3})^2(1 + 0.0367072 * 18.3 * 10^{-3})$$
$$= 3.350nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{2.0x10^{-5}}{2}(18.30 * 10^{-3})^2$$
$$= 3.347nA$$

PMOS (voltage low)

$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{1.2\ x\ 10^{-6} * 10^5}{261.977 * 10^{-2}}$$
$$= 45.81mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{0.8 * 10^{-5}}{2}(45.81 * 10^{-3})^2(1 + 0.0612279 * 45.81 * 10^{-3})$$
$$= 8.416nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{0.8 * 10^{-5}}{2}(45.81 * 10^{-3})^2$$
$$= 8.39nA$$

For L_p = 0.6µm

NMOS (voltage high)

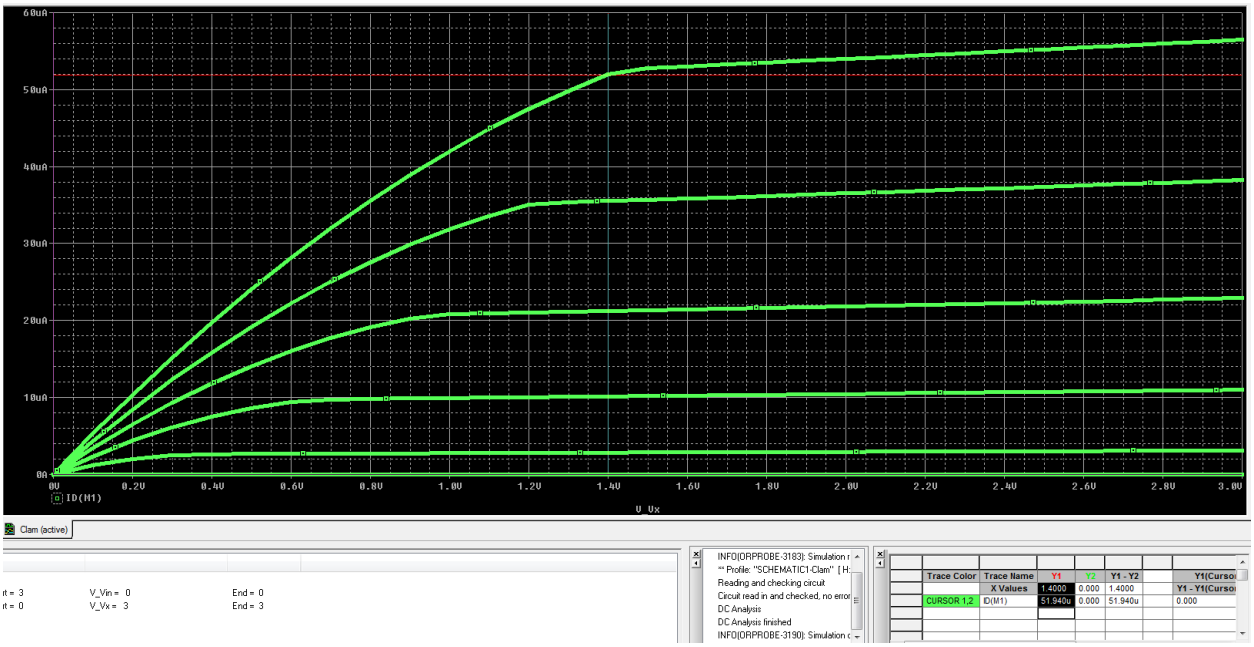
$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{0.6\ x\ 10^{-6} * 10^5}{655.881 * 10^{-2}}$$
$$= 9.15mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{2 * 10^{-5}}{2}(9.15 * 10^{-3})^2(1 + 0.0367072 * 9.15 * 10^{-3})$$
$$= 0.837nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{2.0x10^{-5}}{2}(9.15 * 10^{-3})^2$$
$$= 0.837nA$$

PMOS (voltage low)

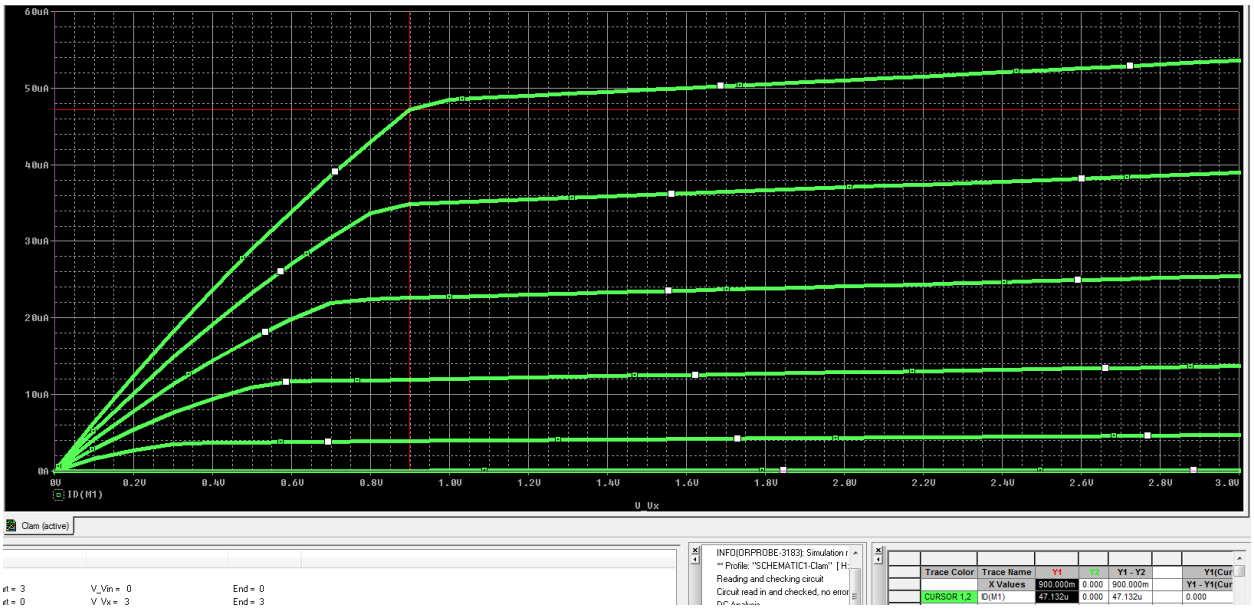
$$V_{DSSAT} = L\frac{v_{sat}}{\mu}$$
$$= \frac{0.6\ x\ 10^{-6} * 10^5}{261.977 * 10^{-2}}$$
$$= 22.90mV$$
$$I_{D(unified)} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$= \frac{0.8 * 10^{-5}}{2}(22.90 * 10^{-3})^2(1 + 0.0612279 * 22.90 * 10^{-3})$$
$$= 2.10nA$$
$$I_{D(squarelaw)} = \frac{k}{2}(V_{GS} - V_T)^2$$
$$= \frac{0.8 * 10^{-5}}{2}(22.90 * 10^{-3})^2$$
$$= 2.10nA$$

These are the drain currents for each of the gate lengths.

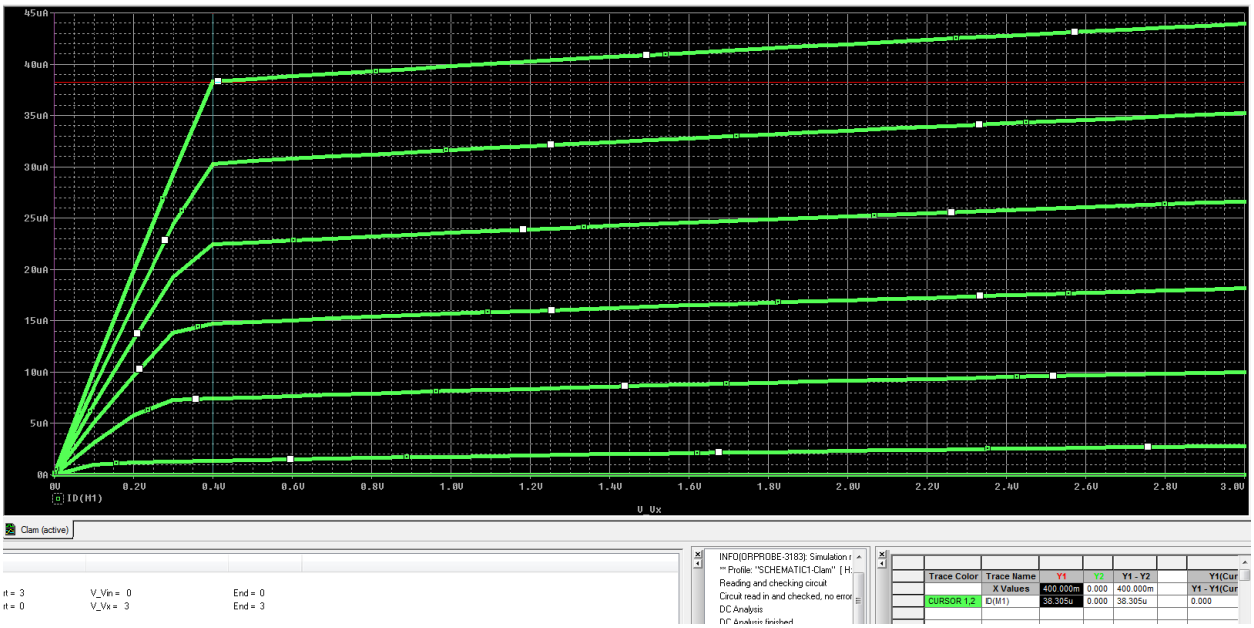
L = 2.5µm, I_D = 51.94µA



L = 1.2µm, I_D = 47.132µA



L = 0.6µm, I_D = 38.305µA



As we see from our calculated results, as the gate length decreases, our V_{DSSAT} and I_D all decrease. This is because V_{DSSAT} is directly proportional to gate length and our drain current is directly proportional to V_{DSSAT}. We notice that there is a minute difference in the calculations our $I_{Dunifiedmodel}$ and $I_{Dsquarelaw}$ until we decrease the gate length to 0.6µm. This is when the short channel effect takes over and we calculate identical drain currents. When we compare the calculated and simulated results, we obtain very different answers.

You got different values for the unit problem.

2) Scaling of the Speed Response of a CMOS Inverter

Given the layout provided, with λ = 0.6μm, we obtained

NMOS	PMOS
L = 1.2um	L = 1.2um
W = 1.8um	W = 5.4um
AD = 6.84pm	AD = 16.2pm
AS = 6.84pm	AS = 16.2pm
PD = 9.6um	PD = 11.4um
PS = 9.6um	PS = 11.4um
NRS = 0.33	NRS = 0.11
NRD = 0.33	NRD = 0.11

Below are the simulated rise and fall times of the DUT. We obtained t_r = 2.478ns and t_f = 1.939ns.

Using a capacitance of C =0.05pF, we obtained rise and fall times of t_r = 4.7802ns and t_f = 3.757ns.

We estimated our effective load capacitance to be C =5.04fF. 50fF

Below are the calculations for the rise and fall times of the DUT under the square law assumption.

$$t_r = \frac{3CV_{DD}^2}{k_L(V_{DD} - V_{TL})^2(2V_{DD} - V_{TL})}$$

$$= \frac{3 * 5.04 * 10^{-15} * 9}{0.8 * 10^{-5}(3 - -0.538861)^2(2 * 3 - -0.538861)}$$

$$= 0.208ns$$

$$t_f = \frac{3CV_{DD}^2}{k_D(V_{DD} - V_{TD})^2(2V_{DD} - V_{TD})}$$

$$= \frac{3 * 5.04 * 10^{-15} * 9}{2 * 10^{-5}(3 - 0.543469)^2(2 * 3 - 0.543469)} = 0.207s$$

Here are the rise and fall times using λ = 0.3µm. We obtained t_r = 1.0323ns and t_f = 0.854ns.

NMOS
L = 0.6um
W = 0.9um
AD = 1.71pm
AS = 1.71pm
PD = 4.8um
PS = 4.8um
NRS = 0.33
NRD = 0.33

PMOS
L = 0.6um
W = 2.7um
AD = 4.05pm
AS = 4.05pm
PD = 5.7um
PS = 5.7um
NRS = 0.11
NRD = 0.11

Using λ = 0.3µm, we obtained an output capacitance of C = 0.015pF and new rise and fall times of t_r = 2.1638ns and t_f = 1.4ns.

Below are the calculations for the rise and fall times for our effective capacitance, C = 3.78fF.

$$t_r = \frac{3CV_{DD}^2}{k_L(V_{DD} - V_{TL})^2(2V_{DD} - V_{TL})}$$

$$= \frac{3 * 3.78 * 10^{-15} * 9}{0.8 * 10^{-5}(3 - -0.538861)^2(2 * 3 - -0.538861)}$$

$$= 0.156ns$$

$$t_f = \frac{3CV_{DD}^2}{k_D(V_{DD} - V_{TD})^2(2V_{DD} - V_{TD})}$$

$$= \frac{3 * 3.78 * 10^{-15} * 9}{2 * 10^{-5}(3 - 0.543469)^2(2 * 3 - 0.543469)}$$

$$= 0.155ns$$

From our simulated values, we achieve lower rise and fall times with λ = 0.3μm.