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100/100
Sahar

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ECE 108 Homework 2

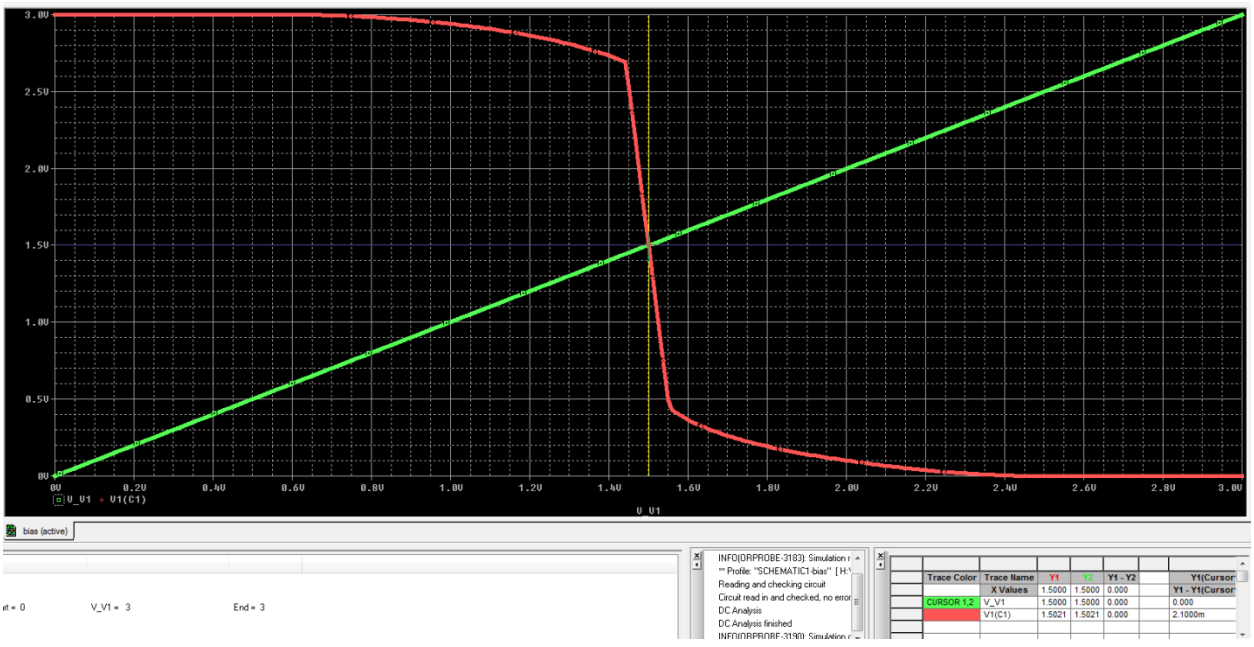
1) CMOS Inverter Design and Characterization

$$k_p = k_n = k'\left(\frac{W}{L}\right)$$

$$9\ x\ 10^{-5}\left(\frac{W_n}{L_n}\right) = 2.20\ x\ 10^{-5}\left(\frac{W_p}{L_p}\right)$$

$$\frac{9\ x\ 10^{-5}}{2.20\ x\ 10^{-5}}1\ x\ 10^{-6} = W_p \rightarrow W_p = 4.09\mu m$$

According to our SPICE simulation, our gate width is 4.7µm. The difference in the width can be attributed to the assumptions made in our calculations. In order for a CMOS inverter to be symmetric, the voltage thresholds should be equal. However, if we look at the SPICE model of the NMOS and PMOS transistors, we observe that the V_T's are slightly off.

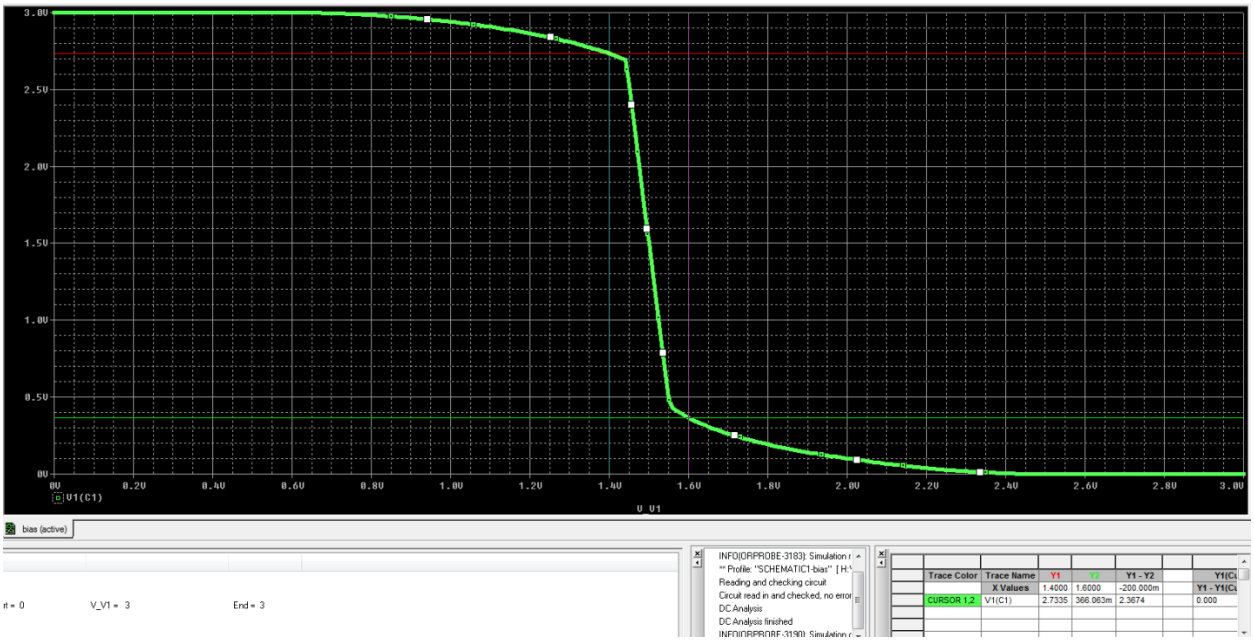


From SPICE, we obtained the output voltages:

For Vin = 1.4V, Vout = 2.7335V.

For Vin = 1.5V, Vout = 1.5V.

For Vin = 1.6V, Vout = 0.366063V.



Below are the calculations for output voltage:

$$for\ V = 1.4V$$

$$V_{out} = V_{in} - V_{TL} + \sqrt{(V_{in} - V_{DD} - V_{TL})^2 - \frac{1}{B}(V_{in} - V_{DD})^2}$$

$$= 1.4 - 0.74 + \sqrt{(1.4 - 3 - .74)^2 - \frac{1}{4.4}(1.4 - 3)^2}$$

$$V_{out} = 2.46V$$

$$for\ = 1.5V$$

$$V_{out} = 1.5V\ by\ definition\ of\ symmetric\ inverter$$

$$for\ V = 1.6V$$

$$V_{out} = V_{in} - V_{TD} - \sqrt{(V_{in} - V_{TD}) - (V_{in} - V_{TD})^2}$$

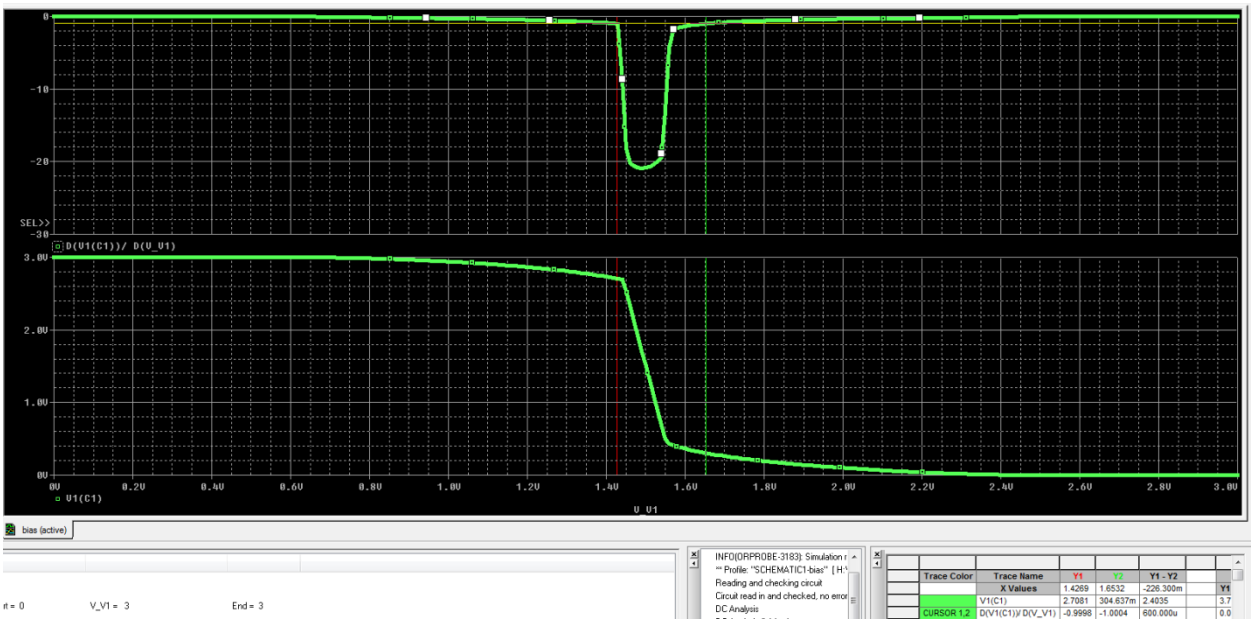
$$= 1.6 - 0.74 - \sqrt{(1.6 - .74) - (1.6 - .74)^2}$$

$$V_{out} = 0.513V$$

As expected, our output voltage for V_{in} = 1.5V is 1.5V. That's because we designed our CMOS inverter to have symmetric characteristics and by definition, $V_{in} = V_{DD}/2$. For V_{in} = 1.4V, we

simulated V_{out} = 2.7335V and we calculated V_{out} = 2.46V. For V_{in} = 1.6V, we calculated V_{out} = 0.513V and we simulated V_{out} = 0.366063V. These slight differences can be attributed to the assumptions made in our calculations and that we used approximated equations to calculate our result.

Our static noise margins for the symmetric CMOS inverter are $NM_L = 1.12$ and $NM_H = 1.05$.



Below are the calculations for the rise and fall times and the propagation delay for 100fF and 1pF:

$$C = 100fF$$

$$t_r = \frac{3CV_{DD}^2}{k_L(V_{DD} - V_{TL})^2(2V_{DD} - V_{TL})}$$

$$= \frac{3 * 100 * 10^{-15} * 9}{2.2 * 10^{-5}(\frac{4.09x10^{-6}}{1x10^{-6}})(3 - 0.73886)^2(2 * 3 - 0.73886)}$$

$$= 1.12ns$$

$$C = 100fF$$

$$t_f = \frac{3CV_{DD}^2}{k_D(V_{DD} - V_{TD})^2(2V_{DD} - V_{TD})}$$

$$= \frac{3 * 100 * 10^{-15} * 9}{9x10^{-5}(\frac{1x10^{-6}}{1x10^{-6}})(3 - 0.743469)^2(2 * 3 - 0.743469)}$$

$$= 1.12ns$$

$$Propagation\ Delay: 1.12\ ns$$

$$C = 1pF$$

$$t_r = \frac{3CV_{DD}^2}{k_L(V_{DD} - V_{TL})^2(2V_{DD} - V_{TL})}$$

$$= \frac{3 * 1 * 10^{-12} * 9}{2.2 * 10^{-5}(\frac{4.09x10^{-6}}{1x10^{-6}})(3 - 0.73886)^2(2 * 3 - 0.73886)}$$

$$= 11.2ns$$

$$C = 1pF$$

$$t_f = \frac{3CV_{DD}^2}{k_D(V_{DD} - V_{TD})^2(2V_{DD} - V_{TD})}$$

$$= \frac{3 * 1 * 10^{-12} * 9}{9x10^{-5}(\frac{4.09x10^{-6}}{1x10^{-6}})(3 - 0.743469)^2(2 * 3 - 0.743469)}$$

$$= 11.2ns$$

$$Propagation\ Delay: 11.2\ ns$$

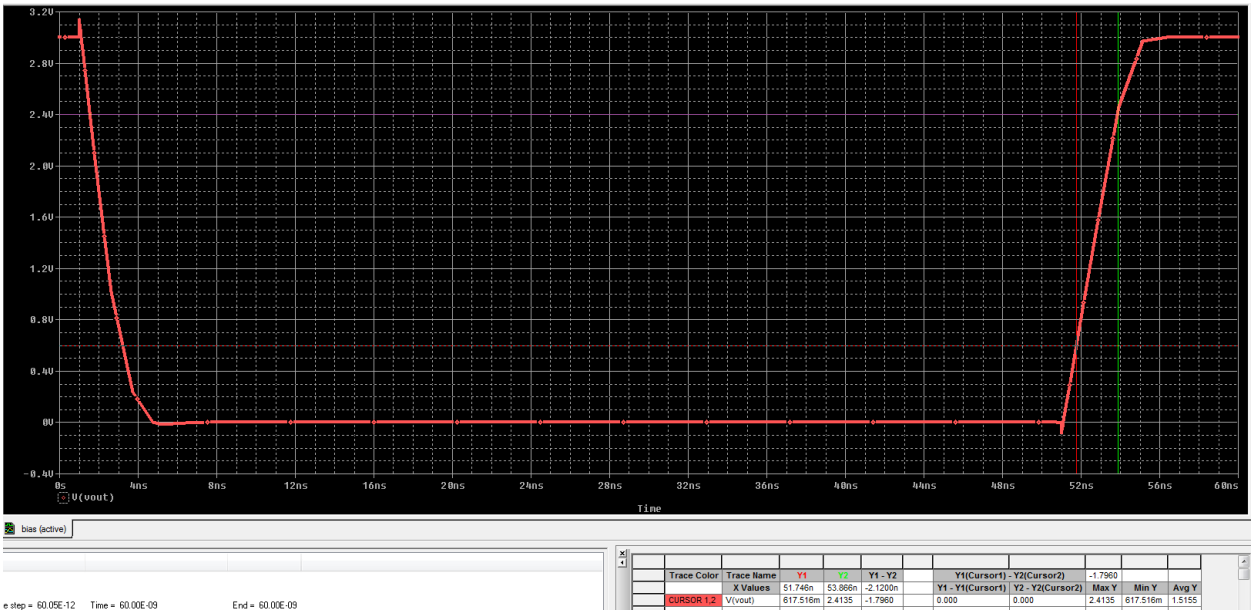
Below is a table with the rise and fall times, as well as the propagation delays, for our SPICE simulations.

C	t_r	t_f	t_{pdr}	t_{pdf}	t_{pd}
C = 100fF	2.12ns	1.6646ns	1.775ns	1.2593ns	1.5172ns
C = 1pF	20.305ns	14.2356ns	16.398ns	11.357ns	13.878ns

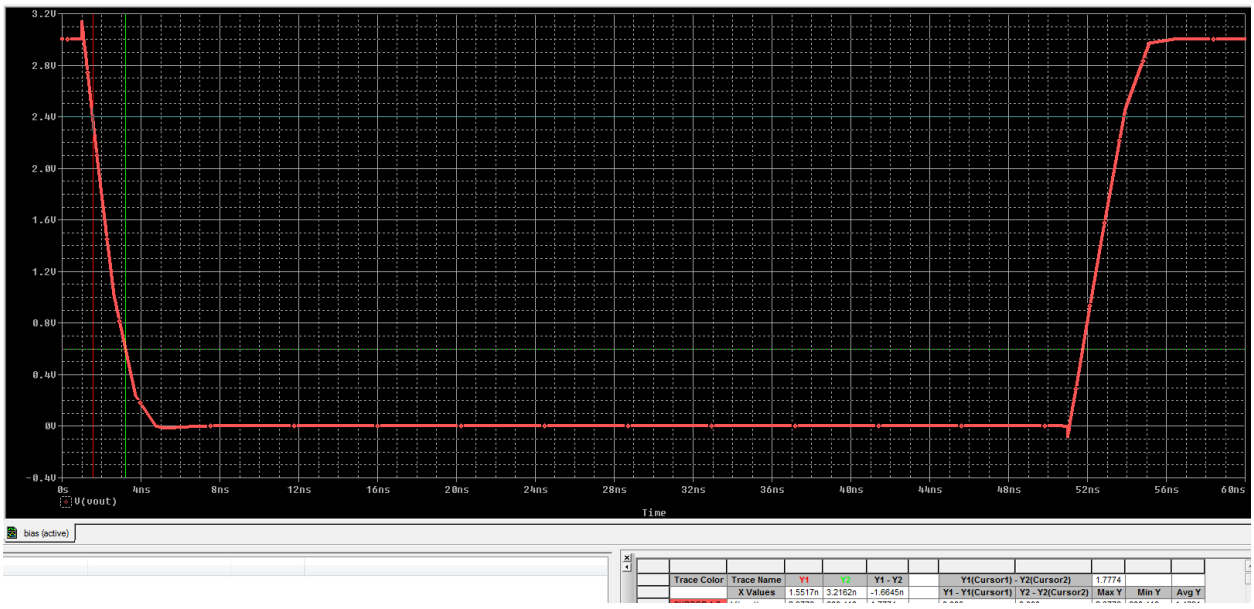
Here are the SPICE simulations for the rise and fall times and propagation delays.

For C = 100fF

t_r

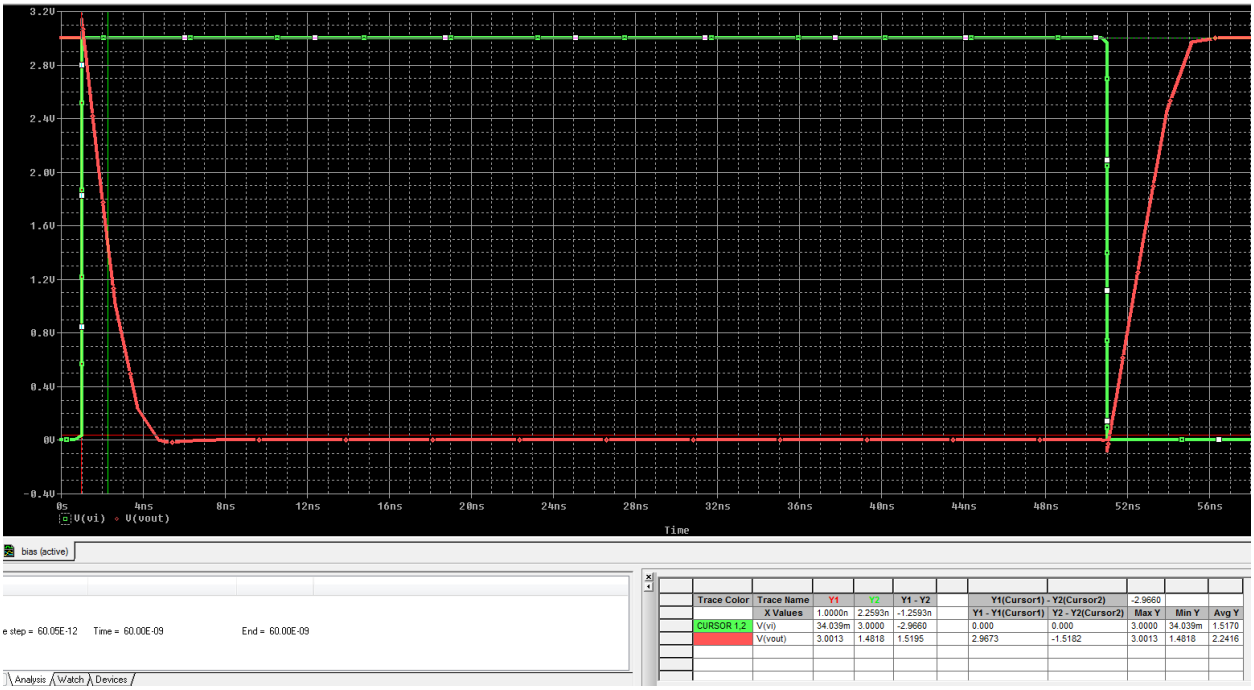

3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0V
-0.4V
0s
4ns
8ns
12ns
16ns
20ns
24ns
28ns
32ns
36ns
40ns
44ns
48ns
52ns
56ns
60ns
V(vout)
Time
bias (active)
Trace Color | Trace Name | Y1 | Y2 | Y1 - Y2 | Y1(Cursor1) - Y2(Cursor2) | -1.7960
X Values | 51.746n | 53.866n | -2.1200n | Y1 - Y1(Cursor1) | Y2 - Y2(Cursor2) | Max Y | Min Y | Avg Y
CURSOR 1,2 | V(vout) | 617.516m | 2.4135 | -1.7960 | 0.000 | 0.000 | 2.4135 | 617.516m | 1.5155
e step = 60.05E-12 Time = 60.00E-09 End = 60.00E-09

t_f


3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0V
-0.4V
0s
4ns
8ns
12ns
16ns
20ns
24ns
28ns
32ns
36ns
40ns
44ns
48ns
52ns
56ns
60ns
V(vout)
Time
bias (active)
Trace Color | Trace Name | Y1 | Y2 | Y1 - Y2 | Y1(Cursor1) - Y2(Cursor2) | 1.7774
X Values | 1.5517n | 3.2162n | -1.6645n | Y1 - Y1(Cursor1) | Y2 - Y2(Cursor2) | Max Y | Min Y | Avg Y

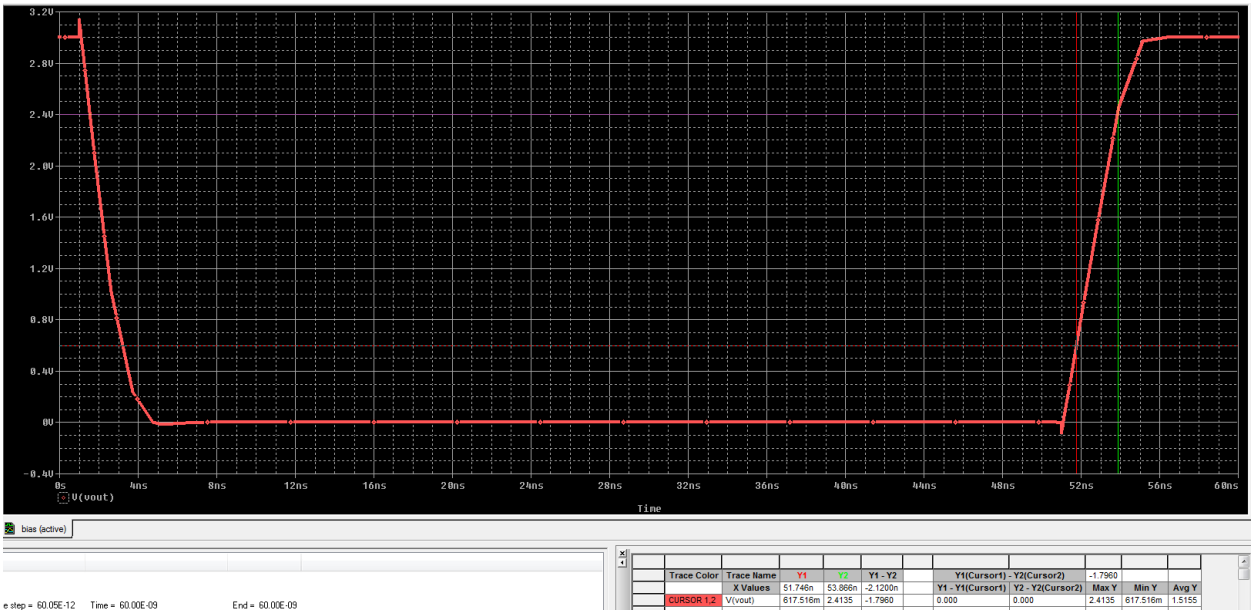
t_{pdr}

t_{pdf}

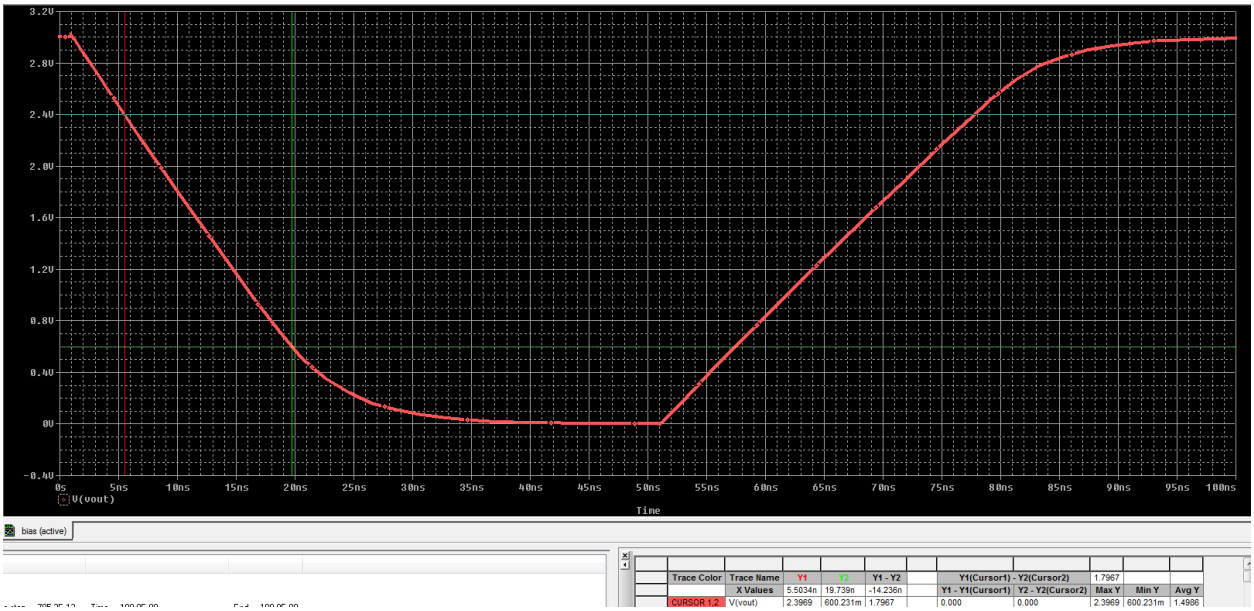


For C = 1pF,

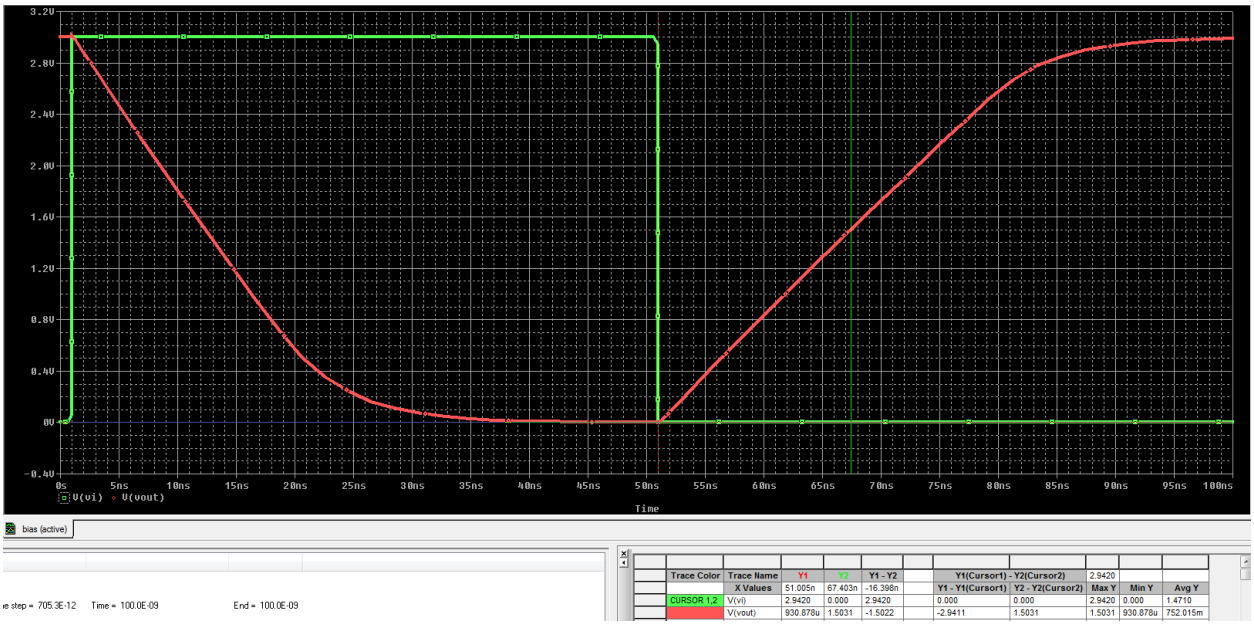
t_r


3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0V
-0.4V
0s 4ns 8ns 12ns 16ns 20ns 24ns 28ns 32ns 36ns 40ns 44ns 48ns 52ns 56ns 60ns
V(vout)
Time
bias (active)
Trace Color Trace Name Y1 Y2 Y1 - Y2 Y1(Cursor1) - Y2(Cursor2) -1.7960
X Values 51.746n 53.866n -2.1200n Y1 - Y1(Cursor1) Y2 - Y2(Cursor2) Max Y Min Y Avg Y
CURSOR 1,2 V(vout) 617.516m 2.4135 -1.7960 0.000 0.000 2.4135 617.516m 1.5155
e step = 60.05E-12 Time = 60.00E-09 End = 60.00E-09

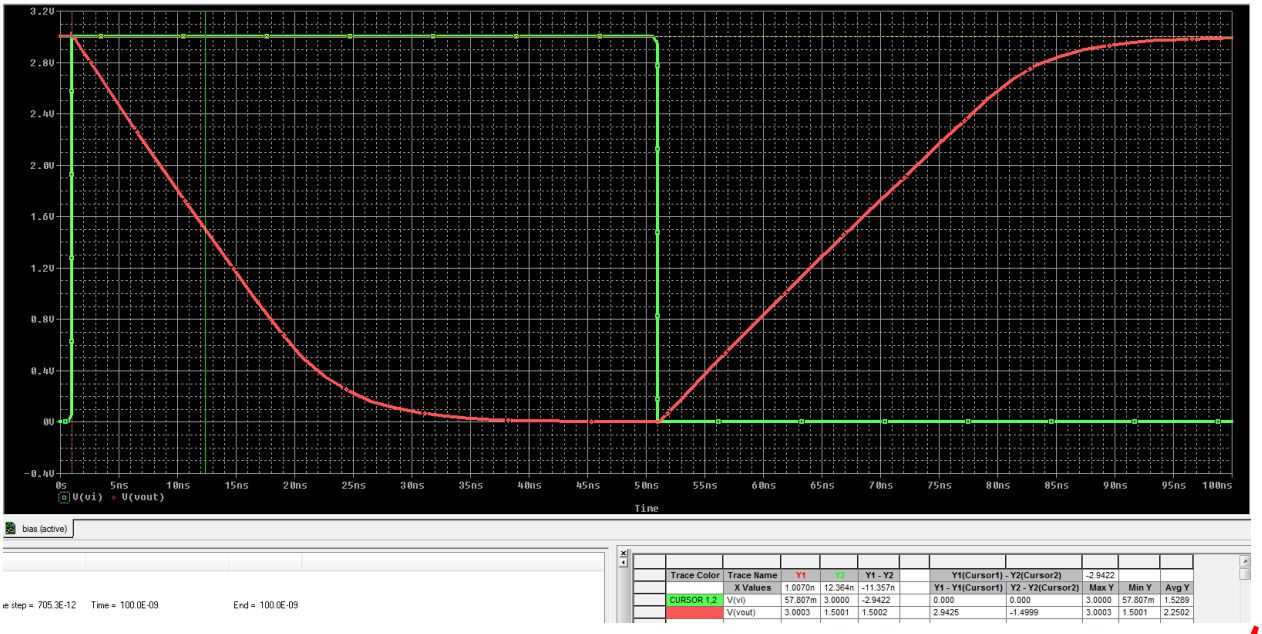
t_f


3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0V
-0.4V
0s 5ns 10ns 15ns 20ns 25ns 30ns 35ns 40ns 45ns 50ns 55ns 60ns 65ns 70ns 75ns 80ns 85ns 90ns 95ns 100ns
V(vout)
Time
bias (active)
Trace Color Trace Name Y1 Y2 Y1 - Y2 Y1(Cursor1) - Y2(Cursor2) 1.7967
X Values 5.5034n 19.739n -14.236n Y1 - Y1(Cursor1) Y2 - Y2(Cursor2) Max Y Min Y Avg Y
CURSOR 1,2 V(vout) 2.3969 600.231m 1.7967 0.000 0.000 2.3969 600.231m 1.4986

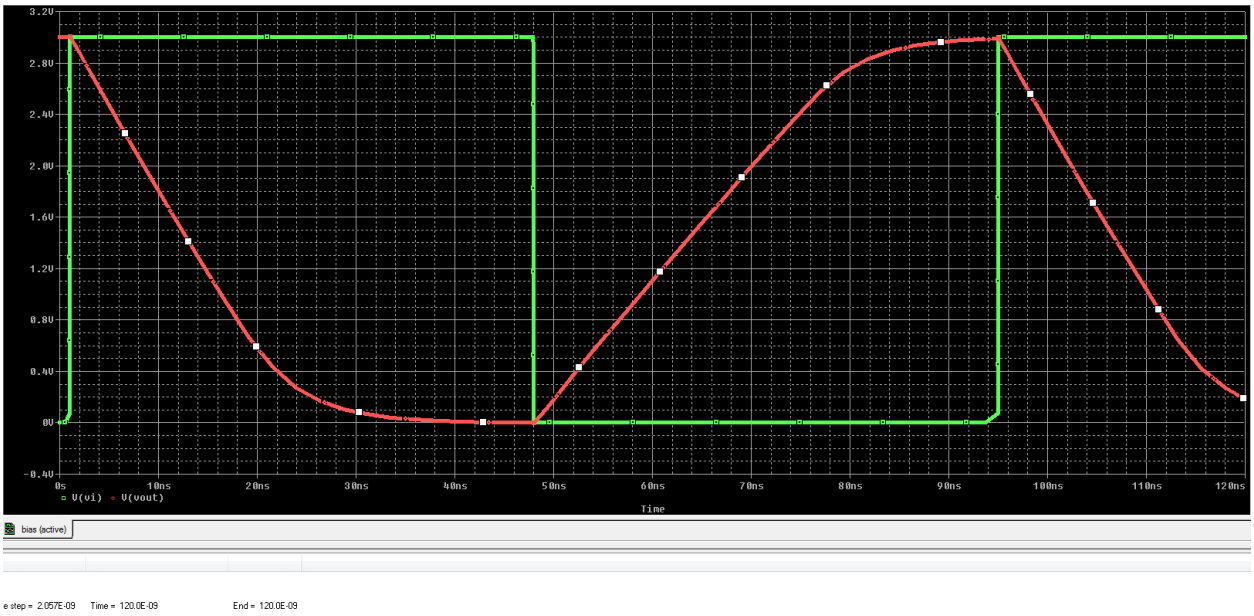
t_{pdr}



t_{pdf}



From the SPICE simulation below, our maximum input frequency is 10.638MHz.



We calculated our power dissipation to be. The following steps show how we calculated our answer:

$$P = CV_{DD}^2 f$$

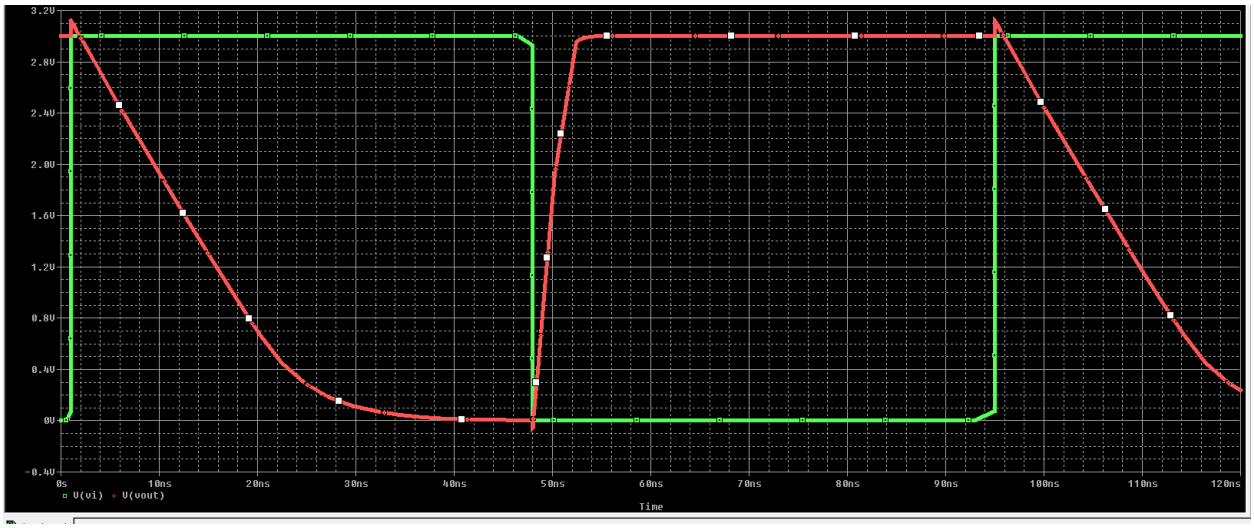
$$= 1 * 10^{-12} * 9 * 10.638x10^6$$

$$= 95.74\mu w$$

Below are the transfer characteristics of our symmetric inverter after increasing the gate width of the PMOS transistor by 10X.

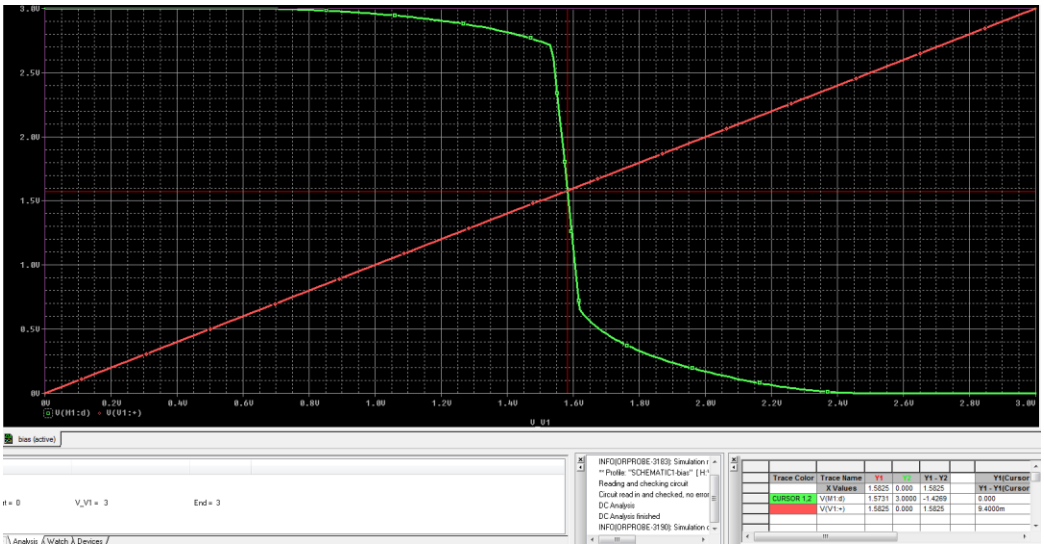
From SPICE, we simulated our noise margins to be $N_{ML} = 2.00$ and $N_{MH} = 0.449$. We observe that our noise margins are now worse with an asymmetric CMOS inverter. N_{MH} decreases because V_{in} must become relatively high(small range for valid V_{in} high) to overcome the large amount of current from the PMOS that fills the capacitor, while the NMOS drains current more slowly. N_{ML} increases since the strong current from the PMOS flows readily into the capacitor for a great range of V_{in} low, while CMOS characteristics guarantee sharp transition and low V_{OL}.

We simulated the rise and fall times for a load capacitance of 1pF to be $t_r = 2.547ns$ and $t_f = 14.55ns$. Since the PMOS transistor is significantly larger, it conducts much more current and is thus able to fill the capacitor much faster. Consequently, the rise time is much faster than the fall time. Therefore the clock cycle is now limited by the NMOS. The power dissipation should increase since we are sinking more current in our CMOS. Especially at transition voltage, more current will flow from V_{DD} to ground. Leakage currents will have more of an effect.

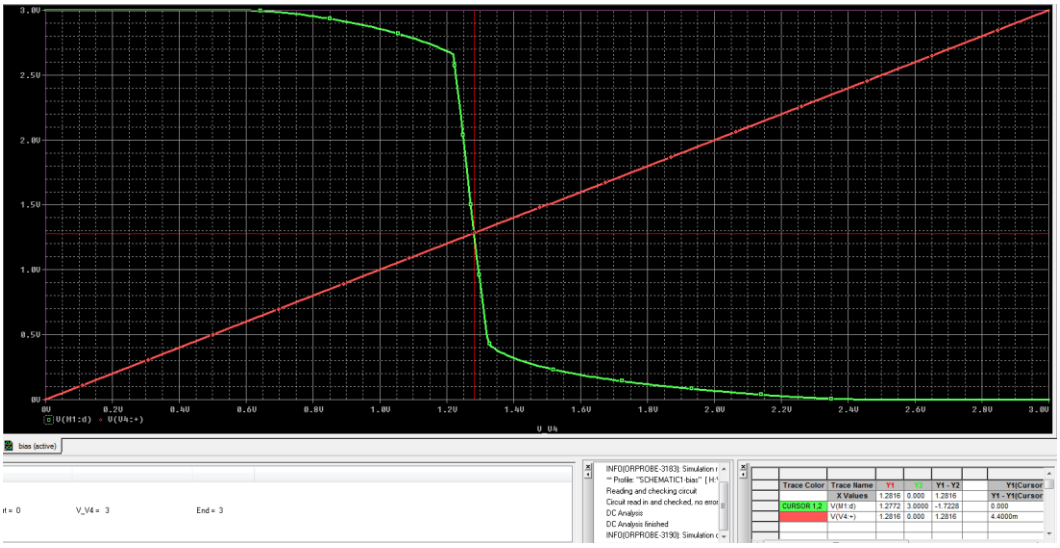


2) CMOS NAND Gate Design and Characterization

For the worst case setup the nMOS pull-down widths should be 2um. This is because the pull-down of the NAND gate is in series. Effective length is 2um, and width must be doubled to match. For the pMOS pull-ups, the worst case is when only one of the pull-ups is on. The W/L ratios remain the same.



Transfer characteristic for $V_{IN1} = V_{IN2}$ swept from 0 to 3V. $V_{INV} = 1.58V$.



Transfer characteristic for $V_{IN1} = V_{DD}$ and V_{IN2} swept from 0 to 3V. $V_{INV} = 1.22V$.

Type up β_r equations and V_{INV} equations.

$$\beta r = \frac{k_D{}' \times \left(\frac{W}{L}\right)_D}{k_L{}' \times \left(\frac{W}{L}\right)_D}$$

Worst case:

$$\beta r = \frac{9e^{-6} \times \frac{2}{2}}{2.2e^{-6} \times \frac{4.09}{1}}$$

$$\beta r = 1$$

$$Vinv = \frac{Vdd + VtL + VtD\left(\sqrt{\beta r}\right)}{1 + \sqrt{\beta r}}$$

$$Vinv = \frac{3 - .73886 + .743469\left(\sqrt{2}\right)}{1 + \sqrt{2}}$$

$$Vinv = 1.502V$$

Best case:

$$\beta r = {}^{1}/_{2}$$

Since inputs are tied,

$$Vinv = \frac{Vdd + VtL + VtD\left(\sqrt{\beta r/n^2}\right)}{1 + \sqrt{\beta r/n^2}}$$

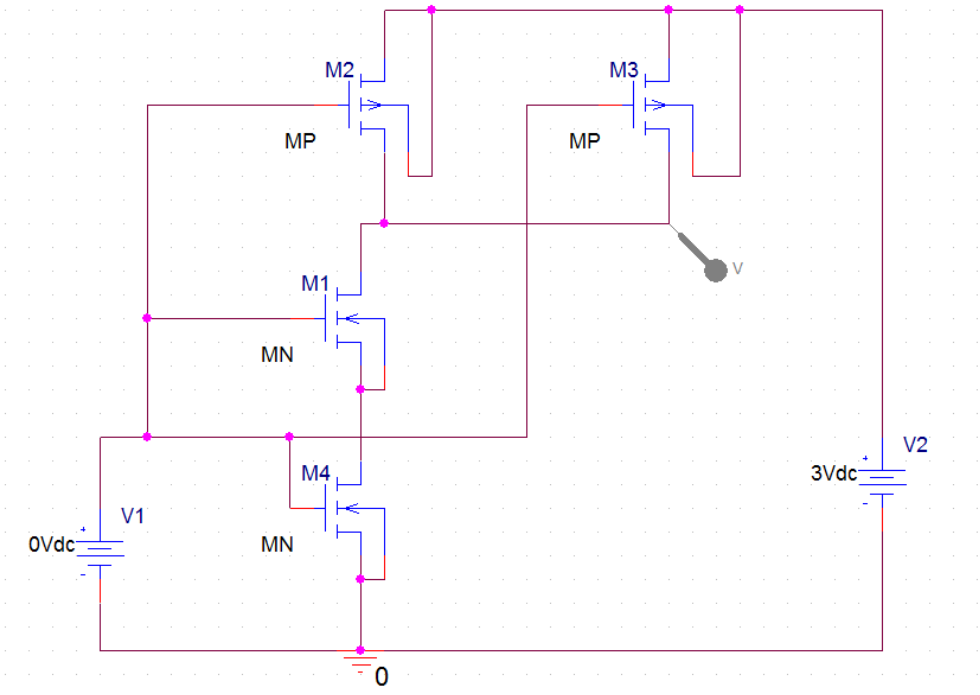
$$Vinv = \frac{3 - .73886 + .743469\left(\sqrt{2/4}\right)}{1 + \sqrt{2/4}}$$

$$Vinv = 1.865V$$

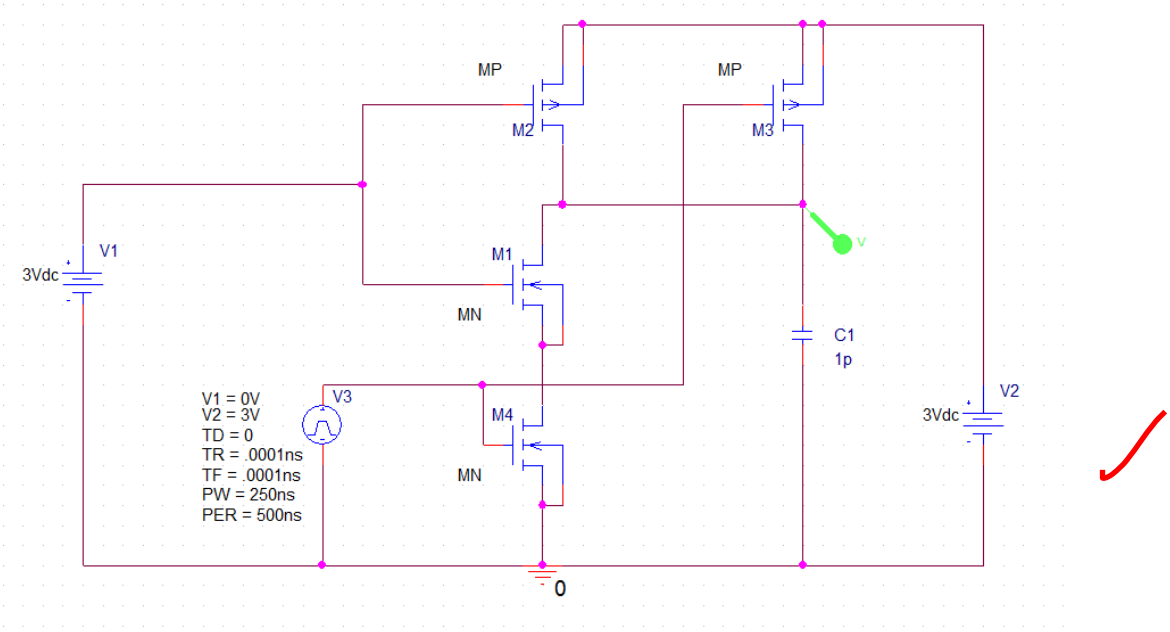
Maximum shift is .363 V

PSPICE shift is .360V

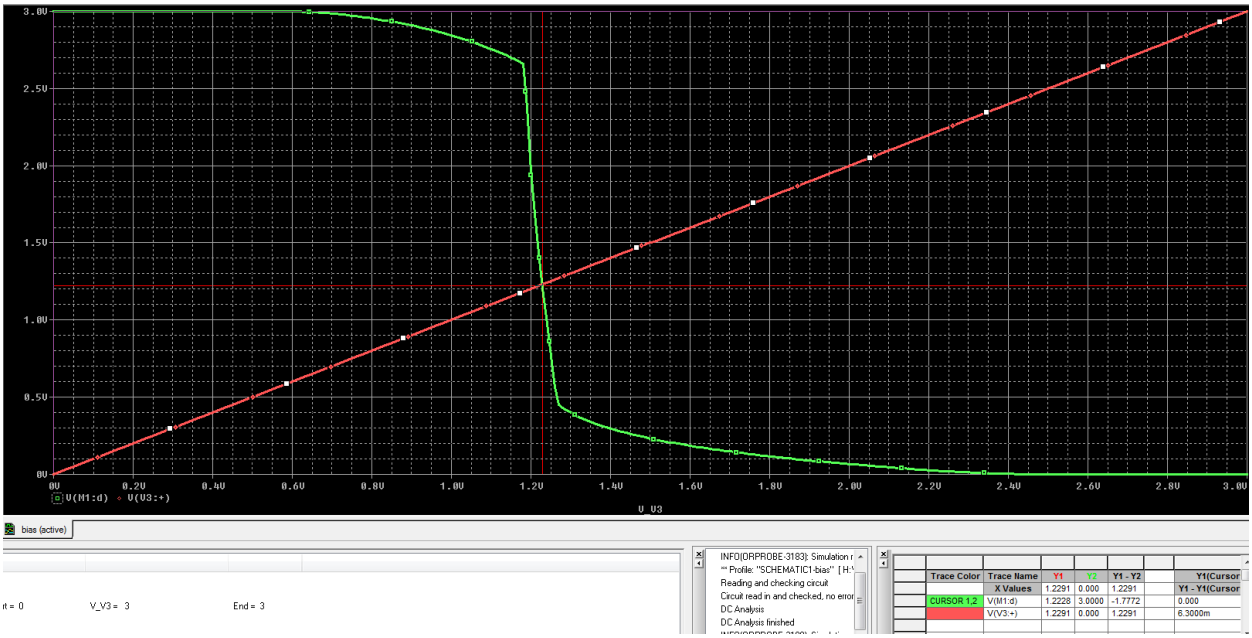
error of .826%



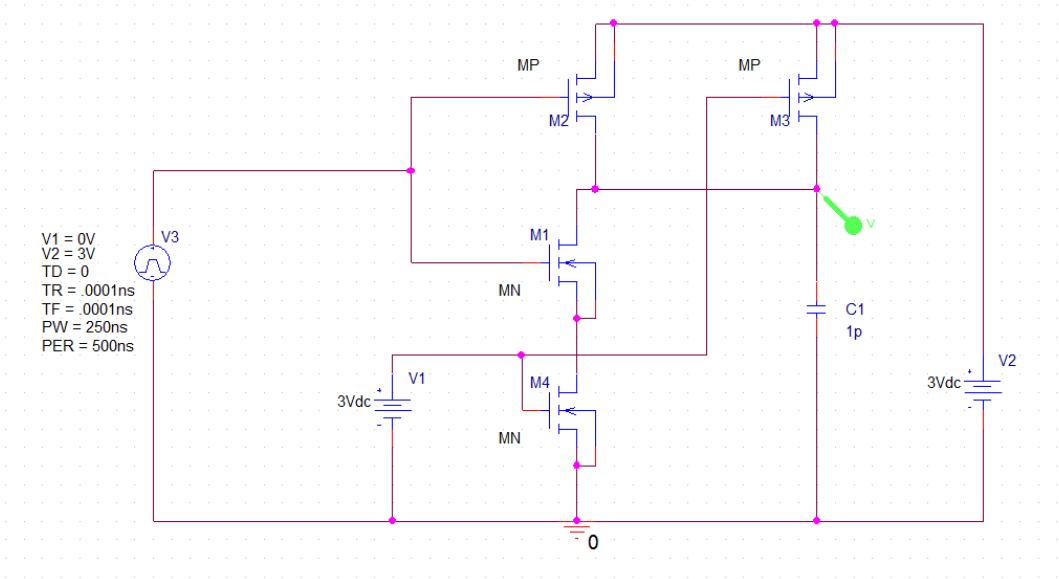
Configuration for part 1.



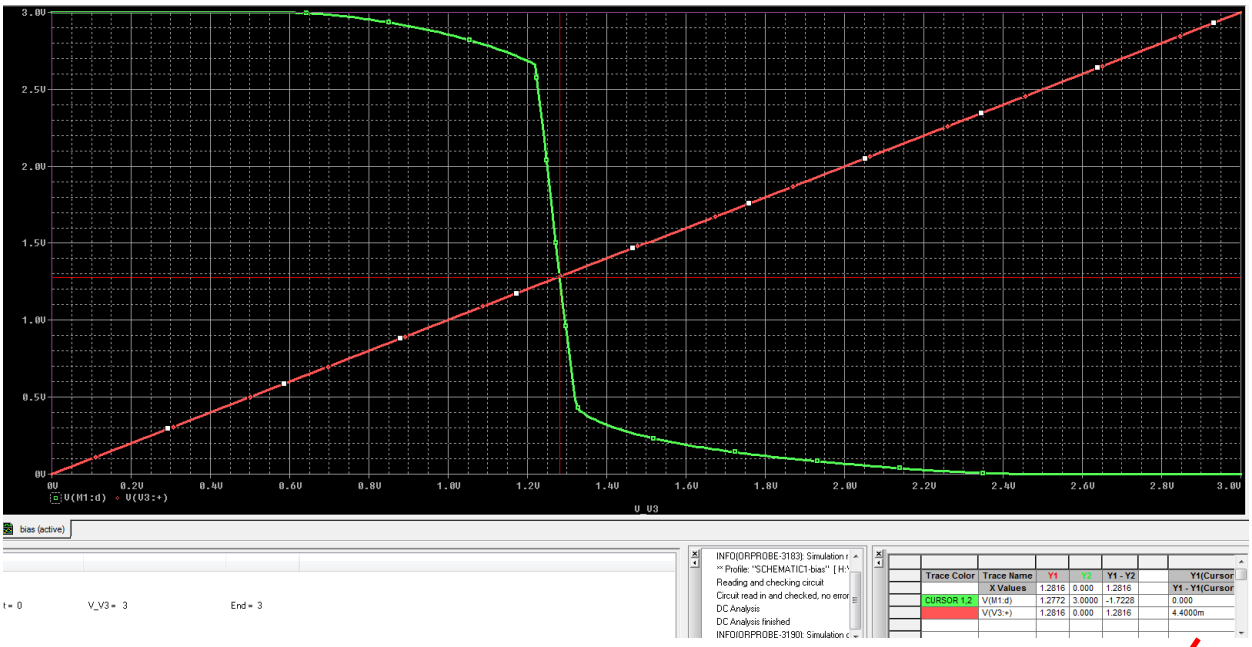
Configuration for part 2.



VTC for part 2. $V_{INV} = 1.22V$ as seen from the cursor.



Configuration for part 3.



VTC for part 3. $V_{INV} = 1.27V$ as seen from the cursor.

	t_r(ns)	t_f(ns)	t_{pdr}(ns)	t_{pdf}(ns)	t_{pd}(ns)
V1 pulse,V2 high	26.684	11.090	19.497	8.191	13.844
V2 pulse, V1 high	21.404	11.800	16.554	8.165	12.360
V1, V2 tied, pulse	10.264	12.296	8.313	8.427	8.379
Inverter	20.305	14.2356	16.398	11.357	13.878

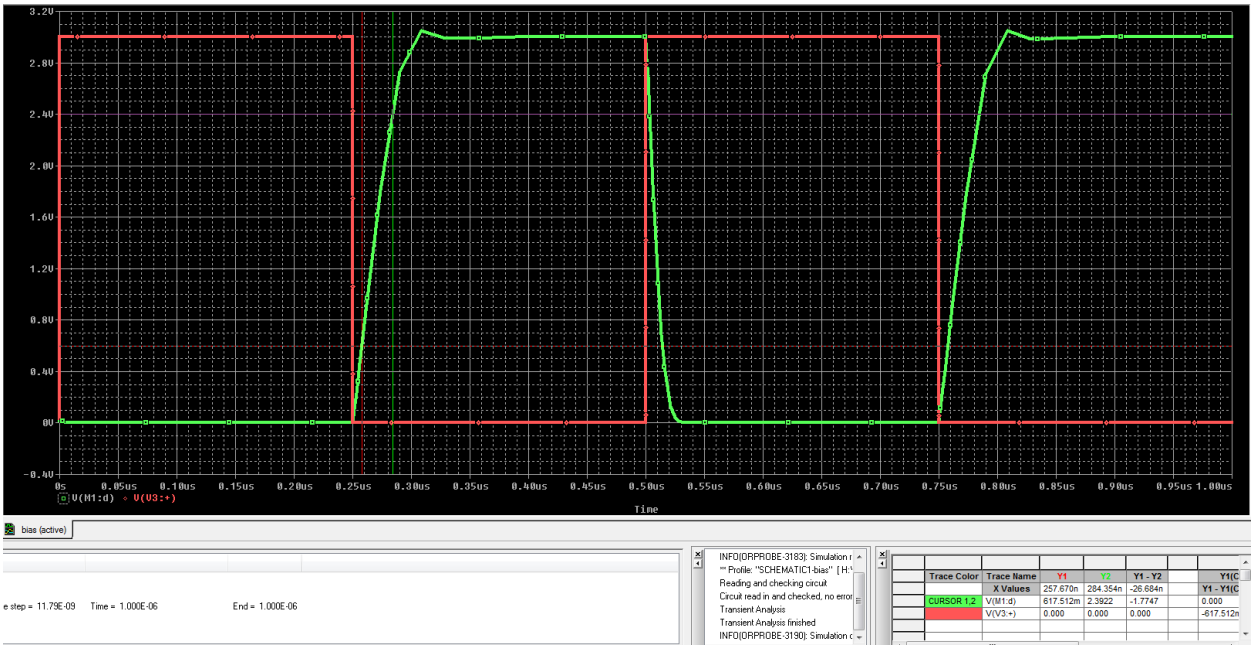
Note some discrepancy between V1 and V2 individual pulse, which is expected to be the same. This was caused by experimental error.

As expected, tied inputs have a significantly reduced rise time and rising propagation delay. This is due to the effective width of the pMOS doubling, which results in more current flow.

Measurements of rise and rising propagation delay are similar for one input pulse in the NAND gate and the reference inverter. The width is doubled for the drivers in the NAND gate to counteract the doubled effective length and match the reference inverter. This results in a small boost in current at the transition point and accounts for the slight decrease in fall and falling propagation delay times.

For V1 pulse, V2 high:

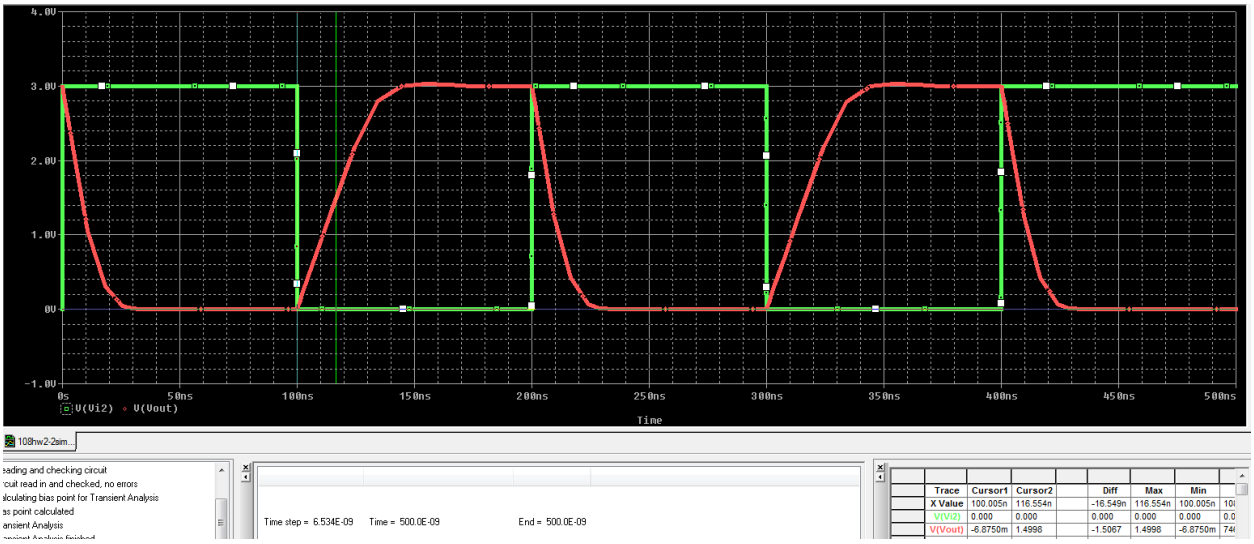
t_f/t_r



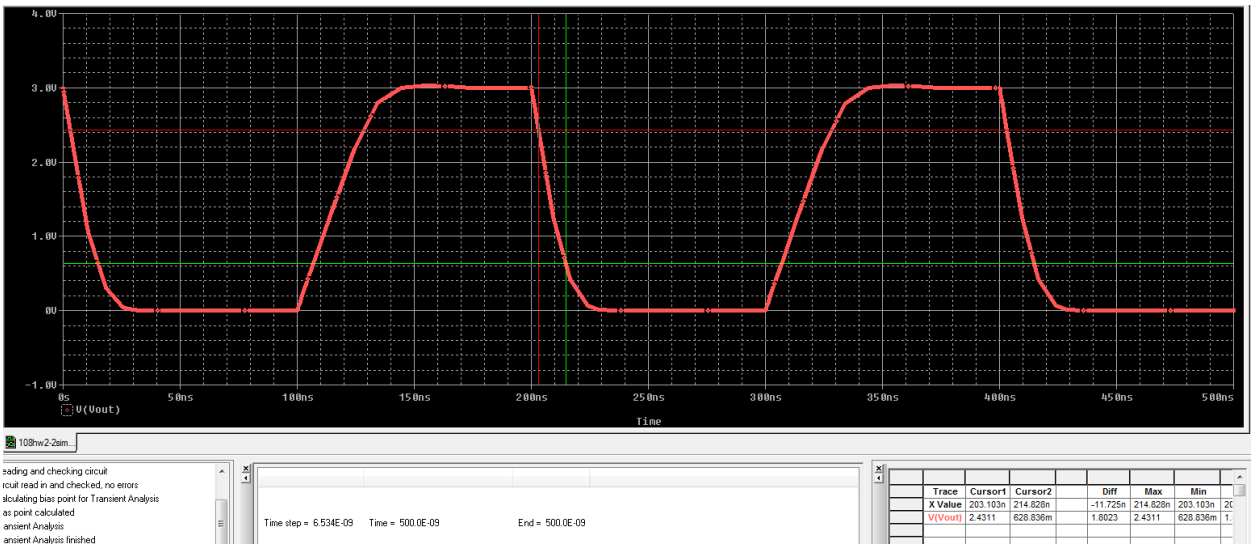
t_{pd}

For V2pulse, V1 high:

t_{pd}

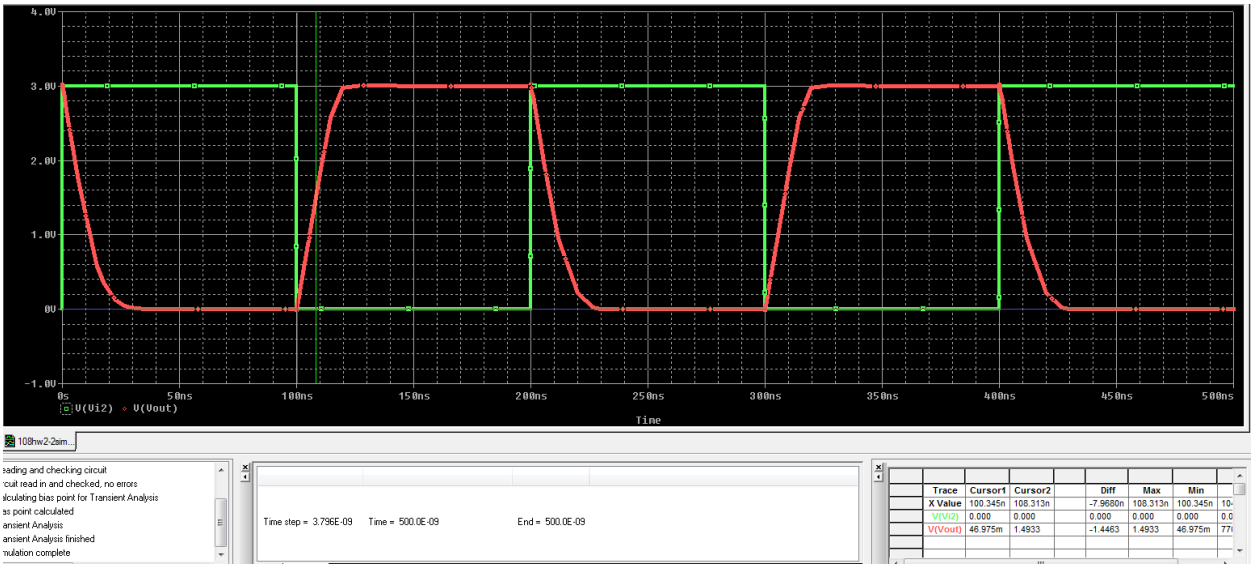


t_f/t_r

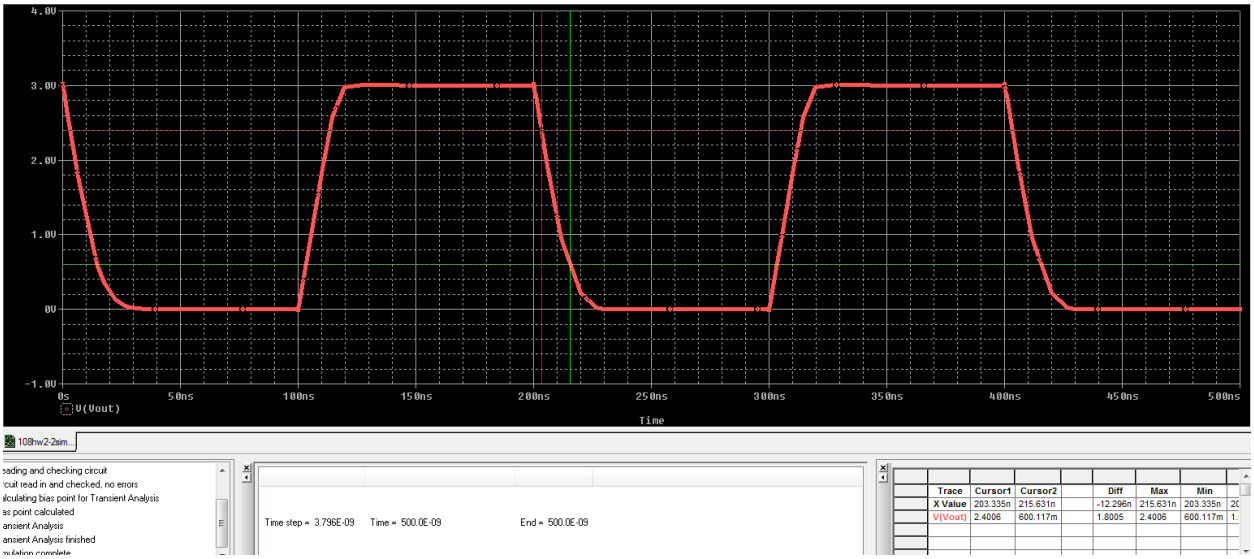


For V1 and V2 tied pulse

t_{pd}



t_f/t_r



Based on our findings with the NAND gate, we would expect slightly slower rise and rising propagation delay times, as the pMOS load carriers are holes. Mainly, since the nMOS are in parallel, we would expect similar performance to the reference inverter in fall and falling propagation delay times for a one input pulse. For a tied input pulse, fall and falling propagation delay times would decrease.

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5/5
Sahar

comparing NOR gate to a NAND gate?