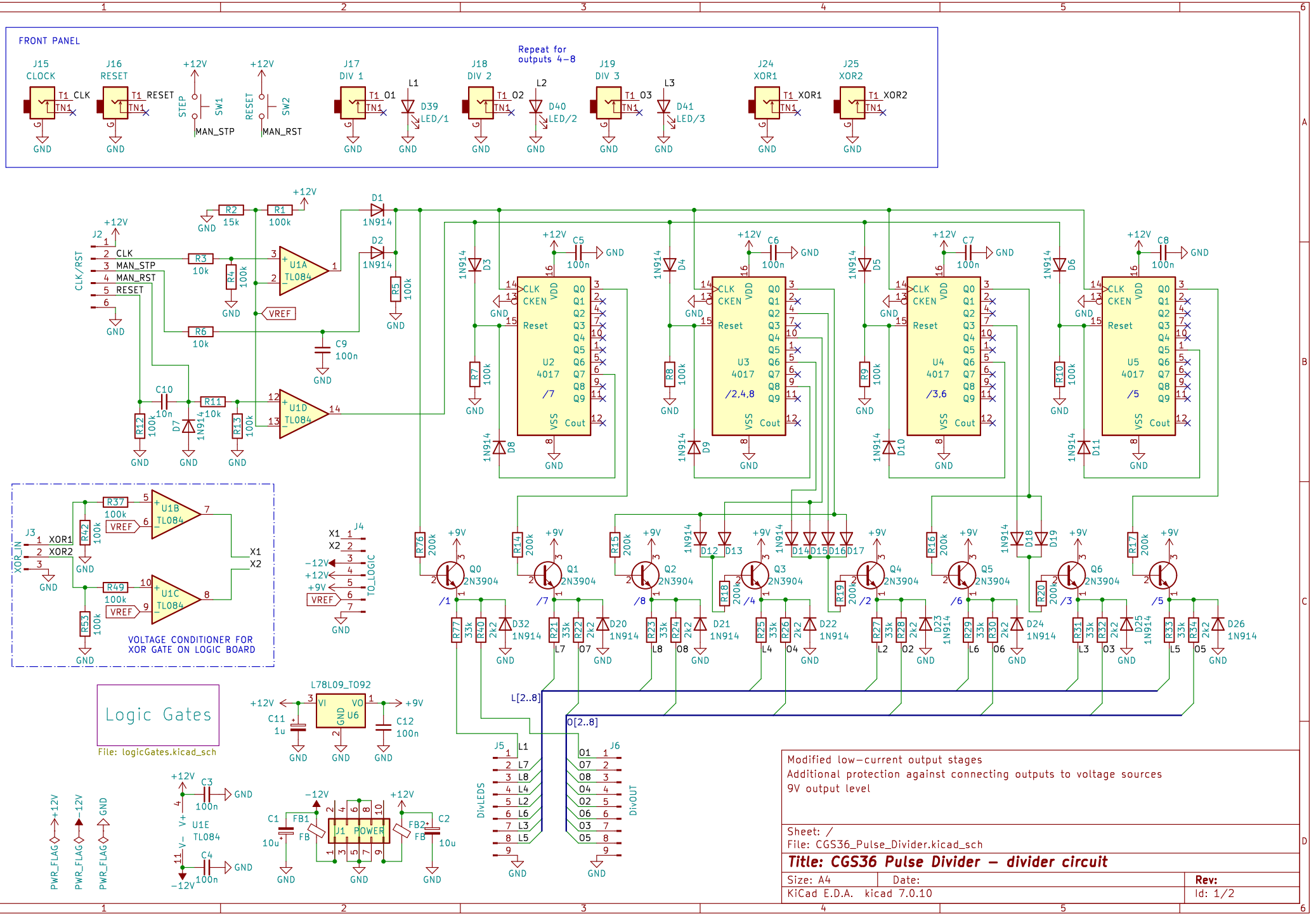
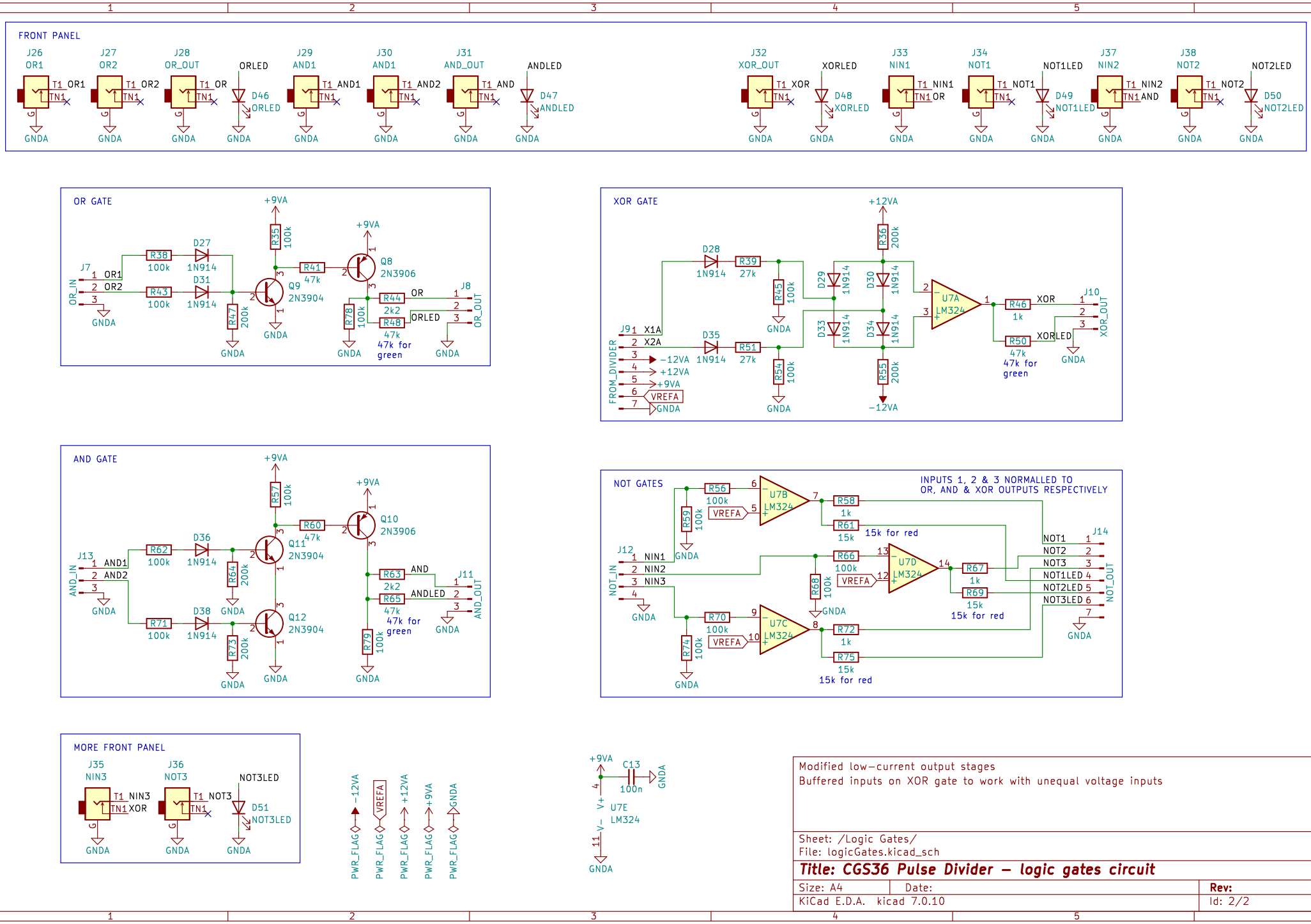

FRONT PANEL
J15 CLOCK
J16 RESET
+12V STEP SW1 MAN_STP
+12V RESET SW2 MAN_RST
J17 DIV 1
J18 DIV 2
J19 DIV 3
Repeat for outputs 4–8
L1 D39 LED/1
L2 D40 LED/2
L3 D41 LED/3
J24 XOR1
J25 XOR2
J2 CLK/RST
CLK
MAN_STP
MAN_RST
RESET
U1A TL084
U1D TL084
VREF
U2 4017 /7
U3 4017 /2,4,8
U4 4017 /3,6
U5 4017 /5
Q0 2N3904 /1
Q1 2N3904 /7
Q2 2N3904 /8
Q3 2N3904 /4
Q4 2N3904 /2
Q5 2N3904 /6
Q6 2N3904 /3
J3 XOR_IN
U1B TL084
U1C TL084
VOLTAGE CONDITIONER FOR XOR GATE ON LOGIC BOARD
J4 TO_LOGIC
L78L09_TO92
U1E TL084
U1 POWER
L[2..8]
O[2..8]
J5 DivLEDS
J6 DivOUT
Logic Gates
File: logicGates.kicad_sch
Modified low-current output stages
Additional protection against connecting outputs to voltage sources
9V output level
Sheet: /
File: CGS36_Pulse_Divider.kicad_sch
Title: CGS36 Pulse Divider – divider circuit
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.10
Id: 1/2


FRONT PANEL
J26 OR1
J27 OR2
J28 OR_OUT
ORLED
D46 ORLED
J29 AND1
J30 AND1
J31 AND_OUT
ANDLED
D47 ANDLED
J32 XOR_OUT
XORLED
D48 XORLED
J33 NIN1
J34 NOT1
NOT1LED
D49 NOT1LED
J37 NIN2
J38 NOT2
NOT2LED
D50 NOT2LED
GNDA
OR GATE
+9VA
J7
OR_IN
R38 100k
R43 100k
D27 1N914
D31 1N914
R47 200k
R35 100k
Q9 2N3906
R41 47k
Q8 2N3906
R44 2k2
R48 47k
47k for green
R78 100k
J8
OR_OUT
XOR GATE
+12VA
D28 1N914
R39 27k
R45 100k
D29 1N914
D33 1N914
D30 1N914
D34 1N914
R36 200k
R55 200k
U7A LM324
R46 1k
R50 47k
47k for green
J9
FROM_DIVIDER
X1A
X2A
−12VA
+12VA
+9VA
VREFA
D35 1N914
R51 27k
R54 100k
J10
XOR_OUT
XOR
XORLED
AND GATE
R57 100k
R60 47k
Q10 2N3906
Q11 2N3904
Q12 2N3904
R62 100k
R64 200k
D36 1N914
R71 100k
R73 200k
D38 1N914
R63 2k2
R65 47k
47k for green
R79 100k
J13
AND_IN
AND1
AND2
J11
AND_OUT
AND
ANDLED
NOT GATES
INPUTS 1, 2 & 3 NORMALLED TO OR, AND & XOR OUTPUTS RESPECTIVELY
R56 100k
R59 100k
U7B LM324
R58 1k
R61 15k
15k for red
J12
NOT_IN
NIN1
NIN2
NIN3
R66 100k
R68 100k
U7D LM324
R67 1k
R69 15k
15k for red
R70 100k
R74 100k
U7C LM324
R72 1k
R75 15k
15k for red
J14
NOT_OUT
NOT1
NOT2
NOT3
NOT1LED
NOT2LED
NOT3LED
MORE FRONT PANEL
J35 NIN3
J36 NOT3
NOT3LED
D51 NOT3LED
PWR_FLAG
−12VA
VREFA
+12VA
+9VA
GNDA
C13 100n
U7E LM324
V+
V−
Modified low−current output stages
Buffered inputs on XOR gate to work with unequal voltage inputs
Sheet: /Logic Gates/
File: logicGates.kicad_sch
Title: CGS36 Pulse Divider – logic gates circuit
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.10
Id: 2/2