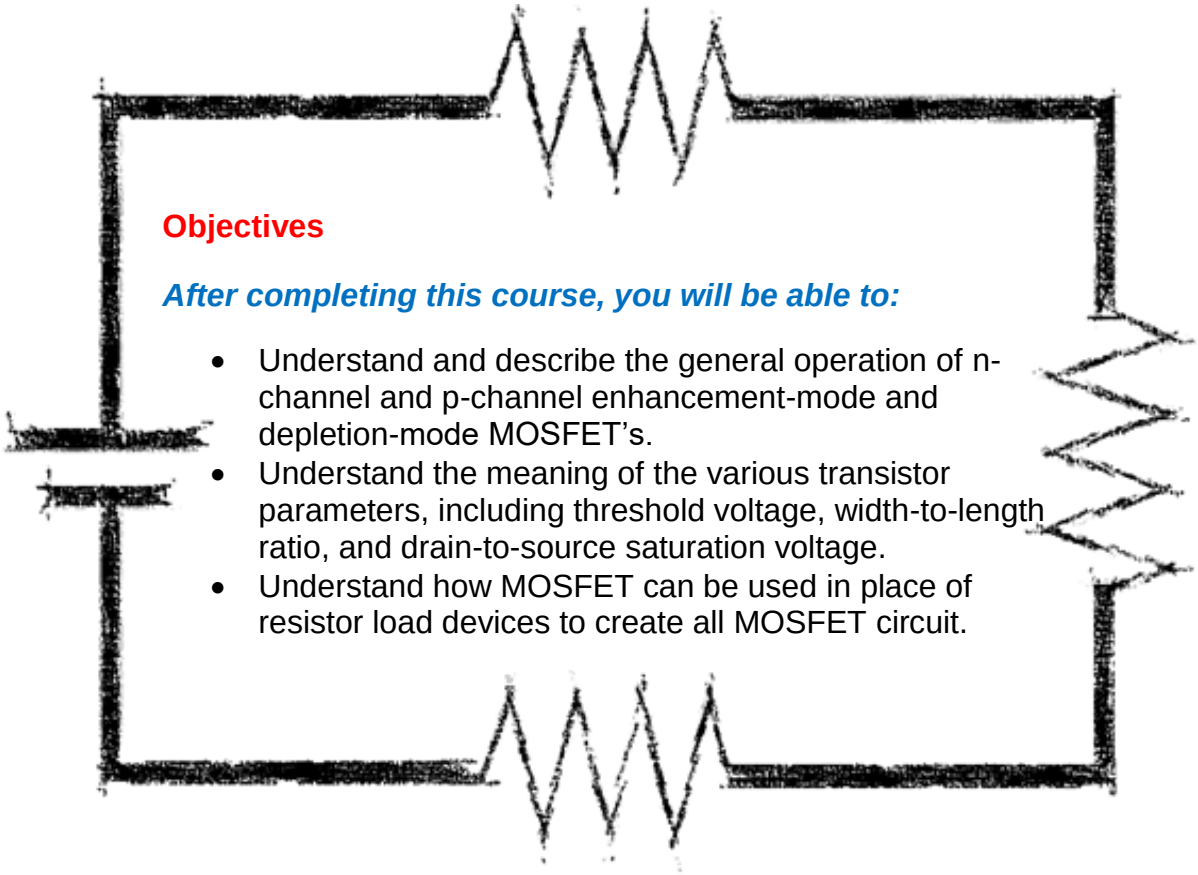
CHAPTER 9
FIELD EFFECT TRANSISTOR



Objectives

After completing this course, you will be able to:

- Understand and describe the general operation of n-channel and p-channel enhancement-mode and depletion-mode MOSFET's.
- Understand the meaning of the various transistor parameters, including threshold voltage, width-to-length ratio, and drain-to-source saturation voltage.
- Understand how MOSFET can be used in place of resistor load devices to create all MOSFET circuit.

What is Field Effect Transistor?

The Field Effect Transistor or simply *FET* however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a "VOLTAGE" operated device.

The Field Effect Transistor is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counter parts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two Ohmic electrical connections at either end commonly called the Drain and the Source respectively.

Comparison of Connection between JFET and BJT

The semiconductor "channel" of the Junction Field Effect Transistor is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

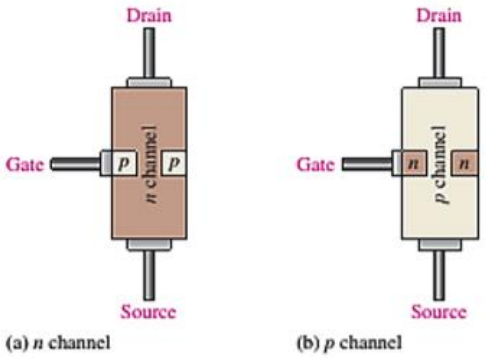


Figure 1: A representation of the basic structure of the two types of JFET.

Figure 1(a) shows the basic structure of an n-channel JFET. Wire leads are connected to each end of the n-channel; the drain is at the upper end (analogous to the collector of a BJT), and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate (analogous to the base of a BJT) lead. For simplicity, the gate lead is shown connected to only one of the p regions.

Operating Of JFET

To illustrate the operation of a JFET, Figure 2 shows DC bias voltages applied to an n-channel device, when the drain is positive with respect to the source and there is no gate source voltage, there is current in the channel. When a negative gate voltage is applied to the FET, the electric field causes the channel to narrow, which in turn causes current to decrease.

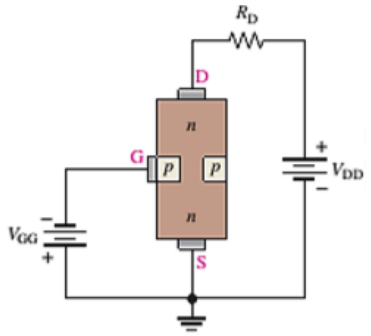


Figure 2: A biased n-channel JFET.

The symbol for an n-channel JFET is shown, along with the proper polarities of the applied dc voltages. For an n-channel device, the gate is always operated with a negative (or zero) voltage with respect to the source.

JFET characteristics and parameters there are three regions in the characteristic curve for a JFET as illustrated for the case when $V_{GS} = 0V$. Between A and B is the Ohmic region, where current and voltage are related by Ohm's law. From B to C is the

active (constant-current) region where current is essentially independent of V_{DS}. Beyond C is the breakdown region. Operation here can damage the FET.

When V_{GS} is set to different values, the relationship between VDS and ID develops a family of characteristic curves for the device. An n-channel characteristic is illustrated Figure 3.

Notice: that V_p is positive and has the same magnitude as V_{GS} (off).

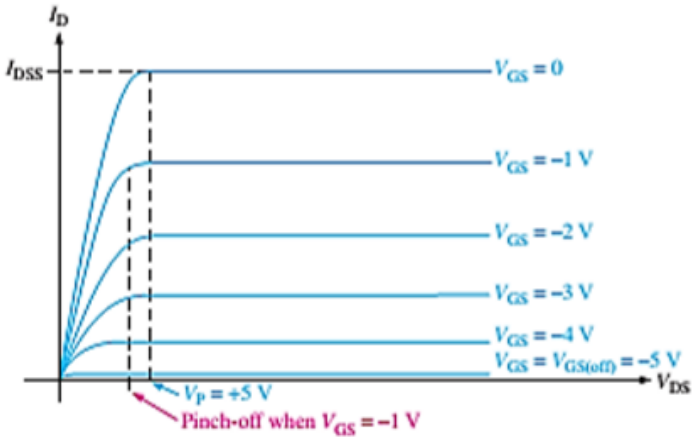


Figure 3: Family of drain characteristic curves.

JFET Universal Transfer Characteristic a plot of V_{GS} to I_D is called the transfer or trans-conductance curve. The transfer curve is a plot of the output current (I_D) to the input voltage (V_{GS}).
The transfer curve is based on the equation

$$\mathrm{I_D} = \mathrm{I_{DSS}}\left(1 - \frac{\mathrm{V_{GS}}}{\mathrm{V_{GS(off)}}}\right)^2$$

By substitution, you can find other points on the curve for plotting the universal curve.

The trans-conductance (transfer conductance), g_m, is the ratio of a change in output current (ΔID) to a change in the input voltage (ΔV_{GS}). This definition is

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The following approximate formula is useful for calculating g_m if you know g_{m0}.

$$g_m = g_{m0}(1 - \frac{VGS}{VGS(off)})$$

The value of gm0 can be found from

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

Because the slope changes at every point along the curve, the trans-conductance is not constant, but depends on where it is measured. The input resistance of a JFET is given by:

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

Where I_{GSS} is the current into the reverse biased gate. JFETs have very high input resistance, but it drops when the temperature increases.

JFET Biasing

Just as with the BJT, the purpose of biasing is to select the proper DC gate-to-source voltage to establish a desired value of drain current and thus, a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and current-source bias.

Self-bias

Self-bias is simple and effective, so it is the most common biasing method for JFETs. The JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for a p-channel JFET. This can be achieved using the self-bias arrangements shown in Figure 4. The gate resistor (R_G) does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0V. R_G is necessary only to force the gate to be at 0V and to isolate an AC signal from ground in amplifier applications.

For the n-channel JFET in Figure 4(a), is produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$ then $V_S = I_{DRS}$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Thus, $V_{GS} = -I_D R_S$ for the p-channel JFET shown in Figure 4(b), the current through RS produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since IS =ID,

$$V_{GS} = +I_D R_S$$

Keep in mind that analysis of the p-channel JFET is the same except for opposite polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

Since VS=IDRS, the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$$

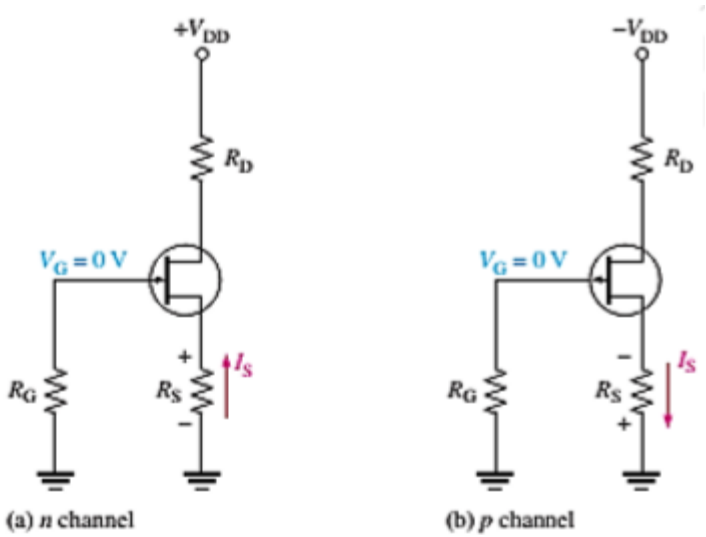


Figure 4: Self-biased JFET's ($I_S = I_D$ in all FETs).

Voltage Divider Bias

Voltage divider biasing is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate. VG is set by the voltage-divider and is independent of V_S. It must be larger than V_G in order to maintain the gate at a negative voltage with respect to the source. Voltage-divider bias helps stabilize the bias for variations between transistors.

Current Source Bias

An even more stable form of bias is current-source bias. The current-source can be either a BJT or another FET. With current-source biasing, the drain current is essentially independent of V_{GS}.

In this circuit, Q2 serves as a current source for Q1. An advantage to this particular circuit is that the output can be adjusted (using RS2) for 0 V DC.

JFET Ohmic Region

As described before, the Ohmic region is between the origin and the active region. A JFET operated in this region can act as a variable resistor. The slopes which represent conductance of successive V_{GS} lines are different in the Ohmic region. JFETs are often biased in the Ohmic region for use as a voltage controlled variable resistor. The control voltage is V_{GS}, and it determines the resistance by varying the Q-point.

Biasing of n-channel JFET

The cross sectional diagram shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area

when no external voltages are applied. JFETs are therefore known as depletion mode devices.

If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of “squeezing” effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

JFET Channel Pinched-off

In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when $V_{GS} = 0$ and maximum “ON” resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET.

Then to close the channel:

- No Gate Voltage (V_{GS}) and V_{DS} is increased from zero.
- No V_{DS} and Gate control is decreased negatively from zero.
- V_{DS} and V_{GS} varying.

The P-channel Junction Field Effect Transistor operates exactly the same as the N-channel above, with the following exceptions:

1). Channel current is positive due to holes.
2). The polarity of the biasing voltage needs to be reversed.

Output Characteristic V-I curves of a typical Junction FET

The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source.

Because a Junction Field Effect Transistor is a voltage controlled device, “NO current flows into the gate!” then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (R_{DS}) is given as:

Drain Sources Channel Resistance

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: g_m is the "trans-conductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

Modes of FET's

Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

Common Source (CS) Configuration

In the Common Source configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain. This is the most common

mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.

Common Gate (CG) Configuration

In the Common Gate configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v). The high input impedance feature of the previous connection is lost in this configuration as the common gate has low input impedance, but high output impedance.

Common Drain (CD) Configuration

In the Common Drain configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has high input impedance and low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase", 0^{o} with the input signal.

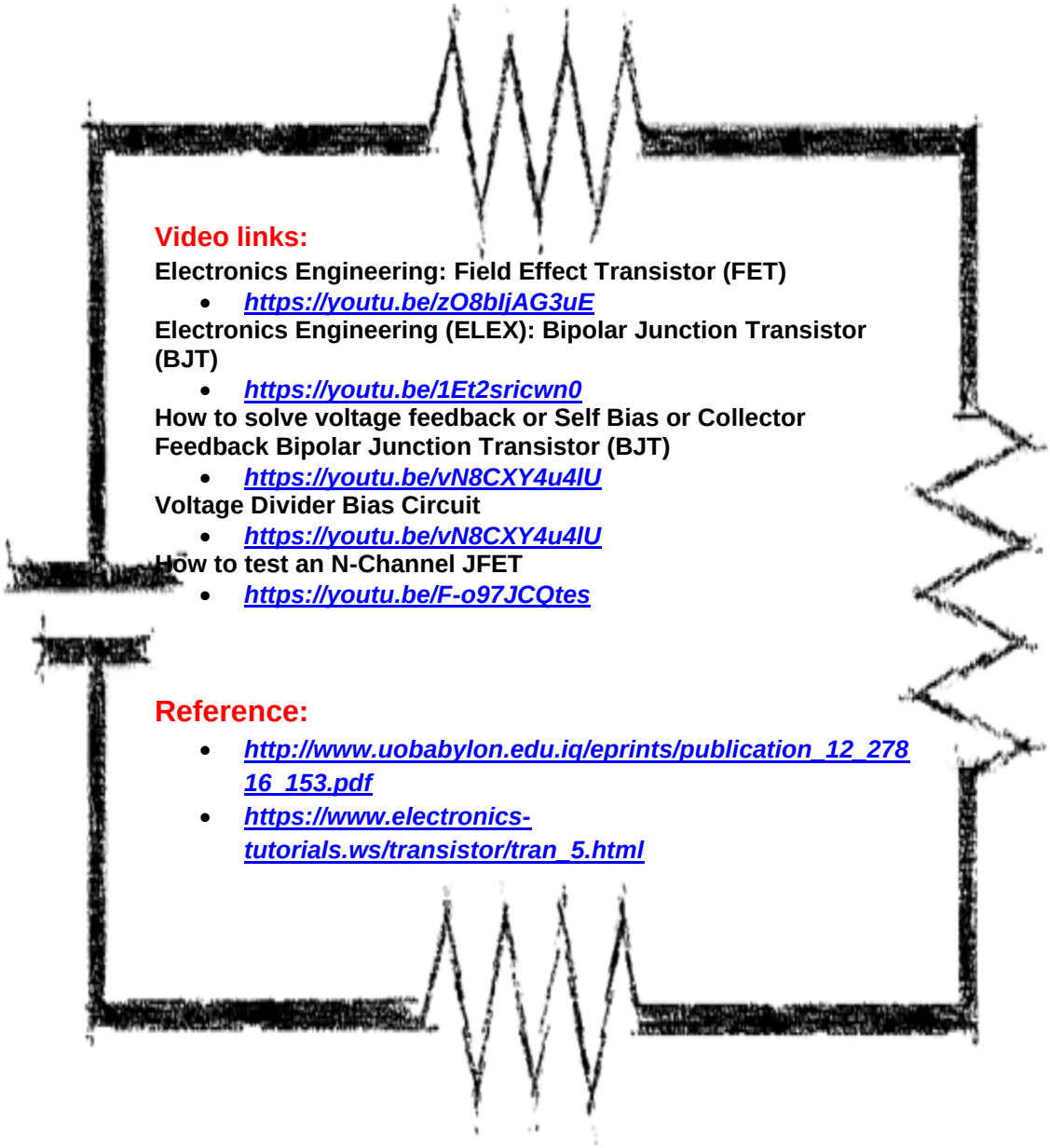
The JFET Amplifier

Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2.

Biasing of JFET Amplifier

This common source (CS) amplifier circuit is biased in class "A" mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor R_S is generally set to be about one quarter of V_{DD}, (V_{DD} /4) but can be any reasonable value.

The required Gate voltage can then be calculated from this R_S value. Since the Gate current is zero, ($I_G = 0$) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.



Video links:

Electronics Engineering: Field Effect Transistor (FET)

- ***https://youtu.be/zO8bIjAG3uE***

Electronics Engineering (ELEX): Bipolar Junction Transistor (BJT)

- ***https://youtu.be/1Et2sricwn0***

How to solve voltage feedback or Self Bias or Collector Feedback Bipolar Junction Transistor (BJT)

- ***https://youtu.be/vN8CXY4u4IU***

Voltage Divider Bias Circuit

- ***https://youtu.be/vN8CXY4u4IU***

How to test an N-Channel JFET

- ***https://youtu.be/F-o97JCQtes***

Reference:

- ***http://www.uobabylon.edu.iq/eprints/publication_12_27816_153.pdf***
- ***https://www.electronics-tutorials.ws/transistor/tran_5.html***