



HC32F460 Series

32-bit ARM® Cortex®-M4 microcontroller

data sheet

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Product Features

ARM Cortex-M4 32bit MCU+FPU up to 250DMIPS up to 512KB Flash, 192KB SRAM, USB FS

(Device/Host), 14 Timers, 2 ADCs, 1 PGA, 3 CMPS, 20 communication ports

ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU,

MPU, DSP supporting SIMD instructions, and CoreSight standard debug unit. The highest operating frequency is 200MHz, and the Flash acceleration unit realizes 0-Wait program execution, reaching 250DMIPS or 680Coremarks

Computing performance

Built-in memory

- Maximum 512KByte Flash memory, support security protection and Data encryption*1
- Maximum 192KByte SRAM, including 32KByte 200MHz single-cycle access high-speed RAM, 4KByte Retention RAM

Power, clock, reset management

- System Power (Vcc): 1.8-3.6V
- 6 independent clock sources: external main clock crystal (4-25MHz), external secondary Crystal oscillator (32.768kHz), internal high-speed RC (16/20MHz), internal Medium speed RC (8MHz), internal low speed RC (32kHz), internal WDT dedicated With RC (10kHz)
- Includes power-on reset (POR), low voltage detect reset (LVDR), port reset
- 14 reset sources including bit (PDR), each reset source has an independent flag bit

Low power consumption operation

- Peripheral functions can be turned off or on independently
- Three low power consumption modes: Sleep, Stop, Power down mode
- Support super high speed mode, high speed mode, Switching Between Ultra Low Speed Modes
- Standby power consumption: Stop mode typ.90uA@25°C, Power Down mode down to 1.8uA@25°C
- In Power down mode, support 16 ports to wake up, support ultra-low Power consumption RTC works, 4KByte SRAM keeps data
- Fast wake-up from standby, wake-up from Stop mode as fast as 2us, Power The fastest wake-up in down mode is 20us

Peripheral operation support system significantly reduces CPU processing load

- 8-channel dual-master DMAC
- DMAC for USBFS
- Data Computing Unit (DCU)
- Support mutual triggering of peripheral events (AOS)

High performance simulation

- 2 independent 12bit 2MSPS ADCs
- 1 programmable gain amplifier (PGA)
- 3 independent voltage comparators (CMP) supporting 2 internal reference voltages
- 1 on-chip temperature sensor (OTS)

Timer

- 3 multifunctional 16bit PWM Timers (Timer6)
- 3 16bit motor PWM Timer (Timer4)
- 6 16bit general-purpose Timers (TimerA)
- 2 16bit basic Timer (Timer0)

Up to 83 GPIOs

- CPU single-cycle access, maximum 100MHz output
- Up to 81 5V-tolerant IOs

Maximum 20 communication interfaces

- 3 I2C, support SMBus protocol
- 4 USARTs, support ISO7816-3 protocol
- 4 SPIs
- 4 I2S, built-in audio PLL supports audio-level sampling accuracy
- 2 SDIO, support SD/MMC/eMMC format
- 1 QSPI, support 200Mbps high-speed access (XIP) 1 CAN, support ISO11898-1 standard protocol
- 1 USB 2.0 FS, built-in PHY, support Device/Host

Data encryption function

- AES/HASH/TRNG

Package form:

LQFP100 14x14mm	VFBGA100 7x7mm
LQFP64 10x10mm	QFN60 7x7mm
QFN48 5x5mm	LQFP48 7x7mm

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window mouth.

Supported models:

HC32F460PETB-LQFP100	HC32F460PEHB-VFBGA100
HC32F460KETA-LQFP64	HC32F460KEUA-QFN60TR
HC32F460JETA-LQFP48	HC32F460JEUA-QFN48TR
HC32F460PCTB-LQFP100	HC32F460KCTA-LQFP64
HC32F460JCTA-LQFP48	



statement

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1 Introduction (Overview)

HC32F460 series is based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200MHz

High-performance MCUs. The Cortex-M4 core integrates a floating-point unit (FPU) and DSP to implement single-precision floating-point arithmetic operations, supporting

Supports all ARM single-precision data processing instructions and data types, and supports a complete DSP instruction set. The core integrates the MPU unit, while stacking

Add DMAC dedicated MPU unit to ensure the security of system operation.

HC32F460 series integrates high-speed on-chip memory, including up to 512KB of Flash and up to 192KB of SRAM. integrated

The Flash access acceleration unit is implemented to realize the single-cycle program execution of the CPU on the Flash. Polled bus matrix supports multiple buses

The host accesses memory and peripherals simultaneously, improving operational performance. The bus master includes CPU, DMA, USB-specific DMA, etc. divide bus moment

Outside the array, it supports data transfer between peripherals, and basic arithmetic operations and events trigger each other, which can significantly reduce the transaction processing load of the CPU.

The HC32F460 series integrates rich peripheral functions. Including 2 independent 12bit 2MSPS ADCs, 1 adjustable gain PGA,

3 voltage comparators (CMP), 3 multi-function 16bit PWM Timers (Timer6) support 6 complementary PWM outputs,

3 motor PWM Timers (Timer4) support 18 complementary PWM outputs, 6 16bit general-purpose Timers (TimerA)

Support 3-way 3-phase quadrature encoding input and 48-way Duty independent PWM output, 11 serial communication ports

(I2C/UART/SPI), 1 QSPI interface, 1 CAN, 4 I2S support audio PLL, 2 SDIO, 1 USB

FS Controller with on-chip FS PHY supports Device/Host.

The HC32F460 series supports wide voltage range (1.8-3.6V), wide temperature range (-40-105°C) and various low power consumption modes.

In Run mode and Sleep mode, you can switch between ultra-high speed mode ($\geq 200\text{MHz}$), high-speed mode ($\geq 168\text{MHz}$) and ultra-low speed mode

($\leq 8\text{MHz}$). Supports fast wake-up in low-power mode, the fastest wake-up in STOP mode is 2us, and the fastest wake-up in Power Down mode

As fast as 20us.

typical application

HC32F460 series provide 48pin, 64pin, 100pin LQFP package, 48pin, 60pin QFN package,

The 100pin VFBGA package is suitable for high-performance motor frequency conversion control, intelligent hardware, IoT connection modules and other fields.

1.1 Model naming rules

HC 32 F 4 6 0 J E U A

Xiaohua Semiconductor

CPU bit width

32: 32bit

product type

F: Universal

CPU type

4: Cortex-M4

Performance ID 6: High

Performance

Function configuration identification code

0: configuration 1

pin count

J: 48Pin

K: 60Pin / 64Pin

P: 100Pin

FLASH capacity

C: 256KB

E: 512KB

package type

T: LQFP

In: QFN

H: VFBGA

Ambient temperature range

B: -40-105°C, industrial grade

A: -40-85°C, industrial grade

1.2 Model function comparison table

Table 1-1 Model function comparison table

Function	Product number																
	HC32F4 60PEHB	HC32F4 60PETB	HC32F4 60PCTB	HC32F4 60KETA	HC32F4 60 KCTA	HC32F4 60JETA	HC32F4 60JCTA	HC32F4 60 KNOW	HC32F4 60 MORE								
Flash Memory KB	512	512	256	512	256	512	256	512	512								
pin count	100	100	100	64	64	48	48	48	60								
Number of GPIOs	83	83	83	52	52	38	38	38	50								
5V Tolerant GPIO Count	81	81	81	50	50	36	36	36	48								
encapsulation	VFBGA	LQFP						QFN									
temperature range	-40~105°C			-40~85°C													
Power supply voltage range	1.8 ~ 3.6 V																
OTP byte	960																
SRAM KB	192																
DMA	2unit * 4ch																
external port interrupt	EIRQ * 16vec + NMI * 1ch																
Communication interface (in brackets is each channel required)	UART	4ch×2															
	SPI	4ch×3															
	2C	3ch×2															
	I2S	4ch×3															
	CAN	1ch×2															
	QSPI	1ch×6															
	SDIO	2ch×3															
	USB-FS	1ch×2															
Timers	Timer0	2 units															
	TimerA	6 units															
	Timer4	3unit															
	Timer6	3unit															
	WDT	1ch															
	SWDT	1ch															
	RTC	1ch															
Analog	12bit ADC	2unit, 16ch				2unit, 10ch			2 units,								
	PGA	1ch															
	CMP	3 ch															

Function	Product number								
	HC32F4 60PEHB	HC32F4 60PETB	HC32F4 60PCTB	HC32F4 60KETA	HC32F4 60 KCTA	HC32F4 60JETA	HC32F4 60JCTA	HC32F4 60 KNOW	HC32F4 60 MORE
OTS	ÿ								
AES128	ÿ								
HASHÿSHA256ÿ	ÿ								
WHITE	ÿ								
Frequency Monitoring Module (FCM)	ÿ								
Programmable voltage detection function (PWD)	ÿ								
debug interface	SWD								
	JTAG								

1.3 Functional Block Diagram

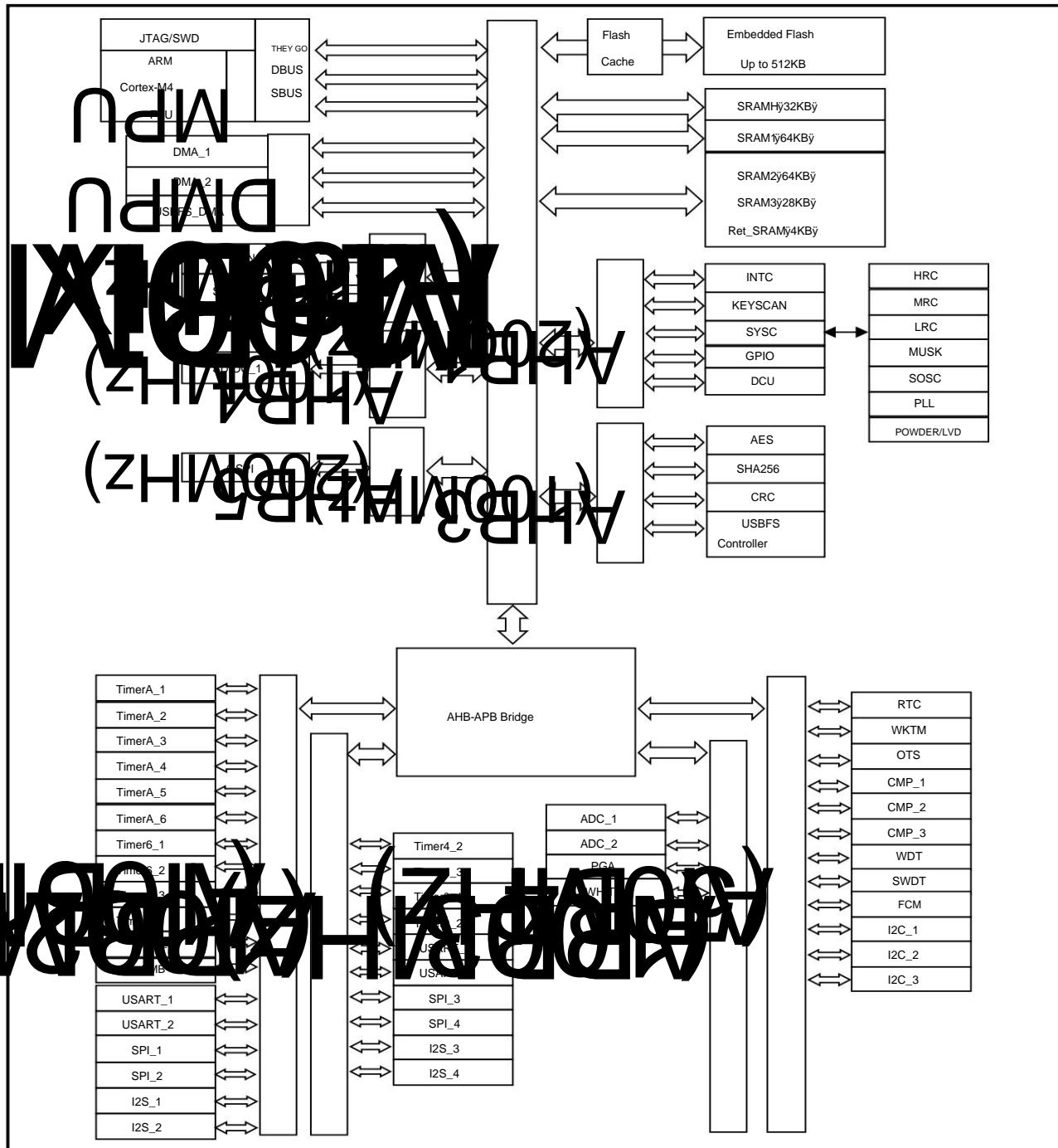


Figure 1-1 Functional block diagram

1.4 Function Introduction

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit reduced instruction

The CPU realizes fewer pins and lower power consumption, while providing excellent computing performance and rapid interrupt response capability. On-chip memory capacity

It can give full play to the excellent instruction efficiency of ARM® Cortex®-M4 with FPU. The CPU supports DSP instructions, which can realize

High-efficiency signal processing operations and complex algorithms are realized. The single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus architecture (BUS)

The main system consists of a 32-bit multilayer AHB bus matrix, which enables interconnection of the following master bus and slave bus.

host bus

- ÿ Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus

- ÿ System DMA_1 bus, system DMA_2 bus

- ÿ USBFS_DMA bus

slave bus

- ÿ Flash ICODE bus

- ÿ Flash DCODE bus

- ÿ Flash MCODE bus (the bus used by hosts other than CPU to access Flash)

- ÿ SRAMH bus (SRAMH 32kB)

- ÿ SRAMA bus (SRAM1 64KB)

- ÿ SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)

- ÿ APB1 peripheral bus (AOS/EMB/Timers/SPI/USART/I2S)

- ÿ APB2 peripheral bus (Timers/SPI/USART/I2S)

- ÿ APB3 peripheral bus (ADC/PGA/TRNG)

- ÿ APB4 peripheral bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)

- ÿ AHB1 peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC) ÿ AHB2

- peripheral bus (CAN/SDIOC) ÿ AHB3

- peripheral bus (AES/HASH/CRC/USB FS)

- ÿ AHB4 peripheral bus (SDIOC)

- ÿ AHB5 peripheral bus (QSPI)

With the help of the bus matrix, efficient concurrent access from the master bus to the slave bus can be achieved.

1.4.3 Reset Control (RMU)

The chip is configured with 14 reset methods.

- ÿ Power-on reset (POR)
- ÿ NRST pin reset (NRST)
- ÿ Brown-out reset (BOR)
- ÿ Programmable voltage detection 1 reset (PVD1R)
- ÿ Programmable voltage detection 2 reset (PVD2R)
- ÿ Watchdog reset (WDTR)
- ÿ Dedicated watchdog reset (SWDTR)
- ÿ Power-down wake-up reset (PDRST)
- ÿ Software reset (SRST)
- ÿ MPU error reset (MPUR)
- ÿ RAM parity reset (RAMPR)
- ÿ RAMECC reset (RAMECCR)
- ÿ Clock exception reset (CKFER)
- ÿ External high-speed oscillator abnormal shutdown reset (XTALER)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including: an external high-speed oscillator, an external low-speed oscillator, two PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a SWDT dedicated internal Low-speed oscillators, clock prescalers, clock multiplexing and clock gating circuits.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) uses the measurement reference clock to measure the target clock Perform monitoring measurements. An interrupt or reset occurs when the setting range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, and the source of the system clock can choose 6 clock sources:

- 1) External high-speed oscillator (XTAL)
- 2) External low-speed oscillator (XTAL32)
- 3) MPLL Clock (MPLL)
- 4) Internal High Speed Oscillator (HRC)
- 5) Internal Medium-speed Oscillator
- (MRC) 6) Internal Low-speed Oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 200MHz. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator tor (SWDTLRC). The real-time clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as a clock source. USB-FS 48MHz clock and I2S communication clock can choose system clock, MPLL, UPLL as the clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply, switching, and detection of multiple power domains of the chip in multiple operating modes and low power consumption modes. power supply

The controller is composed of power control logic (PWCL) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8V to 3.6V. A voltage regulator (LDO) supplies power to the VDD and VDDR domains, and the VDDR

A voltage regulator (RLDO) supplies power to the VDDR domain during power-down mode. The chip provides ultra-high speed, high

Three operating modes of high speed and ultra low speed, three low power consumption modes of sleep, stop and power down.

The power voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), and programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the reset action of the chip by detecting the VCC voltage.

PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 passed

Detect VCC voltage or external input detection voltage, and generate reset or interrupt according to register selection.

After the chip enters the power-down mode, the VDDR area can maintain power through RLDO to ensure that the real-time clock module (RTC), wake-up timer

(WKTM) can continue to operate and keep the data of 4KB low-power SRAM (Ret-SRAM). The analog module is equipped with a dedicated power supply

pin, which improves analog performance.

1.4.6 Initial Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_041F (where

0x0000_0408~0x0000_041F is a reserved function address, the 24byte address needs to be set by the user to all 1s to ensure that the chip operates normally) to load data into the initialization configuration register, the user needs to program or erase FLASH sector 0 to modify the initialization configuration set register.

1.4.7 Embedded FLASH interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE and MCODE buses, and this interface can execute the programming of the FLASH

program, sector erase, and full erase operations; code execution is accelerated through instruction prefetch and cache mechanisms.

Main features:

- ÿ Maximum 512KByte FLASH space
- ÿ I-CODE bus 16Byte prefetch value
- ÿ Shared 64 buffers (1Kbyte) on I-CODE and D-CODE buses
- ÿ Provide 960Bbyte one-time programming area (OTP)
- ÿ Support low power read operation
- ÿ Support boot swap function
- ÿ Support security protection and data encryption*1

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window

1.4.8 Built-in SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (Ret_SRAM) and 188KB system SRAM (SRAMH/SRAM1/

SRAM2/SRAM3...)

SRAM can be accessed as bytes, halfwords (16 bits), or fullwords (32 bits). Read and write operations are performed at CPU speed, insertable wait cycles

Expect.

Ret_SRAM can provide 4KB of data holding space in Power down mode.

SRAM3 has ECC check (Error Checking and Correcting). ECC check is one-check-two code, that is, it can correct one bit error and check two bit errors; SRAMH/SRAM1/

SRAM2/Ret_SRAM has parity check (Even

parity check), each byte of data has a parity bit.

1.4.9 General IO (GPIO)

GPIO main features:

ÿ Each group of Port is equipped with 16 I/O Pins, which may be less than 16 according to the actual configuration

ÿ Support pull-up

ÿ Support push-pull, open-drain output mode

ÿ Support high, medium and low drive modes

ÿ Support external interrupt input

ÿ Support peripheral function multiplexing of I/O pin, each I/O pin can have up to 16 selectable multiplexing functions, and some I/O can have up to

64 functions selectable

ÿ Each I/O pin can be programmed independently

Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The function of the interrupt controller (INTC) is to select the interrupt event request as an interrupt input to the NVIC to wake up the WFI; as an event input,

Wake up the WFE. Select interrupt event request as wake-up condition for low-power modes (sleep mode and stop mode); external pins NMI and

Interrupt control function of EIRQ; interrupt/event selection function of software interrupt.

Main Specifications:

1) NVIC interrupt vector: Please refer to the user manual for the actual number of interrupt vectors used (excluding the 16 interrupt lines of Cortex™-M4F), each

interrupt vector can select the corresponding peripheral interrupt event request according to the interrupt selection register. For more descriptions about

exceptions and NVIC programming, please refer to Chapter 5: Exceptions and

Chapter 8: Nested Vectored Interrupt Controller.

2) Programmable priority levels: 16 programmable priority levels (using 4-bit interrupt priority levels).

3) Non-maskable interrupt: In addition to the NMI pin as a non-maskable interrupt source, multiple system interrupt event requests can be independently selected

As a non-maskable interrupt, each interrupt event request is equipped with independent enable selection, pending, and clearing pending registers.

- 4) Equipped with 16 external pin interrupts.
- 5) Configure various peripheral interrupt event requests, please refer to the list of interrupt event request numbers for details.
- 6) Equipped with 32 software interrupt event requests.
- 7) Interrupts can wake up the system from sleep mode and stop mode.

1.4.11 Automatic Operating System (AOS)

The automatic operation system (Automatic Operation System) is used to realize the linkage between the peripheral hardware circuits without the help of the CPU. Use events generated by peripheral circuits as AOS source (AOS Source), such as timer comparison match, timing Overflow, periodic signal of RTC, various states of sending and receiving data of the communication module (idle, full of receiving data, end of sending data, sending Data empty), ADC conversion end, etc., to trigger other peripheral circuit actions. The triggered peripheral circuit action is called AOS target (AOS Target).

1.4.12 Keyboard scan (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, column It is driven by an independent scan output KEYOUT_m (m=0~7), and the row KEYIN_n (n=0~15) is used as EIRQ_n (n=0~15) input is detected. This module realizes the key recognition function through the line scan query method.

1.4.13 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, which can improve the security of the system by preventing unauthorized access.

This product has built-in four MPU units for host and one MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA read and write access control to the entire 4G address space.

When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IP MPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between the memory and the peripheral function module, and can realize the storage between the memory without the participation of the CPU.

Data exchange between the controller and peripheral function modules and between peripheral function modules.

ÿ The DMA bus is independent of the CPU bus, and is transmitted according to the AMBA AHB-Lite bus protocol

ÿ With 8 independent channels (4 channels for DMA_1 and DMA_2), different DMA transfer functions can be operated independently

ÿ The start request source of each channel is configured through an independent trigger source selection register

ÿ One block of data is transferred per request

ÿ The minimum data block is 1 data, and the maximum can be 1024 data

- ÿ Each data can be configured as 8bit, 16bit or 32bit
- ÿ A maximum of 65535 transfers can be configured
- ÿ The source address and target address can be independently configured as fixed, self-incrementing, self-decreasing, looping or jumping with a specified offset
- ÿ Three types of interrupts can be generated, block transfer complete interrupt, transfer complete interrupt, transfer error interrupt. Each interrupt can be configured whether to screen shield. Among them, the block transmission is completed, and the transmission completion can be used as an event output, which can be used as the trigger source output of other peripheral modules with hardware trigger function.
- enter
- ÿ Support chain transmission function, which can realize the transmission of multiple data blocks at a time
- ÿ Support channel reset triggered by external events
- ÿ When not in use, it can be set to enter the module stop state to reduce power consumption

1.4.15 Comparator (CMP)

CMP is a peripheral module that compares two analog voltages INP and INM and outputs the comparison result. CMP has 3 independent ratios

There are 4 input sources for the analog voltages INP and INM of each comparison channel. An INP and a

The INM performs a single comparison, and multiple INPs can also be scanned against the same INM. The comparison result can be read through the register,

It can also be output to external pins, and can also generate interrupts and events.

1.4.16 Analog-to-Digital Converter (ADC)

A 12-bit ADC is an analog-to-digital converter that uses successive approximation. It has a maximum of 16 analog input channels, which can convert

external ports and internal analog signals. These channels can be arbitrarily combined into a sequence for scan-by-scan conversion, and the sequence can be

times, or consecutive scan conversions. It supports multiple consecutive conversions on any specified channel and averages the conversion results. ADC module

It is also equipped with an analog watchdog function to monitor the conversion result of any specified channel and detect whether it exceeds the threshold set by the user.

ADC main features:

ÿ High performance

- Configurable 12-bit, 10-bit and 8-bit resolution

- The frequency ratio of peripheral clock PCLK4 and A/D conversion clock ADCLK can be selected:

· PCLK4ÿADCLK=1ÿ1ÿ2ÿ1ÿ4ÿ1ÿ8ÿ1ÿ1ÿ2ÿ1ÿ

ADCLK can be selected as a PLL asynchronous to the system clock HCLK, at this time the clock sources of PCLK4 and ADCLK are fixed at the same time

Set as PLL, and the frequency ratio is 1:1, the original frequency division setting is invalid

- 2MSPS (PCLK4=ADCLK=60MHz, 12 bits, sampling 17 cycles)

- Independent programming of sampling time for each channel

- Separate data registers for each channel

- Data register configurable data alignment

- Consecutive multiple conversion average function

- Analog watchdog to monitor conversion results

- The ADC module can be set to stop when not in use
- ÿ Analog input channel
 - Maximum 16 external analog input channels
 - 1 internal voltage reference
- ÿ Conversion start condition
 - Software setting conversion starts
 - Peripherals synchronously trigger conversion start
 - External pin trigger conversion start
- ÿ Conversion mode
 - 2 scan sequences A, B, single or multiple channels can be specified arbitrarily
 - Sequence A single scan
 - Sequence A continuous scan
 - Dual sequence scanning, sequence A and B independently select the trigger source, sequence B has a higher priority than A
 - Synchronous mode (for devices with two or three ADCs)
- ÿ Interrupt and event signal output
 - Sequence A scan end interrupt EOCA_INT and event EOCA_EVENT
 - End of sequence B-scan interrupt EOCB_INT and event EOCB_EVENT
 - Analog watchdog channel compare interrupt CHCMP_INT and event CHCMP_EVENT, sequence compare interrupt SEQCMP_INT and event SEQCMP_EVENT
 - All 4 events above can start DMA

1.4.17 Temperature Sensor (OTS)

OTS can obtain the temperature inside the chip to support the reliable operation of the system. After using software or hardware trigger to start temperature measurement, OTS

Provide a set of digital quantities related to temperature, and the temperature value can be calculated through the calculation formula.

1.4.18 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can be used to count and generate different forms of time

Clock waveform, output for external use. The timer supports two waveform modes of triangle wave and sawtooth wave, which can generate various PWM waveforms;

Between elements, software synchronous counting and hardware synchronous counting can be realized; each reference value register supports cache function; supports 2-phase quadrature encoding and 3-phase

Orthogonal encoding; supports EMB control. Three units of Timer6 are installed in this series.

1.4.19 General Control Timer (Timer4)

General-purpose control Timer 4 (Timer4) is a timer module for three-phase motor control, providing a variety of three-phase motors for different applications

Control plan. The timer supports two waveform modes of triangle wave and sawtooth wave, and can generate various PWM waveforms; supports buffer function; supports

EMB control. Three units of Timer4 are installed in this series.

1.4.20 Emergency Brake Module (EMB)

The emergency brake module is a functional module that notifies the timer when certain conditions are met, so that the timer stops outputting PWM signals to the external motor.

The following events are used to generate notifications:

- ÿ External port input level change
- ÿ PWM output port levels are in phase (same high or same low)
- ÿ Voltage comparator comparison result
- ÿ The external oscillator stops oscillating
- ÿ Write register software control

1.4.21 General-purpose timer (TimerA)

General-purpose Timer A (TimerA) is a timer with 16-bit count width and 8 PWM outputs. The timer supports triangular

Wave and sawtooth wave two waveform modes, can generate various PWM waveforms; support software synchronous start counting; comparison reference value register supports buffering

Memory function; support 2-phase quadrature code counting and 3-phase quadrature code counting. This series of products is equipped with 6 units TimerA, the largest real

Now there are 48 PWM outputs.

1.4.22 General purpose timer (Timer0)

General-purpose timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2

channels that can generate compare match events during counting. This event can trigger an interrupt, and can also be used as an event output to control other modules

wait. Two units of Timer0 are installed in this series.

1.4.23 Real Time Clock (RTC)

A real-time clock (RTC) is a counter that holds time information in BCD format. Record the specific calendar from 00 to 99

time. Supports 12/24 hour time format, and automatically calculates the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

1.4.24 Watchdog Counter (WDT)

There are two watchdog counters, one is a dedicated watchdog counter whose counting clock source is a dedicated internal RC (WDTCLK: 10KHz)

(SWDT), and the other is a general-purpose watchdog counter (WDT) whose count clock source is PCLK3. Dedicated Watchdog and General Watchdog are

16-bit down counter, used to monitor the deviation from the normal operation of the application program due to external disturbances or unforeseen logic conditions

A software failure occurred.

Both watchdogs support window functions. The window interval can be preset before the count starts, and the counter can be refreshed when the count value is within the window interval.

Counting restarts.

1.4.25 Serial communication interface (USART)

This product is equipped with 4 units of serial communication interface module (USART). The serial communication interface module (USART) can flexibly communicate with external devices. The device performs full-duplex data exchange; this USART supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, intelligent card interface (ISO/IEC7816-3). Support modem operation (CTS/RTS operation), multiprocessor operation.

1.4.26 Integrated Circuit Bus (I2C)

This product is equipped with integrated circuit bus (I2C) 3 units. I2C is used as an interface between the microcontroller and the I2C serial bus. Provide more The master mode function can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported.

1.4.27 Serial Peripheral Interface (SPI)

This product is equipped with 4-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data communication with peripheral devices. According to the exchange. Users can set three-wire/four-wire, master/slave and baud rate range according to their needs.

1.4.28 Quad-wire Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. communication. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.29 Integrated Circuit Built-in Audio Bus (I2S)

I2S (Inter_IC Sound Bus), integrated circuit built-in audio bus, which is dedicated to data transmission between audio devices.

This product is equipped with 4 I2S and has the following features.

Function	main features
way of communication	<ul style="list-style-type: none"> · Support full-duplex and half-duplex communication · Support master mode or slave mode operation
Data Format	<ul style="list-style-type: none"> Optional channel length: 16/32 bits Optional transfer data length: 16/24/32 bits · Data shift sequence: MSB start
baud rate	<ul style="list-style-type: none"> 8-bit programmable linear prescaler for precise audio sampling frequency · Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k <p>Can output driving clock to drive external audio components, the ratio is fixed at 256*Fs (Fs is the audio sampling frequency)</p>
Support I2S protocol	<ul style="list-style-type: none"> · I2S Philips standard · MSB alignment standard · LSB alignment standard · PCM standard
data buffer	<ul style="list-style-type: none"> · With 2 words deep, 32-bit wide input and output FIFO buffer area
clock source	<ul style="list-style-type: none"> Can use the internal I2SCLK (UPLL/R/UPLLQ/UPLL/PPLL/R/PPLLQ/MPLL/PMLLP); External clock on I2S_EXCK pin provides
to interrupt	<ul style="list-style-type: none"> Generate an interrupt when the effective space of the send buffer reaches the alarm threshold Generate an interrupt when the effective space of the receive buffer reaches the alarm threshold · The receive data area is full and there is still a request to write data, and the receive overflows · The sending data area is empty and there is still sending request, sending underflow The send data area is full and there is still a request to write data, and the send overflows

1.4.30 CAN communication interface (CAN)

This product is equipped with a CAN communication interface module (CAN), and is equipped with 512Byte RAM for storing sending/receiving messages for CAN. It supports CAN2.0B protocol stipulated in ISO11898-1 and TTCAN protocol stipulated in ISO11898-4.

1.4.31 USB2.0 Full Speed Module (USB FS)

This product is equipped with one unit of USB2.0 full-speed module (USB FS), and built-in full-speed PHY on chip. USB FS is a dual-role

(DRD) controller that supports both slave and master functions. In host mode, USB FS supports full-speed and low-speed transceivers, while slave

Only full-speed transceivers are supported in machine mode.

The USB FS module equipped with this product can generate SOF tokens successfully in host mode or receive SOF tokens in slave mode.

A SOF event occurs.

1.4.32 Cryptographic Coprocessing Module (CPM)

Encryption co-processing module (CPM) includes AES encryption and decryption algorithm processor, HASH secure hash algorithm, TRNG true random number generator

Three submodules.

The AES encryption and decryption algorithm processor follows the standard data encryption and decryption standards, and can realize encryption and decryption operations with a key length of 128 bits.

Calculate.

HASH The secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the

The national standard "FIPS PUB 180-3" issued by the Bureau of Standards and Technology can generate 256 bits for messages whose length does not exceed 2^64 bits bit message digest output.

TRNG True Random Number Generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Computing Unit (DCU)

Data Computing Unit (Data Computing Unit) is a simple data processing module without the help of CPU. Each DCU unit has 3 data registers, which can add, subtract and compare the size of 2 data, as well as the window comparison function. This product is equipped with 4 Each DCU unit can complete its own function independently.

1.4.34 CRC Calculation Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC13239, using 32-bit and 16-bit CRC respectively. The generation of CRC32 is more

The term is $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$. The generator polynomial of CRC16 is

$X^{16}+X^{12}+X^5+1$

1.4.35 SDIO Controller (SDIOC)

The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has 2 SDIO controllers, each SDIO controller

Each controller provides a host interface for SD card supporting SD2.0 protocol, SDIO device and supporting eMMC4.51 protocol

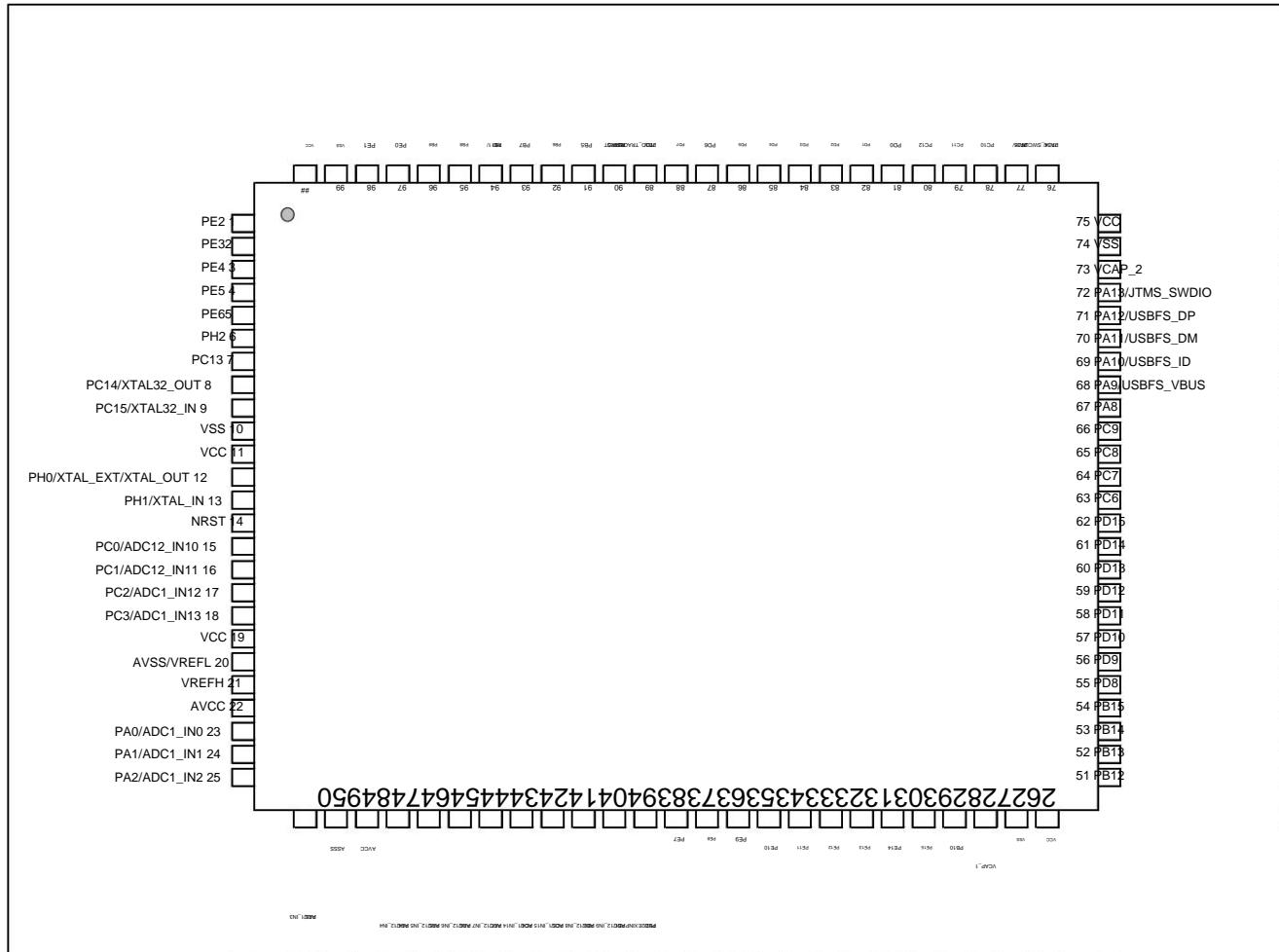
communicate with the proposed MMC device. The characteristics of SDIOC are as follows:

- ÿ Support SDSC, SDHC, SDXC format SD card and SDIO device
- ÿ Support one-line (1bit) and four-wire (4bit) SD bus
- ÿ Support one-wire (1bit), four-wire (4bit) and eight-wire (8bit) MMC bus
- ÿ With card identification and hardware write protection function

2 Pin configuration and function (Pinouts)

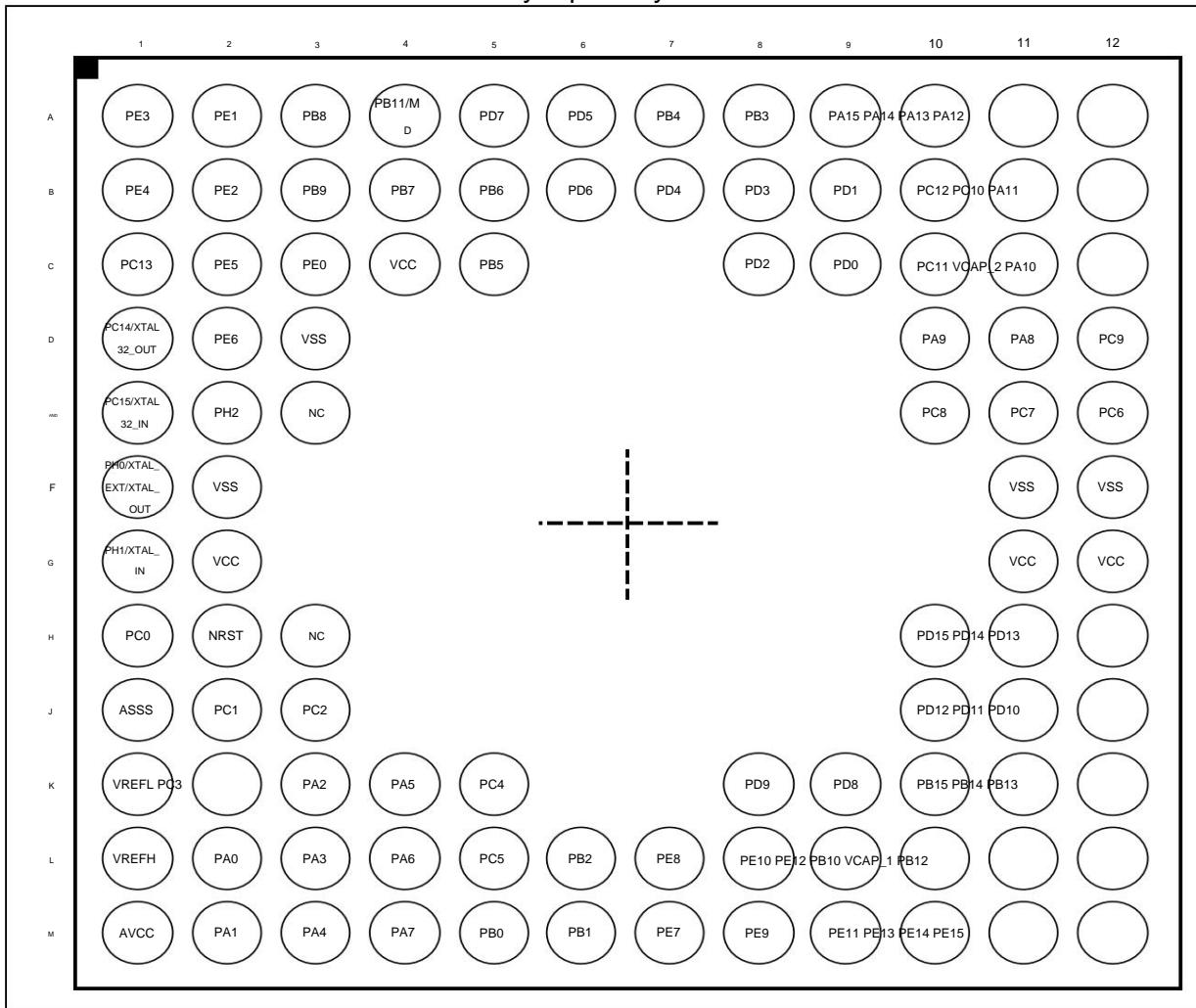
2.1 Pin Configuration Diagram

HC32F460PETB-LQFP100 / HC32F460PCTB-LQFP100



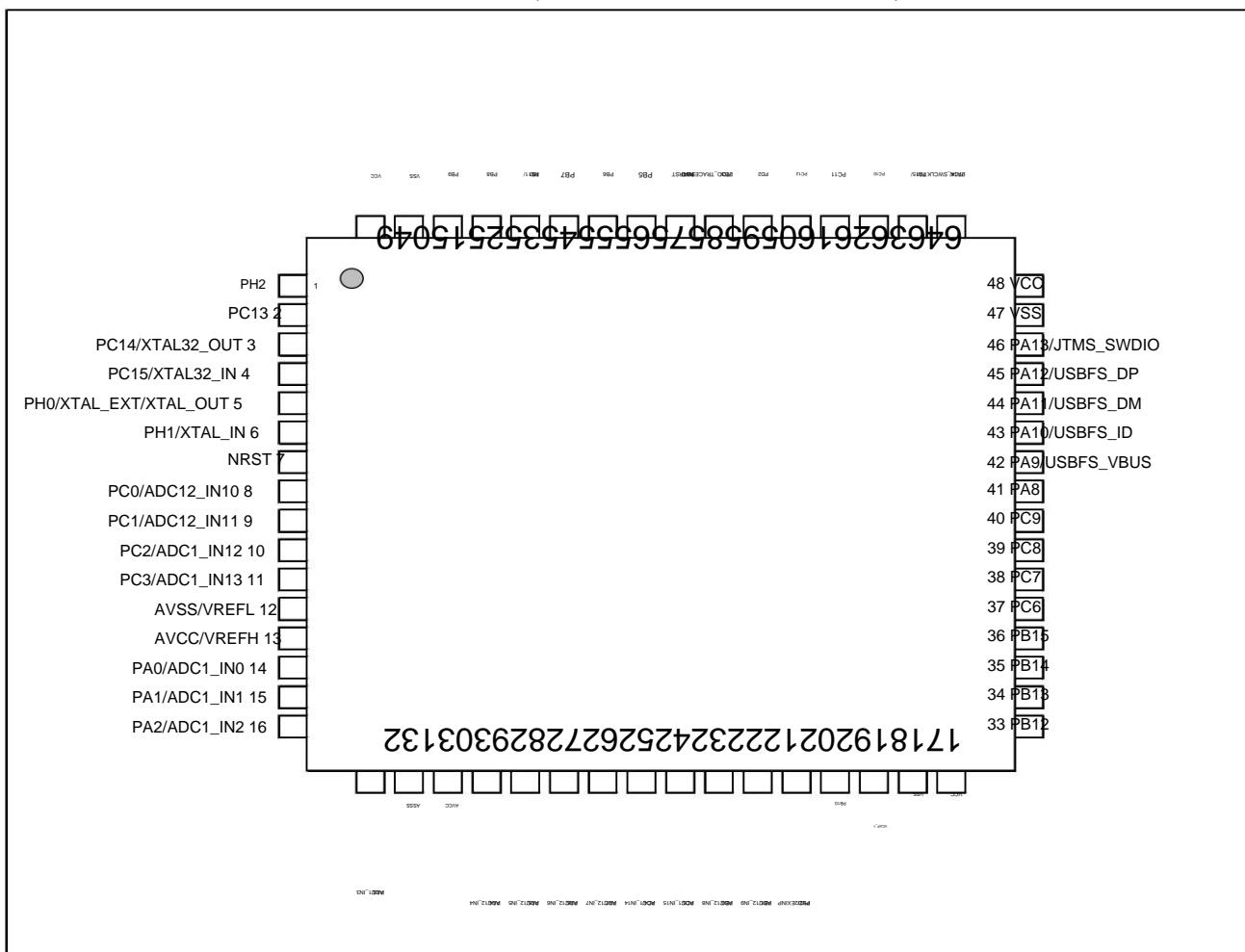
HC32F460PEHB-VFBGA100

Top View

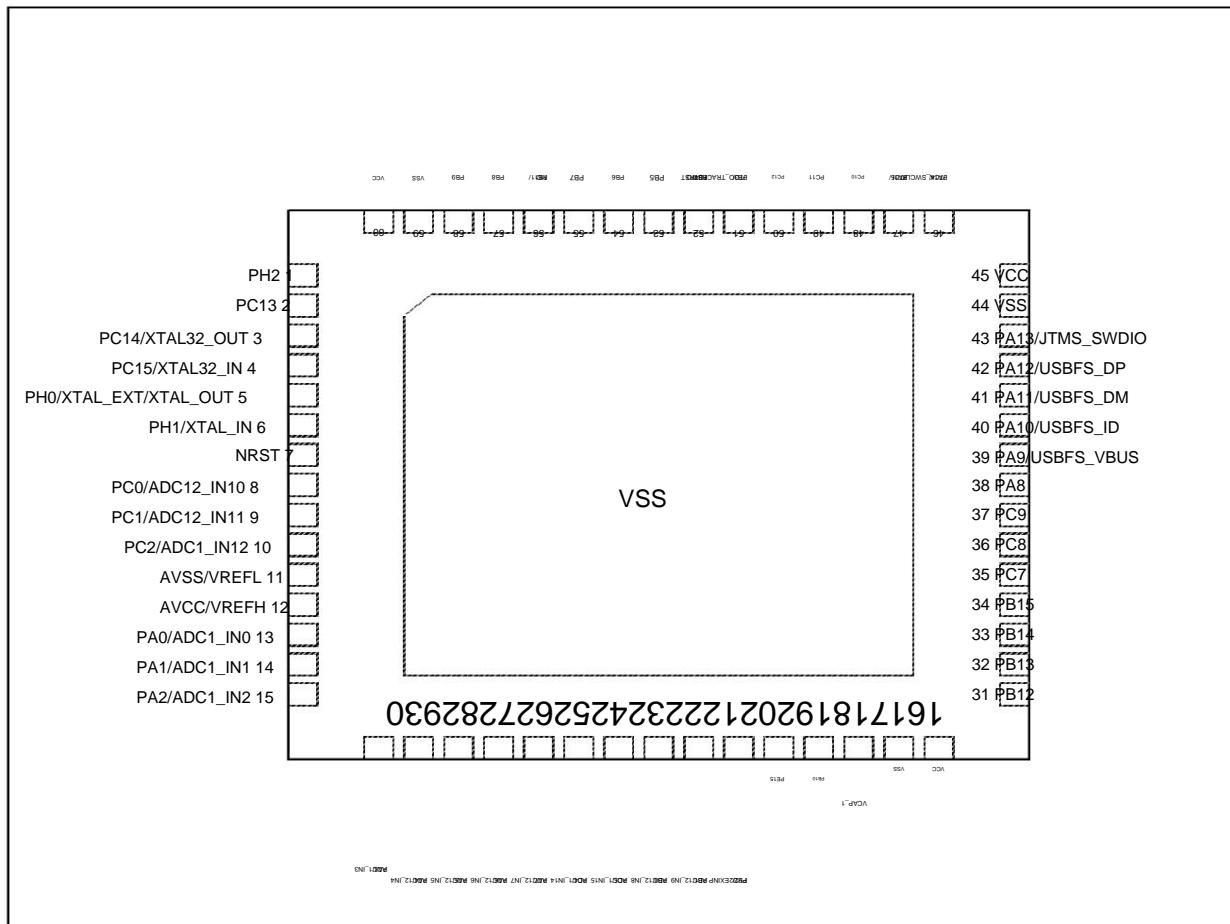


Note: A1 is Pin 1.

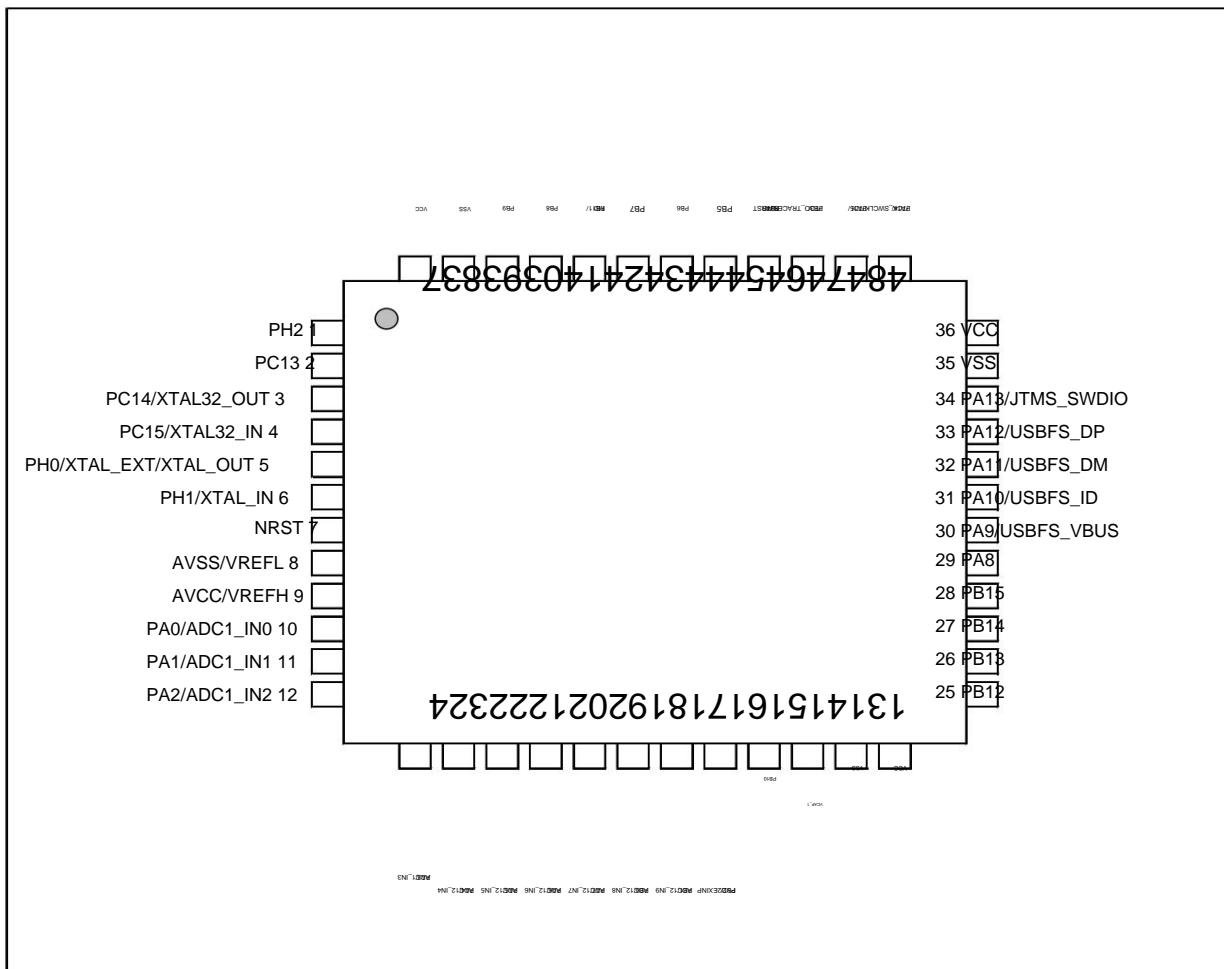
HC32F460KETA-LQFP64/ HC32F460KCTA-LQFP64



HC32F460KEUA-QFN60TR



HC32F460JETA-LQFP48 / HC32F460JCTA-LQFP48



HC32F460JEUA-QFN48TR

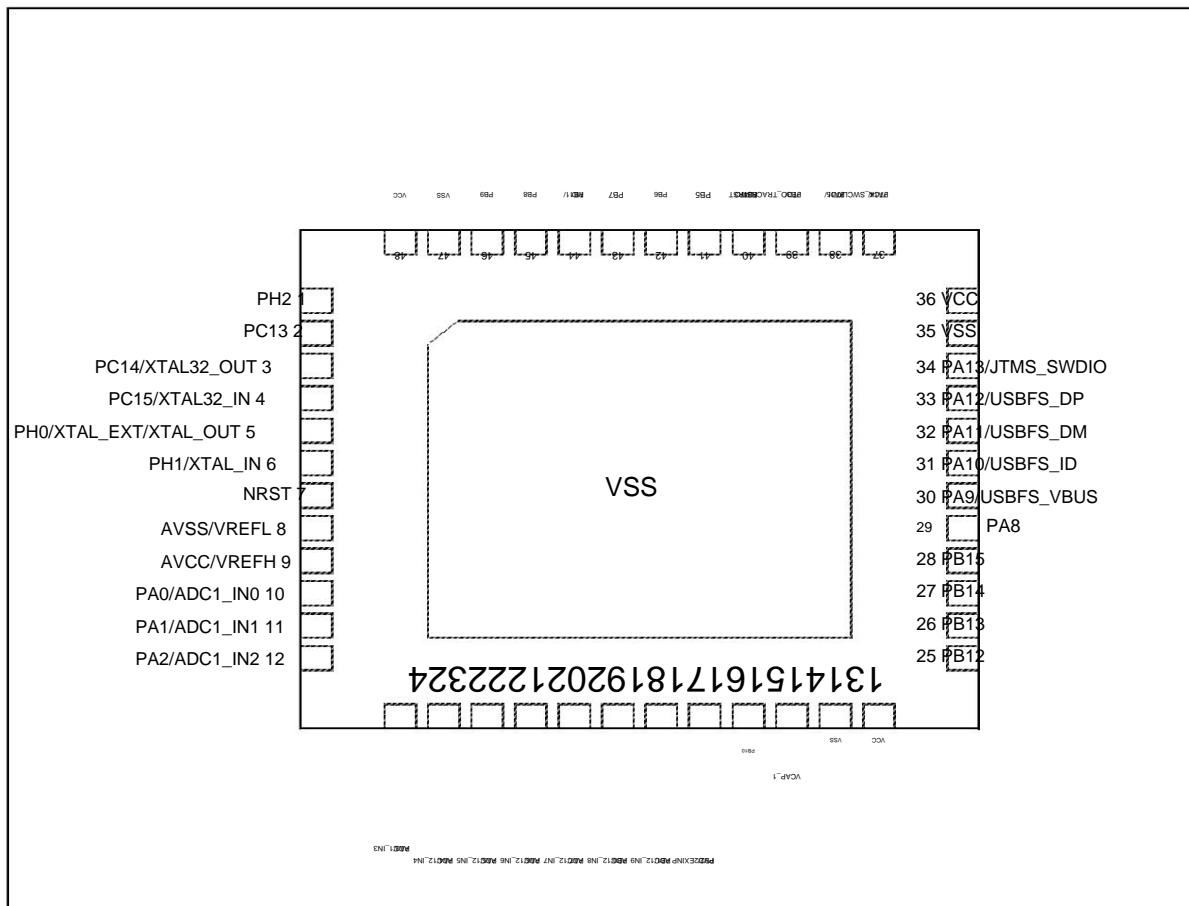


Figure 2-1 Pin configuration diagram

2.2 Pin function table

Table 2-1 Pin Function Table

LQFP100 VFBGA100 LQFP64 QFN60 LQFP/QFN48		Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14			Function 15	Func16~31	Func32~63	
GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TIMA	USART/SPV/QSPI KEY	SDIO	USBFS/I2S	-	-	EVNTPT	EVENTOUT-		Communication Funcs											
1	B2	PE2		EIRQ2	TRACECK	GPO			TIMA_3_PWM5			USART3_CK											EVENTOUT		Func_Grp2	
2	A1	PE3		EIRQ3	TRACED0	GPO			TIMA_3_PWM6			USART4_CK											EVENTOUT		Func_Grp2	
3	B1	PE4		EIRQ4	TRACED1	GPO			TIMA_3_PWM7														EVENTOUT		Func_Grp2	
4	C2	PE5		EIRQ5	TRACED2	GPO			TIMA_3_PWM8														EVENTOUT		Func_Grp2	
5	D2	PE6		EIRQ6	TRACED3	GPO																	EVENTOUT		Func_Grp2	
6	E2	1	1	1	PH2		GPO	FCMREF	TIM4_2_CLK		TIMA_4_PWM7		EMB_IN4			SDIO2_D4_I2S3_EXCK							EVENTOUT		Func_Grp2	
7	C1	2	2	2	PC13		EIRQ13		GPO	RTC_OUT		TIMA_4_PWM8				SDIO2_CK_I2S3_MCK							EVNTP313		Func_Grp2	
8	D1	3	3	3	PC14	XTAL32_OUT	EIRQ14		GPO		TIMA_4_PWM5												EVNTP314			
9	E1	4	4	4	PC15	XTAL32_IN	EIRQ15		GPO		TIMA_4_PWM6												EVNTP315			
10	F2			VSS																						
11	G2			VCC																						
12	F1	5	5	5	PH0	XTAL_EXT/XTAL_OUT	EIRQ0		GPO			TIMA_5_PWM3														
13	G1	6	6	6	PH1	XTAL_IN	EIRQ1		GPO			TIMA_5_PWM4														
14	H2	7	7	7	NRST																					
15	H1	8	8	PC0	ADC12_IN10/CMP3_INP3	EIRQ0		GPO		TIMA_2_PWM5						SDIO2_D5							EVNTP300_EVENTOUT		Func_Grp1	
16	J2	9	9	PC1	ADC12_IN11	EIRQ1		GPO		TIMA_2_PWM6						SDIO2_D6							EVNTP301_EVENTOUT		Func_Grp1	
17	J3	10	10	PC2	ADC1_IN12	EIRQ2		GPO		TIMA_2_PWM7			EMB_IN3			SDIO2_D7							EVNTP302_EVENTOUT		Func_Grp1	
18	K2	11		PC3	ADC1_IN13/CMP1_INM2	EIRQ3		GPO		TIMA_2_PWM8						SDIO1_WP							EVNTP303_EVENTOUT		Func_Grp1	
19				VCC																						
20	J1	12	11	8	ASSS																					
	K1			VREFL																						
21	L1			VREFH																						
22	M1	13	12	9	AVCC																					
23	L2	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0		GPO	TIM4_2_OUH		TIMA_2_PWM1/TIMA_2_CLKA		TIMA_2_TRIG SPI1_SS1		SDIO2_D4							EVNTP100_EVENTOUT		Func_Grp1	
24	M2	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1		GPO	TIM4_2_OUL		TIMA_2_PWM2/TIMA_2_CLKB TIMA_3_TRIG			SP1_SS2	SDIO2_D5							EVNTP101_EVENTOUT		Func_Grp1	
25	K3	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2		GPO	TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA	SP1_SS3	SDIO2_D6								EVNTP102_EVENTOUT		Func_Grp1	
26	L3	17	16	13	PA3	ADC1_IN3/PGAVSS/CMP1_INP4	EIRQ3		GPO	TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB				SDIO2_D7							EVNTP103_EVENTOUT		Func_Grp1
27		18		ASSS																						
	E3			NC																						
28		19		AVCC																						
29	M3	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4		GPO	TIM4_2_OWH		TIMA_3_PWM5		USART2_CK	KEYOUT0	I2S1_EXCK							EVNTP104_EVENTOUT		Func_Grp1	
30	K4	21	18	15	PA5	ADC12_INS/CMP2_INP2	EIRQ5		GPO	TIM4_2_OWL		TIMA_2_PWM1/TIMA_2_CLKA TIMA_3_PWM6		TEAM_2_TRIG	KEYOUT1	I2S1_MCK							EVNTP105_EVENTOUT		Func_Grp1	
31	L4	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6		GPO				TIMA_3_PWM1/TIMA_3_CLKA EMB_IN2			KEYOUT2 SDIO1_CMD							EVNTP106_EVENTOUT		Func_Grp1	
32	M4	23	20	17	PA7	ADC12_IN7/CMP1_INN1/CMP2_INN1/CMP3_INN1	EIRQ7		GPO	TIM4_1_OUL TIM6_1_PWM TIMA_1_PWM5		TIMA_3_PWM2/TIMA_3_CLKB EMB_IN3			KEYOUT3 SDIO2_WP							EVNTP107_EVENTOUT		Func_Grp1		
33	K5	24	21		PC4	ADC1_IN14/CMP2_INM2	EIRQ4		GPO	TIM4_2_OUH		TIMA_3_PWM7		USART1_CK	SDIO1_CD							EVNTP104_EVENTOUT		Func_Grp1		
34	L5	25	22		PC5	ADC1_IN15/CMP3_INM2	EIRQ5		GPO	TIM4_2_OUL		TIMA_3_PWM8			SDIO2_CMD							EVNTP105_EVENTOUT		Func_Grp1		
35	M5	26	23	18	PB0	ADC12_IN8/CMP3_INP1	EIRQ0		GPO	TIM4_1_OVL TIM6_2_PWM TIMA_1_PWM6		TIMA_3_PWM3		USART4_CK	KEYOUT4 SDIO2_CMD							EVNTP200_EVENTOUT		Func_Grp1		
36	M6	27	24	19	PB1	ADC12_IN9/CMP3_INP2	EIRQ1/WKUP0_1		GPO	TIM4_1_OWL TIM6_3_PWM TIMA_1_PWM7		TIMA_3_PWM4		QSPI_QSN	KEYOUT5 SDIO2_D3_I2S2_EXCK							EVNTP201_EVENTOUT		Func_Grp1		
37	L6	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_2		GPO	VCOUT123		TIM6_TRIGGER TIMA_1_TRIGGER		EMB_IN1	QSPI_QSOI3	SDIO2_D2_I2S2_MCK							EVNTP202_EVENTOUT		Func_Grp1	
38	M7			PE7			EIRQ7		GPO	ADTRG1		TIM6_TRIGGER TIMA_1_TRIGGER		USART1_CK								EVENTOUT				
39	L7			PE8			EIRQ8		GPO		TIM4_1_OUL TIM6_1_PWM TIMA_1_PWM5											EVENTOUT				
40	M8			PE9			EIRQ9		GPO		TIM4_1_OUH TIM6_1_PWM TIMA_1_PWM6	TIMA_1_CLKA										EVENTOUT				
41	L8			PE10			EIRQ10		GPO		TIM4_1_OVL TIM6_2_PWM TIMA_1_PWM6											EVENTOUT				
42	M9																									

Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16~31	Func32~63
				GPO	other	TIM4	TIM6	TEAM	TEAM	EML,TIMA	USART/SPI/QSPI KEY		SDIO	USBFS/I2S		-	EVNTPT	EVENTOUT -		Communication Funcs		
96 B3	62	58	46	PB9		EIRQ9		GPO	TIM4_3_OUH		TIMA_4_PWM4	TEAM_6_TRIG		SPI2_SS1	KEYOUT6 SDIO1_D5				EVNTP209 EVENTOUT		Func_Grp2	
97 C3				PE0		EIRQ0		GPO	MCO_1		TEAM_4_TRIG			SPI2_SS2					EVENTOUT		Func_Grp2	
98 A2				PE1		EIRQ1		GPO	MCO_2	TIM4_3_CLK				SPI2_SS3					EVENTOUT		Func_Grp2	
99 D3	63	59	47	VSS																		
100 C4	64	60	48	VCC																		
H3			-	NC																		

Note:

- In the above table, there are 64 pins that support the function selection of Func32~63. Func32~63 are mainly for serial communication functions (including USART, SPI, I2C, I2S, CAN), which are divided into two groups, Func_Grp1 and Func_Grp2. Please refer to Table 2-2 for details.

Table 2-2 Func32~63 table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	I work 47
Func_Grp1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK	
Func_Grp2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK	
	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table 2-3 Port configuration

Package	Port Group	Bits															Pin Count Total
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LQFP100	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
VFBGA100	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	Door	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortH	---	---	---	---	---	---	---	---	---	---	---	---	---	---	0 0 0 3	
LQFP64	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortD	---	---	---	---	---	---	---	---	---	---	---	---	---	0 -	1	
	PortH	---	---	---	---	---	---	---	---	---	---	---	---	---	0 0 0 3		
QFN60	Brings	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	- yes -	---	---	---	---	---	---	0 0 0 14		
	Door	---	---	---	---	---	---	---	---	---	---	---	---	---	0 1		
	PortH	---	---	---	---	---	---	---	---	---	---	---	---	---	0 0 0 3		
LQFP48	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
QFN48	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	-	-	-	-	-	-	-	-	-	-	-	0 0 0 3	3
	PortH	---	---	---	---	---	---	---	---	---	---	---	---	---	0 0 0 3		
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 2-4 General function specifications

Port		pull up	open drain output	Drive capacity 5V withstand voltage	remarks
Brings	PA0~PA10	support	support	Low, Medium, High Support *	
	PA13~PA15				
	PA11~PA12	support	support	Low, medium, high not supported	
PortB	PB0~PB10,	support	support	Low, medium, high supported*	
	PB12~PB15				
	PB11	support			support input only
PortC	PC0~PC15	support	support	Low, Medium, High Support*	
PortD	PD0~PD15	support	support	low, medium, high support	
Door	PE0~PE15	support	support	Low, medium, high support Low,	
PortH	PH0~PH2	support	support	medium, high support	

Note:

- When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin function description

Table 2-5 Pin function description

category	function name	I/O	illustrate
Power	VCC	I Power	
	VSS	I power ground	
	VCAP_1~2	IO core voltage	
	AVCC	I Analog power	
	ASSS	I Analog power ground	
	VREFH	I Analog reference voltage	
	VREFL	I Analog reference voltage	
System	NRST	I Reset pin, active low	
	MD	I mode pin	
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	IO External Main Clock Oscillator Interface	
	XTAL_EXT/XTAL_OUT	IO XTAL_EXT External clock input	
	XTAL32_IN	I External sub clock (32K) oscillator interface	
	XTAL32_OUT	O	
	MCO_1~2	O Internal clock output	
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO General input and output	
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I Maskable external interrupt	
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I Non-maskable external interrupt	
Event Port	EVNTPxy (x=1~4, y=0~15)		IO event port input and output function
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I In-circuit debugging interface	
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	O Trace	debug sync clock output
	TRACED0~3	O Trace	debug data output
FCM	FCMREF	I External	reference clock input for clock frequency measurement
RTC	RTCOUT	O	1Hz clock output
Timer4 (x=1~3)	TIM4_x_CLK	I Count	clock port input
	TIM4_x_OUH	IO PWM	port U-phase output

category	function name	I/O	illustrate
(x=1~5)	TIM4_x_OUL	IO PWM port U-phase output	
	TIM4_x_OVH	IO PWM port V-phase output	
	TIM4_x_OVL	IO PWM port V-phase output	
	TIM4_x_OWH	IO PWM port W phase output	
	TIM4_x_OWL	IO PWM port W phase output	
Timer6 (x=1~3)	TIM6_TRIGA	I External event triggers A input	
	TIM6_TRIGB	I External event triggers B input	
	TIM6_x_PWMA	IO external event trigger input or PWM port output	
	TIM6_x_PWMB	IO external event trigger input or PWM port output	
TimerA (x=1~6)	TEAM_x_TRIG	I External event trigger input	
	TIMA_x_PWM1/TIMA_x_CLKA	IO External event trigger input or PWM port output or count clock port input	
	TIMA_x_PWM2/TIMA_x_CLKB	IO External event trigger input or PWM port output or count clock port input	
	TIMA_x_PWMy (y=3~8)	IO external event trigger input or PWM port output	
EMB	EMB_INx (x=1~4)	I Groupx (x=1~4) port input control signal	
USARTx (x=1~4)	USARTx_TX	IO send data	
	USARTx_RX	IO receive data	
	USARTx_CK	IO communication clock	
	USARTx_RTS	O request to send a signal	
	USARTx_CTS	I clear send signal	
SPIx (x=1~4)	SPIx_MISO	IO master input/slave output data transfer pin	
	SPIx_MOSI	IO master output/slave input data transfer pin	
	SPIx_SCK	IO transfer clock	
	SPIx_SS0	IO slave select input and output pins	
	SPIx_SS1~3	O Slave select output pin	
QSPI	QSPI_QSIO0~3	IO data line	
	QSPI_QSCK	O clock output	
	QSPI_QSSN	O slave selection	
I2Cx (x=1~3)	I2Cx_SCL	IO clock line	
	I2Cx_SDA	IO data line	
I2Sx (x=1~4)	I2Sx_SD	IO serial data	
	I2Sx_SDIN	I Full-duplex serial data input	
	I2Sx_WS	IO word selection	
	I2Sx_CK	IO serial clock	
	I2Sx_EXCK	I External clock source	
	I2Sx_MCK	O master clock	
CAN	CAN_TxD	O send data	
	CAN_RxD	I receive data	
SDIOx	SDIOx_Dy (y=0~7)	IO SD data signal	

category	function name	I/O	illustrate
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signal
	SDIOx_CD	I	SD card recognition status signal
	SDIOx_WP	I	SD card write protection status signal
USBFS	USBFS_DM	IO	USBFS On-Chip Full Speed PHY D-Signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver permission signal
CMPx (x=1~3)	VCOUT1	O	Analog comparison channel 1 result output
	VCOUT2	O	Analog comparison channel 2 result output
	VCOUT3	O	Analog comparison channel 3 result output
	VCOUT123	O	Analog comparison channel 1~3 result OR output
	CMPx_INPx	I	Analog Comparator Channel x Positive Terminal Voltage y Input
	CMPx_INMy	I	Analog Comparator Channel x Negative Terminal Voltage y Input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADC1_INx (x=0~3,12~15) I		ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share the external analog input port
	PGAVS	I	PGA Ground input

2.4 Pin Usage Instructions

Table 2-6 Pin Usage Description

pin name	Instructions for use
VCC	Power supply, connected to a voltage of 1.8V~3.6V, and a decoupling capacitor connected to the VSS pin nearby (refer to electrical characteristics)
VSS	Power ground, connected to 0V
VCAP_1~2	Core voltage, connect a capacitor to the VSS pin nearby to stabilize the core voltage (refer to electrical characteristics)
AVCC	Analog power supply, supplying power to analog modules, connected to the same voltage as VCC (refer to electrical characteristics) When not using the analog module, please short it with VCC
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (refer to electrical characteristics) When not using the analog module, please short it with VSS
VREFH	Analog reference voltage of ADC1 and ADC2, connected to a voltage not higher than AVCC When not using ADC, please short it with AVCC
PB11/MD	Mode input, fixed as input state. When the reset pin (NRST) is released (from low level to high level), this pin must be fixed Set to high level. It is recommended to connect a resistor (4.7K Ω) to VCC (pull-up)
NRST	Reset pin, active low. When not in use, connect a resistor to VCC (pull up)
Pxy, x=A~E,H, y=0~15	General purpose pin. When used as an input function, the input voltage should not exceed 5V. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Leave floating when not in use, or connect a resistor to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter conditions

All voltages are referenced to VSS unless otherwise noted.

3.1.1 Minimum and maximum values

Unless otherwise specified, all device minimum and maximum values are guaranteed by design under worst-case ambient temperature, supply voltage, and clock frequency conditions or feature test guarantee.

3.1.2 Typical values

Unless otherwise specified, typical data are analyzed by design or characterization at $TA = 25^\circ\text{C}$, $VCC = 3.3\text{ V}$ get.

3.1.3 Typical curves

Unless otherwise specified, all typical curves are not tested and are for design guidance only.

3.1.4 Load capacitance

The load conditions used to measure pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin input voltage

Figure 3-1 (right) shows how to measure the input voltage at the device pins.

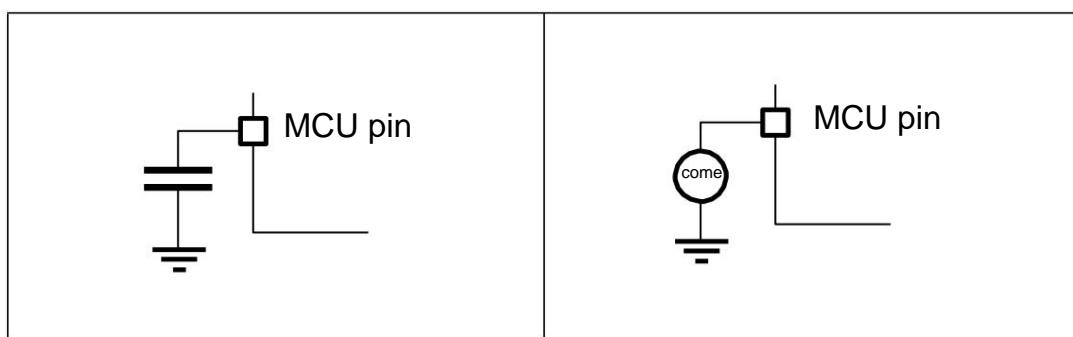


Figure 3-1 Pin load condition (left) and input voltage measurement (right)

3.1.6 Power scheme

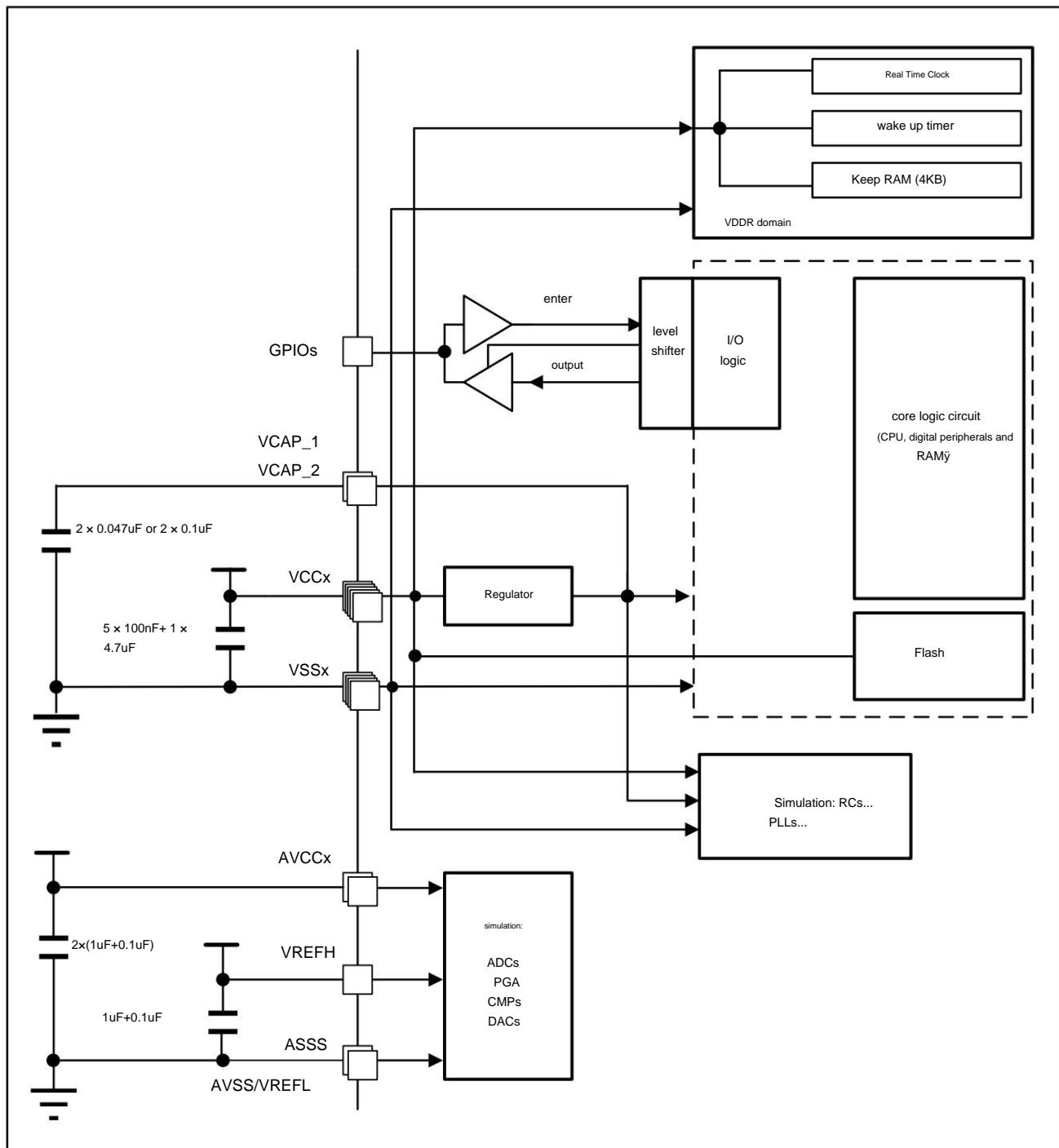


Figure 3-2 Power solution (HC32F460PETB-LQFP100, HC32F460PEHB-VFBGA100)

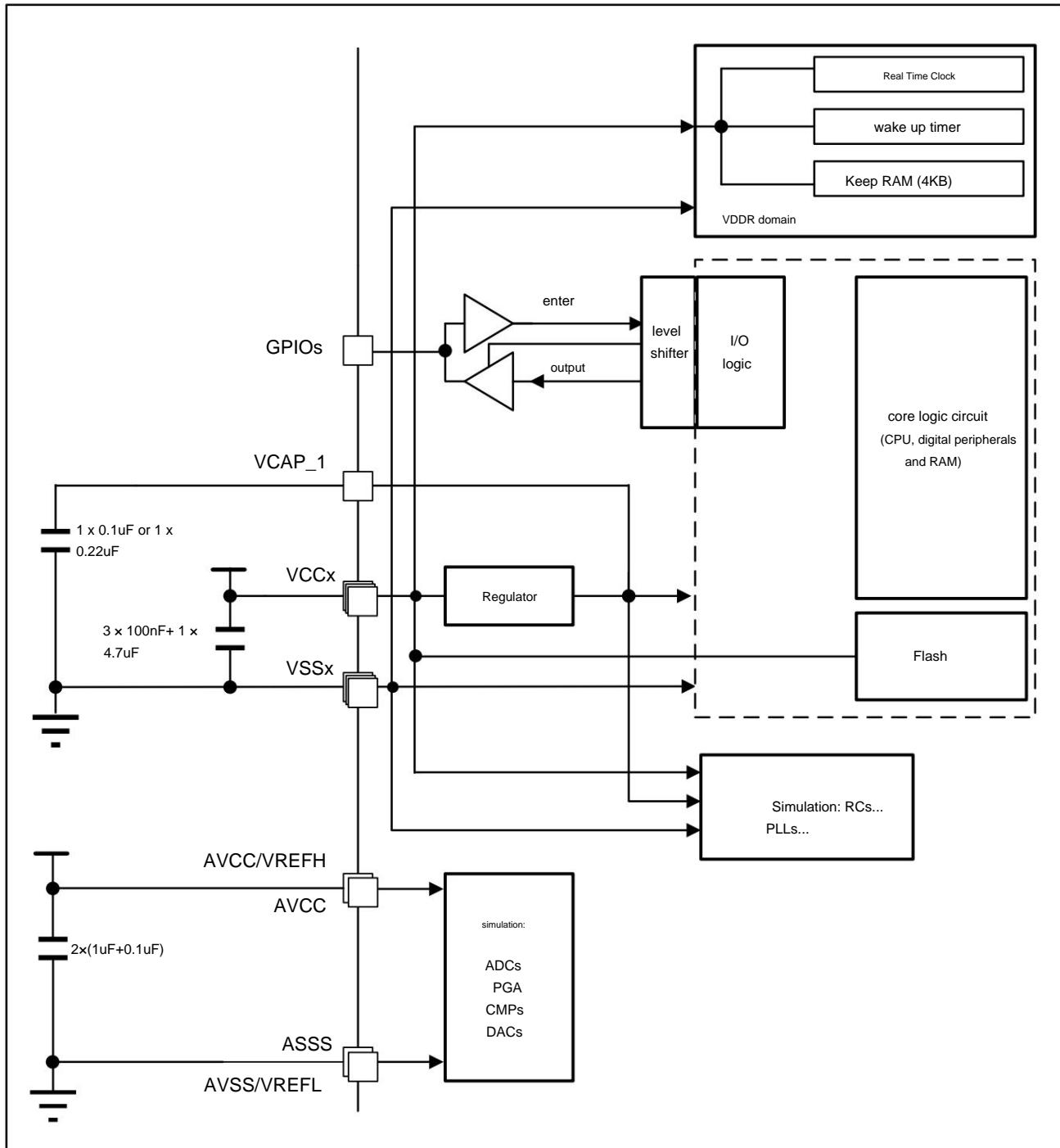


Figure 3-3 Power solution (HC32F460KETA-LQFP64)

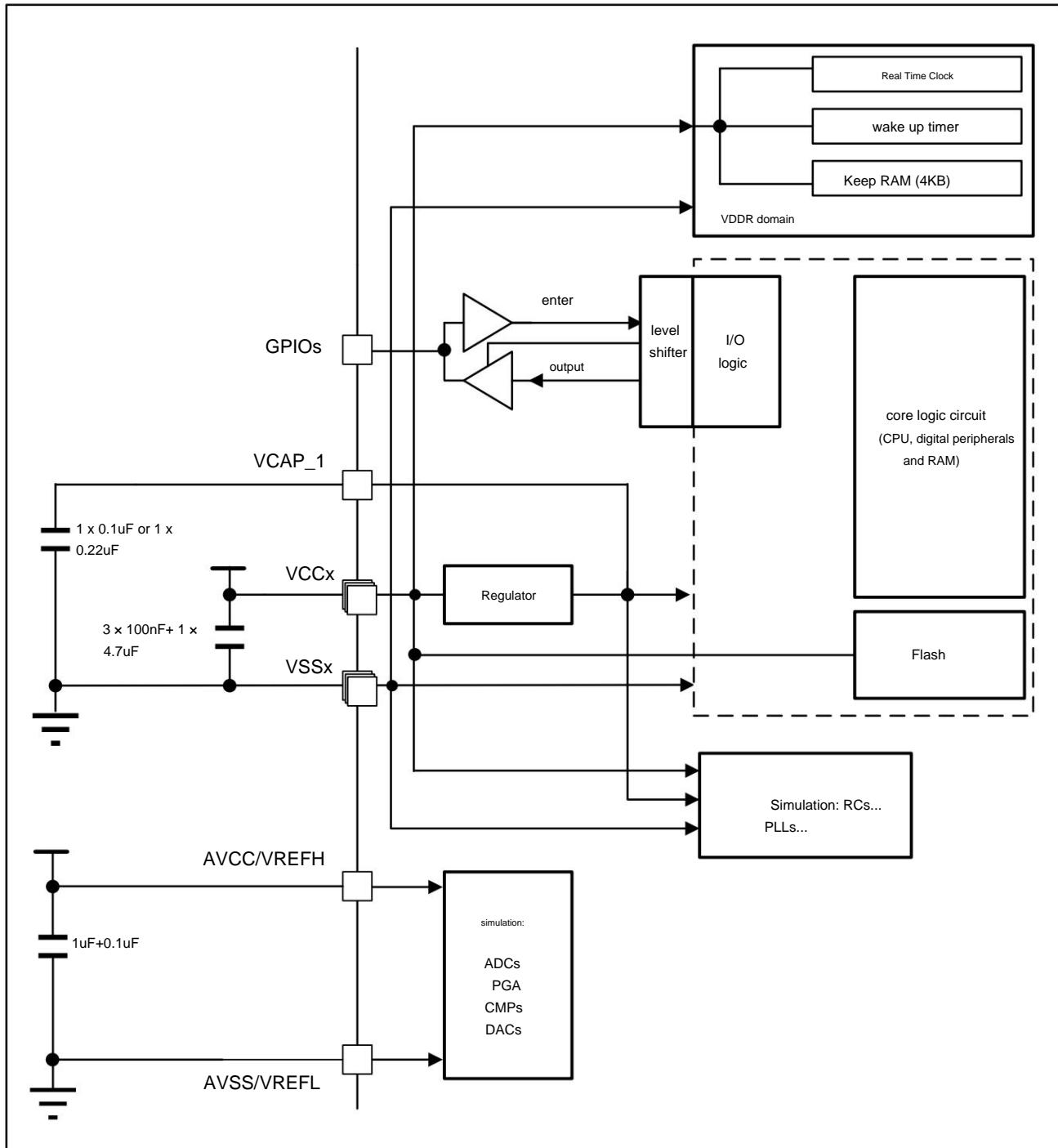


Figure 3-4 Power solution (HC32F460KEUA-QFN60TR/HC32F460JETA-LQFP48/HC32F460JEUA-QFN48TR)

1. A $4.7\mu F$ ceramic capacitor must be connected to one of the VCC pins.
2. $AVSS=VSS_y$
3. Each power supply pair (eg VCC/VSS, AVCC/AVSS...) must be decoupled with the filter ceramic capacitors mentioned above. this

These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure proper device operation. Filtering is not recommended

Capacitors to reduce PCB size or cost. This may cause the device to malfunction.

4. The capacitors used by the VCAP_1/VCAP_2 pins of the chip are as follows: 1) There are VCAP_1 and VCAP_2 pins at the same time Chip, each pin can use $0.047\mu F$ or $0.1\mu F$ capacitor (the total capacity is $0.094\mu F$ or $0.2\mu F$).

2) Chips with only VCAP_1 pins can use 0.1uF or 0.22uF capacitors. When waking up from power-down mode, the VCAP_1/VCAP_2 needs to be charged during the core voltage establishment process. On the one hand, the smaller VCAP_1/VCAP_2 The total capacity can shorten the charging time and bring fast response capability to the application; on the other hand, the larger VCAP_1/VCAP_2 Total capacity increases charging time, but also provides greater electromagnetic compatibility (EMC). Users can select according to electromagnetic compatibility and To meet the requirements of system response speed, choose a larger or smaller capacitor value. The total capacity of VCAP_1/VCAP_2 of the chip must be Matches the assignment of the PWC_PWRC3.PDTS bits. The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, you need to make sure the PWC_PWRC3.PDTS bit is cleared before entering power-down mode.

When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, it is necessary to ensure The PWC_PWRC3.PDTS bit is set.

5. The stability of the main voltage regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin,

The capacitance value CEXT is determined according to the stability requirement of the system. The capacitance value CEXT and ESR requirements are as follows:

Table 3-1 VCAP_1/VCAP_2 working conditions

symbol	parameter	condition
CEXT	The capacitance value of the external capacitor	0.047μF / 0.1μF / 0.22uF
ESR	Equivalent series resistance ESR of external capacitor	< 0.3 Ÿ

3.1.7 Current consumption measurement

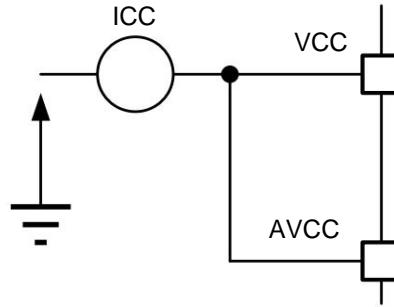


Figure 3-5 Current consumption measurement scheme

3.2 Absolute Maximum Ratings

If the load applied to the device exceeds the absolute

maximum ratings, permanent damage to the device may result. These values are stress ratings only and do not imply that the device will function properly under these conditions often. Exposure to maximum ratings for extended periods of time may affect device reliability.

Table 3-2 Voltage characteristics

symbol	project	minimum value	maximum value	unit
VCC-VSS external	main supply voltage (including AVCC, VCC)(1)	-0.3	4.0	
COME	Input voltage on 5V tolerant pin(2)	VSS-0.3	VCC+4.0 (Maximum 5.8V)	IN
	on PA11/USBFS_DM and PA12/USBFS_DP pins			
	input voltage	VSS-0.3	4.0	
VESD (HBM) electrostatic discharge voltage (human body model)	Please refer to 3.3.5 Electrical Sensitivity			-

1. To the extent allowed, all main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to

External power supply.

2. The maximum value of VIN must always be respected . See Table 3-3 for the maximum allowable injected current values.

Table 3-3 Current characteristics

symbol	project	unit of maximum	
$\dot{y}IVCC$	Total current flowing into all VCCX power lines (source current)(1)	240	
$\dot{y}IVSS$	Total current flowing (sinking) out of all VSSX ground wires (1)	-240	
IVCC	Maximum current into each VCCX supply line (source current) (1)	100	
IVSS	Maximum current (sink) out of each VSSX ground wire (1)	-100	
IIO	Output current sink for any I/O and control pin	40	mA
	Output current source for any I/O and control pin	-40	
$\dot{y}IIO$	Total output sink current on all I/O and control pins	120	
	Total output source current on all I/O and control pins	-120	

1. To the extent allowed, all main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to

External power supply.

Table 3-4 Thermal characteristics

symbol	project	value	unit
TSTG	storage temperature range	-55 to +125	°C
TJ	maximum junction temperature	125	°C

3.3 Working conditions

3.3.1 General working conditions

Table 3-5 General working conditions

symbol	parameter	condition	Min	Typ	Max	Unit		
fHCLK internal AHB clock frequency		Super Speed Mode[1] PWRC2.DVS=00 PWRC2.DDAS=1111	0	-	-	200	MHz	
		High speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	-	-	168		
		super low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	-	-	8		
VCC	Standard working voltage	-	1.8	-	-	3.6	IN	
VAVCC(2) analog working voltage	-	-	1.8	-	-	3.6		
COME	Input voltage on 5V tolerant pin (3)	2 V \leq VCC \leq 3.6 V	-0.3	-	-	5.5		
		VCC \leq 2 V	-0.3	-	-	5.2		
	PA11/USBFS_DM Input voltage of PA12/ USBFS_DP pin	-	-0.3	-	-	VCC+0.3		
TJ	Junction temperature range	-	-40	-	-	125	°C	

1. Mass production test guarantee.

2. If the VREFH pin is present, the following condition must be considered: VAVCC-VREFH < 1.2 V.

3. To keep the voltage above VCC+0.3, the internal pull-up/pull-down resistors must be disabled.

3.3.2 Operating conditions at power-on/power-off

TA is subject to general working conditions.

Table 3-6 Working conditions at power-on/power-off

symbol	parameter	minimum value	maximum value	unit
tVCC	VCC rise time rate	20	20000	μs/V
	VCC Fall Time Rate	20	20000	

3.3.3 Reset and power control module characteristics

Table 3-7 Features of reset and power control modules

symbol	parameter	condition	Min	Typ	Max	Unit
VBOR	Supervisor of BOR Measuring voltage	Super high speed mode ICG1.BOR_lev[1:0]=00	1.88	1.99	2.09	IN
		ICG1.BOR_lev [1:0]=01 1.99 2.09 2.20				IN
		ICG1.BOR_lev [1:0]=10 2.09 2.20 2.30				IN
		ICG1.BOR_lev [1:0]=11 2.30 2.40 2.51				IN
	high speed mode Ultra low speed mode	ICG1.BOR_lev[1:0]=00	1.80	1.90	2.00	IN
		ICG1.BOR_lev [1:0]=01 1.90 2.00 2.10				IN
		ICG1.BOR_lev [1:0]=10 2.00 2.10 2.20				IN
		ICG1.BOR_lev [1:0]=11 2.20 2.30 2.40				IN
		PVD1LVL[2:0]=000	1.99	2.09	2.20	IN
		PVD1LVL[2:0]=001	2.09	2.20	2.30	IN
VPVD1	PVD1 monitoring voltage(3)	PVD1LVL[2:0]=010	2.30	2.40	2.51	IN
		PVD1LVL[2:0]=011	2.54	2.67	2.79	IN
		PVD1LVL[2:0]=100	2.65	2.77	2.90	IN
		PVD1LVL[2:0]=101	2.75	2.88	3.00	IN
		PVD1LVL[2:0]=110	2.85	2.98	3.11	IN
		PVD1LVL[2:0]=111	2.96	3.08	3.21	IN
	high speed mode Ultra low speed mode	PVD1LVL[2:0]=000	1.90	2.00	2.10	IN
		PVD1LVL[2:0]=001	2.00	2.10	2.20	IN
		PVD1LVL[2:0]=010	2.20	2.30	2.40	IN
		PVD1LVL[2:0]=011	2.43	2.55	2.67	IN
		PVD1LVL[2:0]=100	2.53	2.65	2.77	IN
		PVD1LVL[2:0]=101	2.63	2.75	2.87	IN
		PVD1LVL[2:0]=110	2.73	2.85	2.97	IN
VPVD2	PVD2 monitoring voltage(3)	PVD1LVL[2:0]=111	2.83	2.95	3.07	IN
		Super high speed mode PVD2LVL[2:0]=000	2.09	2.20	2.30	IN
		PVD2LVL[2:0]=001	2.30	2.40	2.51	IN
		PVD2LVL[2:0]=010	2.54	2.67	2.79	IN

symbol	parameter	condition	Min	Typ	Max	Unit		
		PVD2LVL[2:0]=011	2.65	2.77	2.90			IN
		PVD2LVL[2:0]=100	2.75	2.88	3.00			IN
		PVD2LVL[2:0]=101	2.85	2.98	3.11			IN
		PVD2LVL[2:0]=110	2.96	3.08	3.21			IN
		PVD2LVL[2:0]=111(2)	1.05	1.15	1.25			IN
		high speed mode PVD2LVL[2:0]=000	2.00	2.10	2.20			IN
		Ultra low speed mode PVD2LVL[2:0]=001	2.20	2.30	2.40			IN
		PVD2LVL[2:0]=010	2.43	2.55	2.67			IN
		PVD2LVL[2:0]=011	2.53	2.65	2.77			IN
		PVD2LVL[2:0]=100	2.63	2.75	2.87			IN
		PVD2LVL[2:0]=101	2.73	2.85	2.97			IN
		PVD2LVL[2:0]=110 (1)	2.83	2.95	3.07			IN
		PVD2LVL[2:0]=111(2)	1.00	1.10	1.20			IN
Vpdhyt	Hysteresis for PVD1,2 (3)				100			mV
VPOR(1)	Power on/off	Rising edge VPOR	1.60	1.68	1.76			IN
	reset threshold	Falling edge VPDR	1.56	1.64	1.72			IN
VPORhyst	POR hysteresis				40			mV
IRUSH	on the regulator power surge current (POR or call from standby Awake)				100	150		mA
TNRST	NRST reset minimum width		500					ns
TIPVD1	PVD1 reset release time		300	380	460		ÿs	
TIPVD2	PVD2 reset release time		300	380	460		ÿs	
TINRST	NRST reset release time		25	35	50		ÿs	
TRIPT	internal reset time		140	160	200		ÿs	
TRSTBOR	BOR reset release time		440	520	610		ÿs	
TRSTPOR	power on reset release time			2500	3000	ÿs		

1. Mass production test guarantee.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is the external input comparison voltage of PVD2EXINP pin.
3. PVD1 monitoring voltage is the monitoring voltage when VCC voltage drops; when PVD2LVL[2:0] is set to 111, PVD2 monitoring
 The voltage is the monitoring voltage when the PVDEXINP voltage drops, when PVD2LVD[2:0] is set to a value other than 111
 The PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1,2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.
 PVD1 monitoring voltage when VCC rises=Vpvd1+Vpvdyhst; PVD2 monitoring voltage when VCC
 rises=Vpvd2+Vpvdyhst.

3.3.4 Supply current characteristics

Current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and the code being run.

The measurement method of current consumption is introduced in Figure 3-5 Current Consumption Measurement Scheme. Current consumption measurements in various operating modes described in this section

The values are obtained under laboratory conditions through a set of test codes running on FLASH.

The specific conditions are as follows:

- 1) All I/O pins are in input mode with static value (no load) on VCC or VSS.
- 2) Clock frequency selection super high speed mode fHCLK=200MHz, high speed mode fHCLK=168MHz/120MHz/24MHz and
 Ultra low speed mode fHCLK=8MHz/1MHz.
- 3) The power consumption mode is divided into: normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, off
 Power mode ICC_PD and Dhrystone working mode ICC_DHRYSTONE.
- 4) Peripheral clock ON/OFF Please refer to the specific current test items.
- 5) In super high speed mode fHCLK=200MHz and high speed mode fHCLK=168MHz/120MHz, PLL is on.

Table 3-8 Current consumption in ultra-high speed mode

Mode Parameter	Symbol	condition	Facing	product specification			Him t
			ÿ°Cÿ	Min	Type(1)	Max(2)	
super high speed mold Mode	fHCLK= 200MHz	ICC_RUN	while(1), full model Block clock OFF	-40		16	mA
			while(1), full model Block clock ON	-40		29	mA
		ICC_DHRYSTONE	CACHE OFF	-40		17	mA
			CACHE ON	-40		19	mA
		ICC_SLEEP	All module clock OFF -40			11	mA
			All module clock ON	-40		24	mA
		ICC_RUN	while(1), all module clock OFF	25		16	mA
			while(1), all module clock ON	25		29	mA
		ICC_DHRYSTONE	CACHE OFF	25		17	mA
			CACHE ON	25		19	mA
		ICC_SLEEP	All module clock OFF	25		11	mA
			All module clock ON	25		24	mA
		ICC_RUN	while(1), full model Block clock OFF	85		22	mA
			while(1), full model Block clock ON	85		35	mA
		ICC_DHRYSTONE	CACHE OFF	85		22	mA
			CACHE ON	85		25	mA
		ICC_SLEEP	All module clock OFF	85		17	mA
			All module clock ON	85		30	mA
		ICC_RUN	while(1), full model Block clock OFF	105		25	mA
			while(1), full model Block clock ON	105		39	mA
		ICC_DHRYSTONE	CACHE OFF	105		24	mA
			CACHE ON	105		29	mA
		ICC_SLEEP	All module clock OFF 105			21	mA
			All module clock ON	105		34	mA

1. Typ voltage condition VCC=3.3V
 2. Max voltage condition VCC=1.8~3.6V

Table 3-9 High-speed mode current consumption1

Mode Parameter	Symbol	condition	Facing	product specification			Unit
			ÿ°C	Min	Typ(1)	Max(2)	
high speed model	fHCLK=168MHz	ICC_RUN	while(1), the whole module Clock OFF	-40		13	mA
			while(1), the whole module Clock ON	-40		23	mA
		ICC_DHRYSTONE	CACHE OFF	-40		14	mA
			CACHE ON	-40		15	mA
		ICC_SLEEP	All module clock OFF	-40		9	mA
			All module clock ON	-40		19	mA
		ICC_RUN	while(1), all module clock OFF	25		13	mA
			while(1), all module clock ON	25		23	mA
		ICC_DHRYSTONE	CACHE OFF	25		14	mA
			CACHE ON	25		15	mA
		ICC_SLEEP	All module clock OFF	25		9	mA
			All module clock ON	25		19	mA
		ICC_RUN	while(1), the whole module Clock OFF	85		18	mA
			while(1), the whole module Clock ON	85		28	mA
		ICC_DHRYSTONE	CACHE OFF	85		18 mA	
			CACHE ON	85		20 mA	
		ICC_SLEEP	All module clock OFF	85		14 mA	
			All module clock ON	85		24 mA	
		ICC_RUN	while(1), the whole module Clock OFF	105		20 mA	
			while(1), the whole module Clock ON	105		31 mA	
		ICC_DHRYSTONE	CACHE OFF	105		19 mA	
			CACHE ON	105		23 mA	
		ICC_SLEEP	All module clock OFF	105		17 mA	
			All module clock ON	105		27 mA	

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Table 3-10 High-speed mode current consumption 2

Mode Parameter	Symbol	condition	Facing	product specification			Unit
			ÿ°C	Min	Typ(1)	Max(2)	
high speed mode	fHCLK=120MHz	ICC_RUN	while(1), when the whole module Bell OFF	-40		9.5	mA
			while(1), when the whole module Bell ON	-40		16.5	mA
		ICC_DHRYSTONE	CACHE OFF	-40		10	mA
			CACHE ON	-40		11.5	mA
		ICC_SLEEP	All module clock OFF	-40		7	mA
			All module clock ON	-40		14.5	mA
		ICC_RUN	while(1), all module clock OFF	25		9.5	mA
			while(1), all module clock ON	25		16.5	mA
		ICC_DHRYSTONE	CACHE OFF	25		10	mA
			CACHE ON	25		11.5	mA
		ICC_SLEEP	All module clock OFF	25		7	mA
			All module clock ON	25		14.5	mA
		ICC_RUN	while(1), when the whole module Bell OFF	85			14 mA
			while(1), when the whole module Bell ON	85			22 mA
		ICC_DHRYSTONE	CACHE OFF	85			14 mA
			CACHE ON	85			17 mA
		ICC_SLEEP	All module clock OFF	85			12 mA
			All module clock ON	85			20 mA
		ICC_RUN	while(1), when the whole module Bell OFF	105			16 mA
			while(1), when the whole module Bell ON	105			25 mA
		ICC_DHRYSTONE	CACHE OFF	105			15 mA
			CACHE ON	105			19 mA
		ICC_SLEEP	All module clock OFF	105			15 mA
			All module clock ON	105			22 mA

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Table 3-11 High-speed mode current consumption 3

Mode Parameter	Symbol	condition	Facing	product specification			Unit
			Y°C	Min	Typ(1)	Max(2)	
high speed model	fHCLK=24MHz	ICC_RUN	while(1), the whole module Clock OFF	-40		3	mA
			while(1), the whole module Clock ON	-40		6	mA
		ICC_DHRYSTONE CACHE OFF		-40		3.5	mA
		ICC_SLEEP	All module clock OFF	-40		2	mA
			All module clock ON	-40		5.5	mA
		ICC_RUN	while(1), all module clock OFF	25		3	mA
			while(1), all module clock ON	25		6	mA
		ICC_DHRYSTONE CACHE OFF		25		3.5	mA
		ICC_SLEEP	All module clock OFF	25		2	mA
			All module clock ON	25		5.5	mA
		ICC_RUN	while(1), the whole module Clock OFF	85		8	mA
			while(1), the whole module Clock ON	85		12 mA	
		ICC_DHRYSTONE CACHE OFF		85		7	mA
		ICC_SLEEP	All module clock OFF	85		8	mA
			All module clock ON	85		11 mA	
		ICC_RUN	while(1), all module clock OFF	105		10	mA
			while(1), all module clock ON	105		14	mA
		ICC_DHRYSTONE CACHE OFF		105		8	mA
		ICC_SLEEP	All module clock OFF	105		10 mA	
			All module clock ON	105		14 mA	

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Table 3-12 Ultra low speed mode current consumption 1

Mode Parameter	Symbol	condition	Facing	product specification			Unit
			$\circ\text{C}$	Min Type(1)	Type(2)	Max(2)	
ultra low speed model	fHCLK=8MHz	ICC_RUN	while(1), all Module clock OFF	-40		1	mA
			while(1), all Module clock ON	-40		3.5	mA
		ICC_DHRYSTONE CACHE OFF		-40		1.5	mA
		ICC_SLEEP	All module clock OFF -40			1.2	mA
			Full module clock ON -40			3.2	mA
		ICC_RUN	while(1), all module clock OFF	25		1	mA
			while(1), all module clock ON	25		3.5	mA
		ICC_DHRYSTONE CACHE OFF		25		1.5	mA
		ICC_SLEEP	All module clock OFF 25			1.2	mA
			All module clock ON	25		3.2	mA
		ICC_RUN	while(1), all Module clock OFF	85		4	mA
			while(1), all Module clock ON	85		6	mA
		ICC_DHRYSTONE CACHE OFF		85		4	mA
		ICC_SLEEP	All module clock OFF 85			3.5 mA	
			All module clock ON	85		6	mA
		ICC_RUN	while(1), all module clock OFF	105		6	mA
			while(1), all module clock ON	105		7	mA
		ICC_DHRYSTONE CACHE OFF		105		4.5 mA	
		ICC_SLEEP	All module clock OFF 105			4	mA
			Full module clock ON 105			6.5 mA	

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Table 3-13 Ultra low speed mode current consumption 2

Mode Parameter		Symbol	condition	Facing	product specification			Unit
				ÿ°C	Min	Typ(1)	Max(2)	
ultra low speed model	fHCLK= 1MHz	ICC_RUN	while(1), full model Block clock OFF	-40		0.7		mA
			while(1), full model Block clock ON	-40		2.5		mA
		ICC_DHRYSTONE CACHE OFF		-40		0.9		mA
		ICC_SLEEP	All module clock OFF	-40		0.9		mA
			All module clock ON	-40		2.4		mA
		ICC_RUN	while(1), all module clock OFF	25		0.7		mA
			while(1), all module clock ON	25		2.5		mA
		ICC_DHRYSTONE CACHE OFF		25		0.9		mA
		ICC_SLEEP	All module clock OFF	25		0.9		mA
			All module clock ON	25		2.4		mA
		ICC_RUN	while(1), full model Block clock OFF	85			4	mA
			while(1), full model Block clock ON	85			5	mA
		ICC_DHRYSTONE CACHE OFF		85			3.5 mA	
		ICC_SLEEP	All module clock OFF	85			3.5 mA	
			All module clock ON	85			5	mA
		ICC_RUN	while(1), all module clock OFF	105			5	mA
			while(1), all module clock ON	105			5.5	mA
		ICC_DHRYSTONE CACHE OFF		105			4 mA	
		ICC_SLEEP	All module clock OFF	105			5	mA
			All module clock ON	105			5.5 mA	

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Table 3-14 Low power mode current consumption

mold Mode	Parameter Symbol		Conditions (VCC=3.3V)	Facing	product specification			Unit
				ÿ°Cÿ	My Type(1)		Max(2)	
stop end mold Mode	ICC_ST P	ICC_ST P	PWC_PWRC1.STPDAS=00	-40		160		uA
			PWC_PWRC1.STPDAS=11	-40		30		uA
			PWC_PWRC1.STPDAS=00	25		220		uA
			PWC_PWRC1.STPDAS=11	25		80		uA
			PWC_PWRC1.STPDAS=00	85			3600 uA	
			PWC_PWRC1.STPDAS=11	85			3400 uA	
			PWC_PWRC1.STPDAS=00	105			4800 uA	
			PWC_PWRC1.STPDAS=11(3)	105			4600 uA	
Lose electricity mold Mode	ICC_PD power down mode 1	ICC_PD power down mode 1		-40		10		uA
			power down mode 2	-40		4		uA
			power down mode 3	-40		1.8		uA
			power down mode 4	-40		1.8		uA
			Power down mode 2+XTAL32+RTC	-40		6		uA
			Power down mode 2+LRC+RTC	-40		9		uA
			power down mode 1	25		10		uA
			power down mode 2	25		4		uA
			power down mode 3	25		1.8		uA
			power down mode 4	25		1.8		uA
			Power down mode 2+XTAL32+RTC	25		6		uA
			Power down mode 2+LRC+RTC	25		9		uA
			power down mode 1	85			21 uA	
			power down mode 2	85			19 uA	
			power down mode 3	85			19 uA	
			power down mode 4	85			19 uA	
			Power down mode 2+XTAL32+RTC	85			21 uA	
			Power down mode 2+LRC+RTC	85			21 uA	
			power down mode 1	105			35 uA	

mold Mode	Parameter Symbol		Conditions (VCC=3.3V)	Facing	product specification			Unit
				ÿ°Cÿ	My Type(1)		Max(2)	
			power down mode 2	105	-	-	33 uA	
			power down mode 3	105	-	-	30 uA	
			Power-down mode 4[3]	105	-	-	30 uA	
			Power down mode 2+XTAL32+RTC	105	-	-	35 uA	
			Power down mode 2+LRC+RTC	105	-	-	35 uA	

1. Typ voltage condition VCC=3.3V 2. Max voltage

condition VCC=1.8~3.6V

3. Mass production test guarantee.

Table 3-15 Current consumption of analog modules

Item Parameter	Symbol	condition (VCC=AVCC=3.3V)	Facing	product specification			Unit
			ÿ°Cÿ	Min	Type	Max	
module electric current	ICC_MODUL AND	Large drive in XTAL oscillation mode 24MHz	25	-	1.8	-	mA
			25	-	1	-	mA
			25	-	0.8	-	mA
			25	-	0.6	-	mA
		XTAL 32K	25	-	0.5	-	mA
		HRC	25	-	0.35	-	mA
		PLL@480MHzÿ	25	-	2.3	-	mA
		PLL@240MHzÿ	25	-	1.4	-	mA
		ADC	25	-	1.2	-	mA
		DAC	25	-	70	-	uA
		CMP	25	-	0.11	-	mA
		PGA	25	-	1	-	mA
		USBFS(1)	25	-	6	-	mA

1. Contains the current when the control section communicates with the USBPHY.

3.3.5 Electrical sensitivity

The chip is tested differently (ESD, LU) using specific measurement methods to determine its performance in terms of electrical susceptibility.

3.3.5.1 Electrostatic Discharge (ESD)

Apply electrostatic discharge to the pins of each sample according to each pin combination. This test complies with the JESD22-A114/C101 standard.

Table 3-16 ESD characteristics

symbol	parameter	condition	unit of maximum	
VESD (HBM)	electrostatic discharge voltage (human body model)	TA =+25 °C per JESD22-A114 Standard 4000		
VESD(CDM)	Electrostatic Discharge Voltage (Charged Device Model)	TA =+25 °C per JESD22-C101 Standard 1000		IN

3.3.5.2 Static Latch-up

To evaluate static latch-up performance, two complementary static latch-up tests are performed on the chip:

- ÿ Overvoltage applied to each power supply and analog input pin
- ÿ Apply current injection to other input, output and configurable I/O pins

These tests comply with the EIA/JESD 78A IC Latch-up standard.

Table 3-17 Static Latch-up features

symbol	parameter	condition	maximum value	unit
LU	Static Latch-up	TA =+105 °C per JESD78A	200	mA

3.3.6 Low-power mode wake-up sequence

The wake-up time is measured from the wake-up event trigger to the first instruction executed by the CPU:

- ÿ For stop or sleep mode: the wakeup event is WFE.
- ÿ WKUP pin is used to wake up from standby, stop, sleep mode. All timings are tested at ambient temperature and VCC=3.3V.

Table 3-18 Low power mode wake-up time

symbol	parameter	condition	Typical Value	Maximum Unit	
TSTOP1	wake up from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, and the program is executed on RAM	2	5	us
TSTOP2	wakes up from stop mode, the system clock is MRC, and the program is executed on Flash		8	15	
TPD1(1)	wakes up from power-down mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	15	25	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	20	30	
TPD2(1)	wakes up from power-down mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	40	50	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	45	55	
TPD3(1)	wakes up from power-down mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	2500	3000	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	2500	3000	
TPD4(1)	wakes up from power-down mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	65	75	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	70	80	

1. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of the PWC_PWRC3.PDTS bit.

When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, it is necessary to ensure

The PWC_PWRC3.PDTS bit is cleared. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF,

It is necessary to ensure that the PWC_PWRC3.PDTS bit is set before entering power-down mode.

3.3.7 I/O port characteristics

General I/O Characteristics

Table 3-19 I/O static characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VIL(1)	input low level	1.8~VCC~3.6	-	-	-	0.2VCC	IN	
VIH(1)	input high level	1.8~VCC~3.6 0.8VCC	-	-	-	-	IN	
VHYS	input hysteresis	1.8~VCC~3.6	-	-	0.2	-	IN	
ILKG(1)	I/O input leakage current	VSS~VIN~VCC	-	-	-	±1	uA	
		VIN = 5.5V(2)	-	-	-	5	uA	
RPU(1)	weak pull-up etc. effective resistance	USBFS_DP~USBFS_DM -	-	-	1.5	-	KΩ	
		In addition to USBFS_DP and Other input pins of USBFS_DM	VIN = VSS	-	30	-	KΩ	
CIO	I/O pull leg capacitance	PA11/USBFS_DM PA12/USBFS_DP	-	-	10	-	pF	
		Except PA11/USBFS_DM and Other output of PA12/USBFS_DP input pin	-	-	5	-	pF	

1. Mass production test guarantee.

2. To keep the voltage above VCC+0.3 V, the internal pull-up/pull-down resistors must be disabled.

The output voltage

Table 3-20 Output voltage characteristics

Driver settings	symbol	parameter	condition	Min	Typ	Max	Unit		
low drive	VOL(1)(2) low level output	IIO=±1.5mA,	1.8VCC<2.7	-	-	-	0.4	IN	
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output	-	IIO=±3mA, 2.7VCC>3.6	-	-	-	0.4		
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output	-	IIO=±6mA, 2.7VCC>3.6	-	-	-	1.3		
	VOH(1)(3) high level output	-		VCC-1.3	-	-	-		
medium drive	VOL(1)(2) low level output	-	IIO=±3mA, 1.8VCC<2.7	-	-	-	0.4		
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output	-	IIO=±5mA, 2.7VCC>3.6	-	-	-	0.4		
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output IIO=±12mA,	-	2.7VCC>3.6	-	-	-	1.3		
	VOH(1)(3) high level output	-		VCC-1.3	-	-	-		
high drive	VOL(1)(2) low level output	-	IIO=±6mA, 1.8VCC<2.7	-	-	-	0.4		
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output	-	IIO=±8mA, 2.7VCC>3.6	-	-	-	0.4		
	VOH(1)(3) high level output	-		VCC-0.4	-	-	-		
	VOL(1)(2) low level output IIO=±20mA, 2.7	-	VCC>3.6	-	-	-	1.3		
	VOH(1)(3) high level output	-		VCC-1.3	-	-	-		

1. Mass production test guarantee.

2. The IIO current sink of the device must always take into account the absolute maximum ratings specified in Table 3-3. IIO (I/O ports and control pins feet) must not exceed IVSS.
3. The IIO source current of the device must always adhere to the absolute maximum ratings listed in Table 3-3, IIO (I/O ports and control pins feet) must not exceed the IVCC.

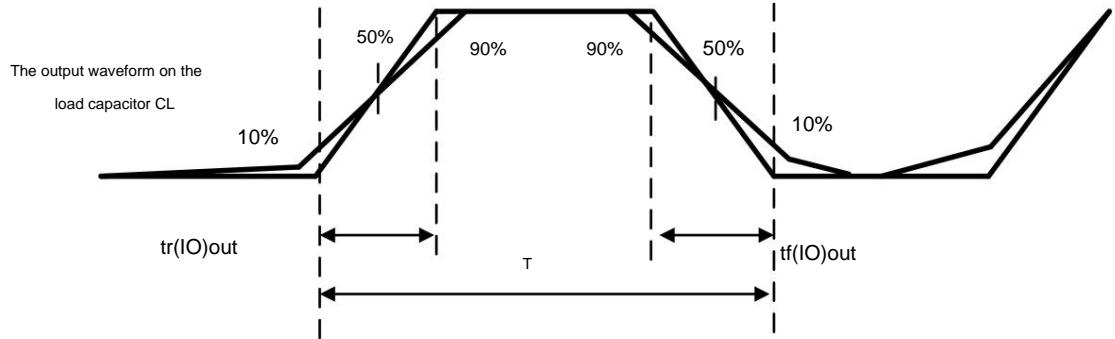
Input/Output AC Characteristics

Table 3-21 I/O AC characteristics

driver settings	symbol	parameter	condition(3)	Min	Typ	Max	Unit		
low drive	fmax(IO)out maximum frequency(1)		CL=30 pF, VCC≥ 2.7V -	-	-	-	20	MHz	
			CL=30 pF, VCC≥1.8V	-	-	-	10		
			CL=10pF, VCC≥2.7V	-	-	-	40		
			CL=10pF, VCC≥1.8V	-	-	-	20		
	tf(IO)out tr(IO)out	output high to low when falling between and the output low to high on the rise time	CL=30 pF, VCC≥2.7V	-	-	-	15	ns	
			CL=30 pF, VCC≥1.8V	-	-	-	25		
			CL=10pF, VCC≥2.7V	-	-	-	7.5		
			CL=10pF, VCC≥1.8V	-	-	-	15		
medium drive	fmax(IO)out maximum frequency(1)		CL=30 pF, VCC≥ 2.7V -	-	-	-	45	MHz	
			CL=30 pF, VCC≥1.8V	-	-	-	22.5		
			CL=10pF, VCC≥2.7V	-	-	-	90		
			CL=10pF, VCC≥1.8V	-	-	-	45		
	tf(IO)out tr(IO)out	output high to low when falling between and the output low to high on the rise time	CL=30 pF, VCC≥2.7V	-	-	-	7.5	ns	
			CL=30 pF, VCC≥1.8V	-	-	-	12		
			CL=10pF, VCC≥2.7V	-	-	-	4		
			CL=10pF, VCC≥1.8V	-	-	-	7.5		
high drive	fmax(IO)out maximum frequency (1)		CL=30 pF, VCC≥2.7V	-	-	-	100	MHz	
			CL=30 pF, VCC≥1.8V	-	-	-	50		
			CL=10pF, VCC≥2.7V	-	-	-	180		
			CL=10pF, VCC≥1.8V	-	-	-	100		
	tf(IO)out tr(IO)out	When the output falls from high to low, CL=30 pF, VCC≥1.8V between and the output low to high on the rise time	CL=30 pF, VCC≥2.7V	-	-	-	4	ns	
			CL=10pF, VCC≥2.7V	-	-	-	6		
			CL=10pF, VCC≥1.8V	-	-	-	2.5		
			CL=10pF, VCC≥1.8V	-	-	-	4		

1. The maximum frequency is defined in Figure 3-6.

2. The load capacitance CL must take into account the capacitance of the PCB and MCU pins (the capacitance of the pins and the circuit board can be roughly estimated is 10 pF).



Maximum frequency condition: $(tr + tf) \leq (2/3)T$ and Duty cycle= 50%±5% (the load capacitance CL is marked in the "Condition" column of the "Input/Output AC Characteristics" table)

Figure 3-6 Definition of I/O AC characteristics

3.3.8 USART interface characteristics

Table 3-22 USART AC Timing

symbol	parameter		min	max	unit	
tcyc	Input clock cycles	UART	4	-	-	tPCLK1
		CSI	6	-	-	
tCKw	Input Clock Width		0.4	0.6	-	tScyc
tCKr	Input Clock Rise Time		-	5	-	ns
tCKf	Input Clock Fall Time		-	5	-	ns
tTD	Send delay time	CSI	-	28	-	ns
tRDS	Receive data setup time	CSI	15	-	-	ns
trDH	Receive data hold time	CSI	5	-	-	ns

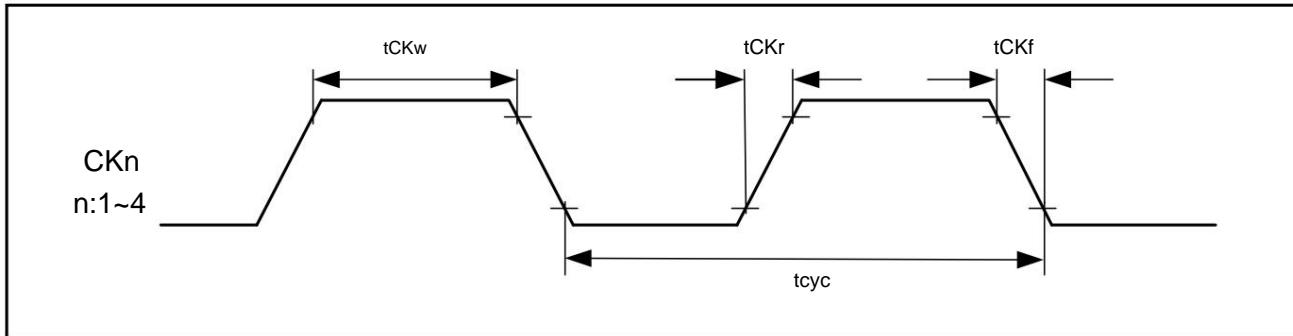


Figure 3-7 USART clock timing

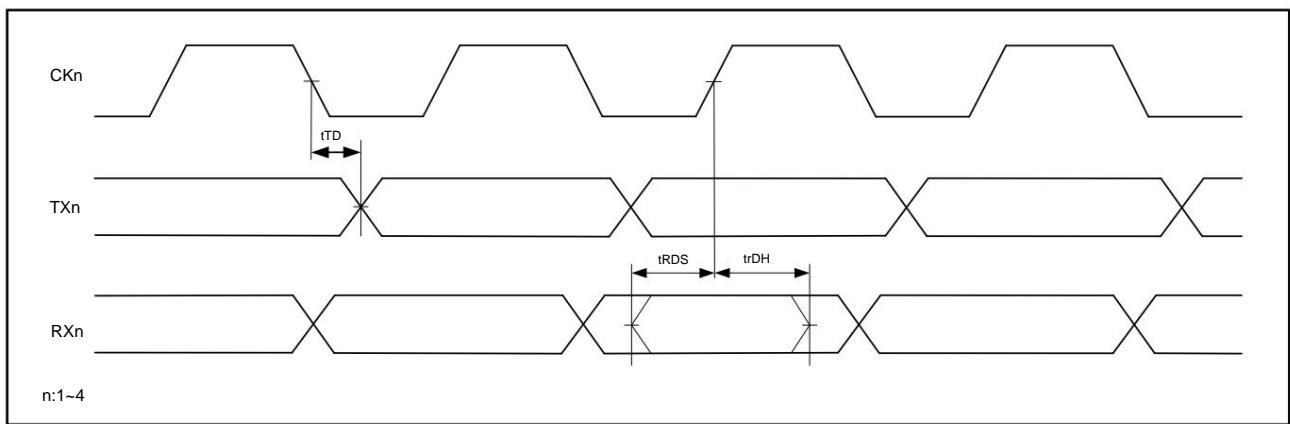


Figure 3-8 USART (CSI) input and output timing

3.3.9 I2S interface characteristics

Table 3-23 I2S electrical characteristics

symbol	Performance	condition	Min	Max	Unit
fMCK	I2S main clock output -		256*8K	256*Fs	MHz
fCK	I2S clock frequency	Master data: 32 bits 20		64*Fs	MHz
		Slave data: 32 bits		64*Fs	
DCK	I2S clock frequency duty cycle	Slave receiver	30	70	%
tv(WS)	WS valid time	Master mode	0	-	ns
th(WS)	WS hold time	Master mode	0	-	
tsu(WS)	WS setup time	Slave mode	1	-	
th(WS)	WS hold time	Slave mode	0	-	
tsu(SD_MR)	Data input setup time	Master receiver	7.5	-	
tsu(SD_SR)		Slave receiver	2	-	
th(SD_MR)	Data input hold time	Master receiver	0	-	
th(SD_SR)		Slave receiver	0	-	
tv(SD_ST)	Data output valid time	Slave transmitter(after enable edge)	-	27	
th(SD_ST)		Master transmitter(after enable edge)	-	20	
tv(SD_MT)		Master transmitter(after enable edge)	2.5	-	
th(SD_MT)	Data output hold time				

1. Fs: I2S sampling frequency

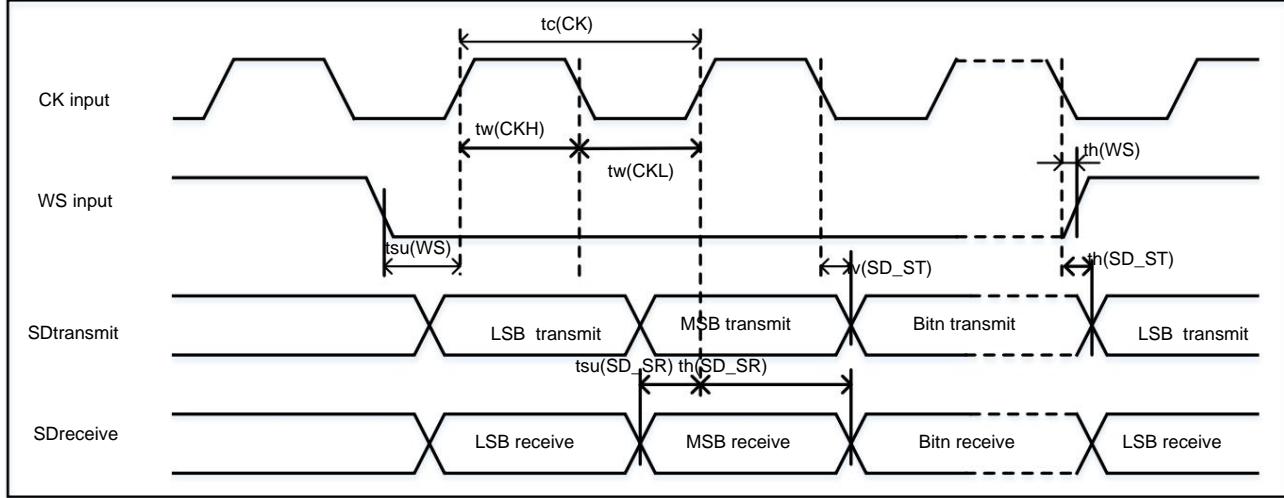


Figure 3-9 I2S slave mode timing (Philips protocol)

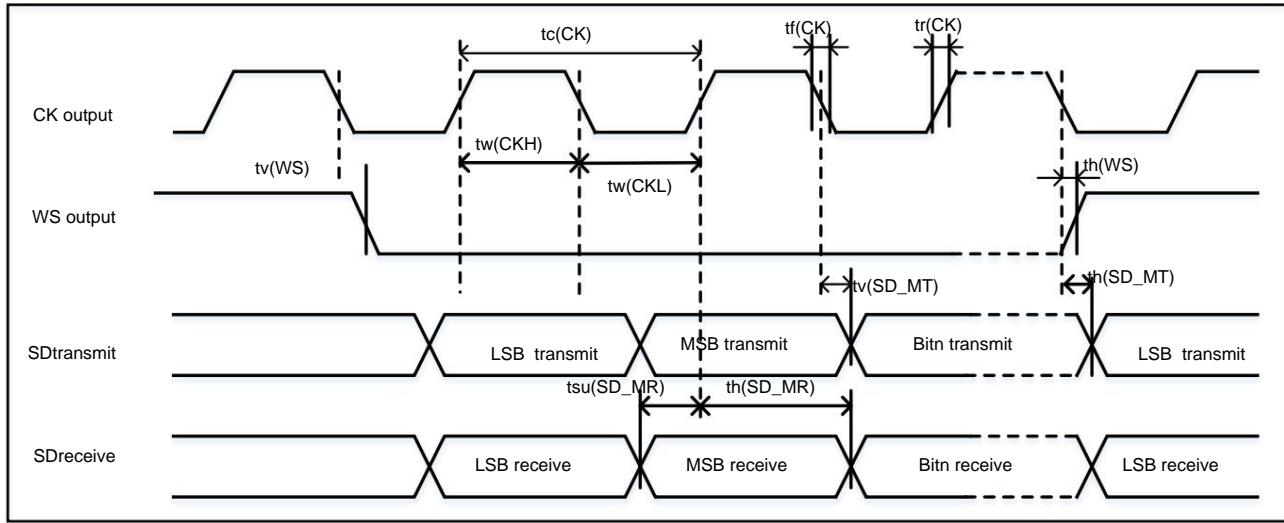


Figure 3-10 I2S master mode timing (Philips protocol)

3.3.10 I2C Interface Features

Table 3-24 I2C electrical characteristics

symbol	parameter	Standard Mode (SM)		Fast Mode (FM)		unit
		Min	Max	Min	Max	
fSCL	SCL frequency	0	100	0	400	KHz
tHD;STA	start condition/restart condition Hold	4.0	-	0.6	-	us
tLOW	SCL low level	4.7	-	1.3	-	us
tHIGH	SCL high level	4	-	0.6	-	us
tSU;STA	restart condition Setup	4.7	-	0.6	-	us
tHD;DAT	Data Hold	0	-	0	-	us
tSU; DAT	Data Setup	50+	tI2C reference clock period	50+	tI2C reference clock period	ns
tR	Rise time of SCL/SDA	-	1000	6.5	300	ns
tF	Fall Time Stop Condition Setup	-	300	6.5	300	ns
tSU;STO	for SCL/SDA	4	-	0.6	-	us
tBUF	BUS idle between stop condition and start condition time	4.7	-	1.3	-	us
C _b	load capacitance	-	400	-	400	pF

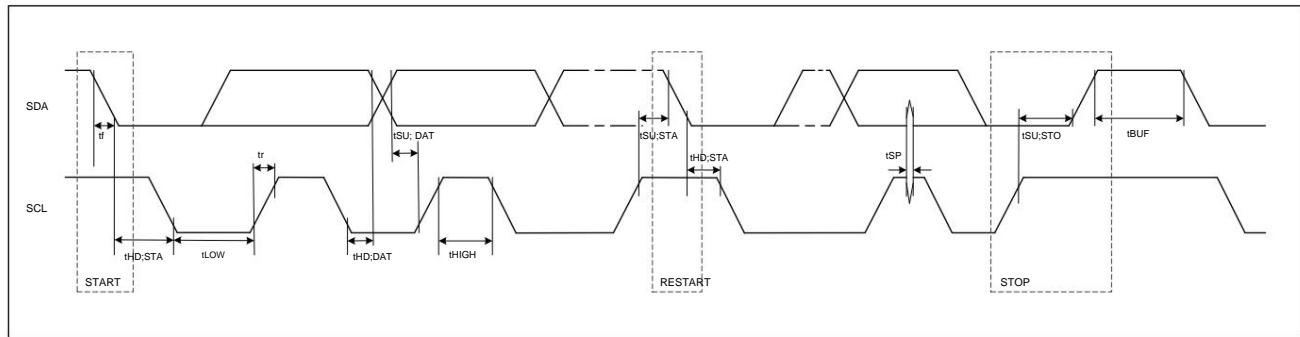


Figure 3-11 I2C bus timing definition

3.3.11 SPI Interface Features

Table 3-25 SPI electrical characteristics

Item	Symbol	Min	Max	Unit	Test conditions
SCK clock cycle	Master tpcyc Slave	2 μ pclk \geq 60MHz 4 μ pclk \leq 60MHz	4096 6	4096	Figure 3-12 C=30pF
SCK clock rise and fall time	Master tsckr Slave	tsckf	-	5	ns
			-	1	
Data input setup time	Master Tsu Slave		4	-	ns Figure 3-13 C=30pF
			5	-	
Data input hold time	Master th Slave		tpcyc	-	ns
			20	-	
Data output delay	Master tod Slave		-	8	ns
			-	20	
Data output hold time	Master toh Slave		0	-	ns
			0	-	
MOSI/MISO lauged and fall time	Master tdr Slave	tdf	-	5	ns
			-	1	
SS rise and fall time	Master tsr Slave	tssf	-	5	ns
			-	1	

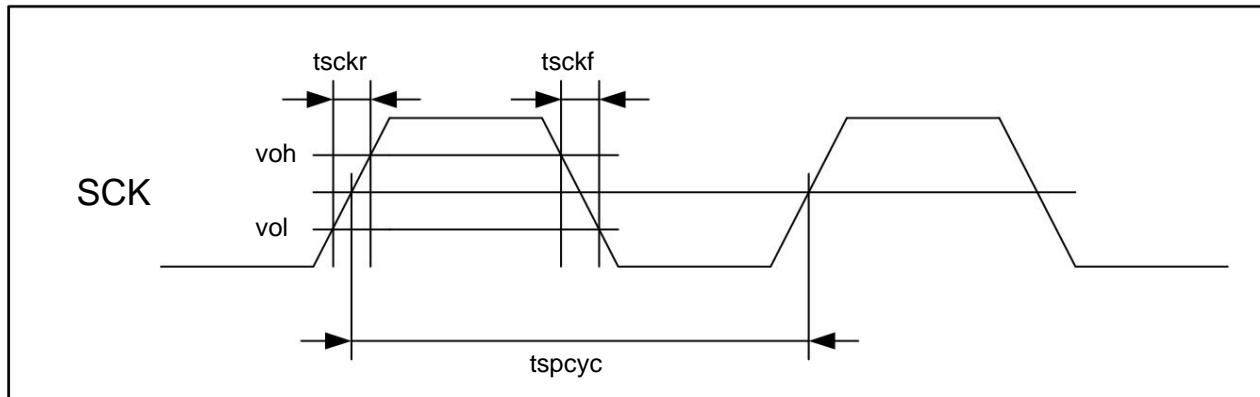


Figure 3-12 SCK Clock definition

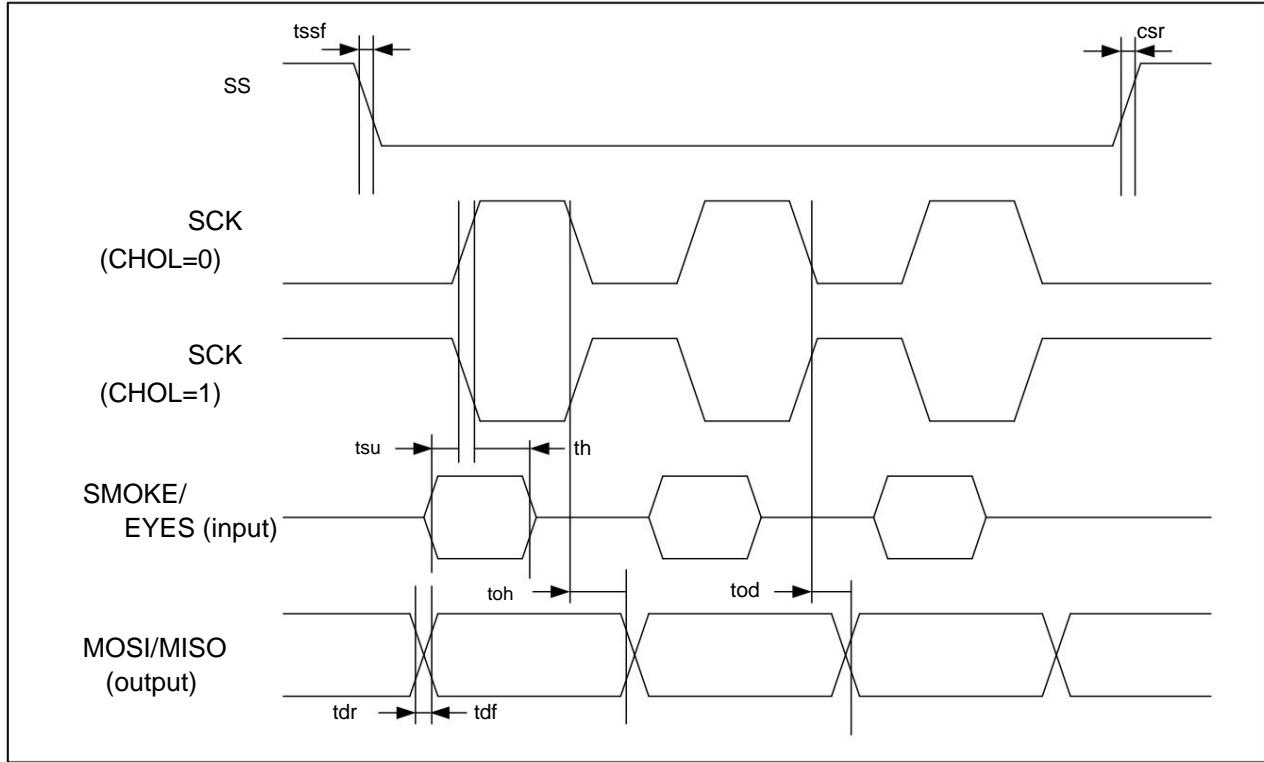


Figure 3-13 SPI interface timing requirements

3.3.12 CAN2.0B interface features

For the port characteristics of CANx_TX and CANx_RX, please refer to 3.3.7 I/O Port Characteristics.

3.3.13 USB Interface Features

Table 3-26 USB Full-Speed electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Type	Max(1) Unit	
enter	VCC working voltage		3.0(2)		3.6	IN
	VIL input low level				0.8	IN
	VIH input high level		2.0			IN
	VDI Differential Input Sensitivity -		0.2			IN
	VCM differential common mode voltage		0.8		2.5	IN
output	VOL(3) Static	output low level RL=1.5k Ω to 3.6V(4)			0.3	IN
	VOH(3) Static	output high level RL=15k Ω to VSS(4)	2.8		3.6	IN
	VCRS	Cross-over electricity to press	CL=50pF	1.3		2.0 IN
	tR	Rise Time	CL=50pF 10%~90% of VOH-VOL	4		20 ns
	tF	fall time	CL=50pF 10%~90% of VOH-VOL	4		20 ns
	tRFMA	Rise and fall time ratio tR/tF	CL=50pF	90		111.1 %
RPD(3)	Pull-down resistor	VIN= VCC $\ddot{\text{y}}$ in host mode		15		k Ω
RPU(3)	Pull-up resistor	VIN= VSS $\ddot{\text{y}}$ idle state	0.900 1.2		1.575	k Ω
		VIN= VSS $\ddot{\text{y}}$ in device mode	1.425 2.3		3.090	k Ω

1. All voltages are measured at local ground potential.

2. When the operating voltage drops to 2.7V, the function of the USB full-speed transceiver can still be guaranteed, but the complete USB full-speed power supply cannot be guaranteed.

gas characteristics, which degrade over a VCC voltage range of 2.7 to 3.0V.

3. Mass production test guarantee.

4. RL is the load connected to the USB full speed drive.

Table 3-27 USB Low-Speed electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit		
Input VCC	working voltage		3.0(2)			3.6	IN	
	VIL input low level					0.8	IN	
	VIH input high level		2.0				IN	
	VDI differential input sensitivity		0.2				IN	
	VCM differential common mode voltage		0.8			2.5	IN	
Output VOL(3)	Static output low level	RL=1.5k Ω to 3.6V(4)				0.3	IN	
	VOH (3) static output high level	RL=15k Ω to VSS(4)	2.8			3.6	IN	
	VCRS(3) Cross-over voltage CL=200pF~600pF		1.3			2.0	IN	
	tR(3) rise time	CL=200pF~600pF 10%~90% of VOH-VOL	75			300	ns	
	tF(3) fall time	CL=200pF~600pF, 10%~90% of VOH-VOL tRFMA(3) Rising and falling time ratio tR/tF CL=200pF~600pF	75			300	ns	
	RPD(3)	Pull-down resistor VIN= VCC in host mode	14.25 -			24.80 k Ω		

1. All voltages are measured at local ground potential.

2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed power supply cannot be guaranteed.

gas characteristics, which degrade in the VCC voltage range of 2.7 to 3.0V.

3. Mass production test guarantee.

4. RL is the load connected to the USB low-speed driver.

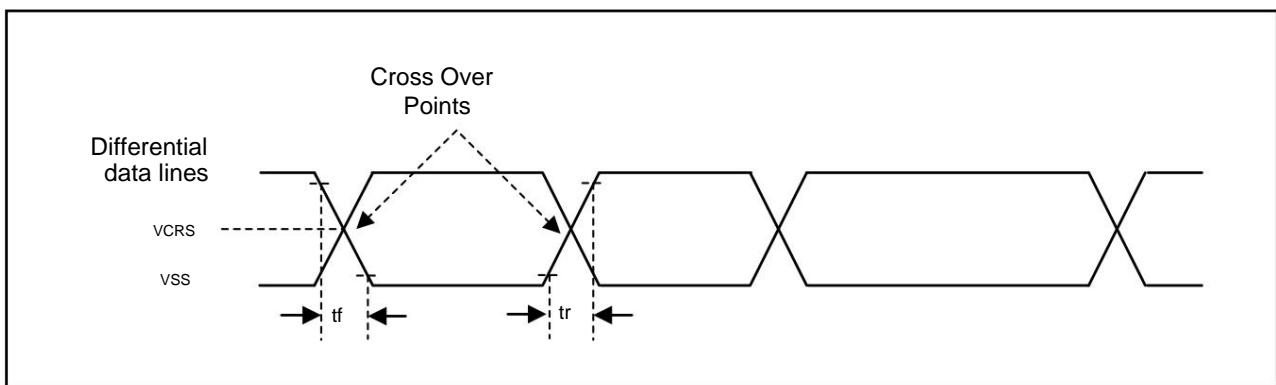


Figure 3-14 Definition of USB rise/fall time and Cross Over voltage

3.3.14 PLL characteristics

Table 3-28 PLL main performance indicators

symbol	parameter	condition	Min	Typ	Max	Unit
fPLL_IN	PLL PFD(Phase Frequency Detector) input clock(1)		1			25 MHz
fPLL_OUT	PLL multiplier output clock			15		240 MHz
fVCO_OUT	PLL VCO output		240		480	MHz
JitterPLL	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak		±100		ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak		±150		
tLOCK	PLL lock time			80	120	μs

1. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.15 JTAG Interface Features

Table 3-29 JTAG interface features

Symbol	Item	Min	Type	Max	Unit
tTCKcyc	JTCK clock cycle time	50	-	-	ns
tTCKH	JTCK clock high pulse width	20	-	-	ns
tTCKL	JTCK clock low pulse width	20	-	-	ns
tTCKr	JTCK clock rise time	-	-	5	ns
tTCKf	JTCK clock fall time	-	-	5	ns
tTMSs	JTMS setup time	8	-	-	ns
tTMSh	JTMS hold time	8	-	-	ns
tTDIs	JTDI setup time	8	-	-	ns
tTDlh	JTDI hold time	8	-	-	ns
tTDOd	JTDO data delay time	-	-	20	ns

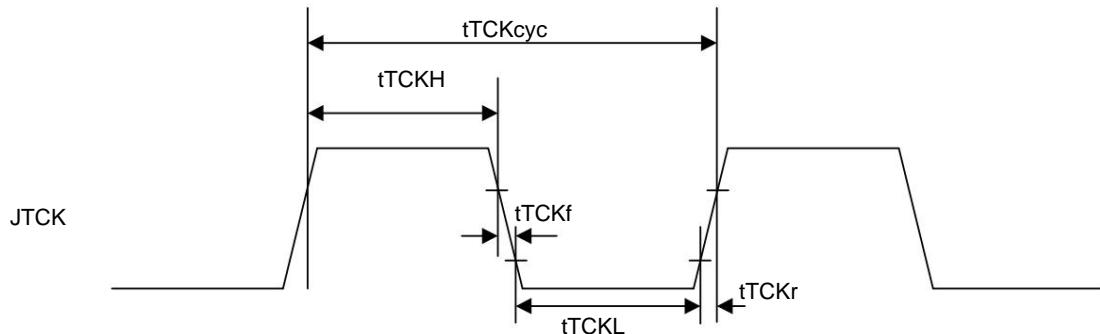


Figure 3-15 JTAG JTCK clock

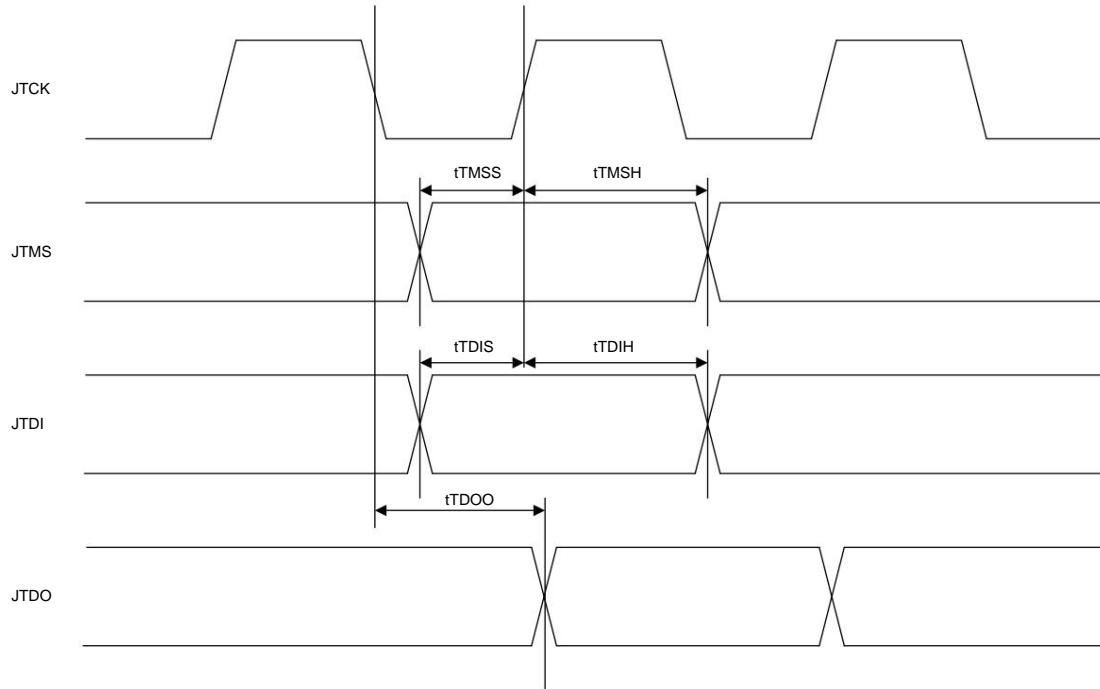


Figure 3-16 JTAG input and output

3.3.16 External Clock Source Characteristics

3.3.16.1 High-speed external user clock from external source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/Os. The external clock signal must take I/O static characteristics into consideration.

Table 3-30 High-speed external user clock characteristics

symbol	parameter	condition	Min	Typ	Max	Unit			
fXTAL_EXT	external clock source frequency		1	-	-	25	MHz		
VIH_XTAL	XTAL_EXT input pin high level		0.8*VCC	-	-	VCC			IN
VIL_XTAL	XTAL_EXT input pin low level		VSS	-	-	0.2*VCC			
tr(XTAL)	XTAL_EXT rise or fall time		-	-	-	5	ns		
tf(XTAL)			40	-	-	60	%		
Duty (XTAL)	duty cycle								

3.3.16.2 High-speed external clock from crystal/ceramic resonator

The high-speed external (XTAL) clock can be generated using a 4 to 25 MHz crystal/resonant oscillator. In the application,

The resonator and load capacitors must be placed as close as possible to the pins of the oscillator to minimize output distortion and start-up settling time. Related resonators

For details of characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-31 XTAL 4-25 MHz oscillator characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
fXTAL_IN	oscillator frequency		4	-	-	25	MHz	
RF(1)	Feedback resistor		-	-	300	-	k Ω	
AXTAL(2)	XTAL precision		-500	-	-	500	ppm	
Gmax	Oscillator Gm	Vibrate	4	-	-	-	mA/V	
tSU(XTAL)(3) startup time		VCC is stable, crystal oscillator=8MHz	-	-	2.0	-	ms	
		VCC is stable, crystal oscillator=4MHz	-	-	4.0	-	ms	

1. Mass production test guarantee.

2. This parameter depends on the resonator used in the application system.

3. tSU(XTAL) is the start-up time, which is measured from the software enabling XTAL until a stable 8MHz oscillation frequency is obtained.

time. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications that meet crystal or resonator requirements (see

See figure below). CL1 and CL2 are usually the same size, CL1=CL2=2*(CL-Cs). Cs is PCB and MCU pin

ÿXTAL_INÿXTAL_OUTÿ stray capacitanceÿ

Resonators with integrated capacitors

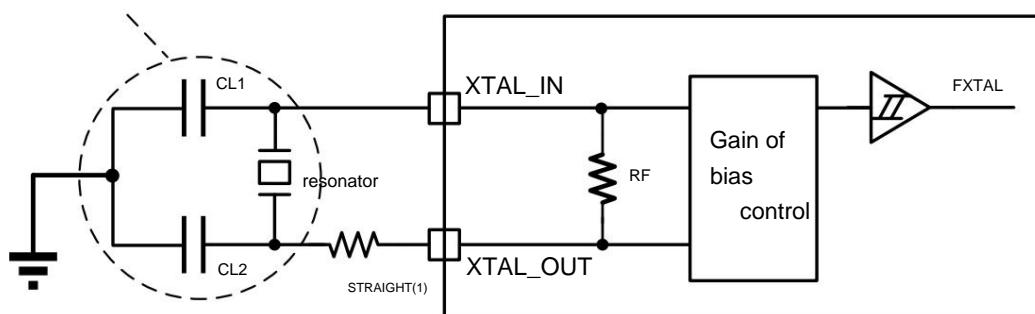


Figure 3-17 Typical application using 8 MHz crystal oscillator

1. The value of REXT depends on the crystal characteristics.

3.3.16.3 Low-speed external clock from crystal/ceramic resonator

A low-speed external clock can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. In application, harmonic The oscillator and load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and start-up settling time. About the resonator Please consult the crystal resonator manufacturer for details on performance (frequency, package, accuracy, etc.).

Table 3-32 XTAL32 oscillator characteristics

symbol	parameter	condition	Specification			unit
			Min	Type	Max	
FXTAL32	frequency	-	-	32.768	-	kHz
RF(1)	Feedback resistor	-	-	15	-	MΩ
IDD_XTAL32 power consumption		XTAL32DRV[2:0]=000	-	0.8	-	μA
AXTAL32(2)	XTAL32 precision	-	-500	-	500	ppm
Gmax	Oscillator Gm	-	5.6	-	-	uA/V
TSUXTAL32	start time(3)	VCC steady state	-	2	-	s

1. Mass production test guarantee.

2. This parameter depends on the resonator used in the application system.

3. TSUXTAL32 is the start-up time, which is measured from the software enabling XTAL32 until a stable 32.768 kHz vibration is obtained.

swing frequency this time. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, high quality external ceramic capacitors are recommended (see figure below). CL1 and CL2 are usually the same size,

CL1=CL2=2*(CL-Cs). Cs is PCB and MCU pin (XTAL32_IN, XTAL32_OUT) stray capacitance. If CL1 and CL2 are greater than 18pF, it is recommended to set

XTAL32DRV[2:0]=001 (large drive, the typical value of power consumption increases by 0.2uA).

Resonators with integrated capacitors

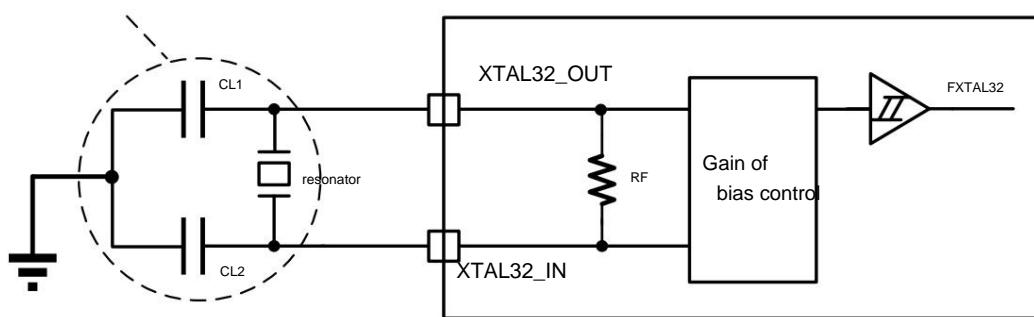


Figure 3-18 Typical application using 32.768 kHz crystal oscillator

3.3.17 Internal Clock Source Characteristics

3.3.17.1 Internal High Speed (HRC) Oscillator

Table 3-33 HRC oscillator characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
fHRC	frequency(1)	mode 1	-	16	-	-	MHz	MHz
		mode 2	-	20	-	-		
	User Adjustment Scale	-	-	-	-	0.2	%	%
		TA = -40 to 105°C	-2	-	-	2	%	%
		TA = -20 to 105°C -1.5	-	-	-	1.5	%	%
		TA = 25 °	-0.5	-	-	0.5	%	%
tst(HRC)	HRC Oscillator Oscillation Stabilization Time-	-	-	-	-	15	μs	μs

1. Mass production test guarantee.

3.3.17.2 Internal Medium Speed (MRC) Oscillator

Table 3-34 MRC oscillator characteristics

symbol	parameter	Min	Typ	Max	Unit			
fMRC(1)	frequency	7.2	8	8.8	MHz			
tst(MRC)	MRC Oscillator Settling Time	-	-	-	3	μs		

1. Mass production test guarantee.

3.3.17.3 Internal Low Speed (LRC) Oscillator

Table 3-35 LRC oscillator characteristics

symbol	parameter	Min	Typ	Max	Unit			
fLRC(1)	frequency	27.853	32.768	37	kHz			
tst(LRC)	LRC oscillator stabilization time	-	-	-	36	μs		

1. Mass production test guarantee.

3.3.17.4 SWDT dedicated internal low-speed (SWDTLRC) oscillator

Table 3-36 SWDTLRC Oscillator Characteristics

symbol	parameter	Min	Typ	Max	Unit			
fSWDTLRC(1)	frequency	9	10	11	kHz			
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	-	-	-	57.1	μs		

1. Mass production test guarantee.

3.3.18 12-bit ADC characteristics

Table 3-37 ADC characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VAVCC	power supply		1.8	-	3.6	IN		
VREFH(1)	Positive reference voltage		1.8	-	VAVCC	IN		
fADC	ADC conversion clock frequency	In super high speed/high speed operation mode VAVCC=2.4 ~3.6V	1	-	60		MHz	
		In super high speed/high speed operation mode VAVCC=1.8 ~2.4V	1	-	30			
		Ultra low speed operation mode	1	-	8			
VAIN	conversion voltage range		VAVSS	-	VREFH	IN		
RAIN	external input impedance	See formula 1 for details	-	-	50	k Ω		
RADC	sampling switch resistance		-	-	6	k Ω		
CADC	internal sample and hold capacitor-		-	-	4	7	pF	
tD	Trigger transition delay	fADC = 60 MHz	-	-	0.3	μ s		

Table 3-38 ADC Characteristics (continued)

symbol	parameter	condition	Min	Typ	Max	Unit	
tS	sampling time	fADC=60MHz	0.183		4.266	μs	
			11		255	1/fADC	
tCONV	Single channel total conversion time (including sampling time)	fADC = 60 MHz 12-bit resolution	0.4			μs	
		fADC = 60 MHz 10-bit resolution	0.36			μs	
		fADC = 60 MHz 8-bit resolution	0.33			μs	
		20 to 268 (sampling time tS+ successively approaching n-bit resolution+1)				1/fADC	
fS	Sampling Rate fADC = 60 MHz	12-bit resolution single ADC			2.5	Msps	
		12-bit resolution time interpolation Dual ADC			4.6		
tST	power on time		-		1	2	μs

1. VAVCC-VREFH<1.2V

Formula 1: RAIN maximum formula

$$= \frac{\bar{y}^1}{x \times \ln(2+2)}$$

The above equation (Equation 1) is used to determine the maximum external impedance that keeps the error below 1/4 LSB, where N = 12 (12-bit resolution), k is the number of sampling periods defined in the ADC_SSTR register.

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=60MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=60MHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	± 4.5	± 6	LSB
EO	offset error		± 3.5	± 6	LSB
EG	gain error		± 3.5	± 6	LSB
ED	Differential Linearity Error		± 1	± 2	LSB
HE	Integral Linearity Error		± 1.5	± 3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=30MHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	± 4.5	± 6	LSB
EO	offset error		± 3.5	± 6	LSB
EG	gain error		± 3.5	± 6	LSB
ED(1)	differential linearity error		± 1	± 2	LSB
EL(1)	integral linearity error		± 1.5	± 3	LSB

1. Mass production test guarantee.

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=30MHz Input source impedance <1k Ω VAVCC=1.8 ~2.4V	± 4.5	± 6	LSB
EO	offset error		± 3.5	± 6	LSB
EG	gain error		± 3.5	± 6	LSB
ED	Differential Linearity Error		± 1	± 2	LSB
HE	Integral Linearity Error		± 2	± 3	LSB

Table 3-42 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=8MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In ultra-low speed operation mode fADC=8MHz Input source impedance <1k Ω VAVCC=1.8 ~3.6V	± 4.5	± 6	LSB
EO	offset error		± 3.5	± 6	LSB
EG	gain error		± 3.5	± 6	LSB
ED	Differential Linearity Error		± 1	± 2	LSB
HE	Integral Linearity Error		± 2	± 3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=60MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=60MHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	± 5.5	± 7	LSB
EO	offset error		± 4.5	± 7	LSB
EG	gain error		± 4.5	± 7	LSB
ED	Differential Linearity Error		± 1.5	± 2	LSB
HE	Integral Linearity Error		± 2.0	± 3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=30MHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	± 5.5	± 7	LSB
EO	offset error		± 4.5	± 7	LSB
EG	gain error		± 4.5	± 7	LSB
ED(1)	differential linearity error		± 1.5	± 2	LSB
EL(1)	integral linearity error		± 2.0	± 3	LSB

1. Mass production test guarantee.

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In super high speed/high speed operation mode fADC=30MHz Input source impedance <1k Ω VAVCC=1.8 ~2.4V	± 5.5	± 7	LSB
EO	offset error		± 4.5	± 7	LSB
EG	gain error		± 4.5	± 7	LSB
ED	Differential Linearity Error		± 1.5	± 2	LSB
HE	Integral Linearity Error		± 2.5	± 3	LSB

Table 3-46 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=8MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
AND	absolute error	In ultra-low speed operation mode fADC=8MHz Input source impedance <1k Ω VAVCC=1.8 ~3.6V	± 5.5	± 7	LSB
EO	offset error		± 4.5	± 7	LSB
EG	gain error		± 4.5	± 7	LSB
ED	Differential Linearity Error		± 1.5	± 2	LSB
HE	Integral Linearity Error		± 2.5	± 3	LSB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 input channel input channel dynamic accuracy @ fADC=60MHz

symbol	parameter	condition	min	max	unit
ENOB effective	number of digits	In super high speed/high speed operation mode fADC=60MHz Input signal frequency=2kHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	10.6	-	Bits
SINAD Signal-to-Noise Harmonic Ratio			64	-	dB
SNR signal to noise ratio			66	-	dB
THD Total Harmonic Distortion			-	-70	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 input channel dynamic accuracy of input channel @ fADC=30MHz

symbol	parameter	condition	min	max	unit
ENOB effective	number of digits	In super high speed/high speed operation mode fADC=30MHz Input signal frequency=2kHz Input source impedance <1k Ω VAVCC=1.8~2.4V	10.4	-	Bits
SINAD Signal-to-Noise Harmonic Ratio			62	-	dB
SNR signal to noise ratio			64	-	dB
THD Total Harmonic Distortion			-	-67	dB

Table 3-49 ADC1_IN0~3, ADC12_IN4~IN7 input channel dynamic accuracy @ fADC=8MHz

symbol	parameter	condition	min	max	unit
ENOB effective	number of digits	In ultra-low speed operation mode fADC=8MHz Input signal frequency=2kHz Input source impedance <1k Ω VAVCC=1.8~3.6V	10.4	-	Bits
SINAD Signal-to-Noise Harmonic Ratio			62	-	dB
SNR signal to noise ratio			64	-	dB
THD Total Harmonic Distortion			-	-67	dB

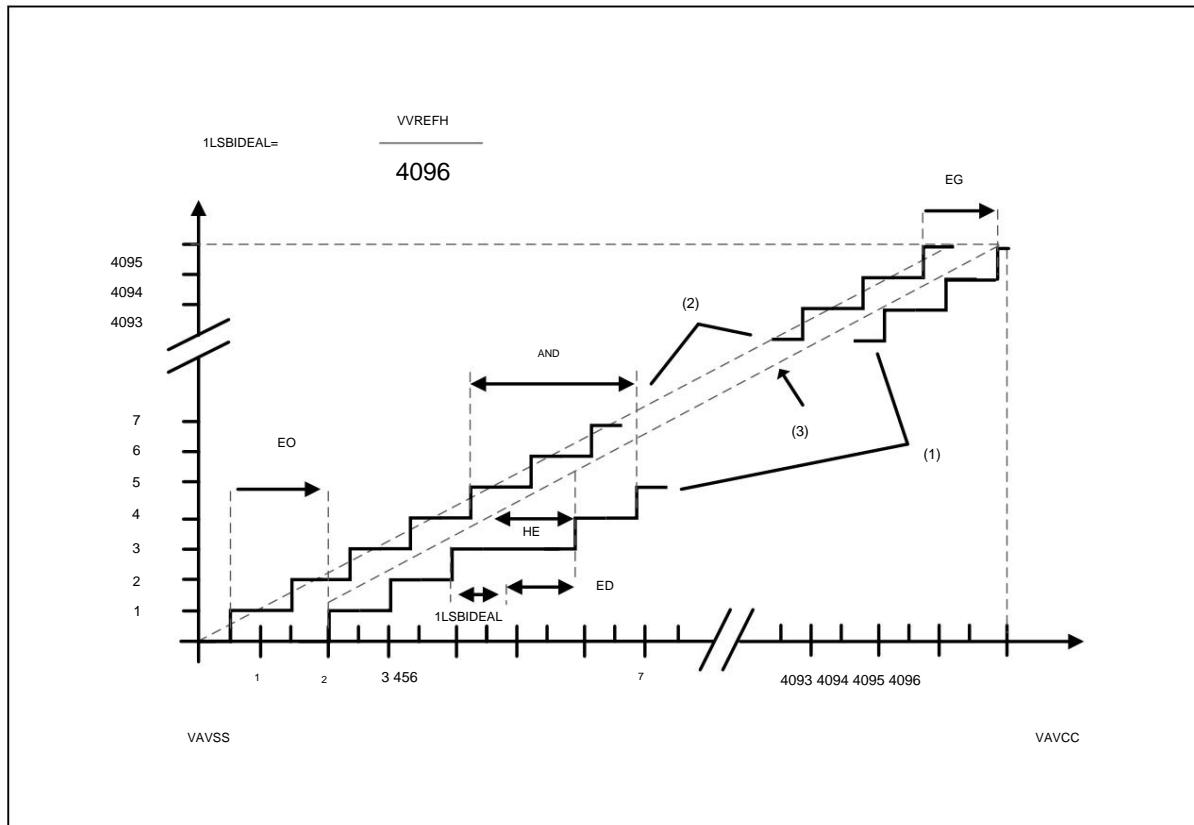


Figure 3-19 ADC Accuracy Characteristics

1. See also the table above.
2. Example of actual transfer curve.
3. Ideal transfer curve.
4. End-point relative lines.
5. ET = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.

EO = Offset Error: The deviation between the first actual transition and the first ideal transition.

EG = Gain Error: The deviation between the last ideal transition and the last actual transition.

ED = Differential Linearity Error: The maximum deviation between the actual step and the ideal.

EL = Integral Linearity Error: The maximum deviation between any actual transformation and the line associated with the endpoints.

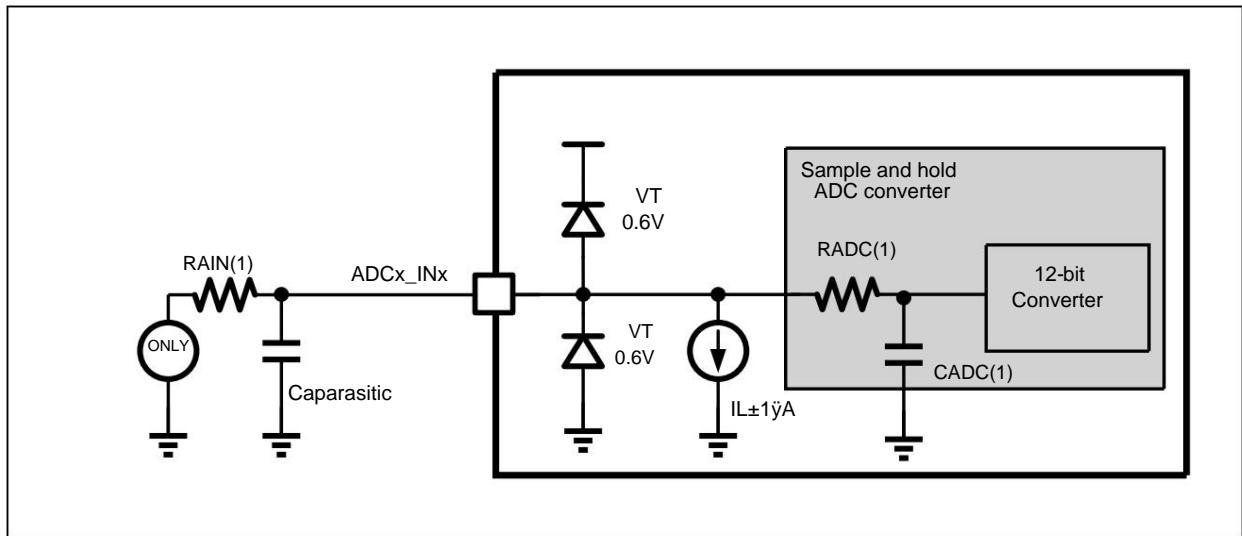


Figure 3-20 Typical connection using ADC

1. See Table 3-37 for RAIN, RADC , and CADC values.
2. Cparasitic means PCB capacitance (depending on soldering and PCB routing quality) and pad capacitance (approximately 5 pF). Higher values of Cparasitic result in less accurate conversions. To solve this problem, fADC should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below, depending on whether VREFH is connected to AVCC or not and the number of AVCC pins.

The 0.1 μ F capacitor should be a (good quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

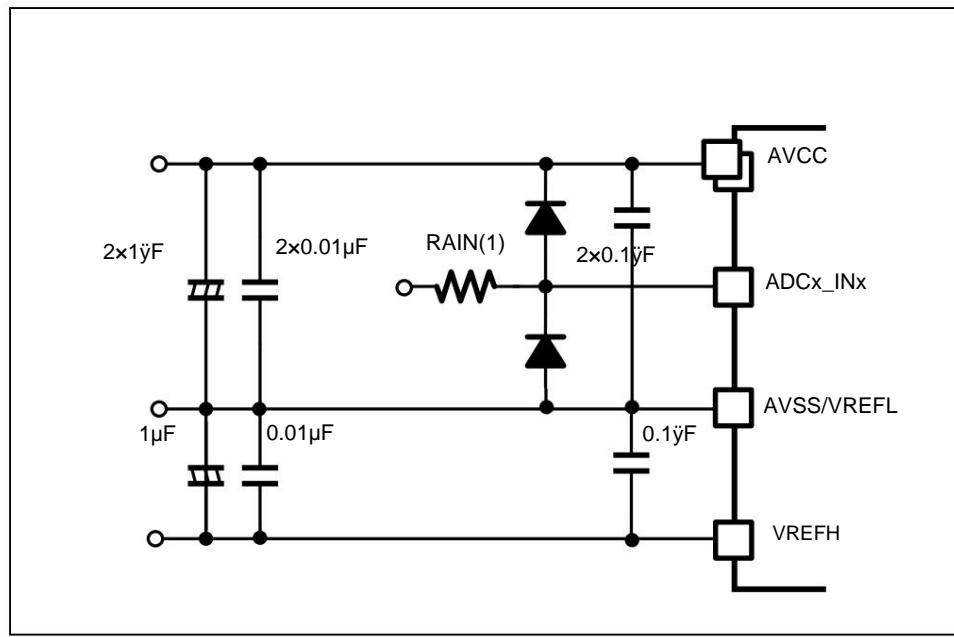


Figure 3-21 Example of decoupling power supply and reference power supply

3.3.19 DAC characteristics

Table 3-50 DAC characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VAVCC	Analog supply voltage		1.8	3.3	3.6	IN		
DNL	Differential nonlinearity error (between two consecutive codes deviation of -1LSB)					±2	LSB	
offset	Offset Error (measured at code (0x80) vs. difference between the ideal value VAVCC/2)					±2	LSB	
SETTLING	Setting Time (Full Scale: Applies to When DA0/DA1 reaches the final value ±4LSB, the maximum 8-bit input between the low input code and the highest input code input code conversion)					8	μs	

3.3.20 Comparator Characteristics

Table 3-51 Comparator characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VAVCC	analog supply voltage		1.8	3.3	3.6	IN		
WE	Input voltage range		0			VAVCC	IN	
Tcmp	compare time	Comparator resolution voltage = 100mV		50	100	ns		
Tset	input channel switching stabilization time			100	200	ns		

3.3.21 Adjustable Gain Amplifier Characteristics

Table 3-52 Gain adjustable amplifier characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
VAVCC	analog supply voltage	-	1.8	3.3	3.6	IN
VOS(1)	input offset voltage	-	-8	-	8	mV
VI	input voltage range	-	0.1*VAVCC/Gain	-	0.9*VAVCC/Gain V	
GE gain error	use external port	Gain=2(1)	-1	-	1	%
		Gain=2.133	-1	-	1	%
		Gain=2.286	-1	-	1	%
		Gain=2.667	-1	-	1	%
		Gain=2.909	-1	-	1	%
		Gain=3.2	-1.5	-	1.5	%
		Gain=3.556	-1.5	-	1.5	%
		PGAVS as PGA	Gain=4.0	-1.5	1.5	%
		Negative input	Gain=4.571	-2	2	%
			Gain=5.333	-2	2	%
			Gain=6.4	-3.0	3.0	%
			Gain=8	-3.0	3.0	%
			Gain=10.667	-4.0	4.0	%
			Gain=16	-4.0	4.0	%
			Gain=32(1)	-7.0	7.0	%
	the simulated ground AVSS for phase input	Gain=2(1)	-2	-	2	%
		Gain=2.133	-2	-	2	%
		Gain=2.286	-2	-	2	%
		Gain=2.667	-2	-	2	%
		Gain=2.909	-2	-	2	%
		Gain=3.2	-2.5	-	2.5	%
		Gain=3.556	-2.5	-	2.5	%
		AVSS for Negative for PGA	Gain=4.0	-2.5	2.5	%
			Gain=4.571	-3.0	3.0	%
			Gain=5.333	-3.0	3.0	%
			Gain=6.4	-4.0	4.0	%
			Gain=8	-4.0	4.0	%
			Gain=10.667	-5.0	5.0	%
			Gain=16	-5.0	5.0	%
			Gain=32(1)	-8.0	8.0	%

1. Mass production test guarantee.

3.3.22 Temperature sensor

Table 3-53 Temperature sensor characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
TL	The relative accuracy is calibrated individually for each chip according to the user manual					±5 °		

3.3.23 Memory Characteristics

3.3.23.1 Flash memory

When the device is shipped to the customer, the flash memory has been erased.

Table 3-54 Flash memory features

symbol	parameter	condition	Min	Typ	Max	Unit		
IVCC	supply current	Read mode, VCC=1.8 V~3.6V	-	-	-	5	mA	
		Programming mode, VCC=1.8V ~3.6V	-	-	-	10		
		Block erase mode, VCC=1.8 V~3.6V	-	-	-	10		
		Full erase mode, VCC=1.8 V~3.6V	-	-	-	10		

Table 3-55 Flash programming and erasing time

symbol	parameter	condition	minimum value	typical value	maximum value	unit
Tprog(1)	Word programming time single programming mode	43+2* Thclk(2) 48+4* Thclk(2)			53+6* Thclk(2)	μs
	Word programming time Continuous programming mode	12+2* Thclk(2) 14+4* Thclk(2)			16+6* Thclk(2)	μs
Terase(1)	block erase time -		16+2* Thclk(2) 18+4* Thclk(2)		20+6* Thclk(2)	ms
Tmas(1)	full erase time-		16+2* Thclk(2) 18+4* Thclk(2)		20+6* Thclk(2)	ms

1. Mass production test guarantee.

2.Thclk is 1 cycle of CPU clock.

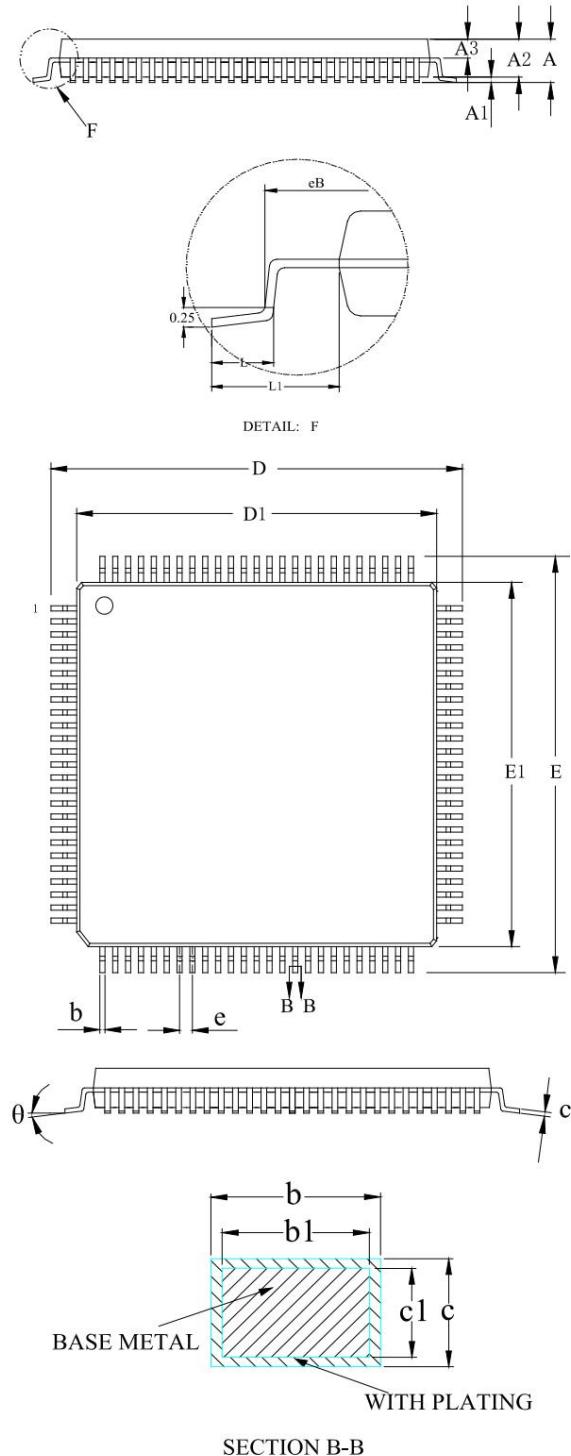
Table 3-56 Flash memory erasable times and data retention period

symbol	parameter	condition	value	unit
			minimum value	
Nend	Program, block erase times TA = 85°C		10	kcycles
Nend	Total erasure times	TA = 85y	10	kcycles
Tret	Data retention period	TA = 85y after 10 kcycles	10	Years

4 Package Information

4.1 Package Dimensions

LQFP100 package

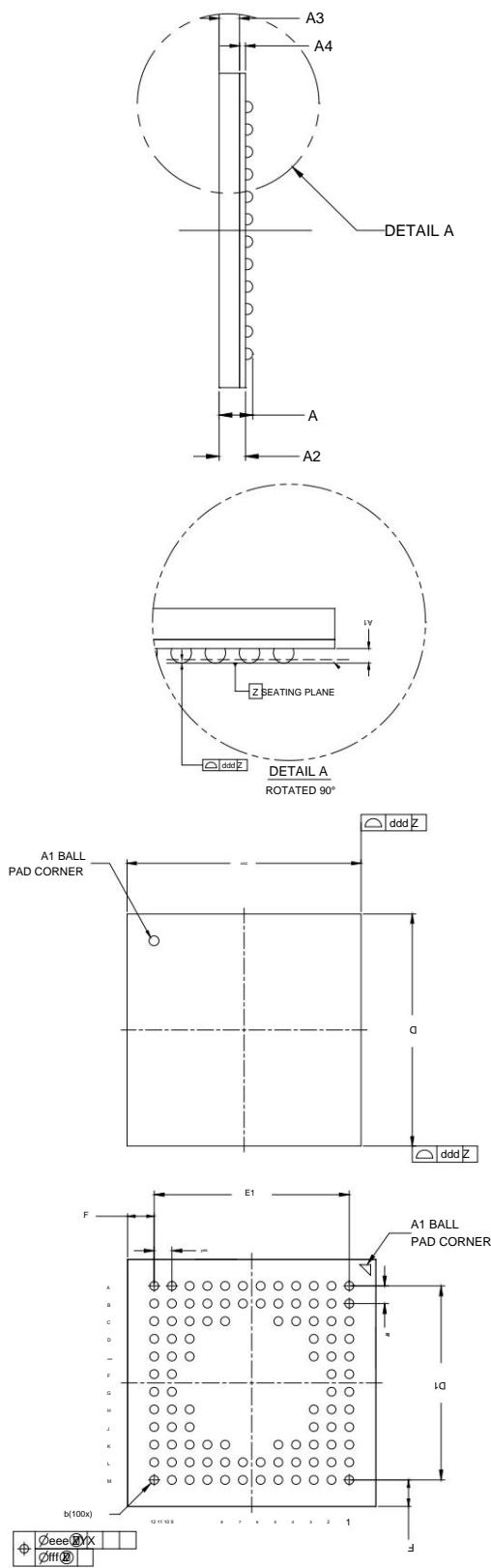


Symbol	14x14 Millimeter		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
i	0	-	7°
It is 0.50BSC			
L	0.45	-	0.75
1.00 REF			

NOTE:

- Dimensions "D1" and "E1" do not include mold flash.

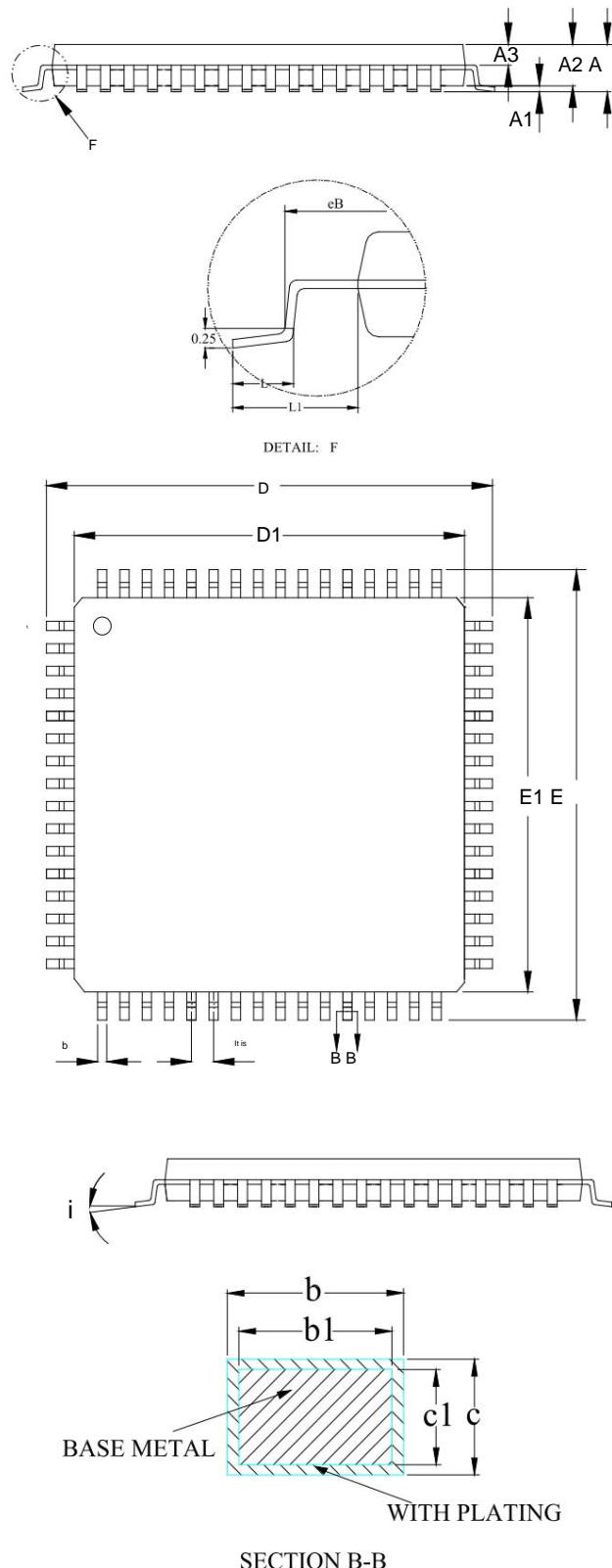
VFBGA100 package



Symbol	7x7 Millimeter		
	Min	Name	Max
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3	0.45REF		
A4	0.13REF		
b	0.20	0.25	0.30
d	6.90	7.00	7.10
D1	-	5.5	-
ddd	6.90	7.00	7.10
E1	-	5.5	-
It is	-	0.5	-
F	0.75REF		
ddd	-	0.10	-
eee	-	0.15	-
fff	-	0.05	-

BOTTOM VIEW

LQFP64 package



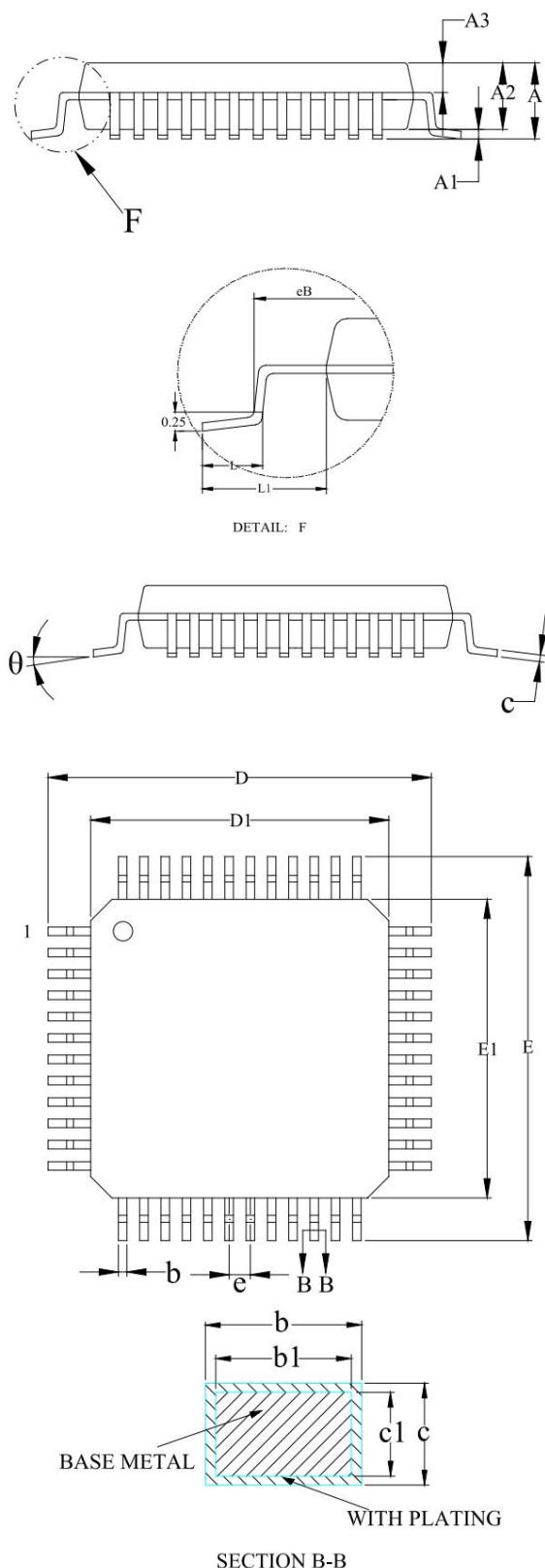
Symbol	10x10 Millimeters		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
d	11.80 12.00 12.20		
D1	9.90	10.00 10.10	
AND	11.80 12.00 12.20		
E1	9.90	10.00 10.10	
0.50BSC			
l	0.45	-	0.75
L1	1.00 REF		
i	0°	-	7°

NOTE:

- Dimensions "D1" and "E1" do

not include mold flash.

LQFP48 package

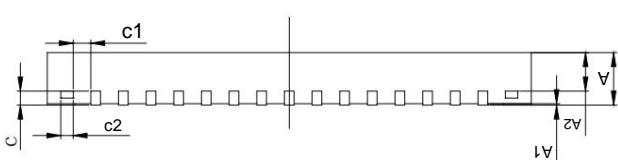
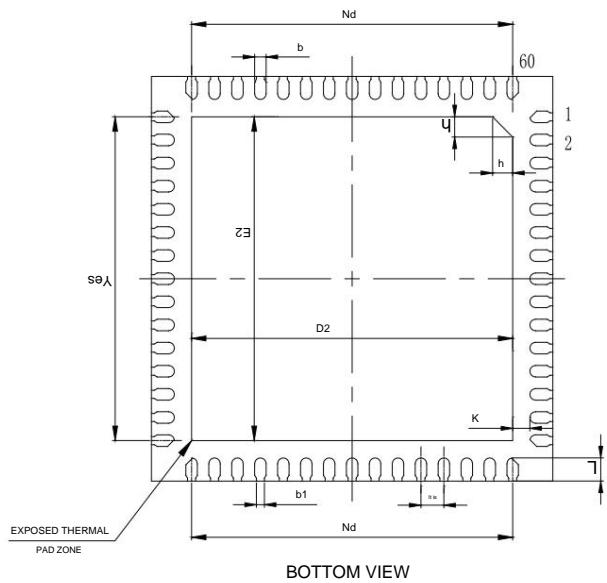
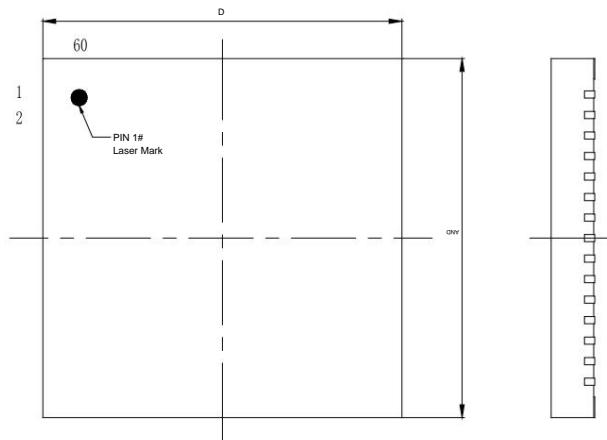


Symbol	7x7 Millimeter		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
AND	8.80	9.00	9.20
E1	6.90	7.00	7.10
It is 0.50BSC			
L	0.40	-	0.65
L1	1.00 REF		
i	0	-	7°

NOTE:

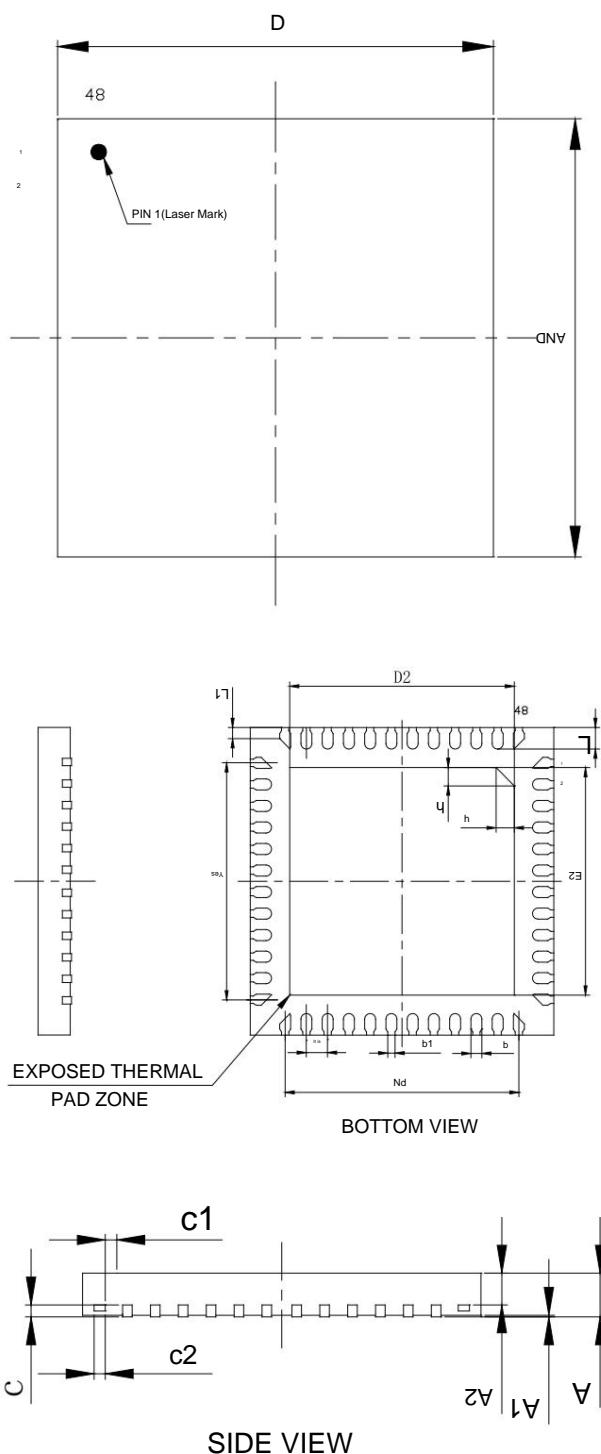
- Dimensions “D1” and “E1” do not include mold flash.

QFN60 package



Symbol	7x7 Millimeter		
	Min	Name	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.547REF		
b	0.15	0.20	0.25
b1	0.14REF		
c	0.20REF		
c1	0.255REF		
c2	0.18REF		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd	5.60BSC		
It is	0.40BSC		
and	6.90	7.00	7.10
E2	5.50	5.60	5.70
Yes	5.60BSC		
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

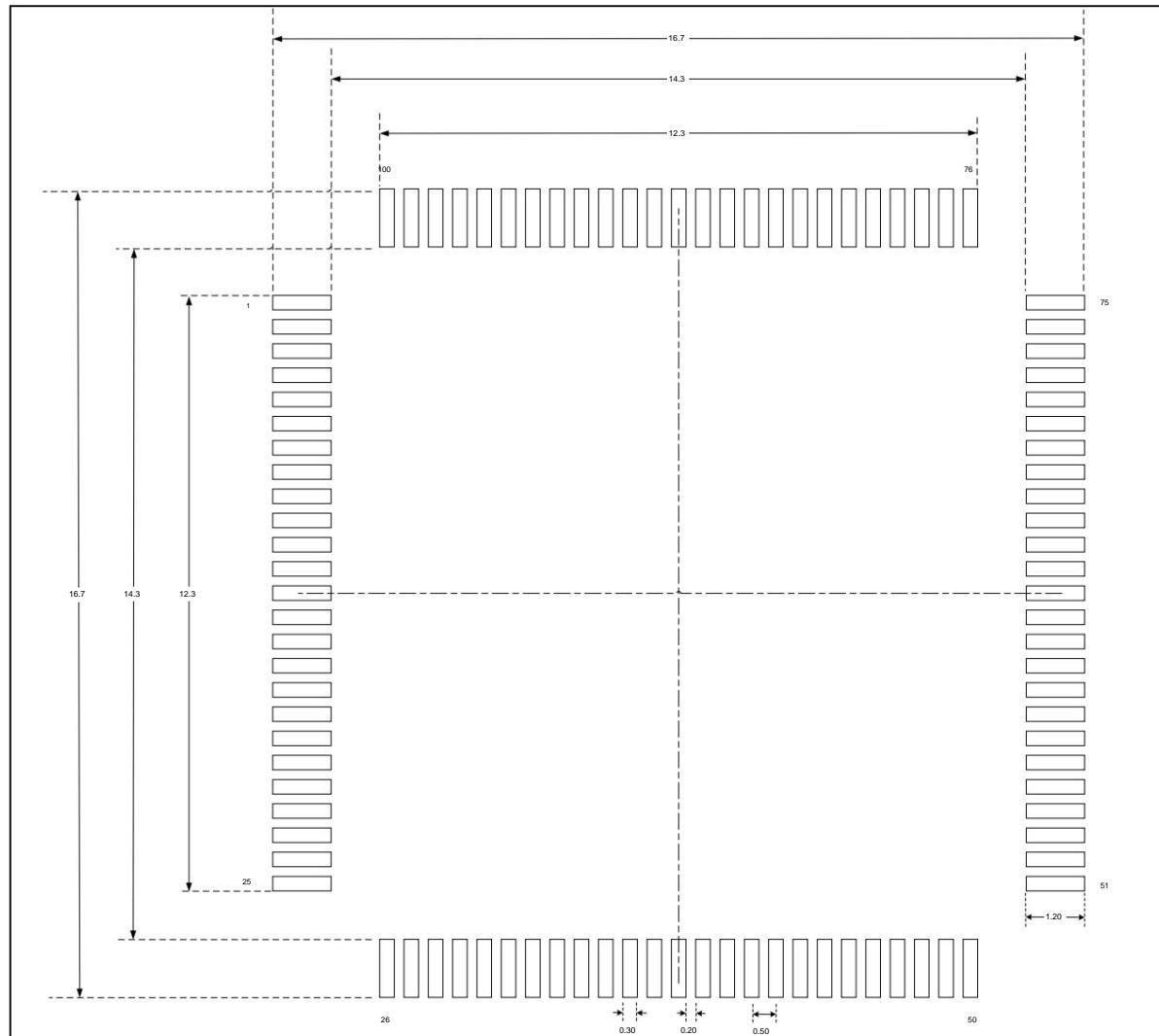
QFN48 package



Symbol	5x5 Millimeter		
	Min	Name	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.40REF		
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
c1	0.145REF		
c2	0.140REF		
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
0.35BSC			
Yes	3.85BSC		
Nd	3.85BSC		
-	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F carrier size	154 x 154		

4.2 Pad diagram

LQFP100 package (14mm x 14mm)

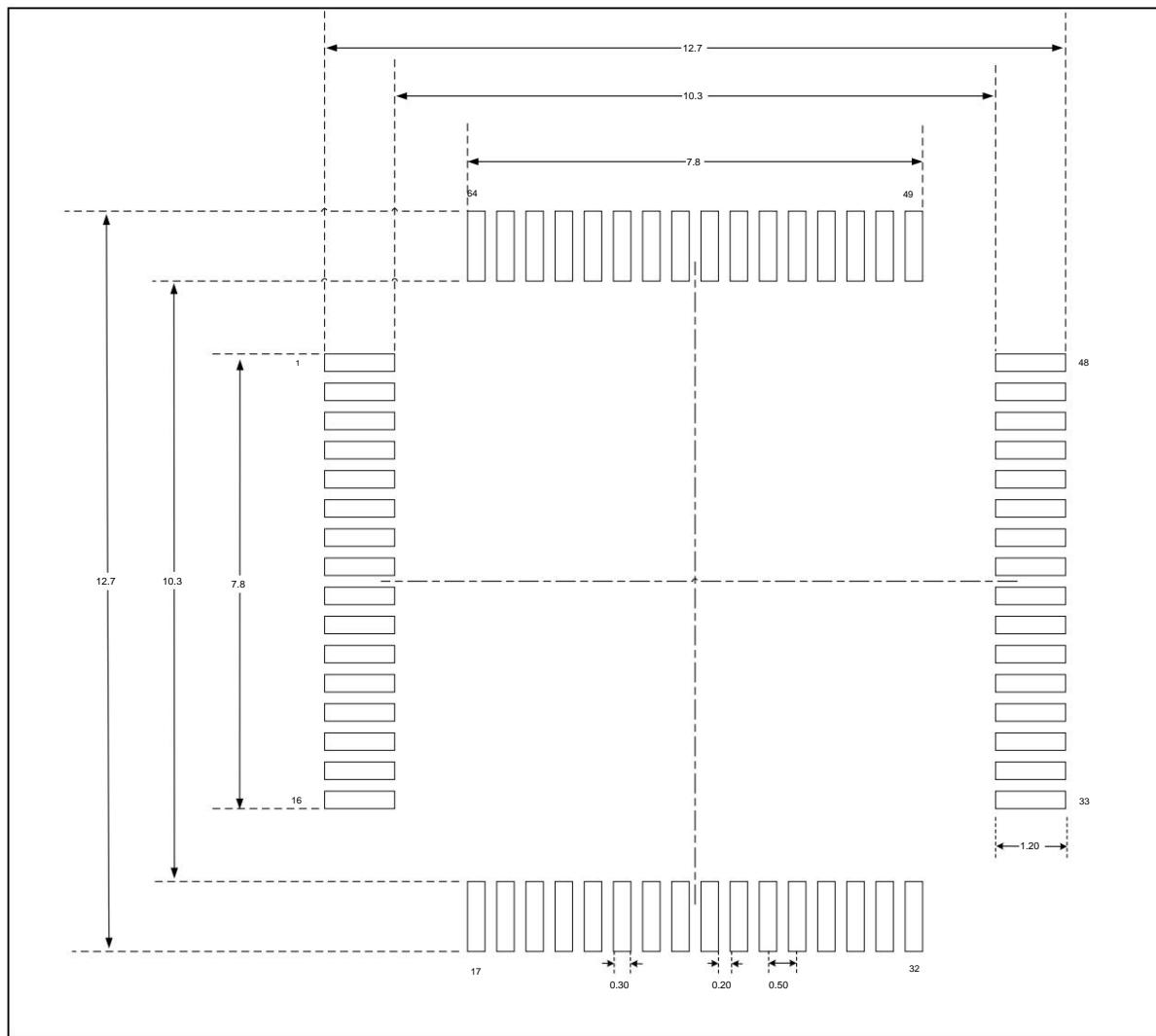


NOTE:

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

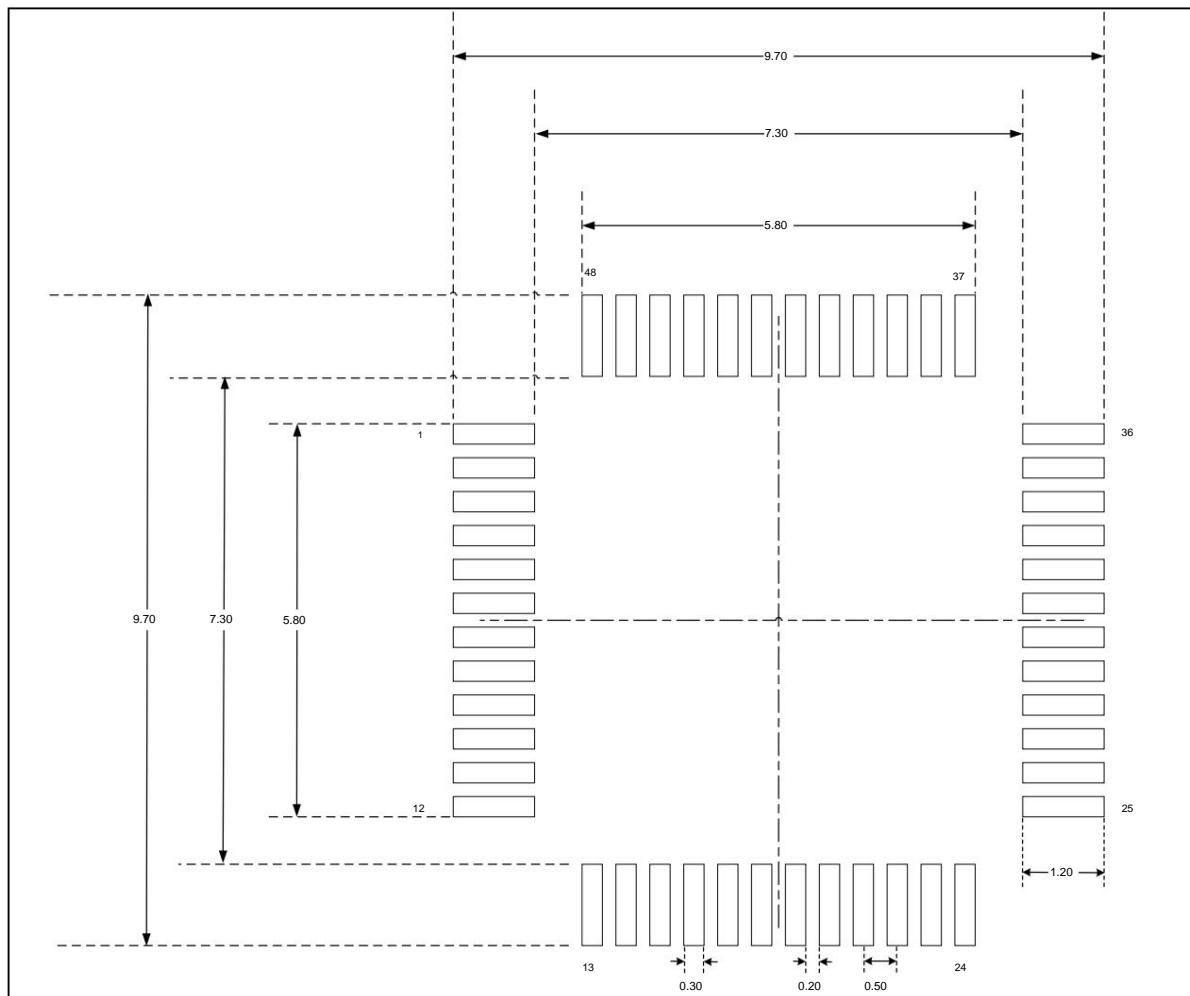
LQFP64 package (10mm x 10mm)

**NOTE:**

- Dimensions are expressed in millimeters.

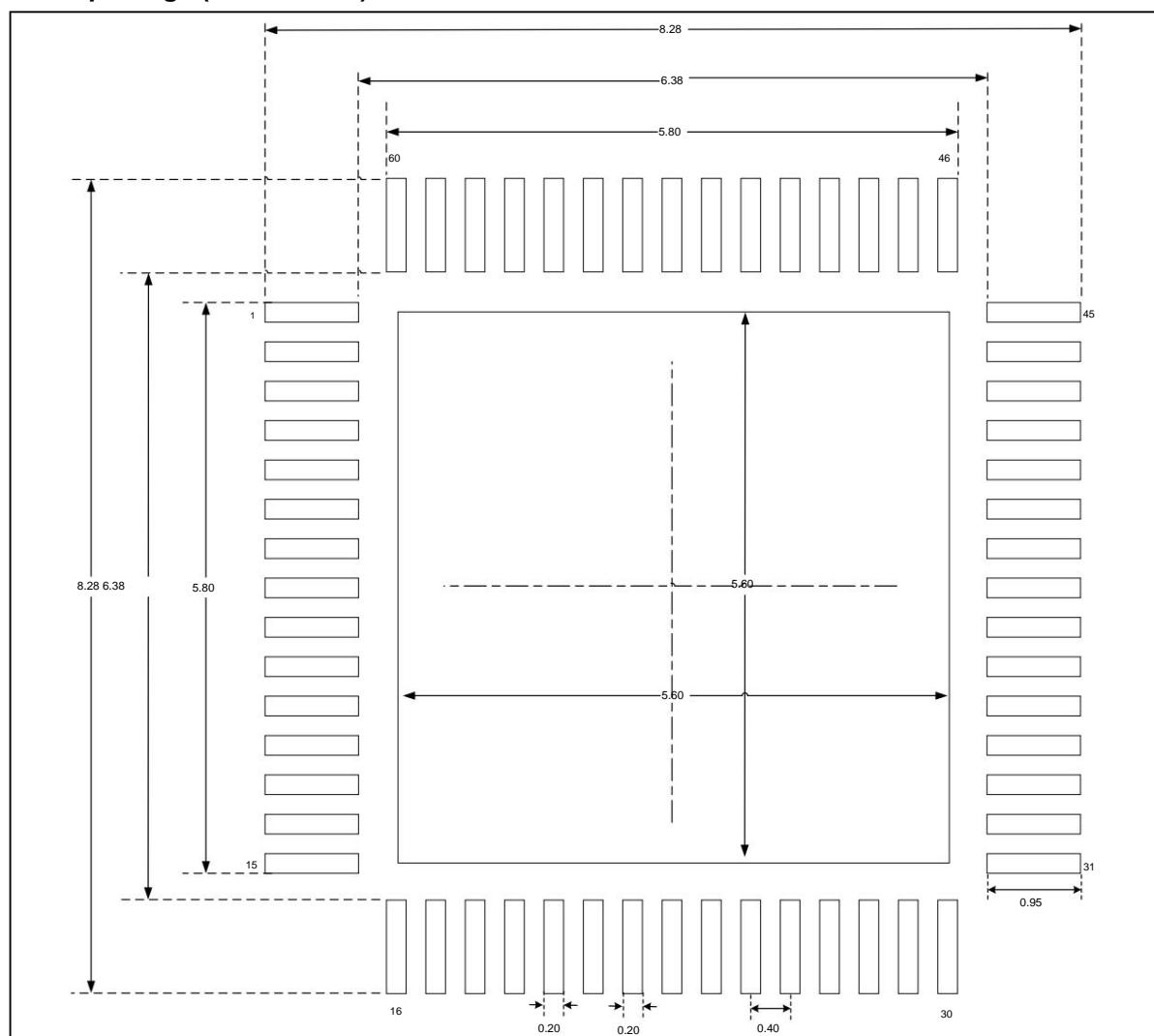
- Dimensions are for reference only.

LQFP48 package (7mm x 7mm)

**NOTE:**

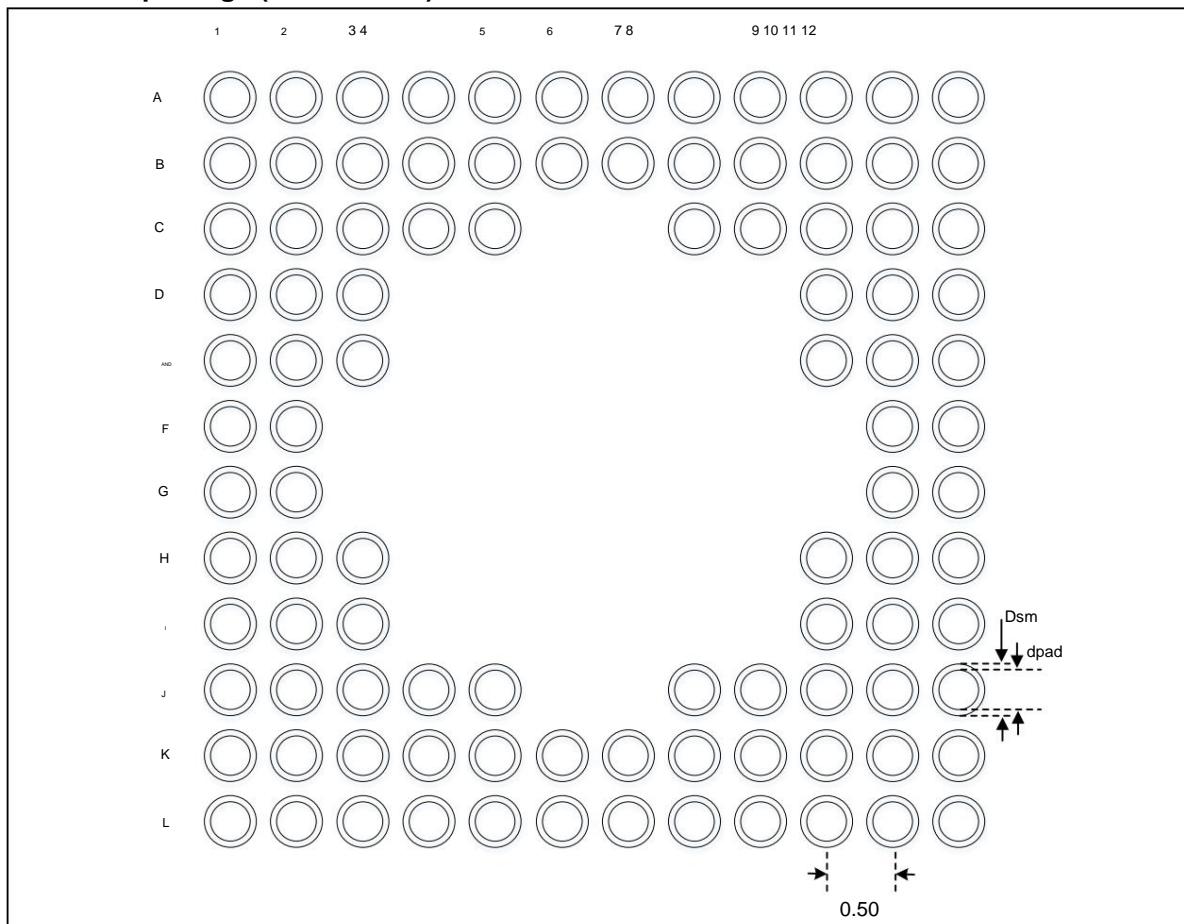
- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

QFN60 package (7mm x 7mm)**NOTE:**

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

VFBGA100 package (7mm x 7mm)**NOTE:**

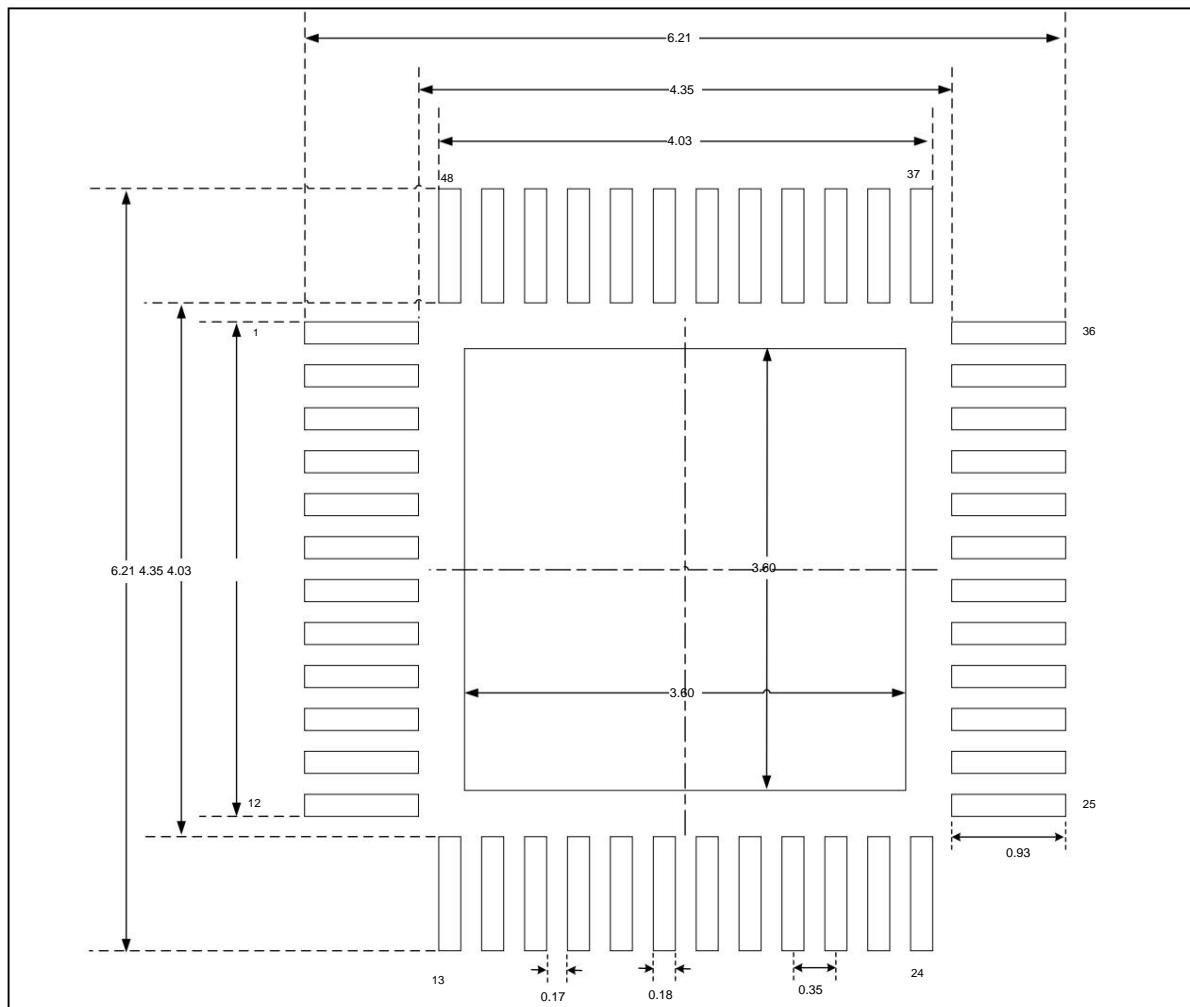
- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

VBGA100 recommended PCB design rules(0.5mm pitch)

Dimension	Recommended values
Pitch	0.5mm
dpad	0.240mm
Dsm	0.340mm typ. depends on the soldermask registration tolerance
Stencil opening	0.240mm
Stencil thickness	Between 0.100mm and 0.125mm

QFN48 package (5mm x 5mm)

**NOTE:**

- Dimensions are expressed in millimeters.

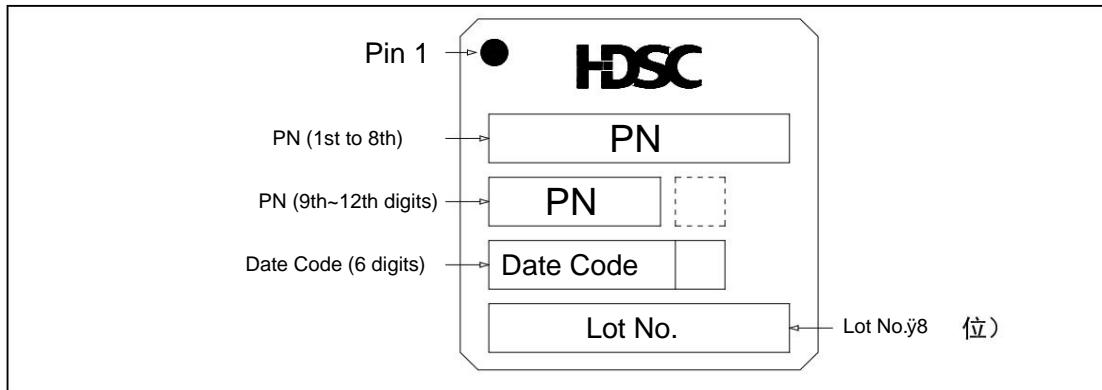
- Dimensions are for reference only.

4.3 Screen printing instruction

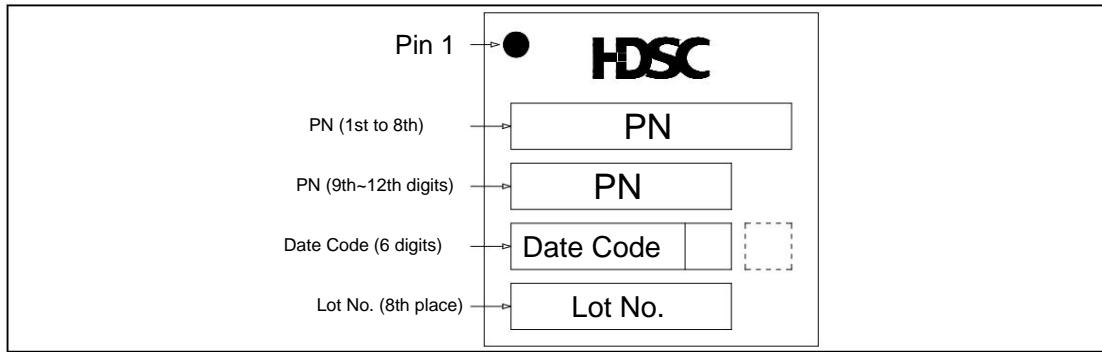
The Pin 1 position and information description of the silkscreen on the front of each package are given below.

LQFP100 package (14mm x 14mm) / LQFP64 package (10mm x 10mm)

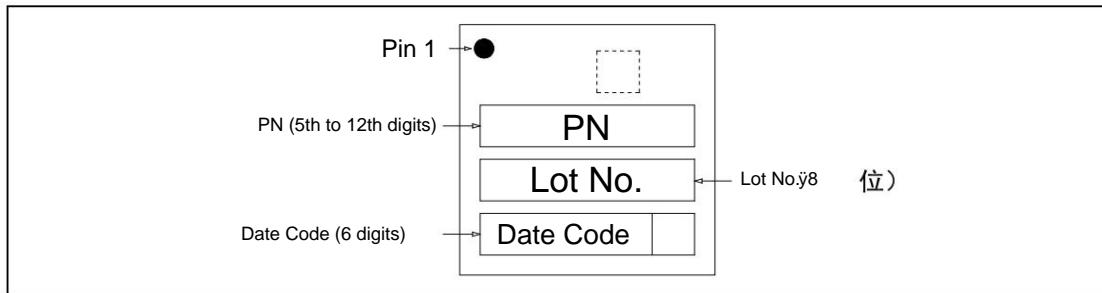
LQFP48 package (7mm x 7mm)



QFN60 package (7mm x 7mm) / VFBGA100 package (7mm x 7mm)



QFN48 package (5mm x 5mm)



Notice:

- The blank boxes in the above figure indicate optional marks related to production, which are not described in this section.

4.4 Package Thermal Resistance Coefficient

When the packaged chip works at the specified working environment temperature, the junction temperature T_j ($^{\circ}$ C) on the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

θ_{amb} refers to the working environment temperature when the packaged chip is working, the unit is $^{\circ}$ C;

θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is $^{\circ}$ /W;

P_D is equal to the sum of internal power consumption and I/O power consumption of the chip, and the unit is W. The internal power consumption of the chip is the product's $IDD \times VDD$, I/O

Power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually, the value of this part is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 4-1 Thermal resistance coefficient of each package

Package Type and Size	Thermal Resistance Junction ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	$^{\circ}$ /W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	$^{\circ}$ /W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	$^{\circ}$ /W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10%	$^{\circ}$ /W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10%	$^{\circ}$ /W

5 Ordering information

Product number	HC32F460JEU-A-QFN48TR HC32F460JETA-LQFP48 HC32F460KEUA-QFN60TR HC32F460KETA-LQFP64			HC32F460PETB-LQFP100 HC32F460PEHB-VFBGA100 HC32F460JCTA-LQFP48 HC32F460KCCTA-LQFP64					HC32F460PCTB-LQFP100
Main frequency (MHz)	200	200	200	200	200	200	200	200	200
kernel	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512	512	512	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5 LQFP100 (14*14) e=0.5 VFBGA100 (7*7) e=0.5			LQFP48 (7*7) e=0.5 LQFP64 (10*10) e=0.5 LQFP100 (14*14) e=0.5		
GPIO	38	38	50	52	83	83	38	52	83
Minimum working voltage	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Maximum working voltage	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
16-bit timer	11	11	11	11	11	11	11	11	11
Motor Control Timer	3	3	3	3	3	3	3	3	3
12-bit ADC conversion unit	2	2	2	2	2	2	2	2	2
12-bit ADC channel count	10	10	15	16	16	16	10	16	16
Comparators	3	3	3	3	3	3	3	3	3
Amplifier PGA	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I2S	4	4	4	4	4	4	4	4	4
I2C	3	3	3	3	3	3	3	3	3
US(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
Full Speed USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
AES128	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
SHA256	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
WHITE	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
CRC	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
KEYSCAN	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
RTC	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
FLASH physical encryption	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
Shipping method	Tape	Plate	Tape	Plate	Plate	Plate	Plate	Plate	Plate

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

Version number	Revision date	Revision content
Rev1.0	2019/11/12	First release
Rev1.1	2020/01/10	<p>1) Add 256KB product description to the full text; 2) Add VFBGA package description to the full text; 3) Modify the current max value at 105°C in power-down mode in the electrical characteristics; 4) Update the silkscreen instructions.</p>
Rev1.2	2020/08/26	<p>1) Add the description of ultra-high-speed operation mode, update CoreMark/DMIPS, and add the description of ultra-high-speed mode. renew Functional block diagram;</p> <p>2) Add 256KB model to the pin configuration diagram; 3) Add pad schematic diagram and package thermal resistance coefficient; 4) Add BOR/PVD characteristics and current characteristics in ultra-high speed mode; 5) Update JTAG/SWJ debug port pins;</p>
Rev1.3	2021/12/10	<p>1) Revise the statement, add the A2/c1/c2 size of QFN48/60 in the package size, and modify the data storage in the flash memory the term;</p> <p>2) External main clock crystal oscillator: (4-24MHz) changed to (4-25MHz); 3) Functional block diagram modification: USB_DMA -> USBFS_DMA; I2S_1 -> I2S_2; Add AOS; 4) 1.4.6 Address 0x00000400H~0x0000041FH -> 0x0000_0400~0x0000_041F 0x00000408~0x0000041F -> 0x0000_0408~0x0000_041F 5) Add the introduction description of "Automatic Operating System (AOS)" and update the description of "KEYSCAN"; 6) Name correction and description optimization; 7) Modify the recommended configuration of bypass capacitors for analog power pins in the power scheme diagram, delete 10nF capacitors, and 10uF capacitors Modified to 1uF; 8) Add parameter items in the reset and power control module characteristic table: TIPVD1/TIPVD2/TINRST/TRSTBOR TRSTTAO->TRSTPOR 9) 3.3.12 Add CAN2.0B interface feature description; 10) In the PLL characteristics, the Max value of fPLL_IN is changed from 24MHz to 25MHz, and the Jitter characteristic is added; 11) 3.3.16.1 The maximum value of fXTAL_EXT is changed to 25MHz; 12) 3.3.16.2 Added the precision index of the external high-speed oscillator XTAL, and modified the description of CL1 and CL2; 13) 3.3.16.3 Added the accuracy index of the external low-speed oscillator XTAL32, and modified the CL1 and CL2 related description.</p>
Rev1.4	2022/03/09	Company Logo updated.
Rev1.41	2022/03/29	<p>1) 3.3.13 USB interface characteristics RPD delete MAX, MIN value, add Typ value 15ky;</p> <p>3.3.16 tSU(XTAL) startup time removes the maximum value and adds the typical value</p> <p>2) 4.1 LQFP100/LQFP64/LQFP48 b MAX value changed to 0.27</p>
Rev1.42	2022/09/14	<p>1) 2.1 "PH0/XTAL_IN" in the pin configuration diagram of each package is changed to "PH0/XTAL_EXT/XTAL_OUT", "PH1/XTAL_OUT" changed to "PH1/XTAL_IN", the style of QFN60 pin configuration diagram is modified, and the QFN48 pin configuration diagram is added;</p>

Version number	Revision date	Revision content
		<p>2.2 "PH0/XTAL_IN" is changed to "PH0/XTAL_EXT/XTAL_OUT", "PH1/XTAL_OUT" changed to "PH1/XTAL_IN";</p> <p>2.3 "XTAL_OUT" is changed to "XTAL_EXT/XTAL_OUT" and description is added "XTAL_EXT external clock input";</p> <p>2) 3.3.16.1 "XTAL_IN" is changed to "XTAL_EXT";</p> <p>3.3.16.2 In Figure 3-17, the names of the "XTAL_IN" and "XTAL_OUT" pins are interchanged;</p> <p>3.3.18 In Figure 3-21, the capacitor value of 10uF is changed to 1uF.</p>

If you have any comments or suggestions during the purchase and use, please free to contact us.

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