



HC32F460 series

32 -bit ARM® Cortex® -M4 microcontroller

HC32F460PETB-LQFP100 / HC32F460PEHB-VFBGA100

HC32F460KETA-LQFP64 / HC32F460KEUA-QFN60TR

HC32F460JETA-LQFP48 / HC32F460JEUA-QFN48TR

HC32F460PCTB-LQFP100 / HC32F460KCTA-LQFP64

HC32F460JCTA-LQFP48

data sheet



Product Features

ARM Cortex-M4 32bit MCU+FPU up to 250DMIPS up to 512KB Flash 192KB SRAM USB FS Device/Host

14 Timers, 2 ADCs, 1 PGA, 3 CMPS, 20 communication ports

ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU,

DSP supporting SIMD instructions, and CoreSight standard debugging unit. The highest operating frequency is 200MHz, and the Flash acceleration unit realizes 0-wait program execution, reaching the computing performance of 250DMIPS or

680Coremarks Built-in memory

– Maximum 512KByte Flash memory, support security

Protection and Data Encryption*1

– Maximum 192KByte of SRAM, including 32KByte

200MHz single-cycle access to high-speed RAM, 4KByte

Retention RAM

Power, Clock, Reset Management –

System Power (Vcc): 1.8-3.6V – 6 Independent

Clock Sources: External Main Clock Crystal (4- 25MHz), External Sub-

Crystal (32.768kHz), Internal High Speed RC (16/20MHz),

internal medium speed RC (8MHz),

Internal low-speed RC (32kHz), internal WDT dedicated RC (10kHz) –

including power-on reset (POR), low voltage detection reset

(LVDR), Port Reset (PDR) including 14 types

Reset source, each reset source has an

independent flag Low

power operation – peripheral functions can be

turned off or on independently – three low power modes: Sleep, Stop, Power down 200Mbps high-speed access (XIP) – 1 CAN, support ISO11898-1 standard protocol – 1 USB 2.0 FS, built-in PHY, support Device/

Every time

– 2 SDIO, support SD/MMC/eMMC format – 1 QSPI, support

model

standard protocol – 1 USB 2.0 FS, built-in PHY, support Device/

– Support ultra-high speed mode in Run mode and Sleep mode,

Host

Switching between high speed mode and ultra low speed mode

– Data encryption function

– Standby power consumption: typ.90uA@25°C in Stop mode, as low

– AES/HASH/TRNG

as 1.8uA@25°C in Power down mode –

– Package form:

Support 16 ports wake-up in Power down mode,

LQFP100 14x14mm VFBGA100 7x7mm

Support ultra-low power consumption RTC work, 4KByte SRAM

LQFP64 10x10mm QFN60 7x7mm

to

QFN48 5x5mm

LQFP48 7x7mm

maintain data - standby fast wake-up, stop mode wake-up as fast as 2us,

The fastest wake-up from Power down mode is 20us

Peripherals support the system to significantly reduce the CPU processing load

*1 :about Flash

– 8-channel dual-master DMAC

For specific specifications of security protection and data encryption, please consult the sales window.

– DMAC for USBFS



statement

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1 Introduction (Overview)

HC32F460 series is based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200MHz

High-performance MCUs. The Cortex-M4 core integrates a floating-point unit (FPU) and DSP to achieve single-precision floating-point calculations

Arithmetic operations, support all ARM single-precision data processing instructions and data types, and support a complete DSP instruction set. kernel

The MPU unit is integrated, and the DMAC-specific MPU unit is superimposed at the same time to ensure the security of the system operation.

The HC32F460 series integrates high-speed on-chip memory, including a maximum of 512KB of Flash and a maximum of 192KB of SRAM.

Integrate the Flash access acceleration unit to realize the single-cycle program execution of the CPU on the Flash. polled bus matrix

Support multiple bus masters to access memory and peripherals at the same time, improving operating performance. The bus master includes CPU, DMA,

USB-specific DMA, etc. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events

It can significantly reduce the transaction processing load of the CPU.

The HC32F460 series integrates rich peripheral functions. Including 2 independent 12bit 2MSPS ADCs, 1 gain

Adjustable PGA, 3 voltage comparators (CMP), 3 multi-functional 16bit PWM Timer (Timer6) supporting 6 channels

Complementary PWM output, 3 motor PWM Timer (Timer4) supports 18 complementary PWM outputs, 6 16bit

The general-purpose Timer (TimerA) supports 3-way 3-phase quadrature encoding input and 48-way Duty independently settable PWM output,

11 serial communication interfaces (I2C/UART/SPI), 1 QSPI interface, 1 CAN, 4 I2S support audio

PLL, 2 SDIOS, 1 USB FS Controller with on-chip FS PHY supporting Device/Host.

The HC32F460 series supports wide voltage range (1.8-3.6V), wide temperature range (-40-105°C) and various low power consumption modes

Mode. Super high-speed mode (≥200MHz) and high-speed mode (≥168MHz) can be switched in Run mode and Sleep mode

and ultra-low speed mode (≤8MHz). Support fast wake-up from low power consumption mode, the fastest wake-up from STOP mode is 2us,

The fastest wake-up from Power Down mode is 20us.

typical application

HC32F460 series provide 48pin, 64pin, 100pin LQFP package, 48pin, 60pin QFN package,

The 100pin VFBGA package is suitable for high-performance motor frequency conversion control, intelligent hardware, IoT connection modules and other fields.

1.1 Model naming rules

HC32 F 4 6 0 J E U A

Xiaohua Semiconductor

CPU bit width

32: 32bit

product type

F: Universal

CPU type

4: Cortex-M4

Performance ID 6: High

Performance

Function configuration identification code

0: configuration 1

pin count

J: 48Pin

K: 60Pin / 64Pin

P: 100Pin

FLASH capacity

C: 256KB

E: 512KB

package type

T: LQFP

In: QFN

H: VFBGA

Ambient temperature range

B: -40-105°C, industrial grade

A: -40-85°C, industrial grade

1.2 Model function comparison table

Function	Product number																	
	HC32F4 60PEHB	HC32F4 60PETB	HC32F4 60PCTB	HC32F4 60KETA	HC32F4 60 KCTA	HC32F4 60JETA	HC32F4 60JCTA	HC32F4 60 KNOW	HC32F4 60 MORE									
Flash Memory KB	512	512	256	512	256	512	256	512	512									
pin count	100	100	100	64	64	48	48	48	60									
Number of GPIOs	83	83	83	52	52	38	38	38	50									
5V Tolerant GPIO Count	81	81	81	50	50	36	36	36	48									
encapsulation	VFBGA	LQFP					QFN											
temperature range	-40-105°C			-40-85°C														
Power supply voltage range	1.8 ~ 3.6 V																	
OTP Byte	960																	
SRAM KB	192																	
DMA	2unit * 4ch																	
external port interrupt	EIRQ * 16vec + NMI * 1ch																	
Communication Interfaces (in brackets is each ch minimum required I)	UART	4ch*2ch																
	SPI	4ch*3ch																
	2C	3ch*2ch																
	I2S	4ch*3ch																
	CAN	1ch*2ch																
	QSPI	1ch*6ch																
	SDIO	2ch*3ch																
	USB-FS	1ch*2ch																
Timers	Timer0	2 units																
	TimerA	6 units																
	Timer4	3unit																
	Timer6	3unit																
	WDT	1ch																
	SWDT	1ch																
	RTC	1ch																
Analog	12bit ADC	2unit, 16ch				2unit, 10ch		2unit, 15ch										
	PGA	1ch																
	CMP	3 ch																
	OTS	1ch																



AES128	ÿ
HASHÿSHA256ÿ	ÿ
WHITE	ÿ
Frequency Monitoring Module (FCM)	ÿ
Programmable voltage detection function (PVD)	ÿ
debug interface	SWD
	JTAG

Table 1-1 Model function comparison table

1.3 Functional block diagram

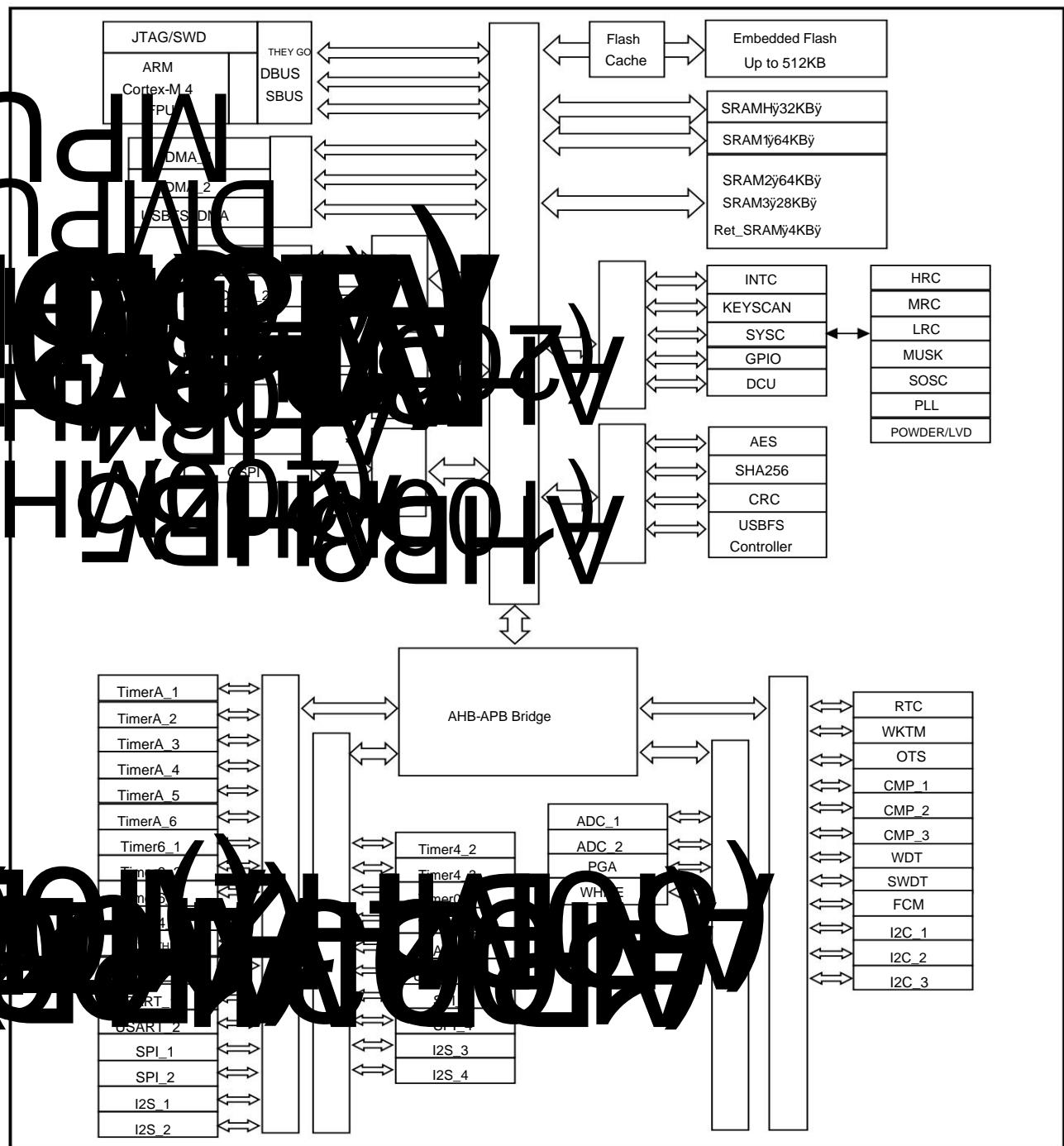


Figure 1-1 Functional block diagram

1.4 Function Introduction

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit reduced instruction

The CPU realizes fewer pins and lower power consumption, while providing excellent computing performance and rapid interrupt response capability. Chip

The integrated memory capacity can give full play to the excellent instruction efficiency of ARM® Cortex®-M4 with FPU. CPU

Supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. Single point precision FPU (Floating Point

Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus architecture (BUS)

The main system consists of a 32-bit multilayer AHB bus matrix, which enables interconnection of the following master bus and slave bus.

host bus

- ÿ Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus

- ÿ System DMA_1 bus, system DMA_2 bus

- ÿ USBFS_DMA bus

slave bus

- ÿ Flash ICODE bus

- ÿ Flash DCODE bus

- ÿ Flash MCODE bus (bus for other hosts other than CPU to access Flash)

- ÿ SRAMH bus (SRAMH 32kB)

- ÿ SRAMA bus (SRAM1 64KB)

- ÿ SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)

- ÿ APB1 peripheral bus (AOS/EMB/Timers/SPI/USART/I2S)

- ÿ APB2 peripheral bus (Timers/SPI/USART/I2S)

- ÿ APB3 peripheral bus (ADC/PGA/TRNG)

- ÿ APB4 peripheral bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)

- ÿ AHB1 peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)

- ÿ AHB2 peripheral bus (CAN/SDIOC)

- ÿ AHB3 peripheral bus (AES/HASH/CRC/USB FS)

ÿ AHB4 peripheral bus (SDIOC)

ÿ AHB5 peripheral bus (QSPI)

With the help of the bus matrix, efficient concurrent access from the master bus to the slave bus can be achieved.

1.4.3 Reset Control (RMU)

The chip is configured with 14 reset methods.

ÿ Power On Reset (POR)

ÿ NRST pin reset (NRST)

ÿ Brown-out Reset (BOR)

ÿ Programmable voltage detection 1 reset (PVD1R)

ÿ Programmable voltage detection 2 reset (PVD2R)

ÿ Watchdog reset (WDTR)

ÿ Dedicated watchdog reset (SWDTR)

ÿ Power-down wake-up reset (PDRST)

ÿ Software reset (SRST)

ÿ MPU error reset (MPUR)

ÿ RAM parity reset (RAMPR)

ÿ RAMECC reset (RAMECCR)

ÿ Clock exception reset (CKFER)

ÿ External high-speed oscillator abnormal shutdown reset (XTALER)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including: an external high-speed oscillator, an external low high-speed oscillator, two PLL clocks, one internal high-speed oscillator, one internal medium-speed oscillator, one internal low-speed oscillator, a SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) uses the measurement reference clock to monitor and measure the measurement target clock. An interrupt or reset occurs when the setting range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, and the source of the system clock can choose 6 clock sources:



1) External high-speed oscillator (XTAL)

2) External low-speed oscillator (XTAL32)

3) MPLL Clock (MPLL)

4) Internal High Speed Oscillator (HRC)

5) Internal Medium Speed Oscillator (MRC)

6) Internal low-speed oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 200MHz. SWDT has an independent clock source: SWDT dedicated

Internal Low Speed Oscillator (SWDTLRC). The real-time clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator

Oscillator as the clock source. The 48MHz clock of USB-FS and I2S communication clock can choose system clock, MPLL,

UPLL as clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply and cut-off of multiple power domains of the chip in multiple operating modes and low power consumption modes.

Change, test. The power controller is composed of power control logic (PWCL) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8V to 3.6V. A voltage regulator (LDO) powers the VDD and VDDR domains,

The VDDR voltage regulator (RLDO) supplies power to the VDDR domain during power-down mode. The chip controls the logic through the power consumption

(PWCL) provides three operating modes of ultra-high speed, high speed, and ultra-low speed, and three low-power modes such as sleep, stop, and power-down.

Mode.

The power voltage detection unit (PVD) provides power-on reset (POR), power-down reset (PDR), brown-out reset (BOR),

Programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2) and other functions, among which POR, PDR, BOR through

Detect VCC voltage, control chip reset action. PVD1 detects the VCC voltage and enables the core according to the register settings.

chip generates a reset or an interrupt. PVD2 detects the voltage by detecting VCC voltage or external input, according to the register

Select to generate reset or interrupt.

The VDDR area can maintain the power supply through RLDO after the chip enters the power-down mode to ensure that the real-time clock module (RTC),

The wake-up timer (WKTM) can continue to operate and keep the data in the 4KB low-power SRAM (Ret-SRAM). mold

The analog modules are equipped with dedicated supply pins for improved analog performance.



1.4.6 Initial Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_041F (where 0x0000_0408~0x0000_041F are reserved function addresses, the 24byte address needs to be set by the user to all 1s to ensure the chip is operating normally) Load data into the initialization configuration register, the user needs to program or erase FLASH sector 0 to modify the initialization configuration register.

1.4.7 Embedded Flash Interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE and MCODE buses. This interface can FLASH performs programming, sector erase, and full erase operations; code execution is accelerated through instruction prefetch and cache mechanisms.

Main features:

- ÿ Maximum 512KByte FLASH space
- ÿ I-CODE bus 16Byte prefetch value
- ÿ Shared 64 buffers (1Kbyte) on I-CODE and D-CODE buses
- ÿ Provide 960Bbyte one-time programming area (OTP)
- ÿ Support low-power read operation
- ÿ Support boot exchange function
- ÿ Support security protection and data encryption*1

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window

1.4.8 Built-in SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (Ret_SRAM) and 188KB system SRAM

ÿSRAMH/SRAM1/ SRAM2/SRAM3ÿ

SRAM can be accessed as bytes, halfwords (16 bits), or fullwords (32 bits). Read and write operations are performed at CPU speed, Wait periods can be inserted.

Ret_SRAM can provide 4KB of data holding space in Power down mode.

SRAM3 has ECC check (Error Checking and Correcting), and ECC check is one-check-two code to correct one bit error, check two bit error; SRAMH/SRAM1/SRAM2/Ret_SRAM with parity (Even-parity check), each byte of data has a parity bit.



1.4.9 General IO (GPIO)

GPIO main features:

- ÿ Each group of Port is equipped with 16 I/O Pins, which may be less than 16 according to the actual configuration
- ÿ Support pull-up
- ÿ Support push-pull, open-drain output mode
- ÿ Support high, medium and low drive modes
- ÿ Support external interrupt input
- ÿ Support peripheral function multiplexing of I/O pin, each I/O pin has up to 16 selectable multiplexing functions, some I/O Up to 64 functions optional
- ÿ Each I/O pin can be programmed independently
- ÿ Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The function of the interrupt controller (INTC) is to select the interrupt event request as an interrupt input to the NVIC and wake up the WFI;

As an event input, wakes up the WFE. Select interrupt event request as low power mode (sleep mode and stop mode)

wake-up condition; external pin NMI and EIRQ interrupt control function; software interrupt interrupt/event selection function
able.

Main Specifications:

1) NVIC interrupt vectors: Please refer to the user manual for the actual number of interrupt vectors used (excluding Cortex™-M4F's 16 Root interrupt line), each interrupt vector can select the corresponding peripheral interrupt event request according to the interrupt selection register.

For more instructions on exceptions and NVIC programming, please refer to "ARM Cortex™-M4F Technical Reference Manual"

Chapter 5: Exceptions and Chapter 8: Nested Vectored Interrupt Controllers.

2) Programmable priority levels: 16 programmable priority levels (using 4-bit interrupt priority levels).

3) Non-maskable interrupt: In addition to the NMI pin as a non-maskable interrupt source, it can be independently selected in various systems

interrupt event request as a non-maskable interrupt, and each interrupt event request is equipped with independent enable selection, suspend, clear
remove the pending register.

4) Equipped with 16 external pin interrupts.

5) Configure various peripheral interrupt event requests, please refer to the list of interrupt event request numbers for details.



- 6) Equipped with 32 software interrupt event requests.
- 7) Interrupts can wake up the system from sleep mode and stop mode.

1.4.11 Automatic Operating System (AOS)

Automatic operation system (Automatic Operation System) is used to realize peripheral hardware without CPU linkage between component circuits. Use events generated by peripheral circuits as AOS sources (AOS Source), such as timers Comparison matching, timing overflow, RTC periodic signal, various states of sending and receiving data of the communication module (idle, Receive data full, send data end, send data empty), ADC conversion end, etc., to trigger other peripheral circuits road action. The triggered peripheral circuit action is called AOS target (AOS Target).

1.4.12 Keyboard scan (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard arrays (line and column) scanning, the column is driven by an independent scan output KEYOUT_m (m=0~7), and the row KEYIN_n (n=0~15) Then it is detected as EIRQ_n (n=0~15) input. This module realizes the key recognition function through the line scan query method.

1.4.13 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, which can improve the security of the system by preventing unauthorized access. This product has built-in four MPU units for host and one MPU unit for IP. Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space. DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA to read and write the entire 4G address space Access control. When accessing the prohibited space, the MPU action can be set to ignore/bus error/disabled Mask interrupt/reset. The IP MPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral function blocks, and can be implemented without CPU involvement Data exchange between memories, between memories and peripheral function modules, and between peripheral function modules. The DMA bus is independent of the CPU bus, and is transmitted according to the AMBA AHB-Lite bus protocol With 8 independent channels (4 channels each for DMA_1 and DMA_2), different DMAs can be operated independently



transfer function

- ÿ The start request source of each channel is configured through an independent trigger source selection register
- ÿ Each request transfers a block of data
- ÿ The minimum data block is 1 data, and the maximum can be 1024 data
- ÿ Each data can be configured as 8bit, 16bit or 32bit
- ÿ A maximum of 65535 transmissions can be configured
- ÿ The source address and target address can be independently configured as fixed, auto-increment, auto-decrement, loop or specified offset jump
- ÿ Can generate 3 kinds of interrupts, block transfer complete interrupt, transfer complete interrupt, transfer error interrupt. Each interrupt can be

To configure whether to shield. Among them, the block transmission is completed, and the transmission completion can be used as an event output for other hardware with hardware

Trigger source input of trigger function peripheral module

- ÿ Support chain transmission function, which can realize the transmission of multiple data blocks at a time
- ÿ Support channel reset triggered by external events
- ÿ When not in use, it can be set to enter the module stop state to reduce power consumption

1.4.15 Voltage Comparator (CMP)

CMP is a peripheral module that compares two analog voltages INP and INM and outputs the comparison result. CMP Total

There are 3 independent comparison channels, each of which has 4 input sources for the analog voltages INP and INM. make

When used, one INP can be selected for a single comparison with one INM, or multiple INPs can be compared with the same INM

Do a scan comparison. The comparison result can be read through the register, can also be output to the external pin, can also generate interrupt and event.

1.4.16 Analog-to-Digital Converter (ADC)

A 12-bit ADC is an analog-to-digital converter that uses successive approximation. It has a maximum of 16 analog input channels

Channel, can convert external port and internal analog signal. These channels can be arbitrarily combined into a sequence for sequential

The sequence can be converted by single scan or continuous scan. Support connection to any specified channel

Repeat multiple conversions and average the conversion results. The ADC module is also equipped with an analog watchdog function, which can

The conversion result of the channel is monitored to detect whether the threshold value set by the user is exceeded.

ADC main features

- ÿ High performance



– Configurable 12-bit, 10-bit and 8-bit resolution

– The frequency ratio of peripheral clock PCLK4 and A/D conversion clock ADCLK can be selected:

ÿ PCLK4÷ADCLK=1÷1÷2÷4÷8÷1÷1÷2÷1÷4

ÿ ADCLK can choose a PLL asynchronous with the system clock HCLK, at this time the timing of PCLK4 and ADCLK

The clock source is fixed to PLL at the same time, and the frequency ratio is 1:1, the original frequency division setting is invalid

– 2MSPS (PCLK4=ADCLK=60MHz, 12 bits, sampling 17 cycles)

– Independent programming of sampling time for each channel

– Independent data registers for each channel

– Data register configurable data alignment

– Averaging function for consecutive multiple transitions

– Analog watchdog to monitor conversion results

– The ADC module can be set to stop when not in use

ÿ Analog input channels

– Up to 16 external analog input channels

– 1 Internal Reference Voltage

ÿ Conversion start condition

– Software settings conversion starts

– Peripheral peripherals trigger conversion start synchronously

– External pin trigger conversion start

ÿ Conversion mode

– 2 scan sequences A, B, single or multiple channels can be specified arbitrarily

– Sequence A single scan

– Sequence A continuous scan

– Dual-sequence scanning, sequence A and B independently select the trigger source, sequence B has a higher priority than A

– Synchronous mode (for devices with two or three ADCs)

ÿ Interrupt and event signal output

– Sequence A scan end interrupt EOCA_INT and event EOCA_EVENT

– End of sequence B-scan interrupt EOCA_INT and event EOCA_EVENT

- Analog watchdog channel compare interrupt CHCMP_INT and event CHCMP_EVENT, sequence compare interrupt SEQCMP_INT and event SEQCMP_EVENT
- All 4 events above can start DMA

1.4.17 Temperature sensor (OTS)

OTS can obtain the temperature inside the chip to support the reliable operation of the system. Use software or hardware trigger to start

After automatic temperature measurement, OTS provides a set of temperature-related digital quantities, and the temperature value can be calculated through the calculation formula.

1.4.18 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width that can be used for count generation

Different forms of clock waveforms are output for external use. The timer supports two waveform modes: triangle wave and sawtooth wave.

Various PWM waveforms can be generated; software synchronous counting and hardware synchronous counting can be realized between units; each reference value

The register supports cache function; supports 2-phase quadrature encoding and 3-phase quadrature encoding; supports EMB control. this series

Three units of Timer6 are installed in the product.

1.4.19 General control timer (Timer4)

General-purpose control Timer 4 (Timer4) is a timer module for three-phase motor control, providing various application

A three-phase motor control scheme for use. The timer supports two waveform modes of triangle wave and sawtooth wave, which can generate various

PWM waveform; support buffer function; support EMB control. Three units of Timer4 are installed in this series.

1.4.20 Emergency Braking Module (EMB)

The emergency brake module notifies the timer when certain conditions are met, so that the timer stops outputting PWM to the external motor

Signal function module, the following events are used to generate notifications:

- ÿ External port input level change
- ÿ The level of the PWM output port is in phase (same high or same low)
- ÿ Voltage comparator comparison result
- ÿ The external oscillator stops oscillating
- ÿ Write register software control



1.4.21 General-purpose timer (TimerA)

General-purpose Timer A (TimerA) is a timer with 16-bit count width and 8 PWM outputs. It should be

The timer supports two waveform modes of triangle wave and sawtooth wave, which can generate various PWM waveforms; support software synchronous start

Counting; comparison reference value register supports buffer function; supports 2-phase quadrature encoding counting and 3-phase quadrature encoding counting.

This series of products is equipped with 6 units of TimerA, which can realize a maximum of 48 channels of PWM output.

1.4.22 General-purpose timer (Timer0)

General-purpose timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting.

The timer contains 2 channels, which can generate compare match events during counting. This event can trigger an interrupt, also

Can be used as an event output to control other modules, etc. Two units of Timer0 are installed in this series.

1.4.23 Real Time Clock (RTC)

A real-time clock (RTC) is a counter that holds time information in BCD format. Records from 00 to 99

The specific calendar time between. Supports 12/24 hours, and automatically calculates the number of days 28 and 29 according to the month and year

(leap year), 30th and 31st.

1.4.24 Watchdog Counter (WDT)

There are two watchdog counters, one is a dedicated internal RC (WDTCLK: 10KHz) counting clock source

Watchdog counter (SWDT), the other is a general watchdog counter (WDT) whose count clock source is PCLK3.

The dedicated watchdog and the general watchdog are 16-bit down counters used to monitor

A software failure that is caused by an application program deviating from normal operation due to logical conditions.

Both watchdogs support window functions. The window interval can be preset before the count starts, and when the count value is within the window interval,

The counter can be refreshed and counting starts over.

1.4.25 Serial communication interface (USART)

This product is equipped with 4 units of serial communication interface module (USART). The serial communication interface module (USART) can

It is flexible enough to exchange full-duplex data with external devices; this USART supports universal asynchronous serial communication interface

(UART), clock synchronization communication interface, smart card interface (ISO/IEC7816-3). Supports modem operation



(CTS/RTS operation), multiprocessor operation.

1.4.26 Integrated Circuit Bus (I2C)

This product is equipped with integrated circuit bus (I2C) 3 units. I2C is used as an interface between the microcontroller and the I2C serial bus interface. Provides multi-master mode function, which can control the protocol and arbitration of all I2C buses. Support standard mode, fast speed mode.

1.4.27 Serial Peripheral Interface (SPI)

This product is equipped with 4-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and is convenient to communicate with peripheral devices for data exchange. Users can set three-wire/four-wire, master/slave and baud rate range as required place.

1.4.28 Four-wire serial peripheral interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed primarily for use with SPI-compatible Serial ROM for communication. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.29 Integrated Circuit Built-in Audio Bus (I2S)

I2S (Inter_IC Sound Bus), integrated circuit built-in audio bus, this bus is dedicated to data communication between audio devices data transmission. This product is equipped with 4 I2S and has the following features.

Function	main features
way of communication	<ul style="list-style-type: none"> ÿ Support full-duplex and half-duplex communication ÿ Support master mode or slave mode operation
Data Format	<ul style="list-style-type: none"> Optional channel length: 16/32 bits ÿ Optional transmission data length: 16/24/32 bits ÿ Data shift order: MSB ÿ start 8-bit programmable linear prescaler for precise
baud rate	<ul style="list-style-type: none"> audio sampling frequency ÿ Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k ÿ Can output drive clock to drive external audio components, ratio Fixed to 256*Fs (Fs is audio sampling frequency) Support I2S protocol ÿ I2S Philips standard ÿ MSB alignment standard ÿ LSB alignment standard ÿ PCM standard



data buffer	ÿ 2-word deep, 32-bit wide input and output FIFO buffer area
clock source	ÿ Internal I2SCLK (UPLL0/UPLLQ/UPLL0/MPLL0/MPLLQ/MPLL0) can be used; The external clock on the I2S_EXCK pin provides an interrupt
to interrupt	when the effective space of the sending buffer reaches the alarm threshold. An interrupt is generated when the effective space of the receiving buffer reaches the alarm threshold. The receive data area is full and there is still a write data request, and the receive overflows. Send The data area is empty and there is still a sending request, sending underflow ÿ The sending data area is full and there is still a request to write data, sending overflow

1.4.30 CAN communication interface (CAN)

This product is equipped with CAN communication interface module (CAN) 1 unit, and is equipped with 512Byte RAM for CAN

to store send/receive messages. Support the CAN2.0B protocol stipulated in ISO11898-1 and ISO11898-4

TTCAN protocol.

1.4.31 USB2.0 full speed module (USB FS)

This product is equipped with one unit of USB2.0 full-speed module (USB FS), and built-in full-speed PHY on chip. USB FS is a

A dual-role (DRD) controller that supports both slave and master functions. In host mode, USB FS supports full

speed and low-speed transceivers, while only full-speed transceivers are supported in slave mode.

The USB FS module equipped with this product successfully sends the SOF token in the host mode or successfully receives the SOF token in the slave mode

A SOF event can be generated when a token is issued.

1.4.32 Encryption Coprocessing Module (CPM)

Encryption co-processing module (CPM) includes AES encryption and decryption algorithm processor, HASH secure hash algorithm, TRNG

Three sub-modules of true random number generator.

The AES encryption and decryption algorithm processor follows the standard data encryption and decryption standards, and can realize encryption with a key length of 128 bits.

encryption and decryption operations.

HASH The secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the

The national standard "FIPS PUB 180-3" issued by the National Bureau of Standards and Technology can be used for messages whose length does not exceed 2^64 bits.

The message produces a 256-bit message digest output.

TRNG True Random Number Generator is a random number generator based on continuous analog noise, providing 64bit random numbers.



1.4.33 Data Computing Unit (DCU)

Data Computing Unit (Data Computing Unit) is a simple data processing module without the help of CPU. Every

Each DCU unit has 3 data registers, capable of adding, subtracting and comparing the size of 2 data, and window

Compare function. This product is equipped with 4 DCU units, and each unit can independently complete its own functions.

1.4.34 CRC calculation unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC13239, using 32-bit and 16-bit CRC respectively. CRC32

The generating polynomial of is $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$. CRC16

The generator polynomial of is $X^{16}+X^{12}+X^5+1$.

1.4.35 SDIO Controller (SDIOC)

The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has 2 SDIO controllers, each

Each SDIO controller provides a host interface for SD cards and SDIO devices that support the SD2.0 protocol

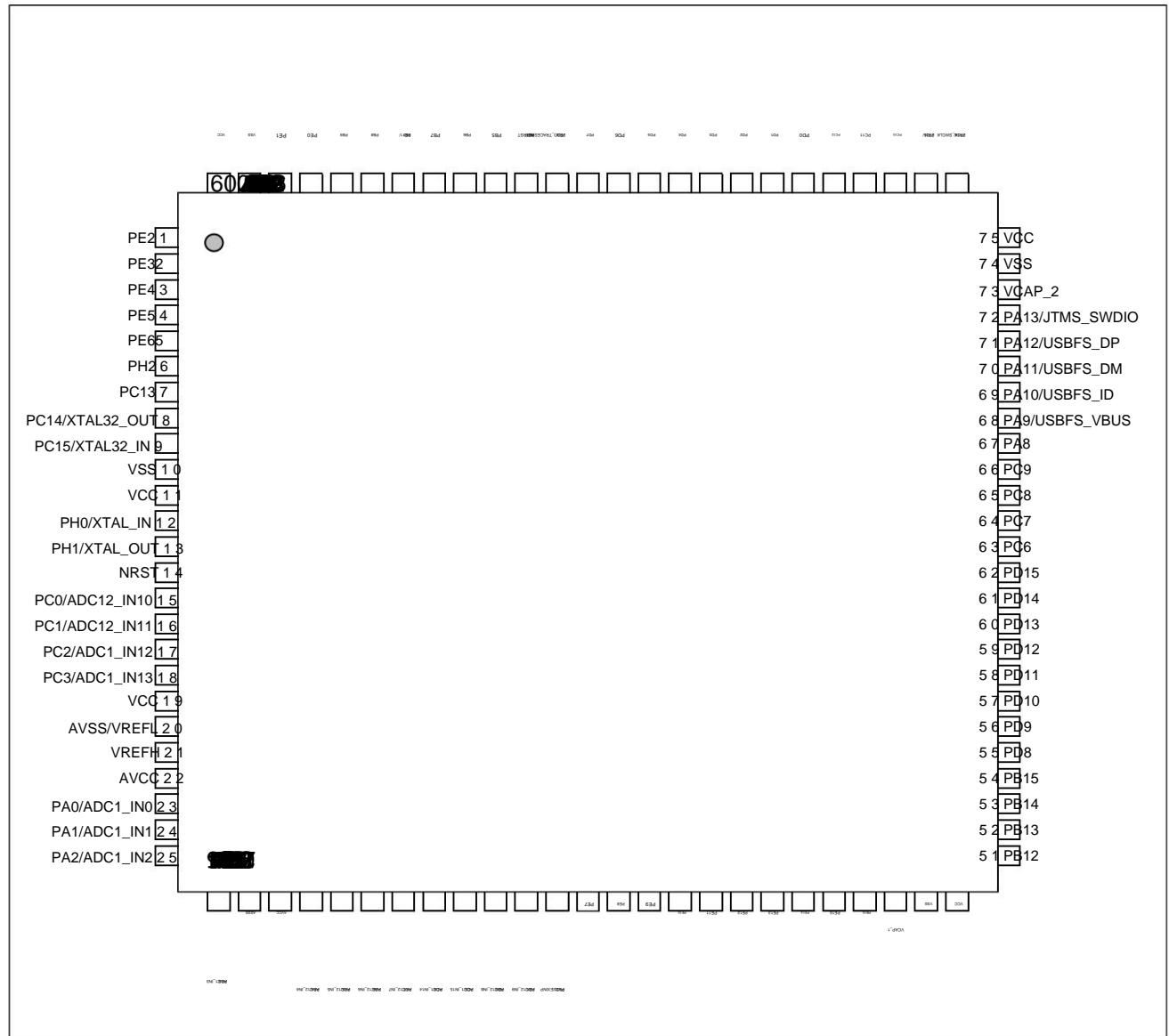
And communicate with MMC devices that support the eMMC4.51 protocol. The characteristics of SDIOC are as follows:

- ÿ Support SDSC, SDHC, SDXC format SD card and SDIO device
- ÿ Support one-wire (1bit) and four-wire (4bit) SD bus
- ÿ Support one-wire (1bit), four-wire (4bit) and eight-wire (8bit) MMC bus
- ÿ With card identification and hardware write protection function

2 pin configuration and function (Pinouts)

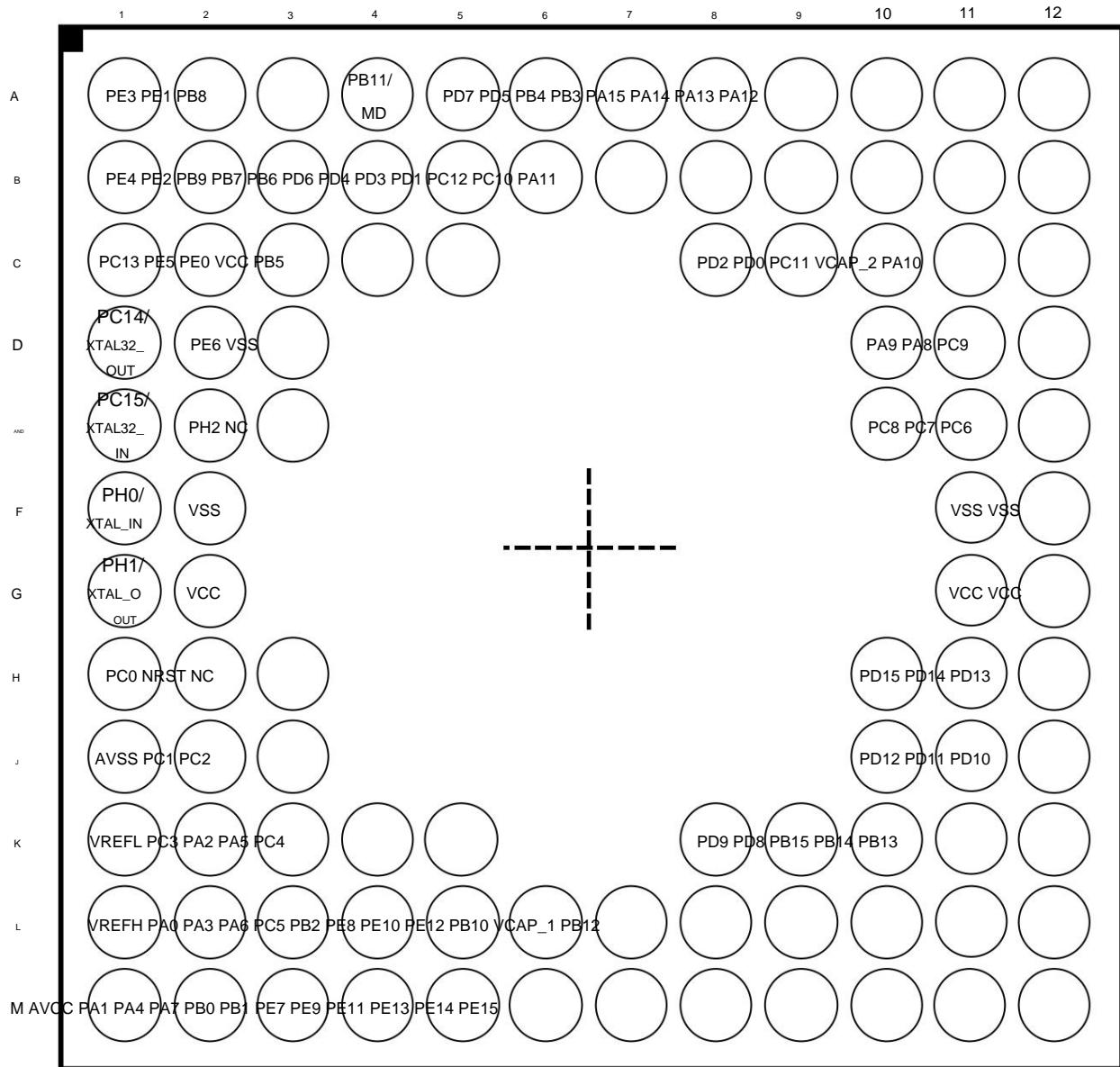
2.1 Pin Configuration Diagram

HC32F460PETB-LQFP100 /HC32F460PCTB-LQFP100



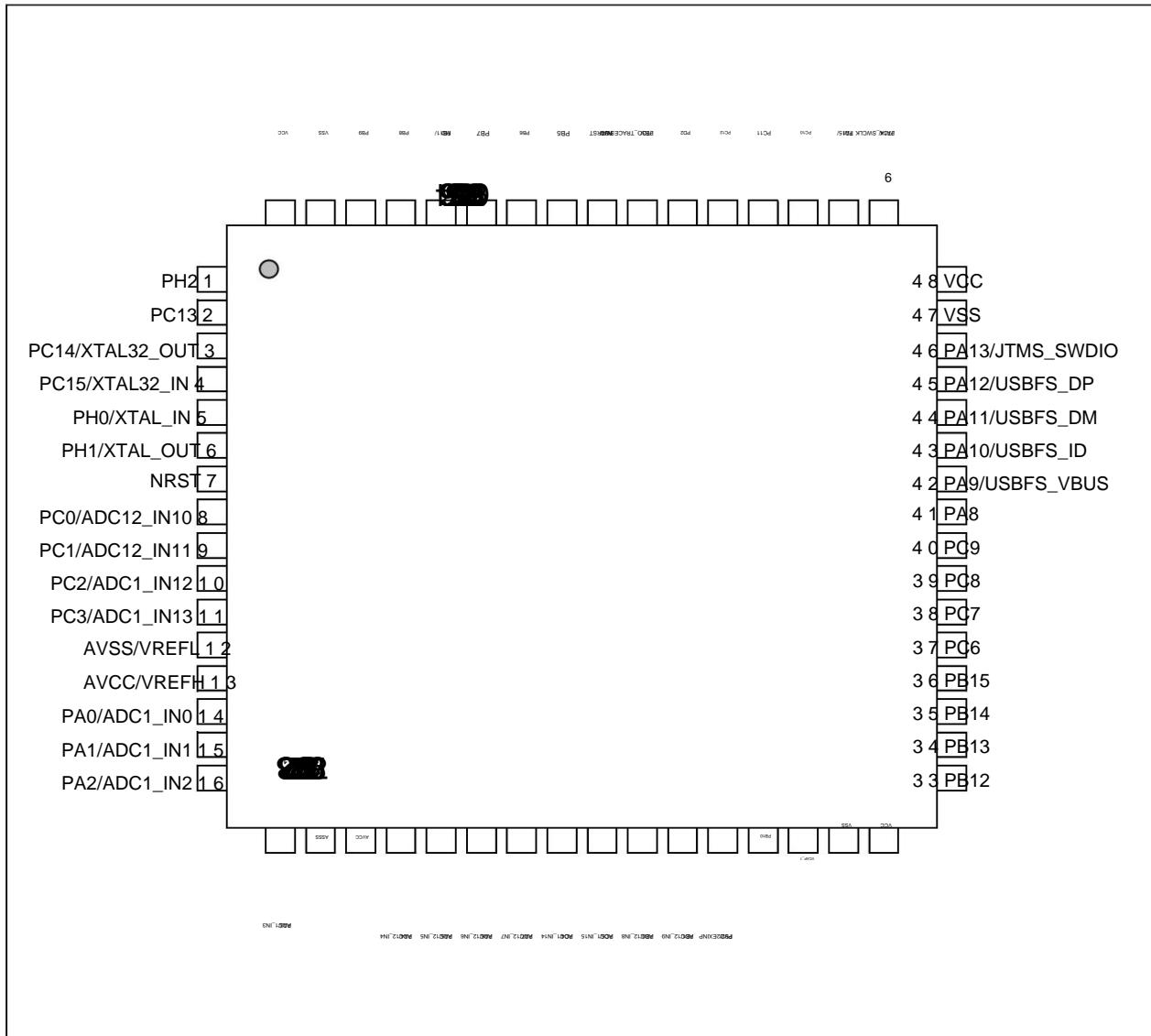
HC32F460PEHB-VFBGA100

"Top View"

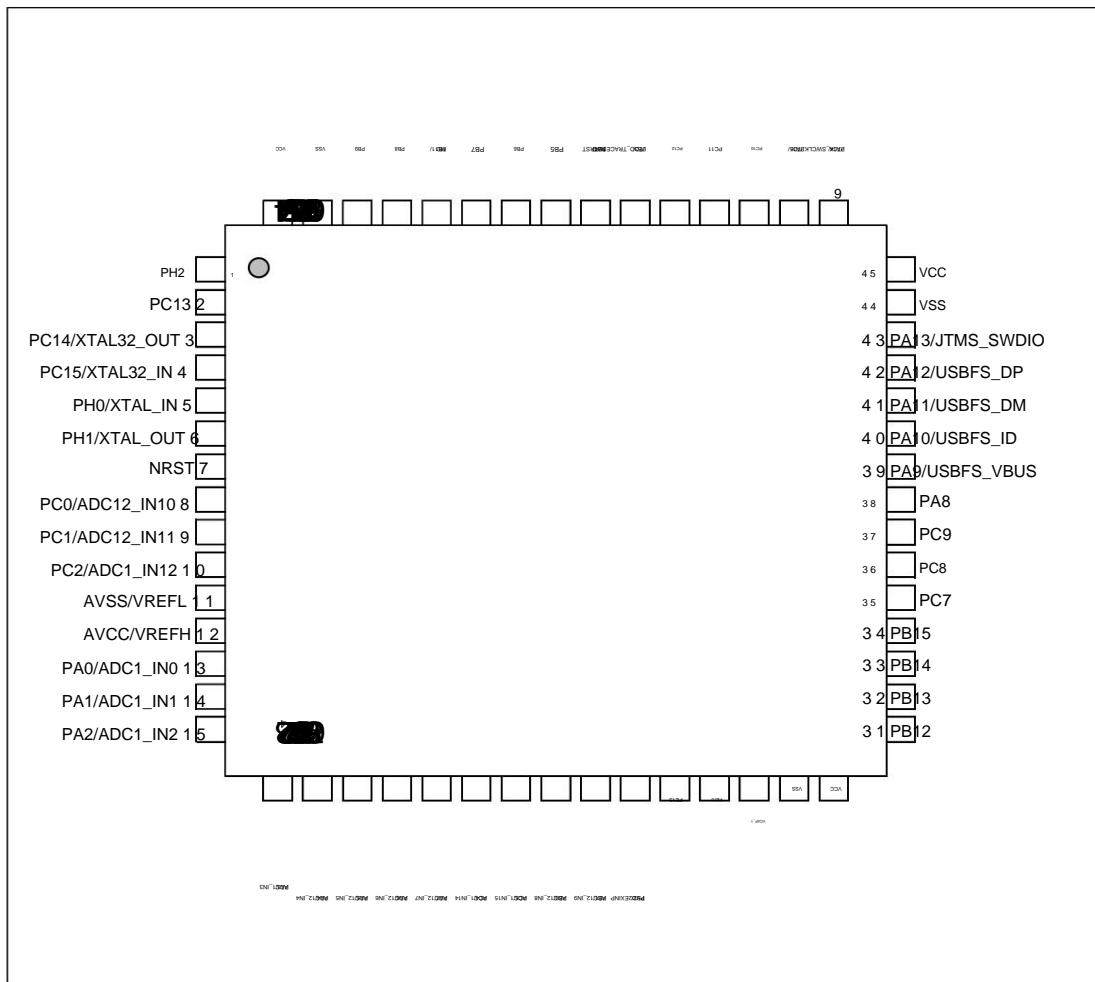


Note: A1 is Pin 1.

HC32F460KETA-LQFP64/ HC32F460KCTA-LQFP64



HC32F460KEUA-QFN60TR



HC32F460JETA-LQFP48 / HC32F460JCTA-LQFP48/HC32F460JEUA-QFN48TR

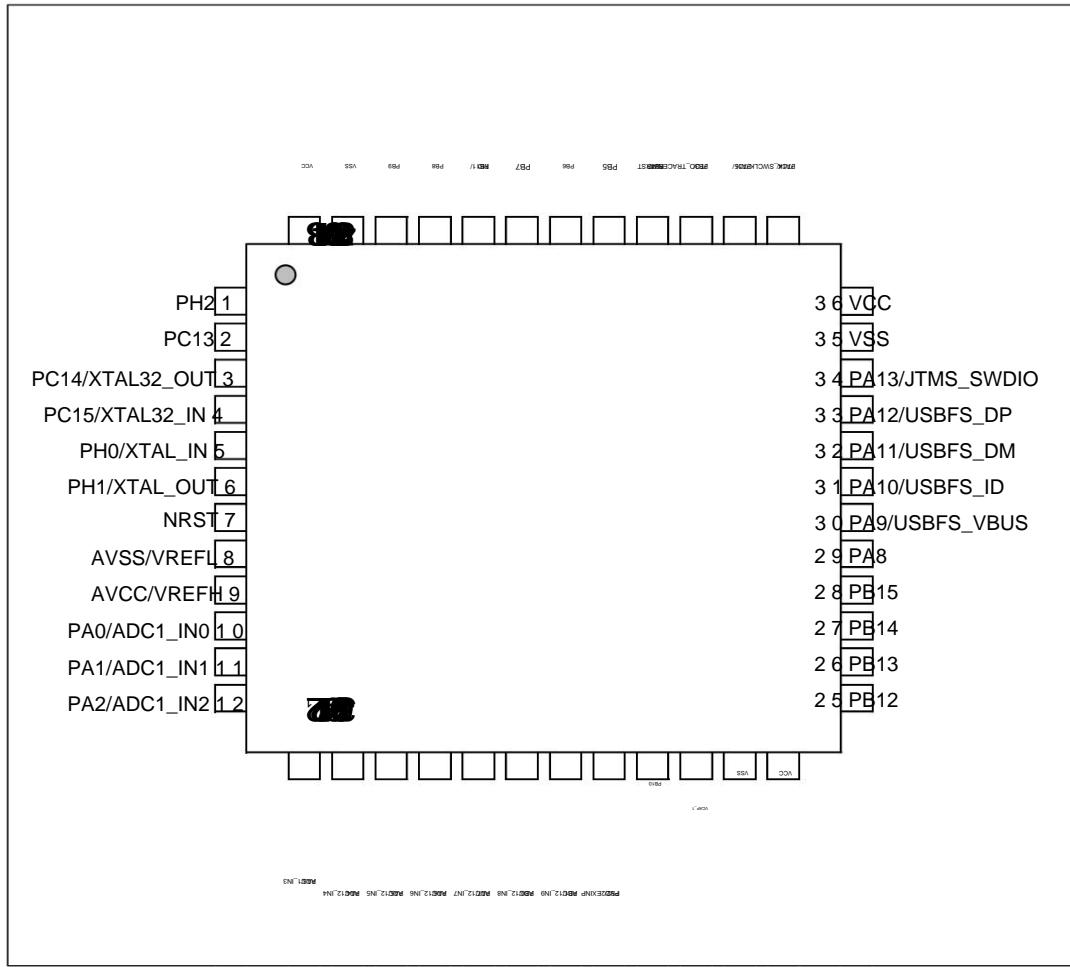


Figure 2-1 Pin configuration diagram



2.2 Pin function table

LQFP 100	VFBG A100	LQFP 64	QFN6 8	LQFP/ QFN4 8	Pin Name	Analog	EIRQ/WK UP	TRACE/JTAG /SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16 -31	Func32-63	
									GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TMA	USART/SPI/Q SPI	KEY	SDIO	USBFS/I2S	-	-	-	-	-	-	-	-	Communication Funcs
-	B2	-	-	-	- PE2			EIRQ2	TRACECK GPO					TIMA_3_PWM 5			USART3_CK										EVENTOUT	Func_Grp2
2	A1	-	-	-	- PE3			EIRQ3	TRACED0	GPO				TIMA_3_PWM 6			USART4_CK										EVENTOUT	Func_Grp2
3	B1	-	-	-	- PE4			EIRQ4	TRACED1	GPO				TIMA_3_PWM 7													EVENTOUT	Func_Grp2
4	C2	-	-	-	- PE5			EIRQ5	TRACED2	GPO				TIMA_3_PWM 8													EVENTOUT	Func_Grp2
5	D2	-	-	-	- PE6			EIRQ6	TRACED3	GPO																EVENTOUT	Func_Grp2	
6	E2	-	-	1 PH2			EIRQ2		GPO	FCMREF	TIM4_2_CLK			TIMA_4_PWM 7		EMB_JN4			SDIO2_D4	I2S3_EXCK							EVENTOUT	Func_Grp2
7	C1	2	2	2 PC13			EIRQ13		GPO	RTC_OUT				TIMA_4_PWM 8				SDIO2_CK	I2S3_MCK							EVNTP313	Func_Grp2	
8	D1	3	3	3 PC14	XTAL32_O OUT		EIRQ14		GPO					TIMA_4_PWM 5													EVNTP314	
9	E1	4	4	4 PC15	XTAL32_I N		EIRQ15		GPO					TIMA_4_PWM 6													EVNTP315	
10	F2	-	-	-	- VSS																							
11	G2	-	-	-	- VCC																							
12	F1	5	5	5 PH0	XTAL_IN	EIRQ0			GPO					TIMA_5_PWM 3														
13	G1	6	6	6 PH1	XTAL_OU T	EIRQ1			GPO					TIMA_5_PWM 4														
14	H2	7	7	7 NRST																								
15	H1	8	8	- PC0	ADC12_IN1 0/CMP3_IN P3	EIRQ0			GPO					TIMA_2_PWM 5				SDIO2_D5								EVNTP300 EVENTOUT	Func_Grp1	
16	J2	9	9	- PC1	ADC12_IN1 1	EIRQ1			GPO					TIMA_2_PWM 6				SDIO2_D6								EVNTP301 EVENTOUT	Func_Grp1	
17	J3	10	10	- PC2	ADC1_IN12 EIRQ2				GPO					TIMA_2_PWM 7		EMB_JN3			SDIO2_D7								EVNTP302 EVENTOUT	Func_Grp1
18	K2	11	-	- PC3	ADC1_IN13 /CMP1_IN M2	EIRQ3			GPO					TIMA_2_PWM 8				SDIO1_WP								EVNTP303 EVENTOUT	Func_Grp1	
19	-	-	-	-	- VCC																							
20	J1	12	11	8 ASSS																								
	K1	-	-	-	- VREFL																							
21	L1	-	-	-	- VREFH																							
22	M1	13	12	9 AVCC																								
23	L2	14	13	10 PA0	ADC1_IN0/ CMP1_INP	EIRQ0/WK UP_0_1			GPO		TIM4_2_OUH			TIMA_2_PWM 1/TIMA_2_CL THE			TIMA_2_TRIG SPH_SS1			SDIO2_D4						EVNTP100 EVENTOUT	Func_Grp1	



LQFP 100	VFBG A100	LQFP 64	QFN60 QFN48	LQFP/ QFN48	Pin Name	Analog	EIRQ/WK UP	TRACE/JTAG /SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16 -31	Func32-63	
									GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TIMA	USART/SPI/Q SPI	KEY	SDIO	USBFS/I2S	-	-	-	-	EVNTPT EVENTOUT	-	Communication Funcs		
24	M2	15	14	11 PA1		ADC1_IN1/ CMP1_INP 2	EIRQ1		GPO		TIM4_2_OUL		TIMA_2_PWM 2/TIMA_2_CL KB	TEAM_3_TRIG		SPI1_SS2		SDIO2_D5							EVNTPT101 EVENTOUT		Func_Grp1	
25	K3	16	15	12PA2		ADC1_IN2/ CMP1_INP 3	EIRQ2		GPO		TIM4_2_OVH		TIMA_2_PWM 1/TIMA_5_CL3 THE		SPI1_SS3		SDIO2_D6								EVNTPT102 EVENTOUT		Func_Grp1	
26	L3	17	16	13PA3		ADC1_IN3/ PGAVSS/C MP1_INP4	EIRQ3		GPO		TIM4_2_OVL		TIMA_2_PWM 4	TIMA_5_PWM 2/TIMA_5_CL KB				SDIO2_D7							EVNTPT103 EVENTOUT		Func_Grp1	
27		18		- AVSS																								
	E3			- NC																								
28		19		- AVCC																								
29	M3	20	17	14 PA4		ADC12_IN4/ CMP2_INP 1/CMP3_IN P4	EIRQ4		GPO		TIM4_2_OWH		TIMA_3_PWM 5		USART2_CK KEYOUT0		I2S1_EXCK								EVNTPT104 EVENTOUT		Func_Grp1	
30	K4	21	18	15PA5		ADC12_IN5/ CMP2_INP 2	EIRQ5		GPO		TIM4_2_OWL		TIMA_2_PWM 1/TIMA_2_CL THE	TIMA_3_PWM 6	TEAM_2_TRIG		KEYOUT1		I2S1_MCK							EVNTPT105 EVENTOUT		Func_Grp1
31	L4	22	19	16 PA6		ADC12_IN6/ CMP2_INP 3	EIRQ6		GPO																EVNTPT106 EVENTOUT		Func_Grp1	
32	M4	23	20	17PA7		ADC12_IN7/ CMP1_IN M1/CMP2_I NM1/CMP3 _INN1	EIRQ7		GPO		TIM4_1_OUL	TIM6_1_PWM B	TIMA_1_PWM 5	TIMA_3_PWM 2/TIMA_3_CL KB	EMB_IN3		KEYOUT3 SDIO2_WF								EVNTPT107 EVENTOUT		Func_Grp1	
33	K5	24	21	- PC4		ADC1_IN4/ CMP2_IN M2	EIRQ4		GPO		TIM4_2_OUH			TIMA_3_PWM 7		USART1_CK		SDIO2_CD								EVNTPT304 EVENTOUT		Func_Grp1
34	L5	25	22	- PC5		ADC1_IN15/ CMP3_IN M2	EIRQ5		GPO		TIM4_2_OUL			TIMA_3_PWM 8				SDIO2_CMD								EVNTPT305 EVENTOUT		Func_Grp1
35	M5	26	23	18 PB0		ADC12_IN8/ CMP3_INP 1	EIRQ0		GPO		TIM4_1_OVL	TIM6_2_PWM B	TIMA_1_PWM B	TIMA_3_PWM 6 3		USART4_CK KEYOUT4	SDIO2_CMD								EVNTPT200 EVENTOUT		Func_Grp1	
36	M6	27	24	19 PB1		ADC12_IN9/ CMP3_INP 2	EIRQ1/WK UP0_1		GPO		TIM4_1_OWL	TIM6_3_PWM B	TIMA_1_PWM 7	TIMA_3_PWM 4	QSPI_QSSN KEYOUT5	SDIO2_D3	I2S2_EXCK								EVNTPT201 EVENTOUT		Func_Grp1	
37	L6	28	25	20 PB2		PVD2EXIN P	EIRQ2/WK UP0_2		GPO	VCOUT123			TIM6_TRIGB	TIMA_1_PWM 8		EMB_IN1	QSPI_QSIO3		SDIO2_D2	I2S2_MCK						EVNTPT202 EVENTOUT		Func_Grp1
38	M7			- PE7			EIRQ7		GPO	ADTRG1			TIM6_TRIGA	TIMA_1_TRIG			USART1_CK								EVENTOUT			
39	L7			- PE8			EIRQ8		GPO		TIM4_1_OUL	TIM6_1_PWM B	TIMA_1_PWM 5												EVENTOUT			
40	M8			- PE9			EIRQ9		GPO		TIM4_1_OUH	TIM6_1_PWM A	TIMA_1_PWM 1/TIMA_1_CL THE												EVENTOUT			
41	L8			PE10			EIRQ10		GPO		TIM4_1_OVL	TIM6_2_PWM B	TIMA_1_PWM 6												EVENTOUT			



LQFP-100	VFBG	LQFP-64	QFN60	LQFP/DFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16-31	Func32-63		
									GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs		
42	M9	-	-	-	PE11		EIRQ11		GPO		TIM4_1_OVH	TIM6_2_PWM_A	TIMA_1_PWM_2/TIMA_1_CLKB													EVENTOUT			
43	L9	-	-	-	PE12		EIRQ12		GPO		TIM4_1_OWL	TIM6_3_PWM_B	TIMA_1_PWM_7			SPI1_SS1											EVENTOUT	Func_Grp2	
44 M10	-	-	-	-	PE13		EIRQ13		GPO		TIM4_1_OWH	TIM6_3_PWM_A	TIMA_1_PWM_3			SPI1_SS2											EVENTOUT	Func_Grp2	
45	M11	-	-	-	PE14		EIRQ14		GPO		TIM4_1_CLK		TIMA_1_PWM_4			SPI1_SS3			SDIO1_CD								EVENTOUT	Func_Grp2	
46 M12	-	26	-	-	PE15		EIRQ15		GPO				TIMA_1_PWM_8	TIMA_5_TRIG EMB_IN2	USART4_CK			SDIO1_WP								EVENTOUT	Func_Grp2		
47	L10	29	27	21	PB10		EIRQ10		GPO	ADTRG2	TIM4_2_OVH		TIMA_2_PWM	TIMA_5_PWM_38	QSPI_QSIO2			SDIO1_D7	I2S3_EXCK							EVNTP210_EVENTOUT	Func_Grp2		
48	L11	30	28	22	VCAP_1																								
49	F12	31	29	23	VSS																								
50	G12	32	30	24	VCC																								
51	L12	33	31	25	PB12		EIRQ12		GPO	VOUT1	TIM4_2_OVL TIM6_TRIGGER	TIMA_1_PWM_8			EMB_IN2	QSPI_QSIO1			SDIO2_D1	I2S3_MCK							EVNTP212_EVENTOUT	Func_Grp2	
52	K12	34	32	26	PB13		EIRQ13		GPO	VOUT2	TIM4_1_OUL	TIM6_1_PWM_B	TIMA_1_PWM_5				QSPI_QSIO0			SDIO2_D0							EVNTP213_EVENTOUT	Func_Grp2	
53	Q11	35	33	27	PB14		EIRQ14		GPO	VOUT3	TIM4_1_OVL	TIM6_2_PWM_B	TIMA_1_PWM_6				QSPI_QSCK			SDIO1_D6							EVNTP214_EVENTOUT	Func_Grp2	
54	K10	36	34	28	PB15		EIRQ15		GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWM_B	TIMA_1_PWM	TIMA_6_TRIGGER EMB_IN47	USART3_CK			SDIO1_CK								EVNTP215_EVENTOUT	Func_Grp2		
55	K9	-	-	-	PD8		EIRQ8		GPO		TIM4_3_EGG			TIMA_6_PWM_1/TIMA_6_CLTHE	QSPI_QSIO0 KEYOUT7											EVNTP408_EVENTOUT	Func_Grp2		
56	K8	-	-	-	PD9		EIRQ9		GPO		TIM4_3_OVL			TIMA_6_PWM_2/TIMA_6_CLKB	QSPI_QSIO1 KEYOUT6											EVNTP409_EVENTOUT	Func_Grp2		
57	J12	-	-	-	PD10		EIRQ10		GPO		TIM4_3_OWL			TIMA_6_PWM_3	QSPI_QSIO2 KEYOUT5											EVNTP410_EVENTOUT	Func_Grp2		
58	J11	-	-	-	PD11		EIRQ11		GPO		TIM4_3_CLK			TIMA_6_PWM_4	QSPI_QSIO3 KEYOUT4											EVNTP411_EVENTOUT	Func_Grp2		
59	J10	-	-	-	PD12		EIRQ12		GPO				TIMA_4_PWM_1/TIMA_4_CLTHE	TIMA_5_PWM_5												EVNTP412_EVENTOUT			
60	H12	-	-	-	PD13		EIRQ13		GPO				TIMA_4_PWM_2/TIMA_4_CLKB	TIMA_5_PWM												EVNTP413_EVENTOUT			
61	H11	-	-	-	PD14		EIRQ14		GPO				TIMA_4_PWM_3	TIMA_5_PWM_7												EVNTP414_EVENTOUT			
62	H10	-	-	-	PD15		EIRQ15		GPO				TIMA_4_PWM_4	TIMA_5_PWM_8												EVNTP415_EVENTOUT			
63	E12	37	36	-	PC6		EIRQ6		GPO				TIMA_3_PWM_1/TIMA_3_CLTHE	TIMA_5_PWM_8				QSPI_QSCK KEYOUT3 SDIO1_D6								EVNTP306_EVENTOUT	Func_Grp2		
64	E11	38	35	-	PC7		EIRQ7		GPO		TIM4_2_CLK			TIMA_3_PWM_2/TIMA_3_CLKB	TIMA_5_PWM				QSPI_QSSN KEYOUT2 SDIO1_D7								EVNTP307_EVENTOUT	Func_Grp2	



LQFP 100	VFBG A100	LQFP 64	QFN60 QFN48	LQFP/ QFN48	Pin Name	Analog	EIRQ/WK UP	TRACE/JTAG /SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16 -31	Func32-63	
									GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TIMA	USART/SPI/Q SPI	KEY	SDIO	USBFS/I2S	-	-	-	-	-	EVNTP EVENTOUT	-	Communication Funcs	
65	E10	39	36	- PC8			EIRQ8		GPO		TIM4_2_OWH		TIMA_3_PWM 3	TIMA_5_PWM 6		USART3_CK KEYOUT	SDIO1_00		I2S2_MCK							EVNTP308 EVENTOUT		Func_Grp2
66	D12	40	37	- PC9			EIRQ9		GPO	MCO_2	TIM4_2_OWL		TIMA_3_PWM 5	TIMA_5_PWM 4			KEYOUT0 SDIO1_D1									EVNTP309 EVENTOUT		Func_Grp1
67	D11	41	38	29 PA8			EIRQ8/WK UP2_0		GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWM A	TIMA_1_PWM 1/TIMA_1_CL THE			USART1_CK		SDIO1_D1	USBFS_SOF							EVNTP108 EVENTOUT		Func_Grp1
68	D10	42	39	30 PA9			EIRQ9/WK UP2_1		GPO		TIM4_1_OVH	TIM6_2_PWM A	TIMA_1_PWM 2/TIMA_1_CL KB					SDIO1_D2	USBFS_VBUS							EVNTP109 EVENTOUT		Func_Grp1
69	C12	43	40	31 PA10			EIRQ10/W KUP2_2		GPO		TIM4_1_OWH	TIM6_3_PWM A	TIMA_1_PWM 3	TIMA_5_TRIG				SDIO1_CD	USBFS_ID							EVNTP110 EVENTOUT		Func_Grp1
70	B12	44	41	32 PA11			EIRQ11/W KUP2_3		GPO		TIM4_1_CLK		TIMA_1_PWM 4		EMB_IN1			SDIO2_CD USBFS_DM								EVNTP111 EVENTOUT		Func_Grp1
71	A12	45	42	33 PA12			EIRQ12/W KUP3_0		GPO		TIM4_3_OWL	TIM6_TRIG TIME_1_TRIG	TIMA_6_PWM 1/TIMA_6_CL THE					SDIO2_WP USBFS_OP								EVNTP112 EVENTOUT		Func_Grp1
72	A11	46	43	34 PA13			EIRQ13/W KUP3_1	JTMS_SWDIO GPO					TIMA_2_PWM 5	TIMA_6_PWM 2/TIMA_6_CL KB		SPI2_SS1		SDIO2_D3								EVNTP113 EVENTOUT		Func_Grp1
73	C11			- VCAP2_2																								
74	F11	47	44	35 VSS																								
75	G11	48	45	36 VCC																								
76	A10	49	46	37 PA14			EIRQ14/W KUP3_2	JTCK_SWCLK GPO					TIMA_2_PWM 6	TIMA_6_PWM 3	TIMA_4_TRIG SPI2_SS2			SDIO2_D2	I2S1_EXCK							EVNTP114 EVENTOUT		Func_Grp1
77	A9	50	47	38 PA15			EIRQ15/W KUP3_3	JTDI	GPO				TIMA_2_PWM 1/TIMA_2_CL THE	TIMA_6_PWM 4	TIMA_2_TRIG SPI2_SS3			SDIO2_D1	I2S1_MCK							EVNTP115 EVENTOUT		Func_Grp1
78	B11	51	48	- PC10			EIRQ10		GPO		TIM4_3_OUH		TIMA_2_PWM 7	TIMA_5_PWM 1/TIMA_5_CL THE				SDIO1_D2							EVNTP310 EVENTOUT		Func_Grp1	
79	Q10	52	49	PC11			EIRQ11		GPO		TIM4_3_OVH		TIMA_2_PWM	TIMA_5_PWM 2/TIMA_5_CL 8 KB				SDIO1_D3							EVNTP311 EVENTOUT		Func_Grp1	
80	B10	53	50	- PC12			EIRQ12		GPO		TIM4_3_OWH		TEAM_4_TRIG	TIMA_5_PWM 3				SDIO1_CK							EVNTP312 EVENTOUT		Func_Grp1	
81	C9			- PD0			EIRQ0		GPO	VCOUT123				TIMA_5_PWM 4											EVNTP400 EVENTOUT		Func_Grp1	
82	B9			- PD1			EIRQ1		GPO				TEAM_3_TRIG	TIMA_6_PWM 5											EVNTP401 EVENTOUT		Func_Grp1	
83	C8	54		- PD2			EIRQ2		GPO				TIMA_2_PWM	TIMA_6_PWM 6				SDIO1_CMD							EVNTP402 EVENTOUT		Func_Grp1	
84	B8			- PD3			EIRQ3		GPO	VCOUT1				TIMA_6_PWM 7											EVNTP403 EVENTOUT			
85	B7			- PD4			EIRQ4		GPO	VCOUT2					TIMA_6_PWM 8											EVNTP404 EVENTOUT		
86	A6			- PD5			EIRQ5		GPO	VCOUT3								USART2_CK							EVNTP405 EVENTOUT			
87	B6			- PD6			EIRQ6		GPO								USART2_CK							EVNTP406 EVENTOUT				
88	A5			- PD7			EIRQ7		GPO								USART2_CK							EVNTP407 EVENTOUT				



LQFP 100	VFBG A100	LQFP 64	QFN60 QFN48	Pin Name	Analog	EIRQ/WK UP	TRACE/UTAG /SWD	Func0	Func1	Func2	Func3	Func4	I work5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14		Function 15	Func16 -31	Func32-63
								GPO	other	TIM4	TIM6	TEAM	TEAM	EMB,TIMA	USART/SPI/Q SPI	KEY	SDIO	USBFS/I2S	-	-	-	-	EVNTP EVENTOUT -		Communication Funcs	
89	A8	55	51	39 PB3		EIRQ3/WK UP0_3	JTDO_TRACE SWO	GPO	FCMREF	TIM4_3_CLK		TIMA_2_PWM 2/TIMA_2_CL KB	TIMA_6_PWM 5				SDIO2_D0						EVNTP203 EVENTOUT		Func_Grp2	
90	A7	56	52	40 PB4		EIRQ4/WK UP1_0	NJTRST	GPO		TIM4_3_OWL		TIMA_3_PWM 1/TIMA_3_CL 6 THE	TIMA_6_PWM				SDIO1_D0						EVNTP204 EVENTOUT		Func_Grp2	
91	C5	57	53	41 PB5		EIRQ5/WK UP1_1		GPO		TIM4_3_OWH		TIMA_3_PWM 2/TIMA_3_CL KB	TIMA_6_PWM 7				SDIO1_D3	I2S4_EXCK					EVNTP205 EVENTOUT		Func_Grp2	
92	B5	58	54	42 PB6		EIRQ6/WK UP1_2		GPO	ADTRG2	TIM4_3_OVL		TIMA_4_PWM 1/TIMA_4_CL 8 THE	TIMA_6_PWM				SDIO2_CK	I2S4_MCK					EVNTP206 EVENTOUT		Func_Grp2	
93	B4	59	55	43 PB7		EIRQ7/WK UP1_3		GPO	ADTRG1	TIM4_3_OVH		TIMA_4_PWM 2/TIMA_4_CL KB				SDIO1_D0						EVNTP207 EVENTOUT		Func_Grp2		
94	A4	60	56	44 PB11/MD		NMI																	EVNTP211			
95	A3	61	57	45 PB8		EIRQ8		GPO		TIM4_3_EGG		TIMA_4_PWM 3				KEYOUT7 SDIO1_D4	USBFS_DRVV BUS						EVNTP208 EVENTOUT		Func_Grp2	
96	B3	62	58	46 PB9		EIRQ9		GPO		TIM4_3_OUH		TIMA_4_PWM 4	TEAM_6_TRIG			SPI2_SS1	KEYOUT6 SDIO1_D5						EVNTP209 EVENTOUT		Func_Grp2	
97	C3		-PE0			EIRQ0		GPO	MCO_1			TEAM_4_TRIG				SPI2_SS2							EVENTOUT		Func_Grp2	
98	A2		-PE1			EIRQ1		GPO	MCO_2	TIM4_3_CLK						SPI2_SS3							EVENTOUT		Func_Grp2	
99	D3	63	59	47 VSS																						
100 C4		64	60	48 VCC																						
	H3	-	-NC																							

Table 2-1 Pin Function Table

Note:

– In the above table, there are 64 pins that support the function selection of Func32~63, and Func32~63 are mainly serial communication functions (including USART, SPI, I2C, I2S, CAN),

Divided into two groups Func_Grp1, Func_Grp2. Please refer to Table 2-2 for details.



	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	I work 47
Func_Grp 1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SC	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SC
Func_Grp 2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SC	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SC

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp 1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp 2	I2C3_SDA	I2C3_SCL	CAN_RXD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK					

Table 2-2 Func32~63 table

Package	Port Group	Bits															Pin Count
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LQFP100	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
VFBGA100	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	Door	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LQFP64	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	O	1
	PortH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
QFN60	Brings	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	and	14
	Door	0	0	0	0	0	0	0	0	0	0	0	0	0	0	O	1
	PortH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LQFP48	PortA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
QFN48	PortB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16
	PortC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
	PortH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 2-3 Port configuration



Port	pull-up	Open-drain output	drive capability 5V with	stand voltage	Remarks	support
Brings	PA0~PA10	support	low, medium and high	support*		
	PA13~PA15					
	PA11, PA12 support		support	Low, medium, high	not supported	
PortB	PB0~PB10, PB12~PB15	support	support	Low, medium, high	supported*	
	PB11	support				input only
PortC	PC0~PC15	support	Support	Support	Low, Medium, High	
PortD	PD0~PD15	support	Support	Support*	Low, Medium, High	
Door	PE0~PE15	support	Support	Support	Low, Medium, High	
PortH	PH0~PH2		Support	Support	Low, Medium, High	Support

Table 2-4 General Function Specifications

Note:

- When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin function description

category	function name	I/O	illustrate
Power	VCC	I Power	
	VSS	I power	ground
	VCAP_1~2	IO	core voltage
	AVCC	I Analog	power
	ASSS	I Analog	power ground
	VREFH	I Analog	reference voltage
	VREFL	I Analog	reference voltage
System	NRST	I Reset	pin, active low
	MD	I mode	pin
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I External	Main Clock Oscillator Interface
	XTAL_OUT	O	
	XTAL32_IN	I External	sub clock (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_1~2	O Internal	clock output
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO	General input and output
EVENTOUT	EVENTOUT	O Cortex-M4	CPU event output
EIRQ	EIRQx (x=0~15)	I Maskable	external interrupt
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I Non-maskable	external interrupt
Event Port	EVNTPxy (x=1~4, y=0~15)	IO event	port input and output function
Key	KEYOUTx(x=0~7)	O KEY	CAN scan output signal
JTAG/SWD	JTCK_SWCLK	I In-circuit	debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	O Trace	debug sync clock output
	TRACED0~3	O Trace	debug data output
FCM	FCMREF	I External	reference clock input for clock frequency measurement
RTC	RTCOUT	O 1Hz	clock output
Timer4	TIM4_x_CLK	I Count	clock port input

category	function name	IO	illustrate
(x=1~3)	TIM4_x_OUH	IO PWM	port U-phase output
	TIM4_x_OUL	IO PWM	port U-phase output
	TIM4_x_OVH	IO PWM	port V-phase output
	TIM4_x_OVL	IO PWM	port V-phase output
	TIM4_x_OWH	IO PWM	port W phase output
	TIM4_x_OWL	IO PWM	port W phase output
Timer6	TIM6_TRIGA	I	External event triggers A input
	TIM6_TRIGB	I	External event triggers B input
	TIM6_x_PWM	IO	external event trigger input or PWM port output
	TIM6_x_PWM	IO	external event trigger input or PWM port output
TimerA	TEAM_x_TRIG	I	External event trigger input
	TIMA_x_PWM1/TIMA_x_CLKA	IO	external event trigger input or PWM port output or count clock port output
	TIMA_x_PWM2/TIMA_x_CLKB	IO	external event trigger input or PWM port output or count clock port output
	TIMA_x_PWM _y (y=3~8)	IO	External event trigger input or PWM port output and input
EMB	EMB_IN _x (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx	USART _x _TX	IO	send data
	USART _x _RX	IO	receive data
	USART _x _CK	IO	communication clock
	USART _x _RTS	O	request to send a signal
	USART _x _CTS	I	clear send signal
SPI _x	SPI _x _MISO	IO	master input/slave output data transfer pin
	SPI _x _MOSI	IO	master output/slave input data transfer pin
	SPI _x _SCK	IO	transfer clock
	SPI _x _SS0	IO	slave select input and output pins
	SPI _x _SS1~3	O	Slave select output pin
QSPI	QSPI_QSIO0~3	IO	data line
	QSPI_QSCK	O	clock output
	QSPI_QSSN	O	slave selection
I ² C _x	I ² C _x _SCL	IO	clock line
	I ² C _x _SDA	IO	data line
I ² S _x	I ² S _x _SD	IO	serial data
	I ² S _x _SDIN	I	Full-duplex serial data input
	I ² S _x _WS	IO	word selection
	I ² S _x _CK	IO	serial clock



category	function name	I/O	illustrate
	I2Sx_EXCK	I External	clock source
	I2Sx_MCK	O master	clock
CAN	CAN_TxD	O send	data
	CAN_RxD	I receive	data
SDIOx	SDIOx_Dy (y=0~7)	IO SD	data signal
	SDIOx_CK	O SD	clock output signal
	SDIOx_CMD	IO SD	command and reply signal
	SDIOx_CD	I	SD card recognition status signal
	SDIOx_WP	I	SD card write protection status signal
USBFS	USBFS_DM	IO USBFS	On-Chip Full Speed PHY D-Signal
	USBFS_DP	IO USBFS	on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O USBFS	SOF pulse output signal
	USBFS_DRVVBUS	O USBFS	VBUS driver permission signal
CMPx (x=1~3)	VCOUT1	O Analog	comparison channel 1 result output
	VCOUT2	O Analog	comparison channel 2 result output
	VCOUT3	O Analog	comparison channel 3 result output
	VCOUT123	O Analog	comparison channel 1~3 result OR output
	CMPx_INPx	I Analog	Comparator Channel x Positive Terminal Voltage y Input
	CMPx_INMy	I Analog	Comparator Channel x Negative Terminal Voltage y Input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADC1_INx (x=0~3,12~15)	I	ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share the external analog input port
	PGAVS	I	PGA Ground Input Table

2-5 Pin Function Description

2.4 Pin Usage Instructions

pin name	Instructions for use
VCC	Power supply, connected to a voltage of 1.8V~3.6V, and a decoupling capacitor connected to the VSS pin nearby (refer to electrical characteristics)
VSS	Power ground, connected to 0V
VCAP_1~2	Core voltage, connect a capacitor to the VSS pin nearby to stabilize the core voltage (refer to electrical characteristics)
AVCC	Analog power supply, supplying power to analog modules, connected to the same voltage as VCC (refer to electrical characteristics) When not using the analog module, please short it with VCC
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (refer to electrical characteristics) When not using the analog module, please short it with VSS
VREFH	Analog reference voltage of ADC1 and ADC2, connected to a voltage not higher than AVCC When not using ADC, please short it with AVCC
PB11/MD	Mode input, fixed as input state. Reset pin (NRST) deasserts (changes from low to high) , this pin must be fixed at high level. It is recommended to connect a resistor (4.7K Ω) to VCC (pull-up)
NRST	Reset pin, active low. When not in use, connect a resistor to VCC (pull up)
Pxy, x=A~E,H, y=0~15	General purpose pin. When used as an input function, the input voltage should not exceed 5V. When used as an analog input, the analog voltage does not To exceed VREFH/AVCC Leave floating when not in use, or connect a resistor to VCC (pull-up)/VSS (pull-down)

Table 2-6 Pin Usage Description

3 Electrical Characteristics (ECs)

3.1 Parameter conditions

All voltages are referenced to VSS unless otherwise noted.

3.1.1 Minimum and maximum values

Unless otherwise specified, all device minimum and maximum values are at worst-case ambient temperature, supply voltage, and clock frequency

Guaranteed by design or characterization tests under conditions.

3.1.2 Typical values

Unless otherwise noted, typical data is by design or characterization at $TA = 25^{\circ}\text{C}$, $VCC = 3.3\text{ V}$

The test analysis is obtained.

3.1.3 Typical curves

Unless otherwise specified, all typical curves are not tested and are for design guidance only.

3.1.4 Load capacitance

The load conditions used to measure pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin input voltage

Figure 3-1 (right) shows how to measure the input voltage at the device pins.

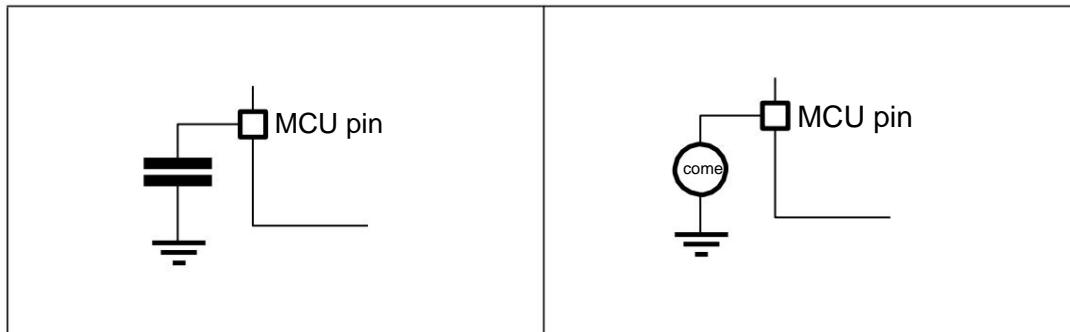


Figure 3-1 Pin load condition (left) and input voltage measurement (right)

3.1.6 Power scheme

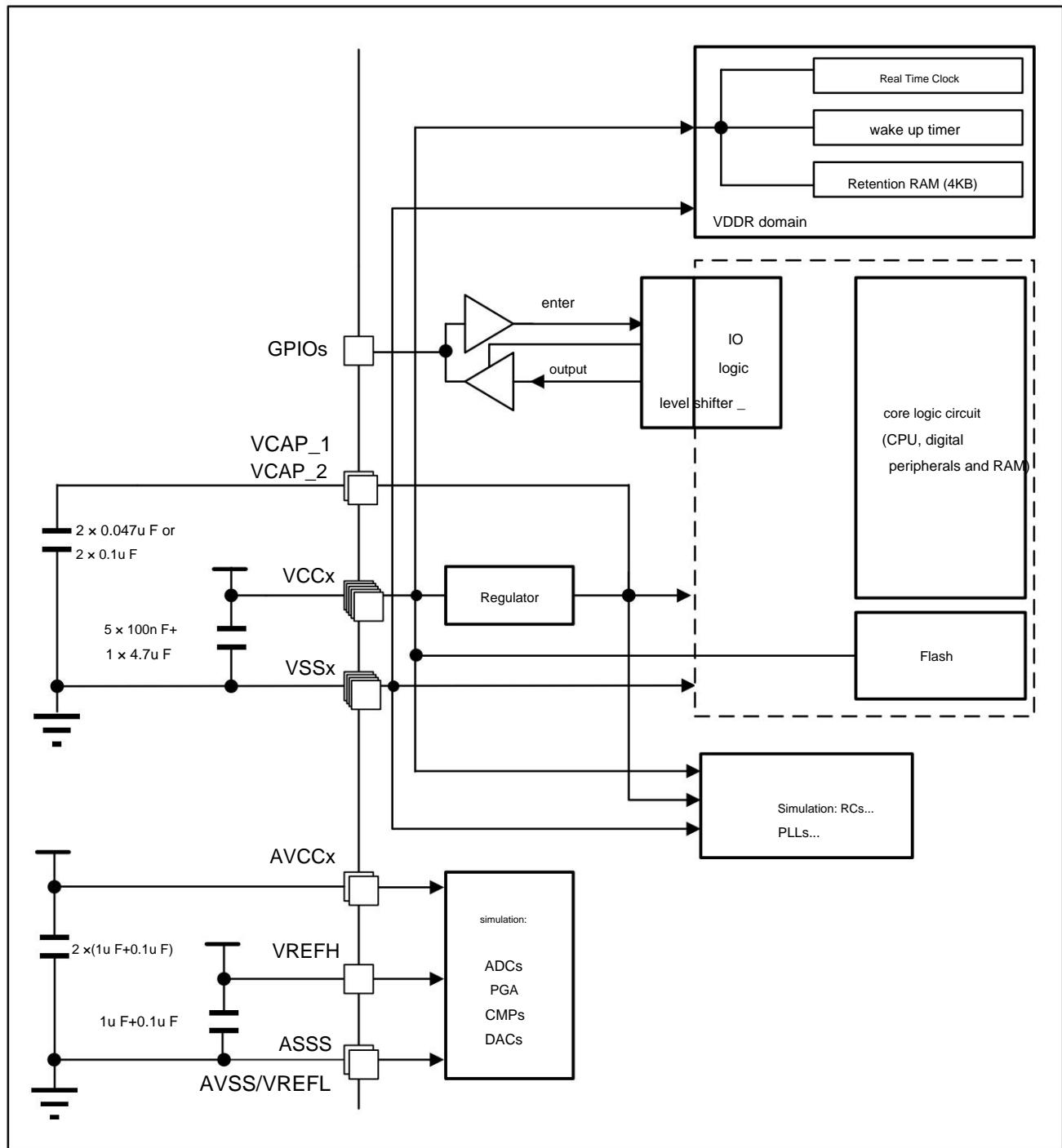


Figure 3-2 Power solution (HC32F460PETB-LQFP100, HC32F460PEHB-VFBGA100)

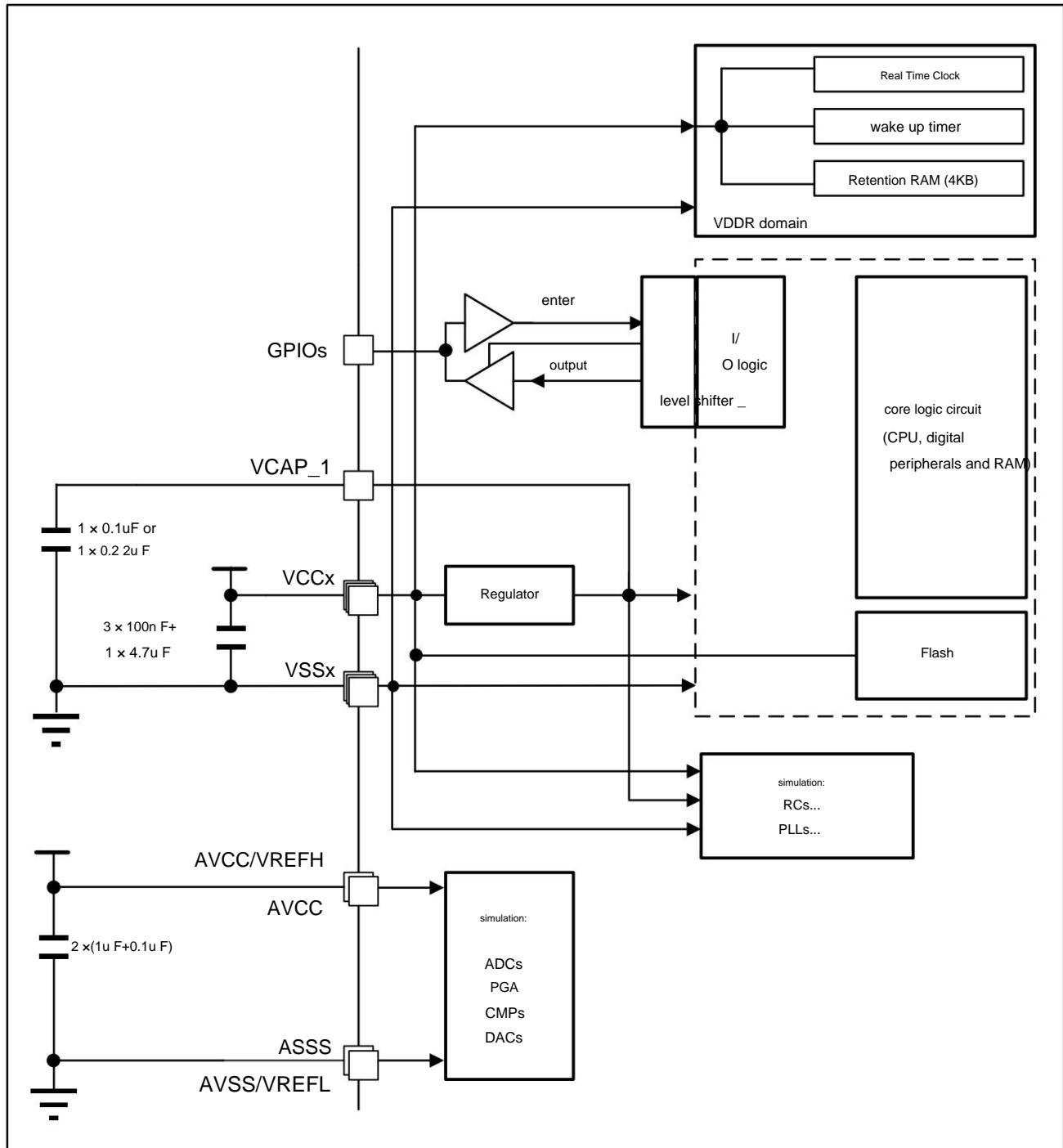


Figure 3-3 Power solution (HC32F460KETA-LQFP64)

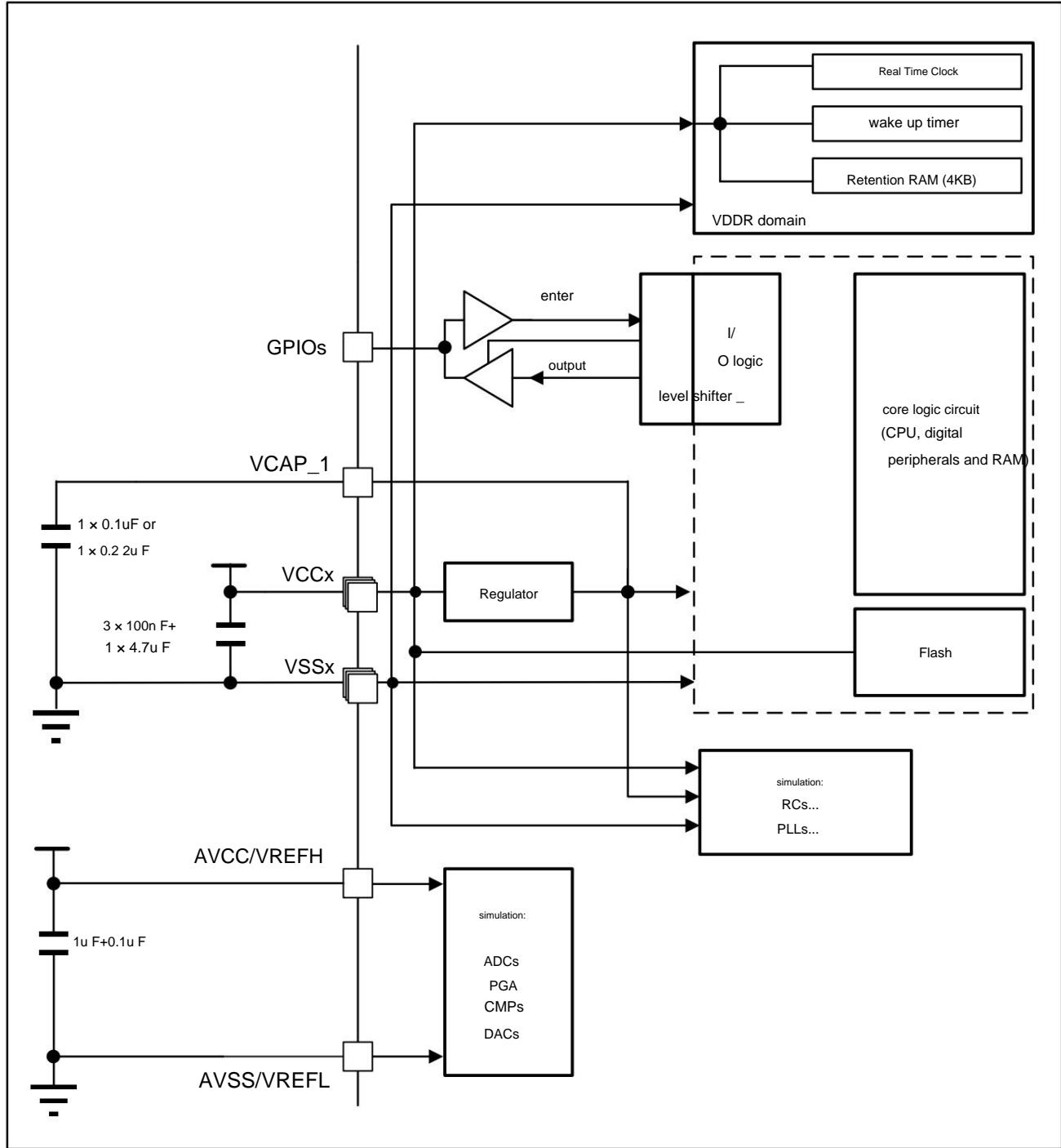


Figure 3-4 Power solution (HC32F460KEUA-QFN60TR/HC32F460JETA-LQFP48/HC32F460JEUA-QFN48TR)

1. A $4.7\mu\text{F}$ ceramic capacitor must be connected to one of the VCC pins.

2. $\text{AVSS}=\text{VSS}_\text{Y}$

3. Each power supply pair (eg VCC/VSS, AVCC/AVSS...) must be decoupled with the filter ceramic capacitors mentioned above. These capacitors

It must be as close to or below the appropriate pins on the underside of the PCB as possible for proper device operation. It is not recommended to remove the filter capacitor to reduce

Low PCB size or cost. This may cause the device to malfunction.

4. The capacitors used by the VCAP_1/VCAP_2 pins of the chip are as follows: 1) The cores with both VCAP_1 and VCAP_2 pins Chip, each pin can use 0.047uF or 0.1uF capacitor (the total capacity is 0.094uF or 0.2uF). 2) only VCAP_1 pin chips can use 0.1uF or 0.22uF capacitors. When waking up from power-down mode, the core voltage builds up VCAP_1/VCAP_2 needs to be charged during the process. On the one hand, the smaller VCAP_1/VCAP_2 total capacity can shorten the charge time, bringing fast responsiveness to the application; on the other hand, larger VCAP_1/VCAP_2 total capacity prolongs charging time, but also provide stronger electromagnetic compatibility (EMC). According to the requirements of electromagnetic compatibility and system response speed, users can choose a larger or smaller capacitor value. The total capacity of VCAP_1/VCAP_2 of the chip must match the PWC_PWRC3.PDTS bit matches the assigned value. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, it needs to be Make sure the PWC_PWRC3.PDTS bit is cleared before. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, it needs to Make sure the PWC_PWRC3.PDTS bit is set before entering power-down mode.

5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin, the

The capacitance value CEXT is determined according to the stability requirement of the system. The capacitance value CEXT and ESR requirements are as follows:

symbol	parameter	condition
CEXT	The capacitance value of the external capacitor	0.047μF / 0.1μF / 0.22μF
ESR	Equivalent series resistance ESR of external capacitor	< 0.3 $\ddot{\mu}$

Table 3-1 VCAP_1/VCAP_2 working conditions

3.1.7 Current consumption measurement

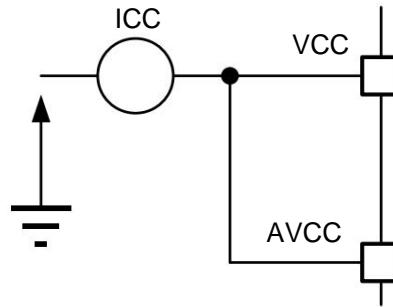


Figure 3-5 Current consumption measurement scheme

3.2 Absolute Maximum Ratings

If the load applied to the device exceeds the

The absolute maximum ratings listed may cause permanent damage to the device. These values are stress ratings only and do not imply means that the device is functioning normally under these conditions. Prolonged operation at maximum ratings may affect the reliability of the device reliability.

symbol	project	minimum value	maximum value	unit
VCC-VSS	external main power supply voltage (including AVCC, VCC)(1) -0.3		4.0	
COME	Input voltage on 5V tolerant pin(2)	VSS-0.3	VCC+4.0 (Maximum 5.8V)	IN
	on PA11/USBFS_DM and PA12/USBFS_DP pins input voltage	VSS-0.3	4.0	
VESD (HBM)	electrostatic discharge voltage (human body model)	Please refer to 3.3.5 Electrical Sensitivity		-

Table 3-2 Voltage characteristics

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external

external power supply.

2. The maximum value of VIN must always be respected . See Table 3-3 for the maximum allowable injected current values.

symbol	project	unit of maximum	
$\dot{y}IVCC$	Total current flowing into all VCCX power lines (source current)(1)	240	
$\dot{y}IVSS$	Total current flowing (sinking) out of all VSSX ground wires (1)	-240	
IVCC	Maximum current into each VCCX supply line (source current) (1)	100	
IVSS	Maximum current (sink) out of each VSSX ground wire (1)	-100	
IIO	Output current sink for any I/O and control pin	40	mA
	Output current source for any I/O and control pin	-40	
$\dot{y}IIO$	Total output sink current on all I/O and control pins	120	
	Total output source current on all I/O and control pins	-120	

Table 3-3 Current characteristics

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external

external power supply.



symbol	project	value	unit
TSTG	storage temperature range	-55 to +125	°C
TJ	maximum junction temperature	125	°C

Table 3-4 Thermal characteristics

3.3 Working conditions

3.3.1 General working conditions

symbol	parameter	condition	Min	Typ	Max	Unit		
fHCLK internal AHB clock frequency		Super Speed Mode[1] PWRC2.DVS=00 PWRC2.DDAS=1111				200	MHz	
		High speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111				168		
		super low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000				8		
			1.8			3.6		
				1.8		3.6		
COME	Input power on 5V tolerant pins Press (3)	2 V \leq VCC \leq 3.6 V VCC \leq 2 V				5.5	IN	
			-0.3			5.2		
	PA11/USBFS_DM PA12/USBFS_DP			-0.3		VCC+0.3		
	The input voltage of the pin							
TJ	Junction temperature range		-40			125	°C	

Table 3-5 General working conditions

1. Mass production test guarantee.
2. If the VREFH pin is present, the following condition must be considered: VAVCC-VREFH $<$ 1.2 V.
3. To keep the voltage above VCC+0.3, the internal pull-up/pull-down resistors must be disabled.

3.3.2 Operating conditions at power-on / power-off

TA is subject to general working conditions.

symbol	parameter	min	max	unit
tVCC	VCC rise time rate	20	20000	μs/V
	VCC Fall Time Rate	20	20000	

Table 3-6 Working conditions at power-on/power-off

3.3.3 Reset and power control module characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
Monitoring voltage of VBOR BOR		Super high speed mode ICG1.BOR_lev[1:0]=00	1.88	1.99	2.09	V		
			ICG1.BOR_lev [1:0]=01	1.99	2.09	2.20	V	
			ICG1.BOR_lev [1:0]=10	2.09	2.20	2.30	V	
			ICG1.BOR_lev [1:0]=11	2.30	2.40	2.51	V	
	high speed mode	ICG1.BOR_lev[1:0]=00	1.80	1.90	2.00	V		
		Ultra low speed mode ICG1.BOR_lev [1:0]=01	1.90	2.00	2.10	V		
			ICG1.BOR_lev [1:0]=10	2.00	2.10	2.20	V	
			ICG1.BOR_lev [1:0]=11	2.20	2.30	2.40	V	
VPVD1 PVD1 Monitoring Voltage(3)		Super high speed mode PVD1LVL[2:0]=000	1.99	2.09	2.20	V		
			PVD1LVL[2:0]=001	2.09	2.20	2.30	V	
			PVD1LVL[2:0]=010	2.30	2.40	2.51	V	
			PVD1LVL[2:0]=011	2.54	2.67	2.79	V	
			PVD1LVL[2:0]=100	2.65	2.77	2.90	V	
			PVD1LVL[2:0]=101	2.75	2.88	3.00	V	
			PVD1LVL[2:0]=110	2.85	2.98	3.11	V	
			PVD1LVL[2:0]=111	2.96	3.08	3.21	V	
	high speed mode	PVD1LVL[2:0]=000	1.90	2.00	2.10	V		
		Ultra low speed mode PVD1LVL[2:0]=001	2.00	2.10	2.20	V		
			PVD1LVL[2:0]=010	2.20	2.30	2.40	V	
			PVD1LVL[2:0]=011	2.43	2.55	2.67	V	
		PVD1LVL[2:0]=100	2.53	2.65	2.77	V		
		PVD1LVL[2:0]=101	2.63	2.75	2.87	V		
		PVD1LVL[2:0]=110	2.73	2.85	2.97	V		
		PVD1LVL[2:0]=111	2.83	2.95	3.07	V		
	VPVD2 PVD2 monitoring voltage (3)	super high speed mode PVD2LVL[2:0]=000	2.09	2.20	2.30	V		

symbol	parameter	condition	Min	Typ	Max	Unit		
		PVD2LVL[2:0]=001	2.30	2.40	2.51	V		
		PVD2LVL[2:0]=010	2.54	2.67	2.79	V		
		PVD2LVL[2:0]=011	2.65		2.77	2.90	V	
		PVD2LVL[2:0]=100	2.75		2.88	3.00	V	
		PVD2LVL[2:0]=101	2.85		2.98	3.11	V	
		PVD2LVL[2:0]=110	2.96	3.08		3.21	V	
		PVD2LVL[2:0]=111(2)	1.05		1.15	1.25	V	
		high speed mode	PVD2LVL[2:0]=000	2.00	2.10	2.20	V	
			PVD2LVL[2:0]=001	2.20	2.30	2.40	V	
			PVD2LVL[2:0]=010	2.43		2.55	2.67	V
			PVD2LVL[2:0]=011	2.53		2.65	2.77	V
			PVD2LVL[2:0]=100	2.63		2.75	2.87	V
			PVD2LVL[2:0]=101	2.73		2.85	2.97	V
			PVD2LVL[2:0]=110 (1)	2.83		2.95	3.07	V
			PVD2LVL[2:0]=111(2)	1.00		1.10	1.20	V
Hysteresis of	Vpdhyst PVD1,2(3)				100		- mV	
VPOR(1) power-on/power-down reset threshold		Rising edge VPOR		1.60	1.68	1.76	V	
		Falling edge VPDR		1.56	1.64	1.72	V	
VPORhyst	POR hysteresis				40		- mV	
IRUSH	The wave when the voltage regulator is powered on Inrush current (POR or from standby machine wake-up)				100		150 mA	
TNRST	NRST reset minimum width		500				ns	
TIPVD1	PVD1 reset release time		300	380	460	ȳs		
TIPVD2	PVD2 reset release time		300	380	460	ȳs		
TINRST	NR\$T reset release time		25	35	50	ȳs		
TRIPT	internal reset time		140	160	200	ȳs		

symbol	parameter	condition	Min	Typ	Max	Unit		
TRSTBOR	BOR reset release time		440	520	610	ÿs		
TRSTPOR	power-on reset release time			2500	3000	ÿs		

Table 3-7 Features of reset and power control modules

1. Mass production test guarantee.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is the external input comparison voltage of PVD2EXINP pin.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL[2:0] is set to 111, the PVD2 monitoring voltage is

The monitoring voltage when the PVDEXINP voltage drops, when PVD2LVD[2:0] is set to a value other than 111, the PVD2 monitoring voltage is VCC

Monitoring voltage during voltage drop.

4. The hysteresis of PVD1,2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.

PVD1 monitoring voltage when VCC rises=Vpvd1+Vpvdhyst;

PVD2 monitoring voltage when VCC is rising=Vpvd2+Vpvdhyst.



3.3.4 Supply current characteristics

Current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin loading, device

Software configuration, operating frequency, I/O pin switching rate, program location in memory, code running, etc.

The measurement method of current consumption is introduced in Figure 3-5 Current Consumption Measurement Scheme. In the various operating modes described in this section

The measured values of current consumption are obtained under laboratory conditions through a set of test codes running on FLASH.

The specific conditions are as follows:

1) All I/O pins are in input mode with static value (no load) on VCC or VSS.

2) Clock frequency selection ultra-high speed mode $f_{HCLK}=200MHz$,

High-speed mode $f_{HCLK}=168MHz/120MHz/24MHz$ and ultra-low-speed mode $f_{HCLK}=8MHz/1MHz$.

3) The power consumption mode is divided into: normal working mode `ICC_RUN`, sleep mode `ICC_SLEEP`, stop mode `ICC_STP`,

Power down mode `ICC_PD` and Dhystone working mode `ICC_DHRYSTONE`.

4) Peripheral clock ON/OFF Please refer to the specific current test items.

5) In super high speed mode $f_{HCLK}=200MHz$, in high speed mode $f_{HCLK}=168MHz/120MHz$, PLL is on

state.

Mode Parameter	Symbol	condition	Facing	product specification			Unit
				Y ^o C _Y Min	Type(1)	Max(2)	
Ultra High Speed fHCLK=200MHz	ICC_RUN	while(1), all module clock OFF	-40		16		mA
		while(1), all module clock ON	-40		29		mA
	ICC_DHRYSTONE	CACHE OFF	-40		17		mA
		CACHE ON	-40		19		mA
	ICC_SLEEP	All module clock OFF	-40		11		mA
		All module clock ON	-40		24		mA
	ICC_RUN	while(1), all module clock OFF	25		16		mA
		while(1), all module clock ON	25		29		mA
	ICC_DHRYSTONE	CACHE OFF	25		17		mA
		CACHE ON	25		19		mA
	ICC_SLEEP	All module clock OFF	25		11		mA
		All module clock ON	25		24		mA
	ICC_RUN	while(1), all module clock OFF	85			22 mA	
		while(1), all module clock ON	85			35 mA	
	ICC_DHRYSTONE	CACHE OFF	85			22 mA	
		CACHE ON	85			25 mA	
	ICC_SLEEP	All module clock OFF	85			17 mA	
		All module clock ON	85			30 mA	
	ICC_RUN	while(1), all module clock OFF	105			25 mA	
		while(1), all module clock ON	105			39 mA	
	ICC_DHRYSTONE	CACHE OFF	105			24 mA	
		CACHE ON	105			29 mA	
	ICC_SLEEP	All module clock OFF	105			21 mA	
		Clock ON for all modules	105			34 mA	

Table 3-8 Current consumption in ultra-high speed mode

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Mode Parameter	Symbol	condition	Facing	product specification			Unit
				Typ	Min	Max(2)	
High speed mode (fCLK=168MHz)	ICC_RUN	while(1), all module clock OFF	-40	-	13	-	mA
		while(1), all module clock ON	-40	-	23	-	mA
	ICC_DHRYSTONE	CACHE OFF	-40	-	14	-	mA
		CACHE ON	-40	-	15	-	mA
	ICC_SLEEP	All module clock OFF	-40	-	9	-	mA
		All module clock ON	-40	-	19	-	mA
	ICC_RUN	while(1), all module clock OFF	25	-	13	-	mA
		while(1), all module clock ON	25	-	23	-	mA
	ICC_DHRYSTONE	CACHE OFF	25	-	14	-	mA
		CACHE ON	25	-	15	-	mA
	ICC_SLEEP	All module clock OFF	25	-	9	-	mA
		All module clock ON	25	-	19	-	mA
	ICC_RUN	while(1), all module clock OFF	85	-	-	18 mA	
		while(1), all module clock ON	85	-	-	28 mA	
	ICC_DHRYSTONE	CACHE OFF	85	-	-	18 mA	
		CACHE ON	85	-	-	20 mA	
	ICC_SLEEP	All module clock OFF	85	-	-	14 mA	
		All module clock ON	85	-	-	24 mA	
	ICC_RUN	while(1), all module clock OFF	105	-	-	20 mA	
		while(1), all module clock ON	105	-	-	31 mA	
	ICC_DHRYSTONE	CACHE OFF	105	-	-	19 mA	
		CACHE ON	105	-	-	23 mA	
	ICC_SLEEP	All module clock OFF	105	-	-	17 mA	
		All module clock ON	105	-	-	27 mA	

Table 3-9 High-speed mode current consumption1

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Mode Parameter	Symbol	condition	Facing -40°C	product specification			Unit
				My Type(1)		Max(2)	
High speed fHCLK=120MHz	ICC_RUN	while(1), all module clock OFF	-40		9.5		mA
		while(1), all module clock ON	-40		16.5		mA
	ICC_DHRYSTONE	CACHE OFF	-40		10		mA
		CACHE ON	-40		11.5		mA
	ICC_SLEEP	All module clock OFF	-40		7		mA
		All module clock ON	-40		14.5		mA
	ICC_RUN	while(1), all module clock OFF	25		9.5		mA
		while(1), all module clock ON	25		16.5		mA
	ICC_DHRYSTONE	CACHE OFF	25		10		mA
		CACHE ON	25		11.5		mA
	ICC_SLEEP	All module clock OFF	25		7		mA
		All module clock ON	25		14.5		mA
	ICC_RUN	while(1), all module clock OFF	85			14 mA	
		while(1), all module clock ON	85			22 mA	
	ICC_DHRYSTONE	CACHE OFF	85			14 mA	
		CACHE ON	85			17 mA	
	ICC_SLEEP	All module clock OFF	85			12 mA	
		All module clock ON	85			20 mA	
	ICC_RUN	while(1), all module clock OFF	105			16 mA	
		while(1), all module clock ON	105			25 mA	
	ICC_DHRYSTONE	CACHE OFF	105			15 mA	
		CACHE ON	105			19 mA	
	ICC_SLEEP	All module clock OFF	105			15 mA	
		All module clock ON	105			22 mA	

Table 3-10 High-speed mode current consumption 2

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Mode Parameter	Symbol	condition	Facing °C	product specification			Unit
				My Type(1)		Max(2)	
High speed fHCLK=24MHz	ICC_RUN	while(1), all module clock OFF	-40	-	3	- mA	
		while(1), all module clock ON	-40	-	6	- mA	
	ICC_DHRYSTONE CACHE OFF		-40	-	3.5	- mA	
	ICC_SLEEP	All module clock OFF	-40	-	2	- mA	
		All module clock ON	-40	-	5.5	- mA	
	ICC_RUN	while(1), all module clock OFF	25	-	3	- mA	
		while(1), all module clock ON	25	-	6	- mA	
	ICC_DHRYSTONE CACHE OFF		25	-	3.5	- mA	
	ICC_SLEEP	All module clock OFF	25	-	2	- mA	
		All module clock ON	25	-	5.5	- mA	
	ICC_RUN	while(1), all module clock OFF	85	-	-	8 mA	
		while(1), all module clock ON	85	-	-	12 mA	
	ICC_DHRYSTONE CACHE OFF		85	-	-	7 mA	
	ICC_SLEEP	All module clock OFF	85	-	-	8 mA	
		All module clock ON	85	-	-	11 mA	
	ICC_RUN	while(1), all module clock OFF	105	-	-	10 mA	
		while(1), all module clock ON	105	-	-	14 mA	
	ICC_DHRYSTONE CACHE OFF		105	-	-	8 mA	
	ICC_SLEEP	All module clock OFF	105	-	-	10 mA	
		All module clock ON	105	-	-	14 mA	

Table 3-11 High-speed mode current consumption 3

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Mode Parameter	Symbol	condition	Facing	product specification			Unit
				Typical	Min	Max(2)	
Ultra low speed mode fHCLK=1MHz Mode 8MHz	ICC_RUN	while(1), all module clock OFF	-40	-	-	-	mA
		while(1), all module clock ON	-40	-	3.5	-	mA
	ICC_DHRYSTONE CACHE OFF		-40	-	1.5	-	mA
	ICC_SLEEP	All module clock OFF	-40	-	1.2	-	mA
		All module clock ON	-40	-	3.2	-	mA
	ICC_RUN	while(1), all module clock OFF	25	-	-	-	mA
		while(1), all module clock ON	25	-	3.5	-	mA
	ICC_DHRYSTONE CACHE OFF		25	-	1.5	-	mA
	ICC_SLEEP	All module clock OFF	25	-	1.2	-	mA
		All module clock ON	25	-	3.2	-	mA
	ICC_RUN	while(1), all module clock OFF	85	-	-	4 mA	
		while(1), all module clock ON	85	-	-	6 mA	
	ICC_DHRYSTONE CACHE OFF		85	-	-	4 mA	
	ICC_SLEEP	All module clock OFF	85	-	-	3.5 mA	
		All module clock ON	85	-	-	6 mA	
	ICC_RUN	while(1), all module clock OFF	105	-	-	6 mA	
		while(1), all module clock ON	105	-	-	7 mA	
	ICC_DHRYSTONE CACHE OFF		105	-	-	4.5 mA	
	ICC_SLEEP	All module clock OFF	105	-	-	4 mA	
		All module clock ON	105	-	-	6.5 mA	

Table 3-12 Ultra low speed mode current consumption 1

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

Mode Parameter	Symbol	condition	Facing °C	product specification			Unit
				Min	Type(1)	Max(2)	
Ultra low speed fHCLK=1MHz	ICC_RUN	while(1), all module clock OFF	-40	-	0.7	- mA	
		while(1), all module clock ON	-40	-	2.5	- mA	
	ICC_DHRYSTONE CACHE OFF		-40	-	0.9	- mA	
		All module clock OFF	-40	-	0.9	- mA	
	ICC_SLEEP	All module clock ON	-40	-	2.4	- mA	
		while(1), all module clock OFF	25	-	0.7	- mA	
		while(1), all module clock ON	25	-	2.5	- mA	
	ICC_DHRYSTONE CACHE OFF		25	-	0.9	- mA	
		All module clock OFF	25	-	0.9	- mA	
	ICC_SLEEP	All module clock ON	25	-	2.4	- mA	
		while(1), all module clock OFF	85	-	-	4 mA	
		while(1), all module clock ON	85	-	-	5 mA	
	ICC_DHRYSTONE CACHE OFF		85	-	-	3.5 mA	
		All module clock OFF	85	-	-	3.5 mA	
	ICC_SLEEP	All module clock ON	85	-	-	5 mA	
		while(1), all module clock OFF	105	-	-	5 mA	
		while(1), all module clock ON	105	-	-	5.5 mA	
	ICC_DHRYSTONE CACHE OFF		105	-	-	4 mA	
		All module clock OFF	105	-	-	5 mA	
	ICC_SLEEP	Clock ON for all modules	105	-	-	5.5 mA	

Table 3-13 Current consumption in ultra-low speed mode 2

1. Typ voltage condition VCC=3.3V
2. Max voltage condition VCC=1.8~3.6V

Mode Parameter		Symbol	Conditions (VCC=3.3V)	Facing °C	product specification			Unit
					Min(1)	Typ(2)	Max(2)	
stop mode -		ICC_STP PWC_PWRC1.STPDAS=00		-40		160		uA
			PWC_PWRC1.STPDAS=11	-40		30		uA
			PWC_PWRC1.STPDAS=00	25		220		uA
			PWC_PWRC1.STPDAS=11	25		80		uA
			PWC_PWRC1.STPDAS=00	85			3600 uA	
			PWC_PWRC1.STPDAS=11	85			3400 uA	
			PWC_PWRC1.STPDAS=00	105			4800 uA	
			PWC_PWRC1.STPDAS=11(3)	105			4600 uA	
Power down mode -		ICC_PD power down mode 1		-40		10		uA
			power down mode 2	-40		4		uA
			power down mode 3	-40		1.8		uA
			power down mode 4	-40		1.8		uA
			Power down mode 2+XTAL32+RTC	-40		6		uA
			Power down mode 2+LRC+RTC	-40		9		uA
			power down mode 1	25		10		uA
			power down mode 2	25		4		uA
			power down mode 3	25		1.8		uA
			power down mode 4	25		1.8		uA
			Power down mode 2+XTAL32+RTC	25		6		uA
			Power down mode 2+LRC+RTC	25		9		uA
			power down mode 1	85			21 uA	
			power down mode 2	85			19 uA	
			power down mode 3	85			19 uA	
			power down mode 4	85			19 uA	
			Power down mode 2+XTAL32+RTC	85			21 uA	
			Power down mode 2+LRC+RTC	85			21 uA	
			power down mode 1	105			35 uA	
			power down mode 2	105			33 uA	

Mode Parameter		Symbol	Conditions (VCC=3.3V)	Facing ÿ°Cÿ	product specification			Unit
					Min	Typ(1)	Max(2)	
			power down mode 3	105	-	-	30 uA	
			Power-down mode 4 [3]	105	-	-	30 uA	
			Power down mode 2+XTAL32+RTC	105	-	-	35 uA	
			Power down mode 2+LRC+RTC	105	-	-	35 uA	

Table 3-14 Low power mode current consumption

1. Typ voltage condition VCC=3.3V

2. Max voltage condition VCC=1.8~3.6V

3. Mass production test guarantee.

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	Facing ÿ°Cÿ	product specification			Unit
					Min	Typ	Max	
module- electric current		ICC_MODULE XTAL oscillator mode large drive 24MHz	Drives 16MHz in oscillator mode	25	-	1.8	- mA	
			Oscillation mode small drive 10MHz	25	-	0.8	- mA	
			Oscillator Mode Ultra Small Driver 8MHz	25	-	0.6	- mA	
			XTAL 32K	25	-	0.5	- mA	
			HRC	25	-	0.35	- mA	
			PLL@480MHz	25	-	2.3	- mA	
			PLL@240MHz	25	-	1.4	- mA	
			ADC	25	-	1.2	- mA	
			DAC	25	-	70	- uA	uA
			CMP	25	-	0.11	- mA	
			PGA	25	-	-	- mA	
			USBFS(1)	25	-	6	- mA	

Table 3-15 Current consumption of analog modules

1. Contains the current when the control section communicates with the USBPHY.

3.3.5 Electrical sensitivity

Chips are tested differently (ESD, LU) using specific measurement methods to determine their electrical susceptibility performance.

3.3.5.1 Electrostatic Discharge (ESD)

Apply electrostatic discharge to the pins of each sample according to each pin combination. This test complies with JESD22-A114/C101 standard.

symbol	parameter	condition	unit of maximum	
VESD (HBM) electrostatic discharge voltage (human body model)		TA =+25 °C per JESD22-A114 Standard 4000		IN
VESD(CDM) Electrostatic Discharge Voltage (Charged Device Model)	TA	=+25 °C per JESD22-C101 Standard 1000		

Table 3-16 ESD characteristics

3.3.5.2 Static Latch-up

To evaluate static latch-up performance, two complementary static latch-up tests are performed on the chip:

- Overvoltage on each supply and analog input pin
- Apply current injection to other input, output and configurable I/O pins

These tests comply with the EIA/JESD 78A IC Latch-up standard.

symbol	parameter	condition	unit of maximum	
LU	Static Latch-up	TA =+105 °C per JESD78A	200	mA

Table 3-17 Static Latch-up features

3.3.6 Low-power mode wake-up sequence

The wake-up time is measured from the wake-up event trigger to the first instruction executed by the CPU:

- For stop or sleep mode: Wakeup event is WFE.
- WKUP pin is used to wake up from standby, stop, sleep mode. All timings are at ambient temperature and VCC=3.3V

Tested out.

symbol	parameter	condition	Typical Value	Maximum	Unit
TSTOP1	wake up from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, the program program executes on RAM	2	5	
TSTOP2	wakes up from stop mode, the system clock is MRC, and the program is executed on Flash		8	15	
TPD1(1)	wakes up from power-down mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	15	25	us
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	20	30	
TPD2(1)	wakes up from power-down mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	40	50	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	45	55	
TPD3(1)	wakes up from power-down mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	2500	3000	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	2500	3000	
TPD4(1)	wakes up from power-down mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	65	75	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	70	80	

Table 3-18 Low power mode wake-up time

1. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of the PWC_PWRC3.PDTS bit.

When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, it is necessary to ensure

The PWC_PWRC3.PDTS bit is cleared. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, it needs to be

Make sure the PWC_PWRC3.PDTS bit is set before entering power-down mode.

3.3.7 I/O port characteristics

General I/O Characteristics

symbol	parameter	Condition	Min	Typ	Max.	Unit			
VIL(1)	input low level	1.8~VCC~3.6	-	-	-	0.2VCC	V		
VIH(1)	input high level	1.8~VCC~3.6	0.8VCC	-	-	-	-	IN	
VHYS	input hysteresis	1.8~VCC~3.6	-	-	0.2	-	-	IN	
ILKG(1)	I/O input leakage current	VSS~VIN~VCC	-	-	-	~1	~1	uA	
		VIN = 5.5V(2)	-	-	-	5	5	uA	
RPU(1)	weak pull-up Equivalent electricity block	USBFS_DP~USBFS_DM -	-	-	1.5	-	-	K μ	
		In addition to USBFS_DP and Other input pins of USBFS_DM foot	VIN = VSS	-	30	-	-	K μ	
		PA11/USBFS_DM PA12/USBFS_DP	-	-	10	-	-	pF	
CIO	I/O pull leg capacitance	Except PA11/USBFS_DM and Other output of PA12/USBFS_DP input pin	-	-	5	-	-	pF	

Table 3-19 I/O static characteristics

1. Mass production test guarantee.

2. To keep the voltage above VCC+0.3 V, the internal pull-up/pull-down resistors must be disabled.



The output voltage

Driver Settings	Symbol	Parameters	condition	Min	Typ	Max	Unit	
low drive		VOL(1)(2) low level output	IIO=≤1.5mA, 1.8≤VCC<2.7		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤3mA, 2.7≤VCC≤3.6		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤6mA, 2.7≤VCC≤3.6		-		1.3	
		VOH(1)(3) high level output		VCC-1.3				
medium drive		VOL(1)(2) low level output	IIO=≤3mA, 1.8≤VCC<2.7		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤5mA, 2.7≤VCC≤3.6		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤12mA, 2.7≤VCC≤3.6		-		1.3	
		VOH(1)(3) high level output		VCC-1.3				
high drive		VOL(1)(2) low level output	IIO=≤6mA, 1.8≤VCC<2.7		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤8mA, 2.7≤VCC≤3.6		-		0.4	
		VOH(1)(3) high level output		VCC-0.4				
		VOL(1)(2) low level output	IIO=≤20mA, 2.7≤VCC≤3.6		-		1.3	
		VOH(1)(3) high level output		VCC-1.3				

Table 3-20 Output voltage characteristics

1. Mass production test guarantee.

2. The IIO current sink of the device must always take into account the absolute maximum ratings specified in Table 3-3. IIO (I/O ports and control pins) of

and must not exceed IVSS.

3. The IIO source current of the device must always adhere to the absolute maximum ratings listed in Table 3-3, the IIO (I/O ports and control pins)

The sum must not exceed the IVCC.

Input/Output AC Characteristics

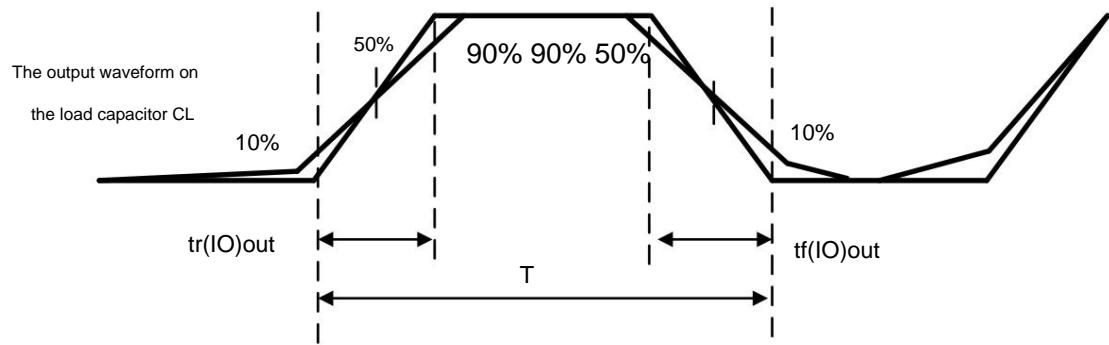
Driver settings symbol		parameter	condition(3)	Min	Typ	Max	Unit	
low drive	fmax(IO)out maximum frequency(1)		CL=30 pF, VCC \geq 2.7V	.	.	.	20	MHz
			CL=30 pF, VCC \geq 1.8V	.	.	.	10	
			CL=10pF, VCC \geq 2.7V	.	.	.	40	
			CL=10pF, VCC \geq 1.8V	.	.	.	20	
	tf(IO)out	output high to low fall time and outputs as low as High rise time	CL=30 pF, VCC \geq 2.7V	.	.	.	15	ns
			CL=30 pF, VCC \geq 1.8V	.	.	.	25	
			CL=10pF, VCC \geq 2.7V	.	.	.	7.5	
			CL=10pF, VCC \geq 1.8V	.	.	.	15	
medium drive	fmax(IO)out maximum frequency(1)		CL=30 pF, VCC \geq 2.7V	.	.	.	45	MHz
			CL=30 pF, VCC \geq 1.8V	.	.	.	22.5	
			CL=10pF, VCC \geq 2.7V	.	.	.	90	
			CL=10pF, VCC \geq 1.8V	.	.	.	45	
	tf(IO)out	output high to low fall time and outputs as low as High rise time	CL=30 pF, VCC \geq 2.7V	.	.	.	7.5	ns
			CL=30 pF, VCC \geq 1.8V	.	.	.	12	
			CL=10pF, VCC \geq 2.7V	.	.	.	4	
			CL=10pF, VCC \geq 1.8V	.	.	.	7.5	
high drive	fmax(IO)out maximum frequency (1)		CL=30 pF, VCC \geq 2.7V	.	.	.	100	MHz
			CL=30 pF, VCC \geq 1.8V	.	.	.	50	
			CL=10pF, VCC \geq 2.7V	.	.	.	180	
			CL=10pF, VCC \geq 1.8V	.	.	.	100	
	tf(IO)out	output high to low fall time and outputs as low as High rise time	CL=30 pF, VCC \geq 2.7V	.	.	.	4	ns
			CL=30 pF, VCC \geq 1.8V	.	.	.	6	
			CL=10pF, VCC \geq 2.7V	.	.	.	2.5	
			CL=10pF, VCC \geq 1.8V Table 3-21 I/	.	.	.	4	

O AC Characteristics

1. The maximum frequency is defined in Figure 3-6.

2. The load capacitance CL must take into account the capacitance of the PCB and MCU pins (the capacitance of the pins and the circuit board can be roughly estimated)

is 10 pF).



Maximum frequency condition: $(tr + tf) \leq (2/3)T$ and Duty cycle = 5.0% ± 5% (the load capacitance CL is marked in the "Condition" column of the "Input/Output AC Characteristics" table)

Figure 3-6 Definition of I/O AC characteristics

3.3.8 USART interface characteristics

symbol	parameter		min	max	unit	
tcyc	Input clock cycles	UART	4	-	-	tPCLK1
		CSI	6	-	-	
tCKw	Input Clock Width		0.4	0.6	-	tScyc
tCKr	Input Clock Rise Time		-	5	-	ns
tCKf	Input Clock Fall Time		-	5	-	ns
tTD	Send delay time	CSI	-	28	-	ns
tRDS	Receive Data Setup Time CSI		15	-	-	ns
trDH	Receive data hold time CSI		5	-	-	ns

Table 3-22 USART AC Timing

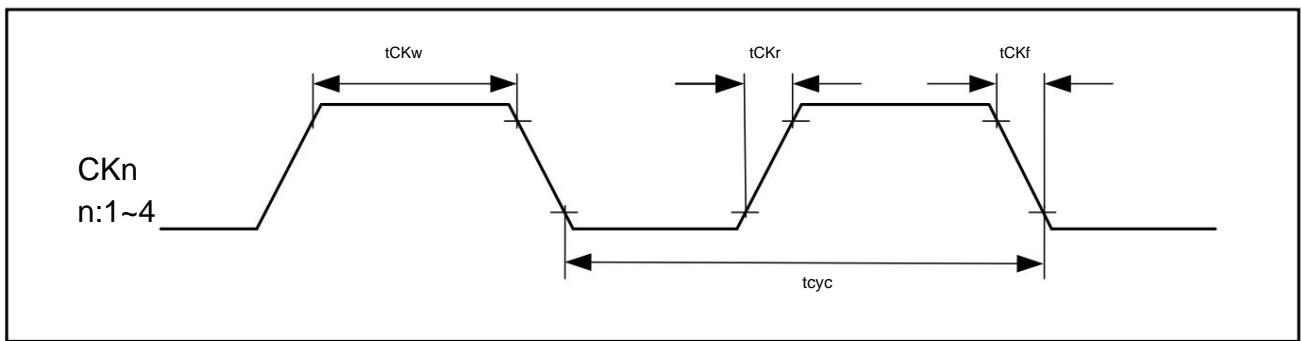


Figure 3-7 USART clock timing

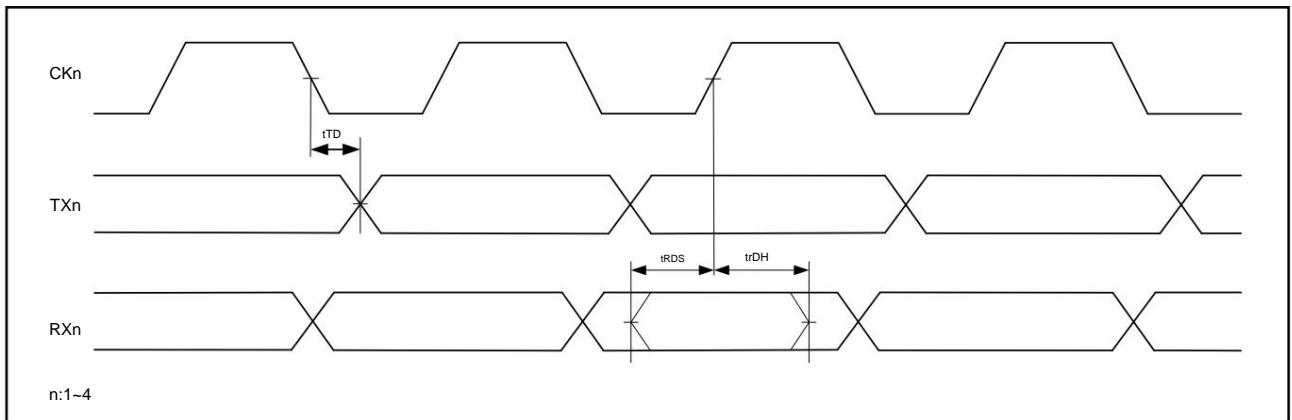


Figure 3-8 USART (CSI) input and output timing

3.3.9 I2S Interface Features

symbol	Performance	condition	Min	Max Unit	
fMCK	I2S main clock output		256 *8K 256*Fs MHz		
fCK	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits		64*Fs	
DCK	I2S clock frequency duty cycle	Slave receiver	30	70	%
tv(WS)	WS valid time	Master mode	0		ns
th(WS)	WS hold time	Master mode	0		
tsu(WS)	WS setup time	Slave mode	1		
th(WS)	WS hold time	Slave mode	0		
tsu(SD_MR)	Data input setup time	Master receiver	7.5		
tsu(SD_SR)		Slave receiver	2		
th(SD_MR)	Data input hold time	Master receiver	0		ns
th(SD_SR)		Slave receiver	0		
tv(SD_ST)	Data output valid time	Slave transmitter(after enable edge)		27	ns
th(SD_ST)		Master transmitter(after enable edge)		20	
tv(SD_MT)	Data output hold time	Master transmitter(after enable edge) Table	2.5		
th(SD_MT)					

3-23 I2S electrical characteristics

1. Fs: I2S sampling frequency

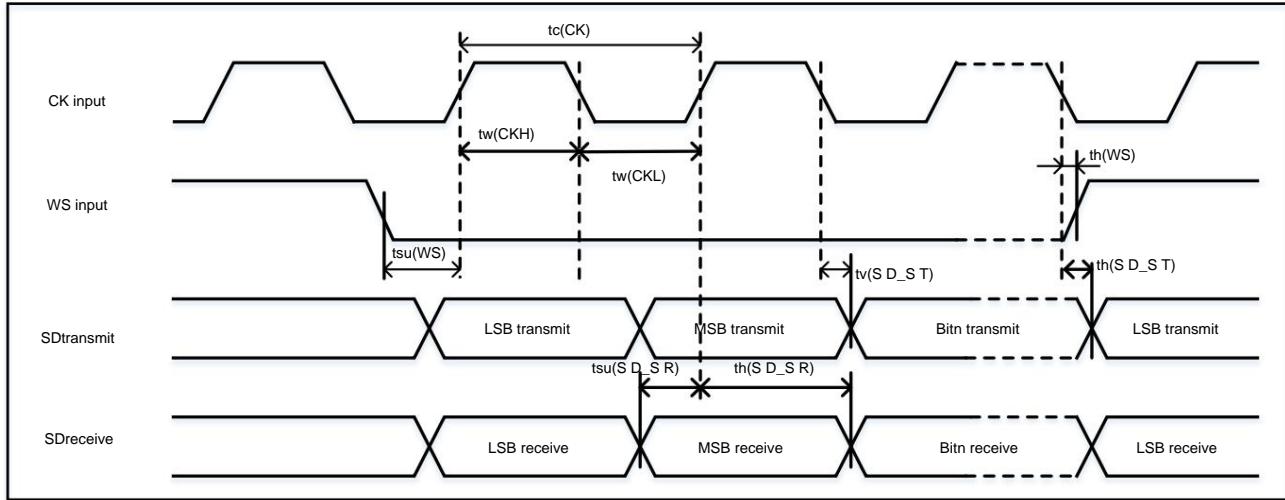


Figure 3-9 I2S slave mode timing (Philips protocol)

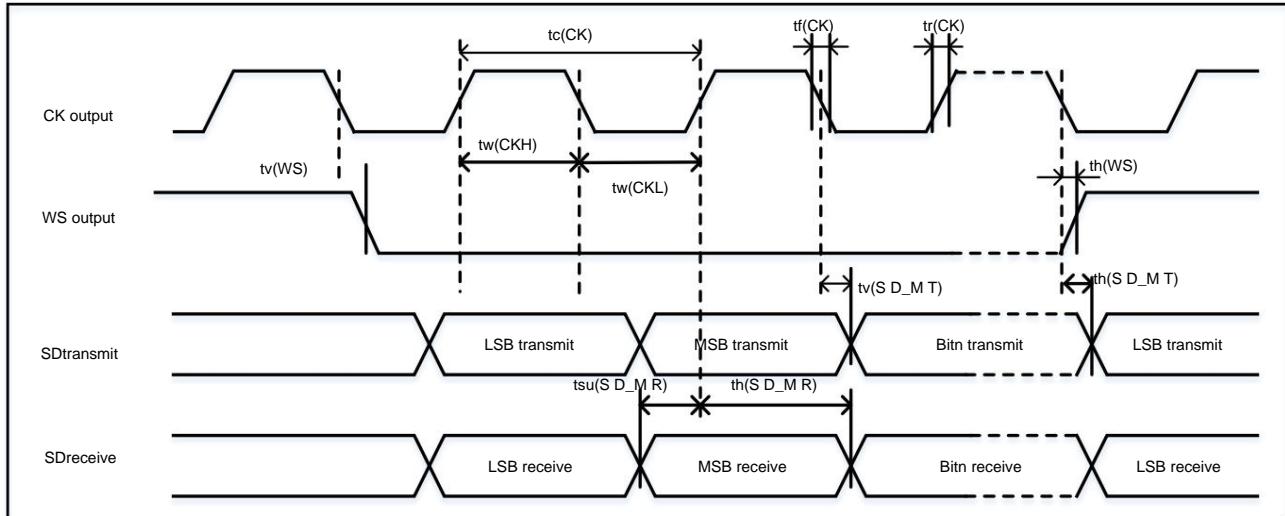


Figure 3-10 I2S master mode timing (Philips protocol)

3.3.10 I2C Interface Features

symbol	parameter	Standard Mode (SM)		Fast Mode (FM)		unit
		Min	Max	Min	Max	
fSCL	SCL frequency	0	100	0	400	KHz
tHD;STA	start condition/restart condition Hold	4.0	-	0.6	-	us
tLOW	SCL low level	4.7	-	1.3	-	us
tHIGH	SCL high level	4	-	0.6	-	us
tSU;STA	restart condition Setup	4.7	-	0.6	-	us
tHD;DAT	Data Hold	0	-	0	-	us
tSU; DAT	Data Setup	50+	tI2C reference clock period	50+	tI2C reference clock period	ns
tR	Rise time of SCL/SDA	-	1000	6.5	300	ns
tF	SCL/SDA fall time	-	300	6.5	300	ns
tSU;STO	Stop condition Setup	4	-	0.6	-	us
tBUF	from stop condition to start condition BUS idle time	4.7	-	1.3	-	us
C _b	load capacitance	-	400	-	400	pF

Table 3-24 I2C electrical characteristics

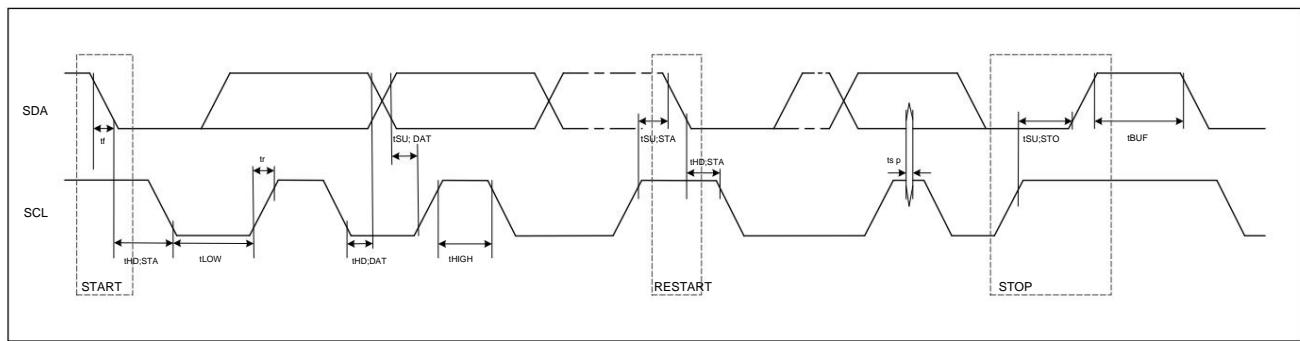


Figure 3-11 I2C bus timing definition

3.3.11 SPI Interface Features

Item	Symbol	Min	Max Unit	Test conditions
SCK clock cycle	Master	tspcyc	2 μ pclk \geq 60MHz	tpcyc Figure 3-12 C=30pF
			4 μ pclk \geq 60MHz	
SCK clock rise and fall time	Slave	tsckf	6	4096
	Master		-	5 ns
Data input setup time	Slave	tsu	-	ns Figure 3-13 C=30pF
	Master		4	
Data input hold time	Slave	th	5	ns
	Master		tpcyc	
Data output delay	Slave	tod	20	ns
	Master		-	
Data output hold time	Slave	toh	-	ns
	Master		0	
MOSI/MISO rise and fall time	Slave	tdr	-	ns
	Master		-	
SS rise and fall time	Master	tdf	-	ns
	Slave		-	
Master	CSR	tssf	-	ns
	Slave		-	

Table 3-25 SPI electrical characteristics

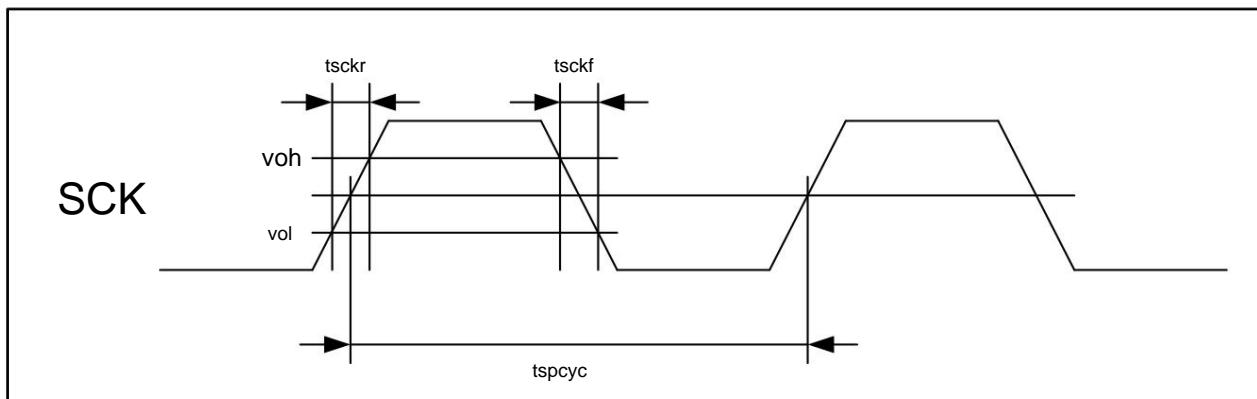


Figure 3-12 SCK Clock definition

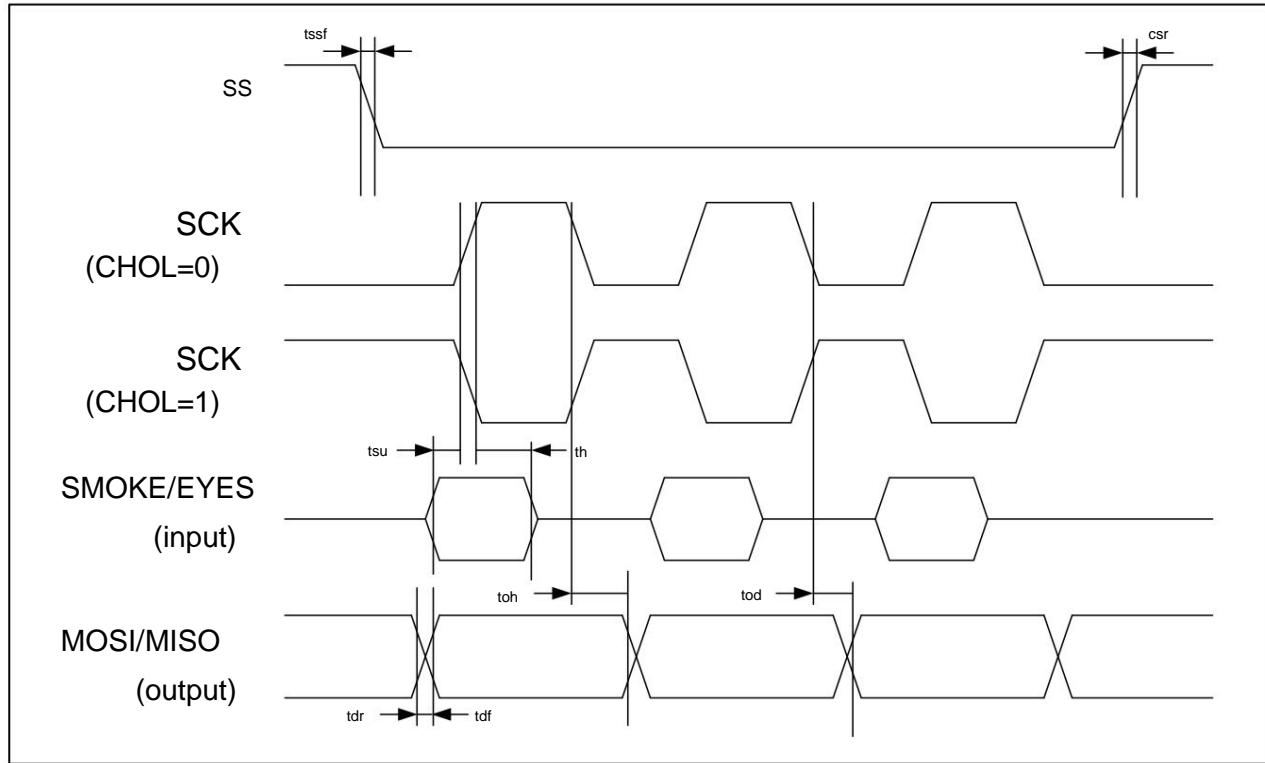


Figure 3-13 SPI interface timing requirements

3.3.12 CAN2.0B interface features

For the port characteristics of CANx_TX and CANx_RX, please refer to 3.3.7 I/O Port Characteristics.

3.3.13 Features of USB interface

Symbol	Parameter	Conditions	Min(1)	Type	Max(1) Unit	
enter	VCC working voltage		3.0(2)		3.6	IN
	VIL input low-				0.8	IN
	VIH input high-		2.0			IN
	VDI Differential Input Sensitivity -		0.2			IN
	VCM differential common mode voltage -		0.8		2.5	IN
output	VOL(3) Static	output low level RL=1.5k Ω to 3.6V(4)			0.3	IN
	VOH(3) Static	output high level RL=15k Ω to VSS(4)	2.8		3.6	IN
	VCRS	Cross-over voltage CL=50pF	1.3		2.0	IN
	tRrise time	CL=50pF $\ddot{\text{Y}}$ 10%~90% of VOH-VOL	4		20	ns
	tF fall time	CL=50pF $\ddot{\text{Y}}$ 10%~90% of VOH-VOL	4		20	ns
	tRFMA	Rise and fall time ratio tR/tF CL=50pF	90		111.1 %	
RPD(3)	Pull-down resistor	VIN= VCC $\ddot{\text{Y}}$ in host mode		15		k Ω
RPU(3)	Pull-up resistor	VIN= VSS $\ddot{\text{Y}}$ idle state	0.900	1.2	1.575 k Ω	
		VIN= VSS $\ddot{\text{Y}}$ in device mode	1.425	2.3	3.090 k Ω	

Table 3-26 USB Full-Speed electrical characteristics

1. All voltages are measured at local ground potential.

2. When the operating voltage drops to 2.7V, the function of the USB full-speed transceiver can still be guaranteed, but the complete USB full-speed electrical

characteristic, the latter degrades over a VCC voltage range of 2.7 to 3.0V .

3. Mass production test guarantee.

4. RL is the load connected to the USB full speed drive.

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit	
Input VCC	working voltage		3.0(2)		3.6	IN	
	VIL input low level				0.8	IN	
	VIH input high level		2.0			IN	
	VDI Differential Input Sensitivity -		0.2			IN	
	VCM differential common mode voltage -		0.8		2.5	IN	
Output VOL	(3) Static output low level RL=1.5k Ω to 3.6V(4)				0.3	IN	
	VOH(3) Static output high level RL=15k Ω to VSS(4)		2.8		3.6	IN	
	VCRS(3) Cross-over voltage	CL=200pF~600pF	1.3		2.0	IN	
	tR (3) rise time	CL=200pF~600pF 10%~90% of VOH-VOL	75		300	ns	
	tF (3) fall time	CL=200pF~600pF 10%~90% of VOH-VOL	75		300	ns	
	tRFMA(3) rise and fall time ratio	CL=200pF~600pF	80		125 %		
RPD(3)	Pull-down resistor	VIN= VCC $\ddot{\text{y}}$ in host mode	14.25		24.80 k Ω		

Table 3-27 USB Low-Speed electrical characteristics

1. All voltages are measured at local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed electrical characteristics, the latter degrades in the VCC voltage range of 2.7 to 3.0V.
3. Mass production test guarantee.
4. RL is the load connected to the USB low-speed driver.

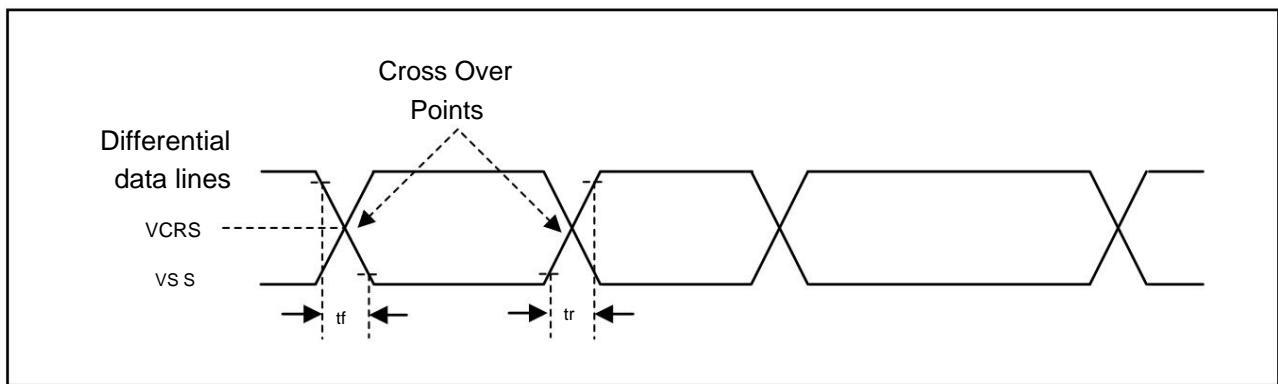


Figure 3-14 Definition of USB rise/fall time and Cross Over voltage

3.3.14 PLL characteristics

symbol	parameter	condition	Min	Typ	Max	Unit
fPLL_IN	PLL PFD(Phase Frequency Detector) input clock(1)				25	MHz
fPLL_OUT	PLL multiplier output clock		15		240	MHz
fVCO_OUT	PLL VCO output		240		480	MHz
JitterPLL	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak		±100		
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak		±150		ps
tLOCK	PLL lock time			80	120	μs

Table 3-28 PLL main performance indicators

1. It is recommended to use a higher input clock to obtain good jitter characteristics.

3.3.15 JTAG Interface Features

Symbol	Item	Min	Type	Max	Unit
tTCKcyc	JTCK clock cycle time	50	-	-	ns
tTCKH	JTCK clock high pulse width	20	-	-	ns
tTCKL	JTCK clock low pulse width	20	-	-	ns
tTCKr	JTCK clock rise time	-	-	5	ns
tTCKf	JTCK clock fall time	-	-	5	ns
tTMSs	JTMS setup time	8	-	-	ns
tTMSh	JTMS hold time	8	-	-	ns
tTDIs	JTDI setup time	8	-	-	ns
tTDIh	JTDI hold time	8	-	-	ns
tTDOd	JTDO data delay time	-	-	20	ns

Table 3-29 JTAG interface features

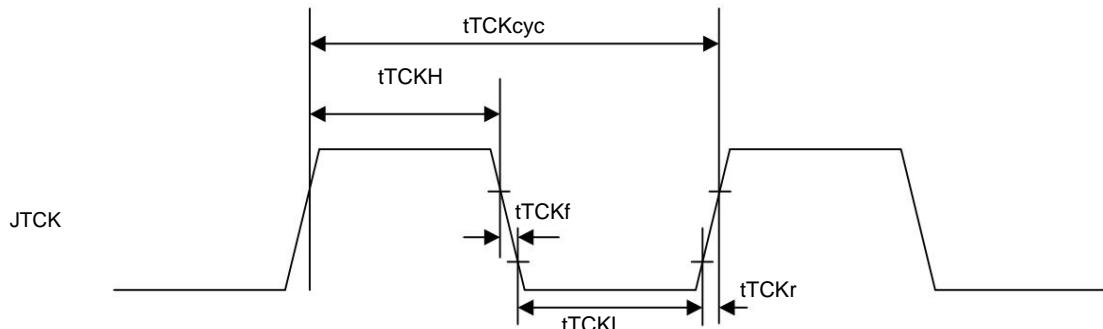


Figure 3-15 JTAG JTCK clock

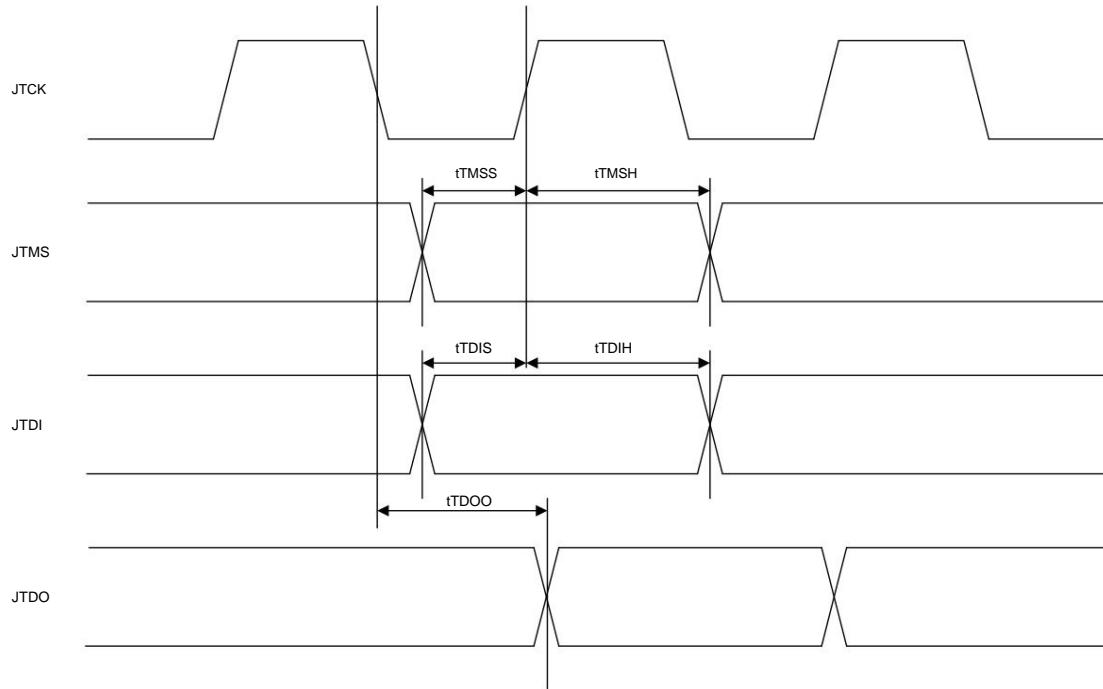


Figure 3-16 JTAG input and output

3.3.16 External clock source characteristics

3.3.16.1 High-Speed External User Clock Generated from External Source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/Os. The external clock signal must take into account the I/O static features.

symbol	parameter	condition	Min	Typ	Max	Unit		
fXTAL_EXT	user external clock source frequency					25 MHz		
VIH_XTAL	XTAL_IN input pin high level		0.8*VCC			VCC		
VIL_XTAL	XTAL_IN input pin low level		VSS			0.2*VCC		IN
tr(XTAL)	XTAL_IN rise or fall time					5		ns
tf(XTAL)								
Duty (XTAL)	duty cycle		40			60 %		

Table 3-30 High-speed external user clock characteristics

3.3.16.2 High Speed External Clock Generated by Crystal / Ceramic Resonator

The high-speed external (XTAL) clock can be generated using a 4 to 25 MHz crystal/resonant oscillator.

In the application, the resonator and load capacitors must be placed as close as possible to the pins of the oscillator to minimize output distortion and start-up stabilization time. For details on resonator characteristics (frequency, package, accuracy, etc.), please consult Crystal Resonator manufacturer.

symbol	parameter	condition	Min	Typ	Max	Unit
fXTAL_IN oscillator frequency			4	-	25	MHz
RF (1)	Feedback resistor		-	300	-	k Ω
AXTAL(2)	XTAL precision	-	-500	-	500	ppm
Gmax	Oscillator Gm	Vibrate	4	-	-	mA/V
tSU(XTAL)(3) startup time		VCC is stable, crystal oscillator=8MHz	-	2.0	-	ms
		VCC is stable, crystal oscillator=4MHz	-	4.0	-	ms

Table 3-31 XTAL 4-25 MHz oscillator characteristics

1. Mass production test guarantee.

2. This parameter depends on the resonator used in the application system.

3. tSU(XTAL) is the start-up time, that is, the time from when XTAL is enabled by software until a stable 8MHz oscillation frequency is obtained

between. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality crystal or resonator designed for high-frequency applications.

External ceramic capacitors (see figure below). CL1 and CL2 are usually the same size, CL1=CL2=2*(CL-Cs).

Cs is PCB and MCU pins (XTAL_IN, XTAL_OUT) stray capacitance.

Resonators with integrated capacitors

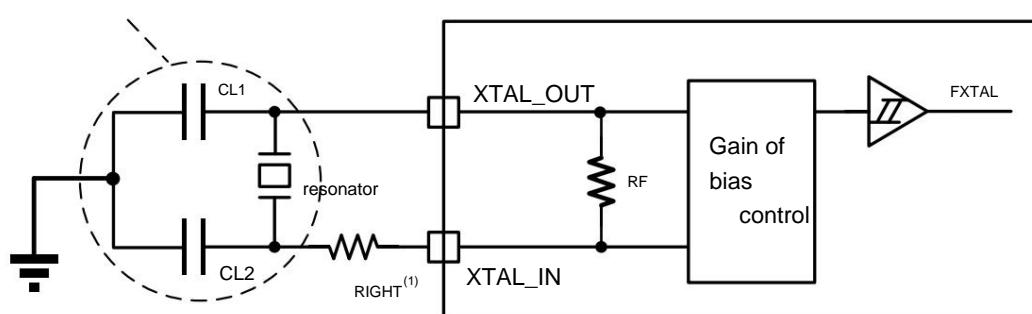


Figure 3-17 Typical application using 8 MHz crystal oscillator

1. The value of REXT depends on the crystal characteristics.

3.3.16.3 Low Speed External Clock Generated by Crystal / Ceramic Resonator

A low-speed external clock can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. In this application, the resonator and load capacitors must be placed as close as possible to the pins of the oscillator to minimize output distortion and start-up stabilization time. For more information on resonator characteristics (frequency, packaging, accuracy, etc.), consult Crystal Resonator vibrator manufacturer.

symbol	parameter	condition	Specification			unit
			Min	Type	Max	
FXTAL32 frequency		-	-	32.768	-	kHz
RF (1)	Feedback Resistor-	-	-	15	- My	
IDD_XTAL32 power consumption		XTAL32DRV[2:0]=000	-	0.8	-	μA
AXTAL32(2) XTAL32 precision -		-	-500	-	500 ppm	
Gmmax	Oscillator Gm	-	5.6	-	-	uA/V
TSUXTAL32 start-up time (3) Table 3-32 XTAL32 oscillator characteristics under VCC		stable state	-	2	-	s

1. Mass production test guarantee.

2. This parameter depends on the resonator used in the application system.

3. TSUXTAL32 is the start-up time, which is measured from the software enabling XTAL32 until a stable 32.768 kHz oscillation frequency is obtained.

rate this time. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, high quality external ceramic capacitors are recommended (see figure below). CL1 and CL2 are large

Small is usually the same, CL1=CL2=2*(CL-Cs). Cs are PCB and MCU pins (XTAL32_IN,

XTAL32_OUT) stray capacitance. If CL1 and CL2 are greater than 18pF, it is recommended to set

XTAL32DRV[2:0]=001 (large drive, the typical value of power consumption increases by 0.2uA).

Resonators with integrated capacitors

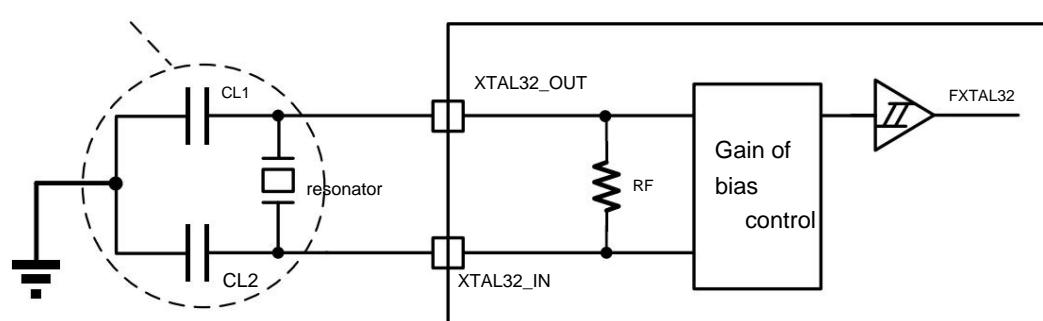


Figure 3-18 Typical application using 32.768 kHz crystal oscillator

3.3.17 Internal clock source characteristics

3.3.17.1 Internal High Speed (HRC) Oscillator

symbol	parameter	condition	Min	Typ	Max	Unit			
fHRC	frequency(1)	mode 1	.		16	.			MHz
		mode 2	.		20	.			
	User Adjustment Scale -		.		.		0.2 %		
	Frequency Accuracy(1)	TA = -40 to 105°C	-2	.	.	2	.	%	
		TA = -20 to 105°C	-1.5	.	.	1.5 %			
		TA = 25 °C	-0.5	.	.	0.5 %			
tst(HRC)	HRC Oscillator Oscillation		15	.	μs

Stable time 1.

Table 3-33 HRC oscillator characteristics

Guaranteed by mass production test.

3.3.17.2 Internal Medium Speed (MRC) Oscillator

symbol	parameter	Min	Typ	Max	Unit			
fMRC(1)	frequency	7.2	8	8.8	MHz			
tst(MRC)	MRC Oscillator Settling Time	.	.	.		3	.	μs

Table 3-34 MRC oscillator characteristics

1. Mass production test guarantee.

3.3.17.3 Internal Low Speed (LRC) Oscillator

symbol	parameter	Min	Typ	Max	Unit		
fLRC(1)	frequency	27.853	32.768	37.683	kHz		
tst(LRC)	LRC oscillator stabilization time					36	μs

Table 3-35 LRC oscillator characteristics

1. Mass production test guarantee.

3.3.17.4 SWDT dedicated internal low-speed (SWDTLRC) oscillator

symbol	parameter	Min	Typ	Max	Unit		
fSWDTLRC(1)	frequency	9	10	11	kHz		
tst(SWDTLRC)	SWDTLRC Oscillator Stabilization Time Table					57.1	μs

3-36 SWDTLRC Oscillator Characteristics

1. Mass production test guarantee.

3.3.18 12-bit ADC characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VAVCC	power supply		1.8	-	-	3.6 V		
VREFH(1)	Positive reference voltage		1.8	-	-	VAVCC V		
fADC	ADC conversion clock frequency	In super high speed/high speed operation mode VAVCC=2.4 ~3.6V	-	-	-	60	MHz	
		In super high speed/high speed operation mode VAVCC=1.8 ~2.4V	-	-	-	30		
		Ultra low speed operation mode	-	-	-	8		
VAIN	conversion voltage range-		VAVSS	-	-	VREFH V		
See Equation 1 for RAIN	external input impedance		-	-	-	50 k Ω		
RADC Sampling	Switch Resistor -		-	-	-	6 k Ω		
CADC internal	sample and hold capacitor-		-	-	4	7 pF		
tD	flip-flop conversion delay fADC = 60 MHz		-	-	-	0.3 μ s		

Table 3-37 ADC characteristics

symbol	parameter	condition	Min	Typ	Max	Unit
tS	sampling time	fADC=60MHz	0.183		4.266	μs
			11		255	1/fADC
tCONV	Single channel total conversion time (including sampling time)	fADC = 60 MHz 12-bit resolution	0.4			μs
		fADC = 60 MHz 10-bit resolution	0.36			μs
		fADC = 60 MHz 8-bit resolution	0.33			μs
		20 to 268 (sampling time tS+ successively approaching n-bit resolution+1) 1/fADC				
fS	Sampling Rate fADC = 60 MHz	12-bit resolution single ADC			2.5	Msps
		12-bit resolution time interpolation			4.6	
		Dual ADC				
tST	power on time				1	2
						μs

Table 3-38 ADC Characteristics (continued)

1. VAVCC-VREFH<1.2V

Formula 1: RAIN maximum formula

$$= \frac{\bar{y}^1}{\times \times \ln(2+2)}$$

The above equation (Equation 1) is used to determine the maximum external impedance that keeps the error below 1/4 LSB, where N = 12 (12 bits

resolution), k is the number of sampling periods defined in the ADC_SSTR register.

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=60MHz	±4.5	±6	LSB
EO offset error			±3.5	±6	LSB
EG gain error			±3.5	±6	LSB
ED Differential Linearity Error		Input source impedance <1k Ω VAVCC=2.4 ~3.6V	±1	±2	LSB
EL integral linearity error			±1.5	±3	LSB

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=60MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=30MHz	±4.5	±6	LSB
EO offset error			±3.5	±6	LSB
EG gain error			±3.5	±6	LSB
ED (1) Differential Linearity Error		Input source impedance <1k Ω VAVCC=2.4 ~3.6V	±1	±2	LSB
EL (1) integral linearity error			±1.5	±3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=30MHz

1. Mass production test guarantee.

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=30MHz	±4.5	±6	LSB
EO offset error			±3.5	±6	LSB
EG gain error			±3.5	±6	LSB
ED Differential Linearity Error		Input source impedance <1k Ω VAVCC=1.8 ~2.4V	±1	±2	LSB
EL integral linearity error			±2	±3	LSB

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In ultra-low speed operation mode fADC=8MHz	±4.5	±6	LSB
EO offset error			±3.5	±6	LSB
EG gain error			±3.5	±6	LSB
ED Differential Linearity Error		Input source impedance <1k Ω VAVCC=1.8 ~3.6V	±1	±2	LSB
EL integral linearity error			±2	±3	LSB

Table 3-42 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ fADC=8MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=60MHz	±5.5	±7	LSB
EO offset error			±4.5	±7	LSB
EG gain error			±4.5	±7	LSB
ED Differential Linearity Error		Input source impedance <1k Ω VAVCC=2.4 ~3.6V	±1.5	±2	LSB
EL integral linearity error			±2.0	±3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=60MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=30MHz	±5.5	±7	LSB
EO offset error			±4.5	±7	LSB
EG gain error			±4.5	±7	LSB
ED (1) Differential Linearity Error		Input source impedance <1k Ω VAVCC=2.4 ~3.6V	±1.5	±2	LSB
EL (1) integral linearity error			±2.0	±3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=30MHz

1. Mass production test guarantee.

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In super high speed/high speed operation mode fADC=30MHz Input source impedance <1k Ω VAVCC=1.8 ~2.4V	± 5.5	± 7	LSB
EO offset error			± 4.5	± 7	LSB
EG gain error			± 4.5	± 7	LSB
ED Differential Linearity Error			± 1.5	± 2	LSB
EL integral linearity error			± 2.5	± 3	LSB

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=30MHz

symbol	parameter	condition	Typical Value	Maximum	Unit
ET absolute error		In ultra-low speed operation mode fADC=8MHz Input source impedance <1k Ω VAVCC=1.8 ~3.6V	± 5.5	± 7	LSB
EO offset error			± 4.5	± 7	LSB
EG gain error			± 4.5	± 7	LSB
ED Differential Linearity Error			± 1.5	± 2	LSB
EL integral linearity error			± 2.5	± 3	LSB

Table 3-46 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ fADC=8MHz

symbol	parameter	condition	min	max	unit
ENOB effective number of digits		In super high speed/high speed operation mode fADC=60MHz Input signal frequency = 2kHz Input source impedance <1k Ω VAVCC=2.4 ~3.6V	10.6	.	Bits
SINAD Signal-to-Noise Harmonic Ratio			64	.	dB
SNR signal to noise ratio			66	.	dB
THD Total Harmonic Distortion			-	-70	dB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 input channel input channel dynamic accuracy @ fADC=60MHz

symbol	parameter	condition	min	max	unit
ENOB	effective number of digits	In super high speed/high speed operation mode fADC=30MHz Input signal frequency=2kHz Input source impedance <1k Ω	10.4	-	Bits
SINAD	Signal-to-Noise Harmonic Ratio		62	-	dB
SNR	signal to noise ratio		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 input channel dynamic accuracy of input channel @ fADC=30MHz

symbol	parameter	condition	min	max	unit
ENOB	effective number of digits	In ultra-low speed operation mode fADC=8MHz Input signal frequency = 2kHz Input source impedance <1k Ω	10.4	-	Bits
SINAD	Signal-to-Noise Harmonic Ratio		62	-	dB
SNR	signal to noise ratio		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

Table 3-49 ADC1_IN0~3, ADC12_IN4~IN7 input channel dynamic accuracy @ fADC=8MHz

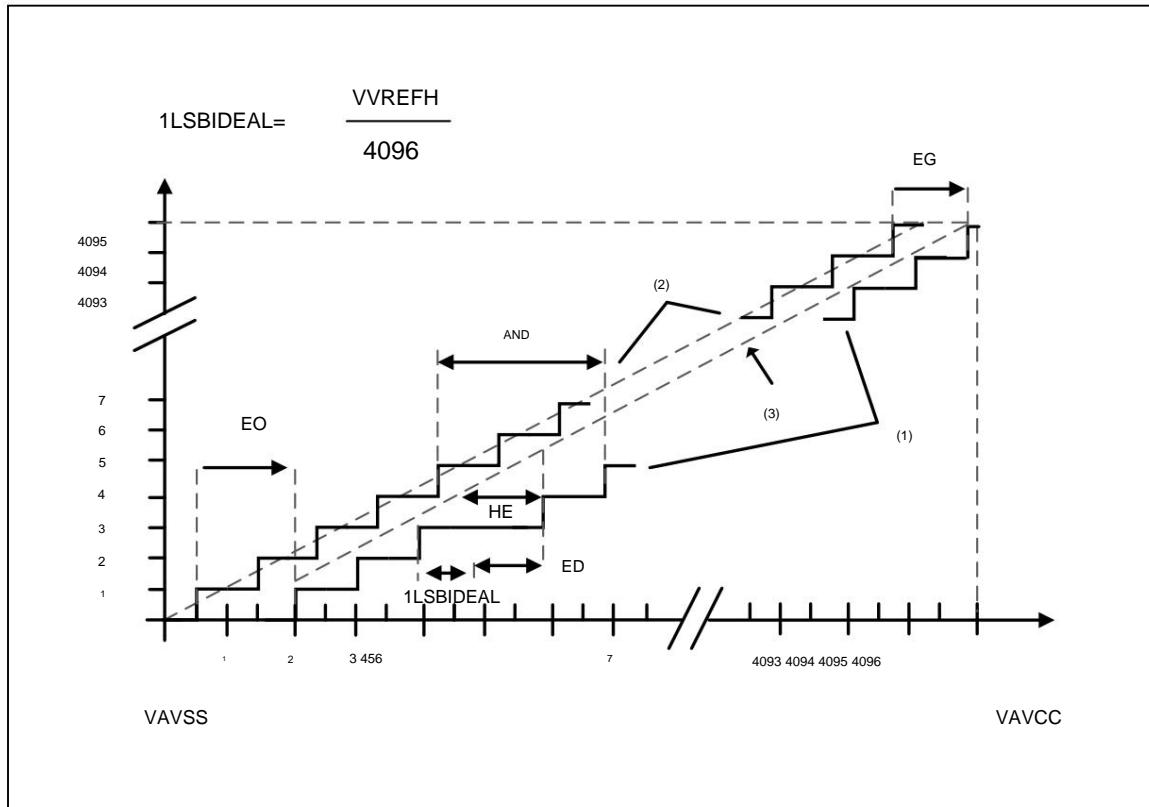


Figure 3-19 ADC Accuracy Characteristics

1. See also the table above.
2. Example of actual transfer curve.
3. Ideal transfer curve.
4. End-point relative lines.
5. ET = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.

EO = Offset Error: The deviation between the first actual transition and the first ideal transition.

EG = Gain Error: The deviation between the last ideal transition and the last actual transition.

ED = Differential Linearity Error: The maximum deviation between the actual step and the ideal.

EL = Integral Linearity Error: The maximum deviation between any actual transformation and the line associated with the endpoints.

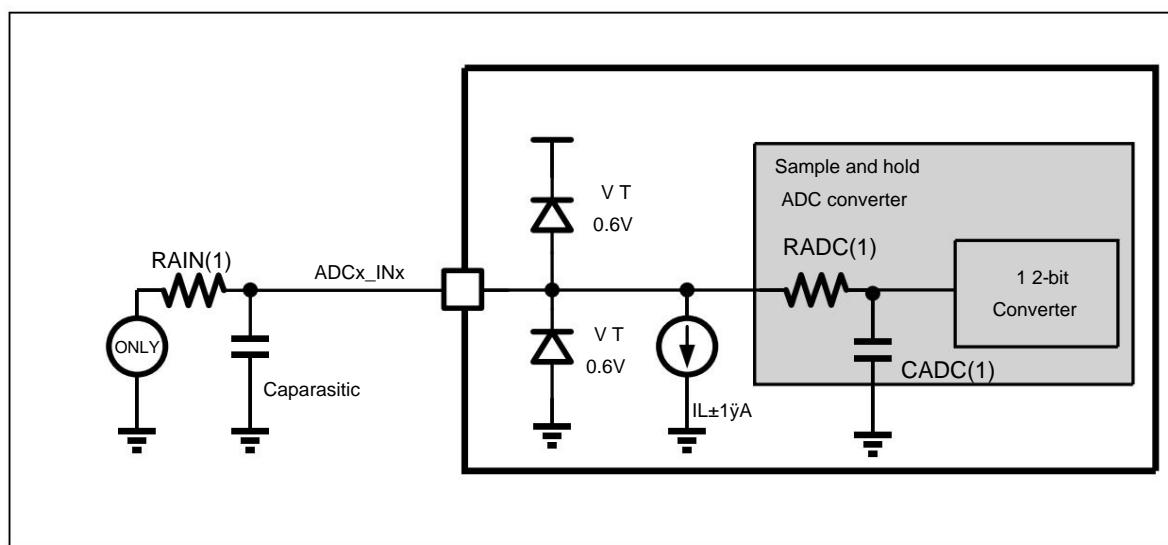


Figure 3-20 Typical connection using ADC

1. See Table 3-37 for RAIN, RADC, and CADC values.
2. Cparasitic means PCB capacitance (depending on soldering and PCB layout quality) and pad capacitance (about 5 pF). Parasitic Higher values result in less accurate conversions. To solve this problem, fADC should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below, depending on whether VREFH is connected to AVCC or not and AVCC

number of pins. The $0.1\text{ }\mu\text{F}$ capacitor should be a (high quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

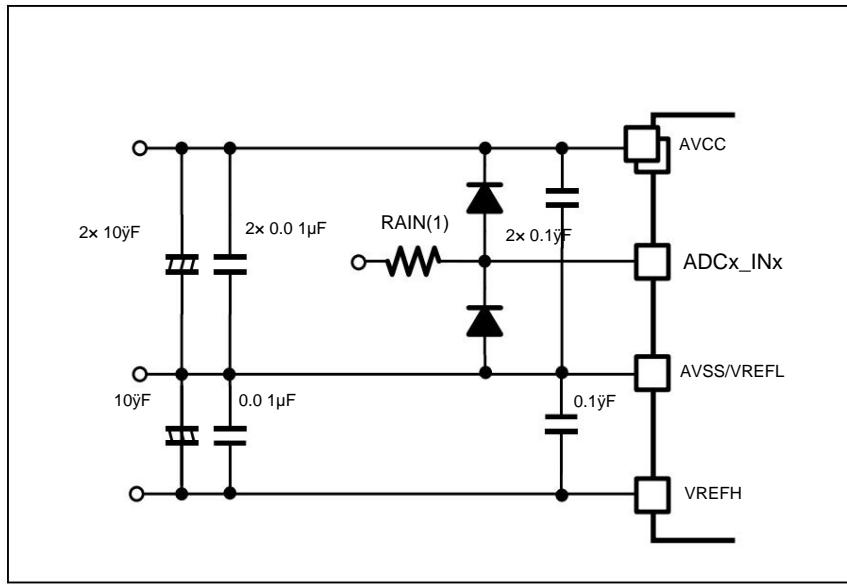


Figure 3-21 Example of decoupling power supply and reference power supply

3.3.19 DAC characteristics

symbol	parameter	Condition	Min	Typ	Max	Unit		
	VAVCC analog supply voltage		1.8	3.3	3.6	IN		
DNL	Differential nonlinearity error (two consecutive codes deviation between -1LSB)					±2	LSB	
offset	Offset Error (measured at code (0x80) value and the ideal value VAVCC/2)					±2	LSB	
SETTLING	Settling Time (Full Scale: Applies to When DA0/DA1 reaches ±4LSB of final value, between the lowest input code and the highest input code between 8-bit input codes)					8	μs	

Table 3-50 DAC characteristics

3.3.20 Comparator Characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
	VAVCC analog supply voltage		1.8	3.3	3.6	V		
WE	Input voltage range		0			VAVCC	V	
Tcmp comparison time		Comparator resolution voltage = 100mV		50	100	ns		
Tset input channel switching stabilization time -			-	100	200	ns		

Table 3-51 Comparator Characteristics

3.3.21 Gain Adjustable Amplifier Characteristics

symbol	parameter	condition	Min	Typ	Max	Unit		
VAVCC	analog supply voltage	-	1.8	3.3	3.6		IN	
YOUR(1)	Input offset voltage	-	-8	-	8		mV	
WE	Input voltage range	-	0.1*VAVCC/Gain	-	0.9*VAVCC/Gain	V		
GE	gain error	use external Mouth PGAVSS as a PGA negative phase input	Gain=2(1)	-1	-	1	%	
			Gain=2.133	-1	-	1	%	
			Gain=2.286	-1	-	1	%	
			Gain=2.667	-1	-	1	%	
			Gain=2.909	-1	-	1	%	
			Gain=3.2	-1.5	-	1.5	%	
			Gain=3.556	-1.5	-	1.5	%	
			Gain=4.0	-1.5	-	1.5	%	
			Gain=4.571	-2	-	2	%	
			Gain=5.333	-2	-	2	%	
			Gain=6.4	-3.0	-	3.0	%	
			Gain=8	-3.0	-	3.0	%	
			Gain=10.667	-4.0	-	4.0	%	
			Gain=16	-4.0	-	4.0	%	
			Gain=32(1)	-7.0	-	7.0	%	
		use internal Simulated AVSS as enter PGA negative phase input	Gain=2(1)	-2	-	2	%	
			Gain=2.133	-2	-	2	%	
			Gain=2.286	-2	-	2	%	
			Gain=2.667	-2	-	2	%	
			Gain=2.909	-2	-	2	%	
			Gain=3.2	-2.5	-	2.5	%	
			Gain=3.556	-2.5	-	2.5	%	

Gain=4.0	-2.5	-	2.5	%
Gain=4.571	-3.0	-	3.0	%
Gain=5.333	-3.0	-	3.0	%
Gain=6.4	-4.0	-	4.0	%
Gain=8	-4.0	-	4.0	%
Gain=10.667	-5.0	-	5.0	%
Gain=16	-5.0	-	5.0	%
Gain=32(1)	-8.0	-	8.0	%

Table 3-52 Gain adjustable amplifier characteristics

1. Mass production test guarantee.

3.3.22 Temperature sensor

symbol	parameter	condition	Min	Typ	Max	Unit		
TL	The relative accuracy is	calibrated individually for each chip according to the user manual -		-		±5	ÿ	

Table 3-53 Temperature sensor characteristics

3.3.23 Memory characteristics

3.3.23.1 Flash memory

When the device is shipped to the customer, the flash memory has been erased.

symbol	parameter	condition	Min	Typ	Max	Unit		
IVCC	supply current	Read mode, VCC=1.8 V~3.6V	-	-	-	5	mA	
		Programming mode, VCC=1.8V ~3.6V	-	-	-	10		
		Block erase mode, VCC=1.8 V~3.6V	-	-	-	10		
		Full erase mode, VCC=1.8 V~3.6V	-	-	-	10		

Table 3-54 Flash memory features

symbol	parameter	condition	minimum value	typical value	unit of maximum	
Tprog (1)	Word programming time single programming mode	43+2* Thclk(2)		48+4* Thclk(2)	53+6* Thclk(2)	μs
	Word programming time Continuous programming mode	12+2* Thclk(2)		14+4* Thclk(2)	16+6* Thclk(2)	μs
Terase (1)	block erase time-		16+2* Thclk(2)	18+4* Thclk(2)	20+6* Thclk(2)	ms
Tmas (1)	Full Erase Time-		16+2* Thclk(2)	18+4* Thclk(2)	20+6* Thclk(2)	ms

Table 3-55 Flash programming and erasing time

1. Mass production test guarantee.

2. Thclk is 1 cycle of CPU clock.

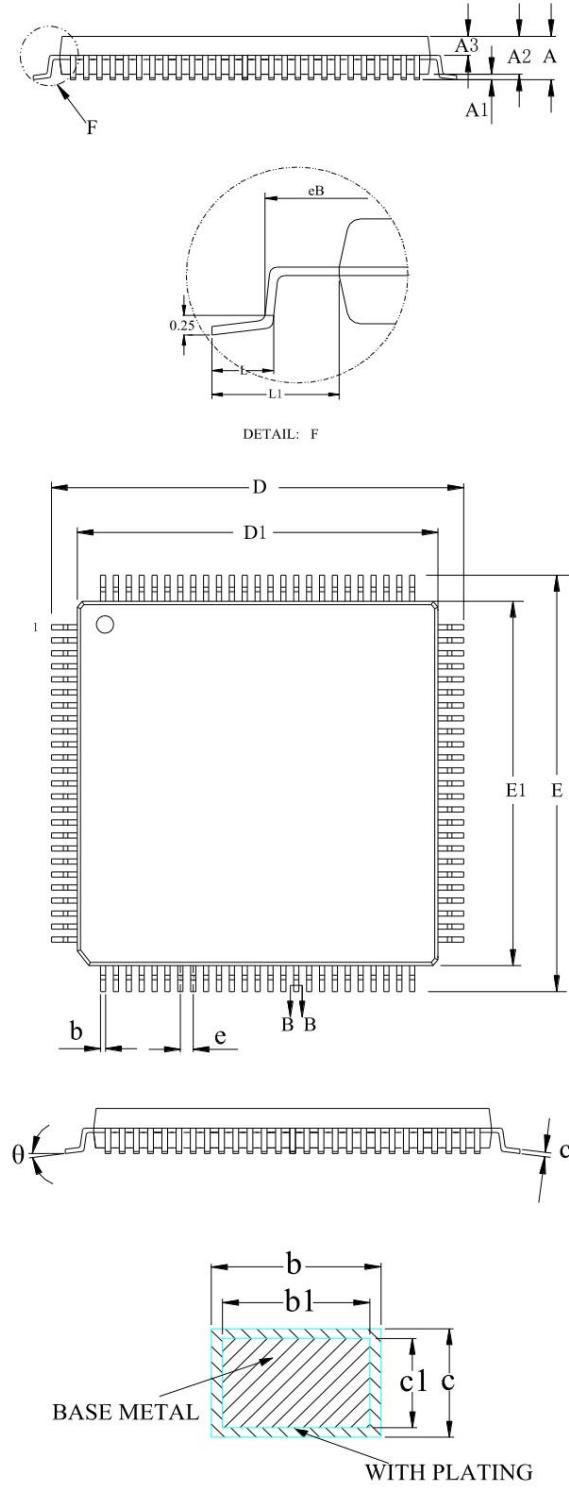
symbol	parameter	condition	value	unit
			minimum value	
Nend	Program, block erase times TA = 85°C		10	kcycles
Nend	Total erasure times	TA = 85°C	10	kcycles
Tret	Data retention period	TA = 85°C after 10 kcycles	10	Years

Table 3-56 Flash memory erasable times and data retention period

4 Package information

4.1 Package size

LQFP100 package



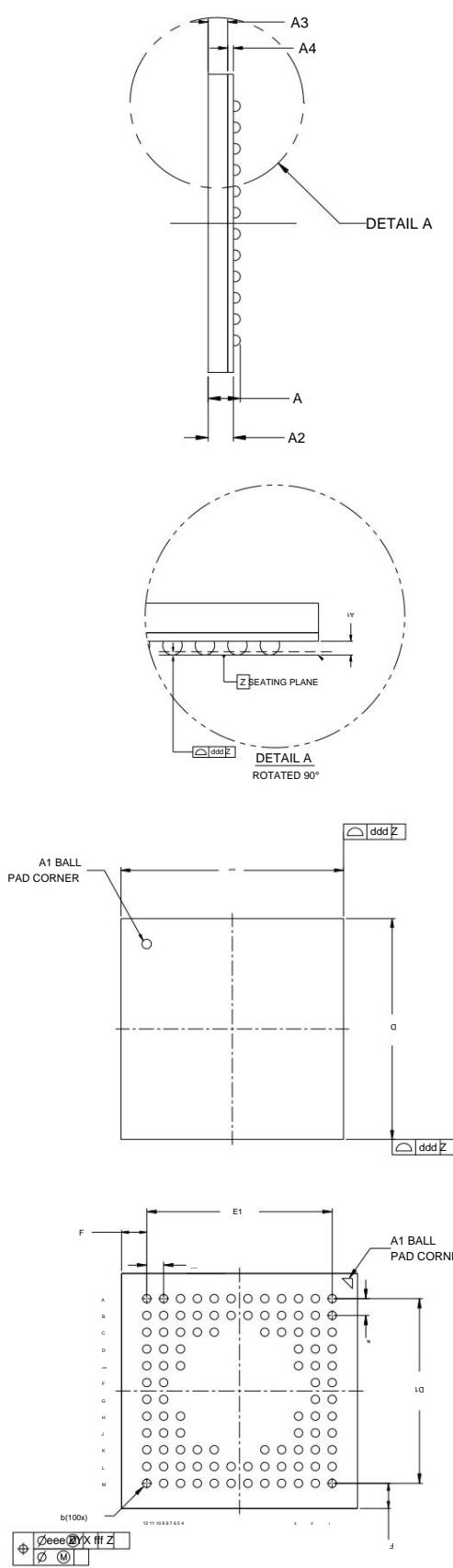
Symbol	14x14 Millimeter		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E1	13.90	14.00	14.10
It is 0.50BSC			
L	0.45	-	0.75
L1	1.00 REF		
i	0	-	7°

NOTE:

- Dimensions "D1" and "E1" do not include

mold flash.

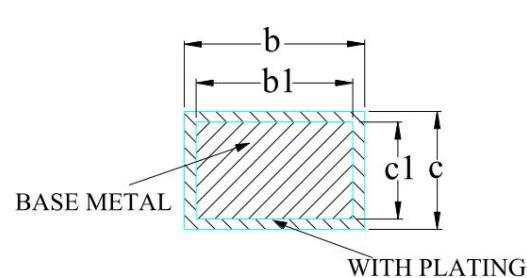
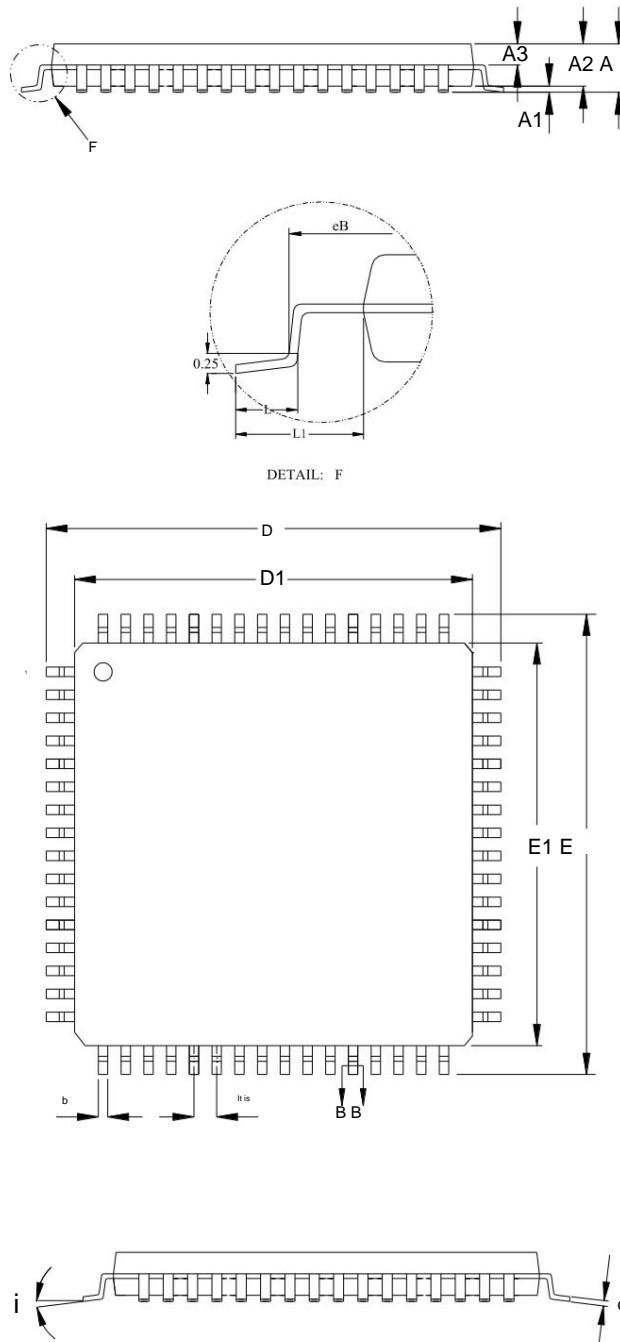
VFBGA100 package



Symbol	7x7 Millimeter		
	Min	Name	Max
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3	0.45REF		
A4	0.13REF		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D1	-	5.5	-
AND	6.90	7.00	7.10
E1	-	5.5	-
It is	-	0.5	-
F	0.75REF		
ddd	-	0.10	-
eee	-	0.15	-
fff	-	0.05	-

BOTTOM VIEW

LQFP64 package



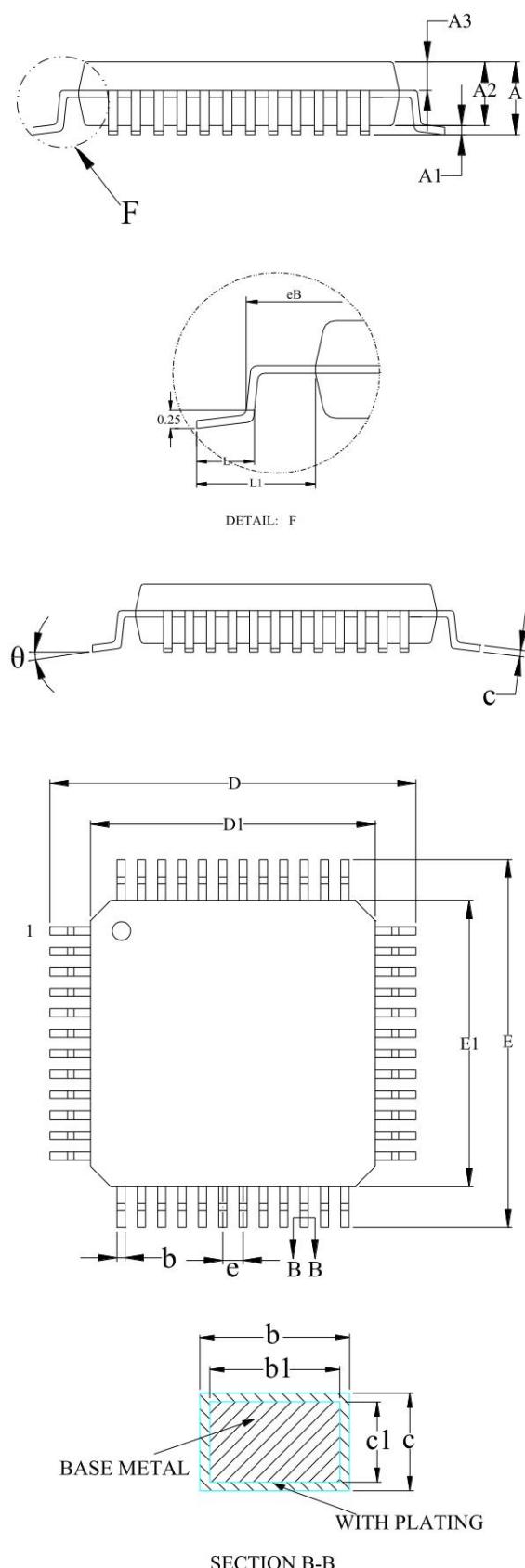
SECTION B-B

Symbol	10x10 Millimeters		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
AND	11.80	12.00	12.20
E1	9.90	10.00	10.10
It is 0.50BSC			
L	0.45	-	0.75
1.00 REF			
i	0°	-	7°

NOTE:

- Dimensions "D1" and "E1" do not include mold flash.

LQFP48 package



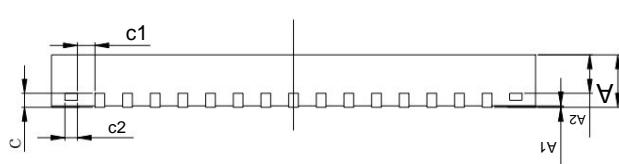
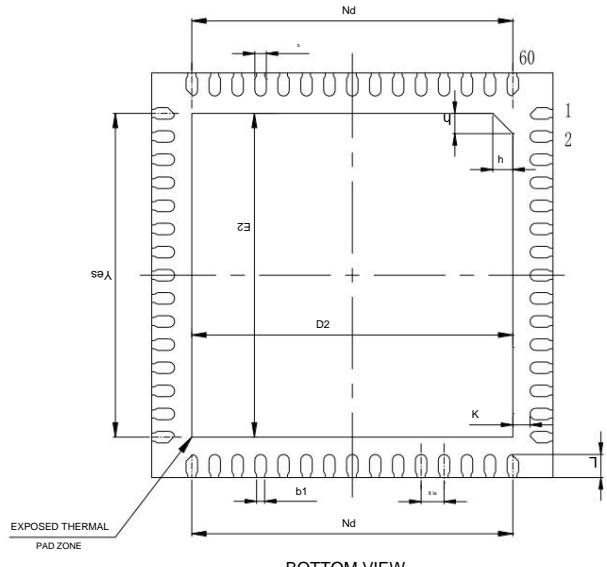
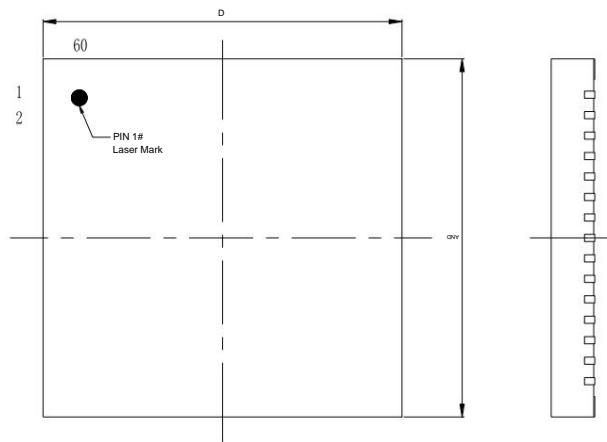
Symbol	7x7 Millimeter		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
AND	8.80	9.00	9.20
E1	6.90	7.00	7.10
It is 0.50BSC			
L	0.40	-	0.65
1.00 REF			
i	0	-	7°

NOTE:

- Dimensions "D1" and "E1" do not include

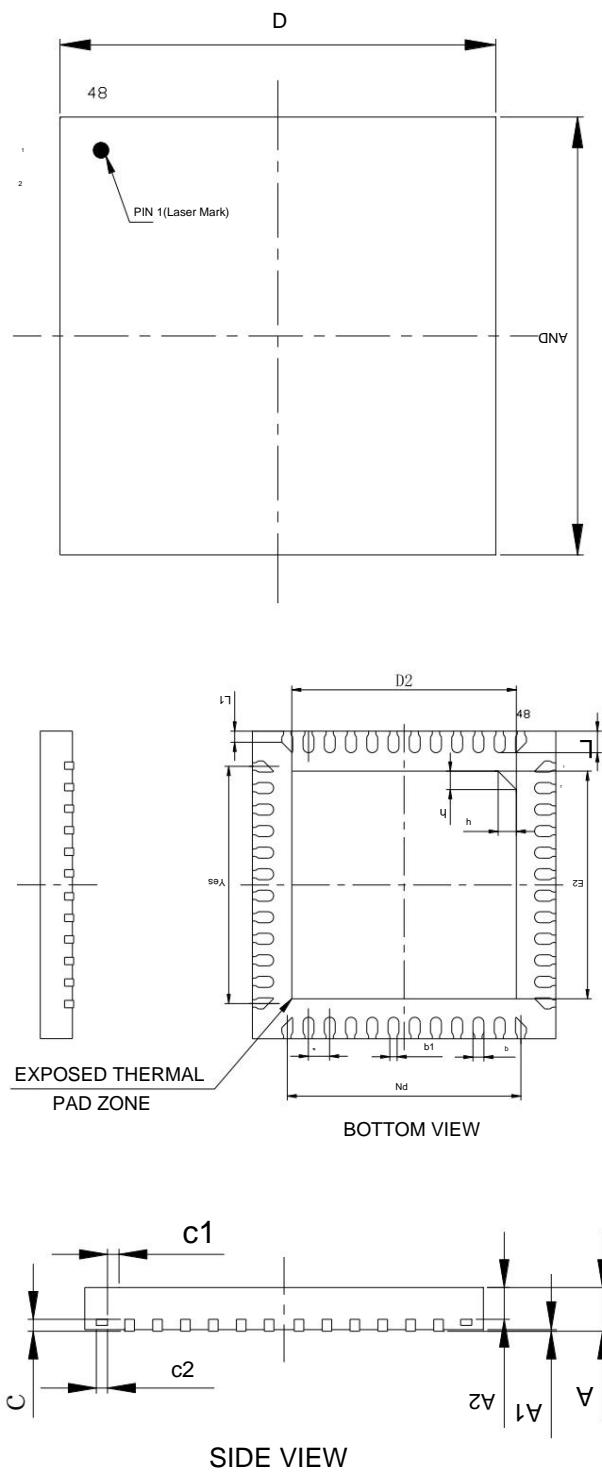
mold flash.

QFN60 package



Symbol	7x7 Millimeter		
	Min	Name	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.547REF		
b	0.15	0.20	0.25
b1	0.14REF		
c	0.20REF		
C1	0.255REF		
c2	0.18REF		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd	5.60BSC		
0.40BSC			
AND	6.90	7.00	7.10
E2	5.50	5.60	5.70
Yes	5.60BSC		
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

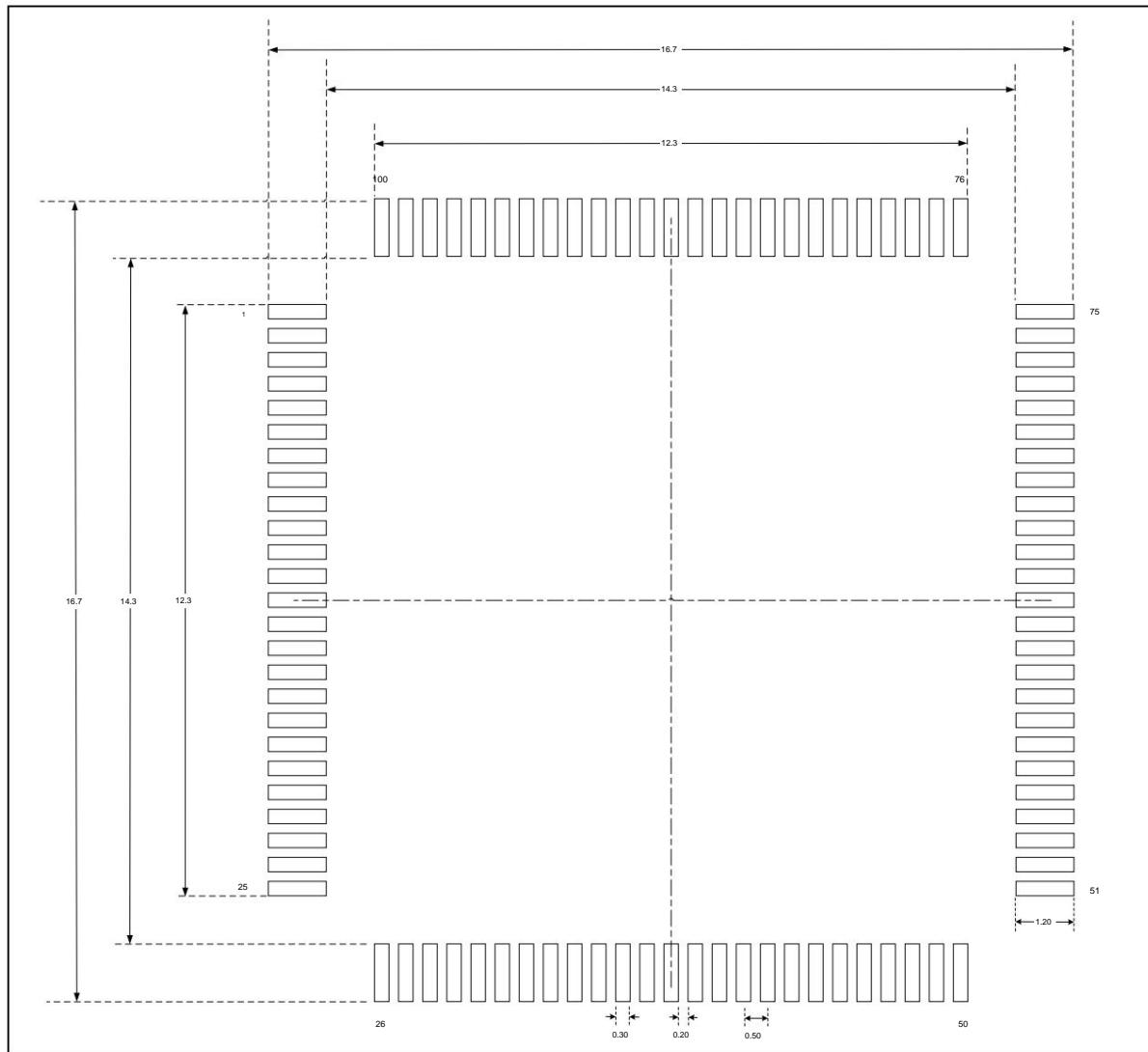
QFN48 package



Symbol	5x5 Millimeter		
	Min	Name	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.40REF		
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
c1	0.145REF		
c2	0.140REF		
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
It is			
Yes	0.35BSC		
Nd	3.85BSC		
AND	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F carrier size			
	154 x 154		

4.2 Pad diagram

LQFP100 package (14mm x 14mm)

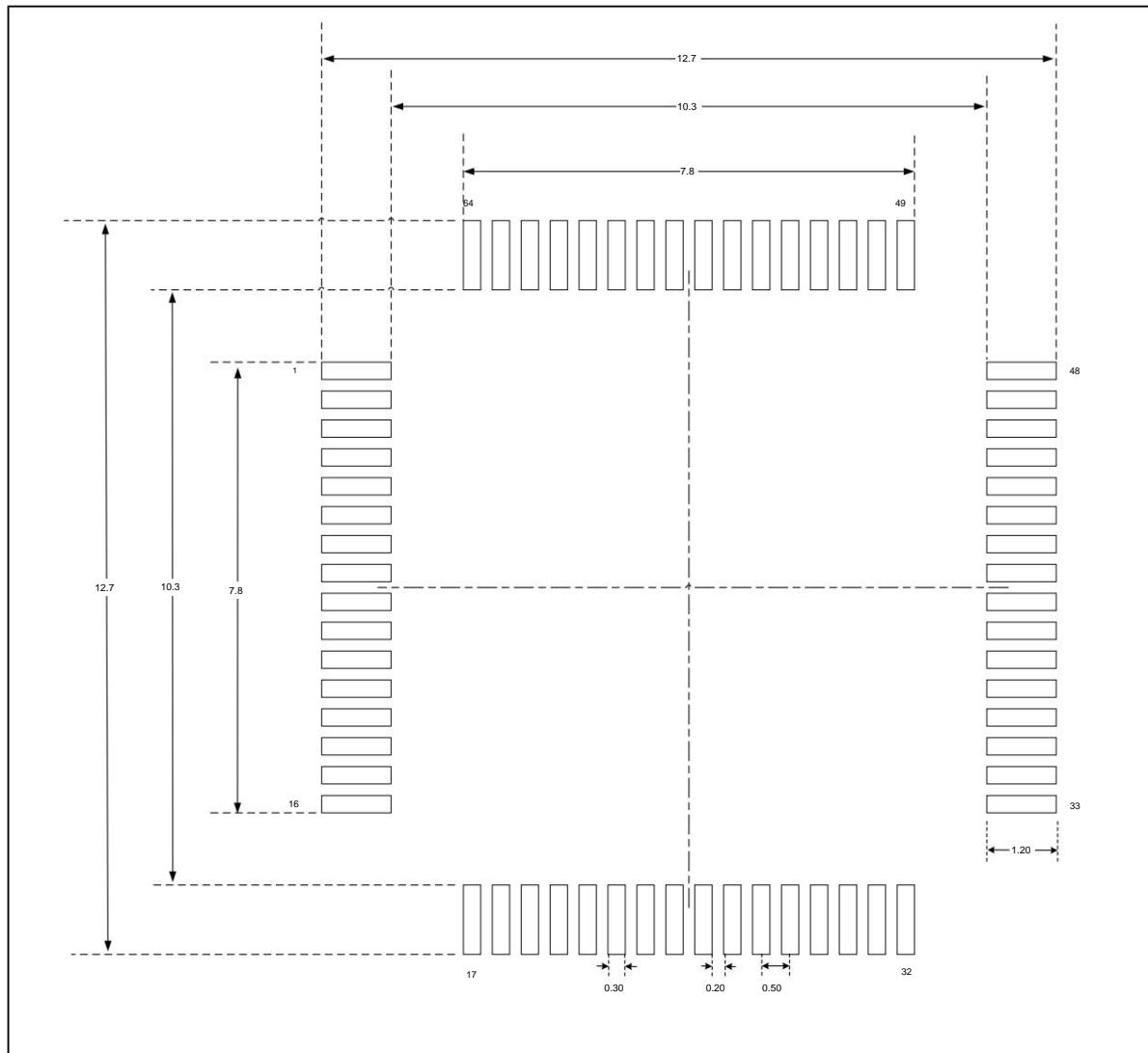


NOTE:

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

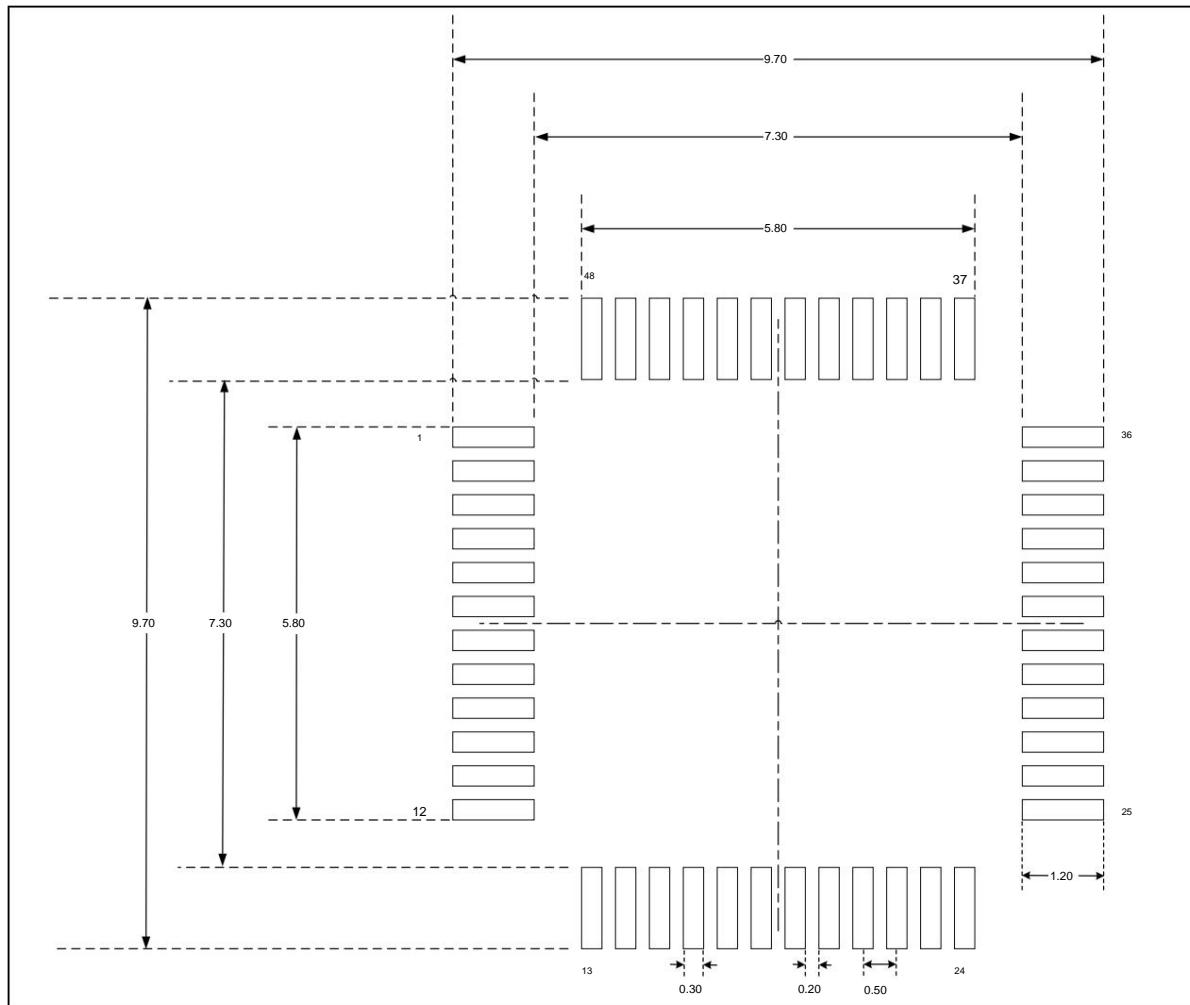
LQFP64 package (10mm x 10mm)

**NOTE:**

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

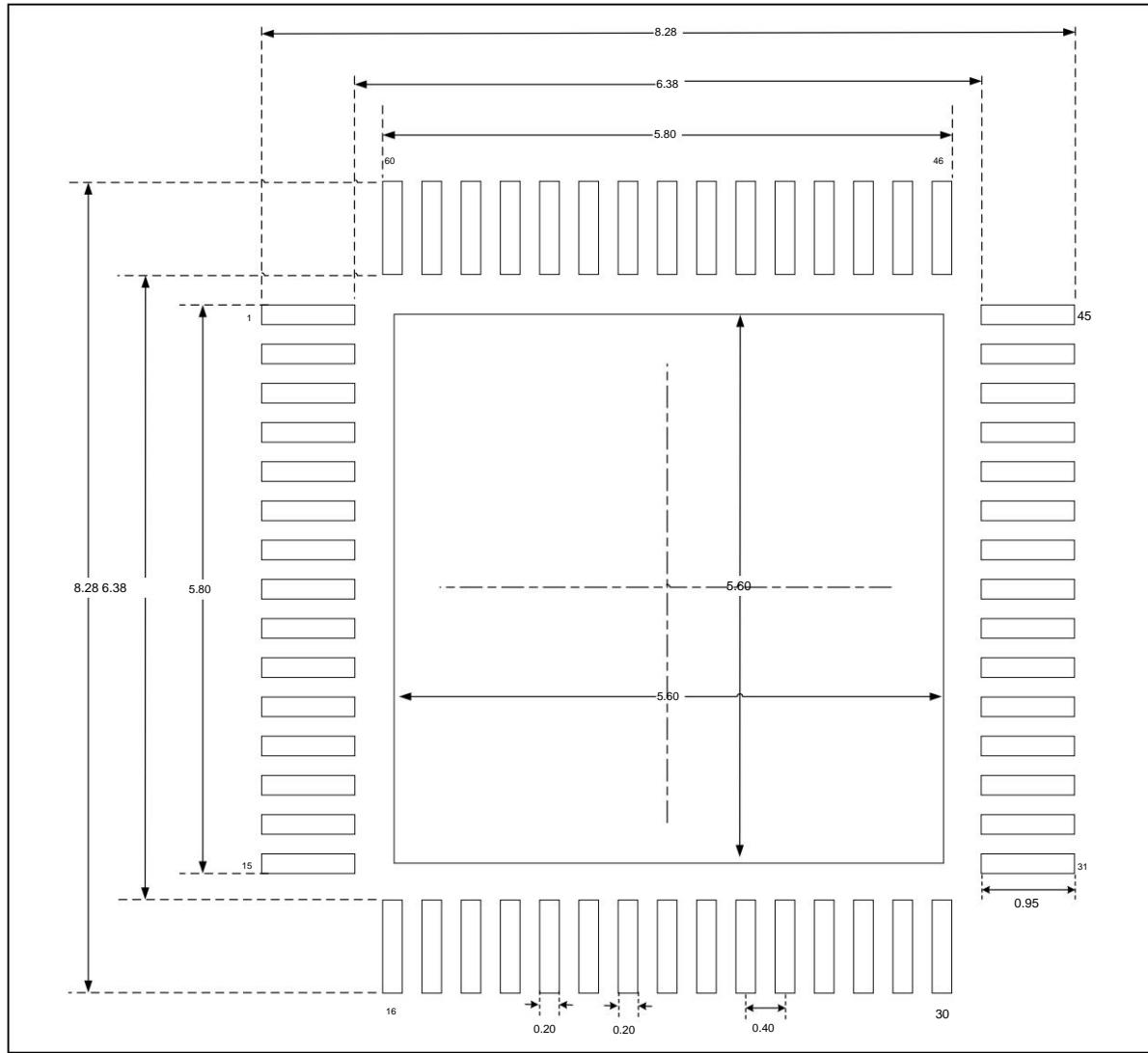
LQFP48 package (7mm x 7mm)

**NOTE:**

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

QFN60 package (7mm x 7mm)

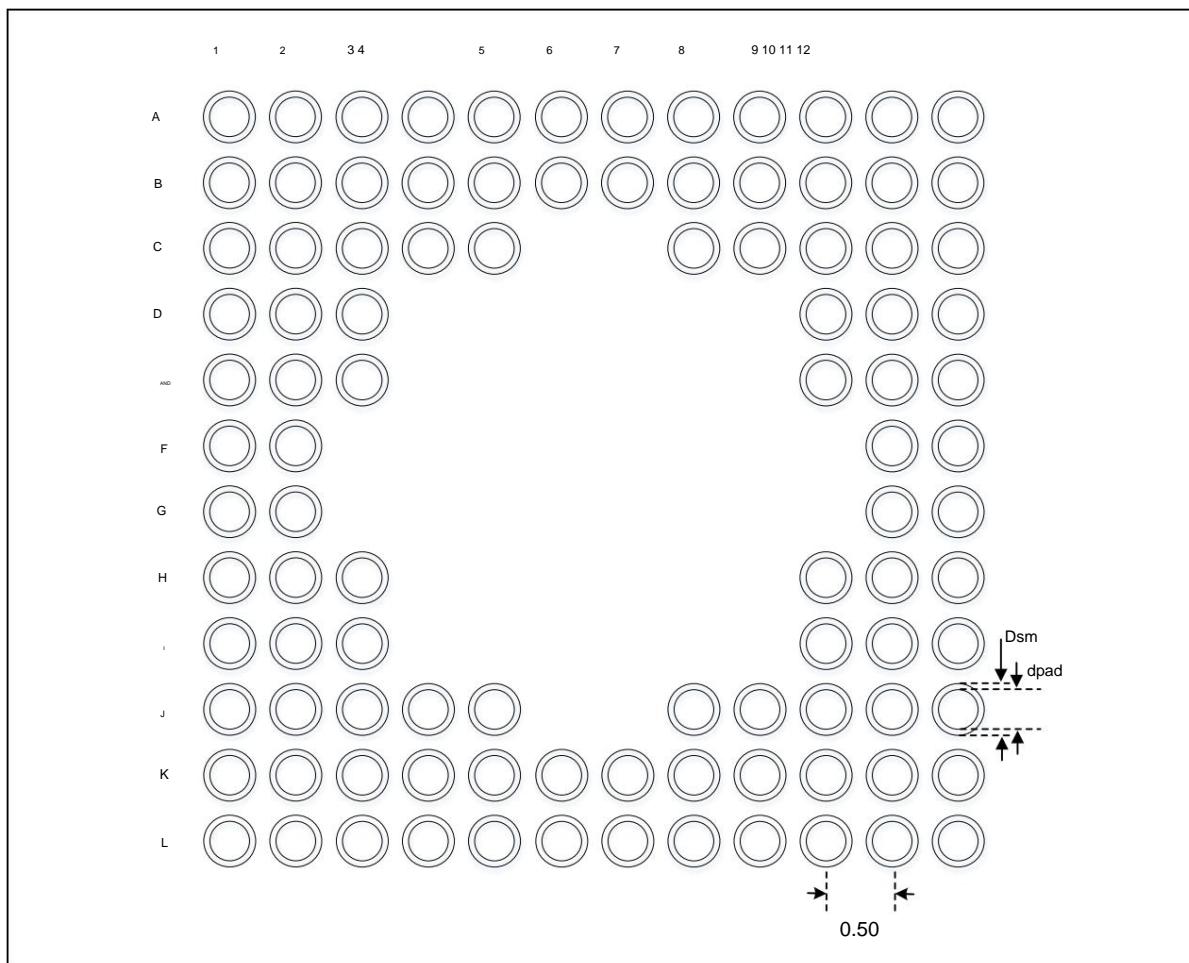


NOTE:

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

VFBGA100 package (7mm x 7mm)

**NOTE:**

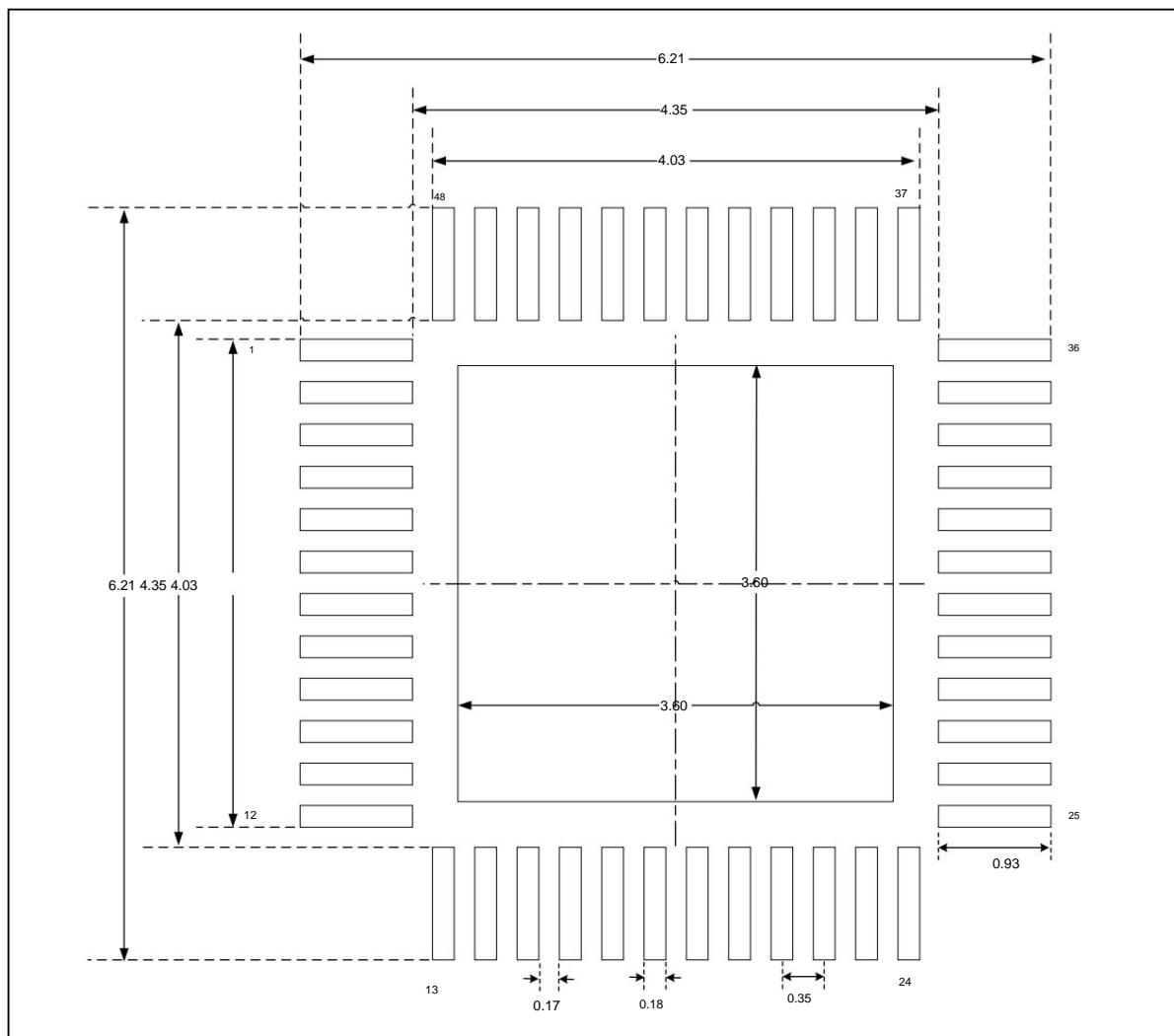
- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

VBGA100 recommended PCB design rules(0.5mm pitch)

Dimension	Recommended values
Pitch	0.5mm
dpad	0.240mm
Dsm	0.340mm typ. depends on the soldermask registration tolerance
Stencil opening	0.240mm
Stencil thickness	Between 0.100mm and 0.125mm

QFN48 package (5mm x 5mm)

**NOTE:**

- Dimensions are expressed in millimeters.

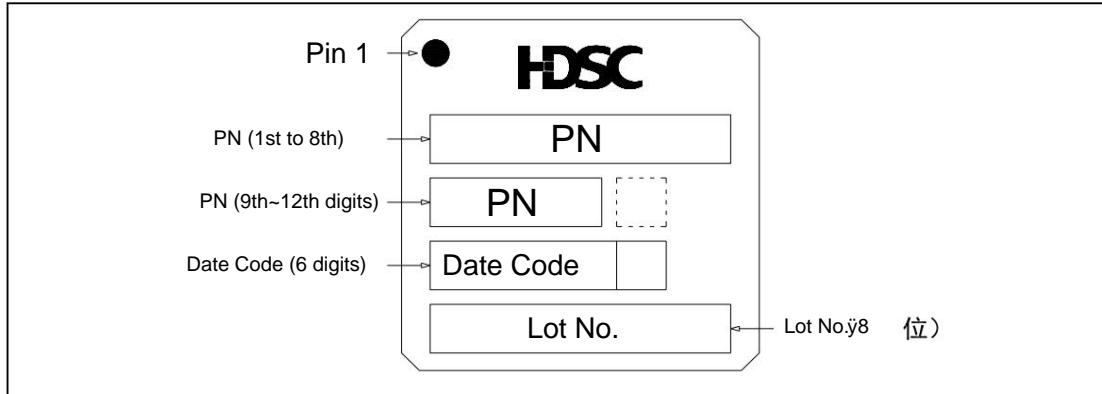
- Dimensions are for reference only.

4.3 Screen printing instructions

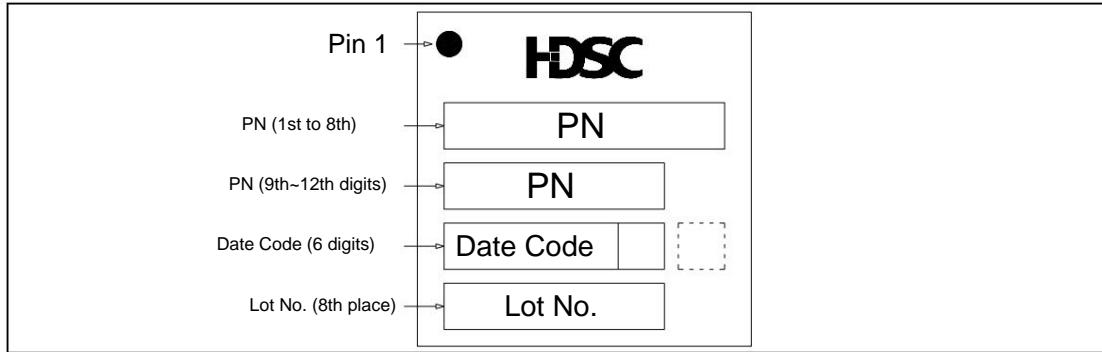
The Pin 1 position and information description of the silkscreen on the front of each package are given below.

LQFP100 package (14mm x 14mm) / LQFP64 package (10mm x 10mm)

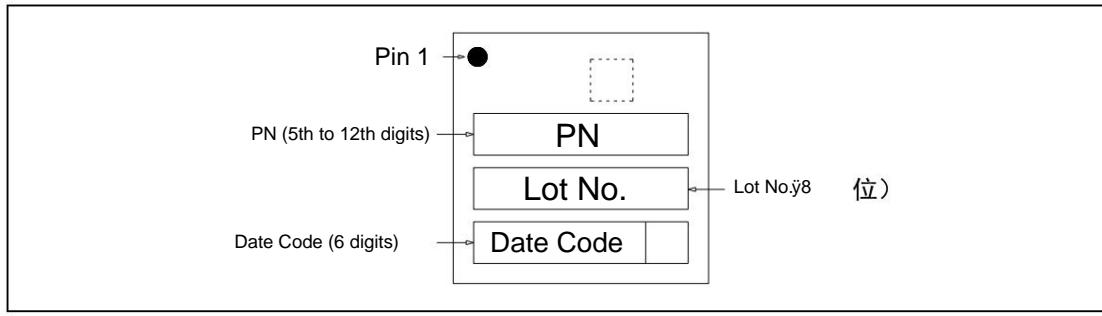
LQFP48 package (7mm x 7mm)



QFN60 package (7mm x 7mm) / VFBGA100 package (7mm x 7mm)



QFN48 package (5mm x 5mm)



Notice:

- The blank boxes in the above figure indicate optional marks related to production, which are not described in this section.



4.4 Package thermal resistance coefficient

When the packaged chip works at the specified working environment temperature, the junction temperature T_j ($^{\circ}\text{C}$) of the chip surface can be calculated according to the following formula

calculate:

$$T_j = T_{\text{amb}} + (P_D \times \theta_{JA})$$

θ T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is θ ;

$\theta \theta_{JA}$ refers to the thermal resistance coefficient of the package to the working environment, the unit is θ/W ;

θP_D is equal to the sum of internal power consumption and I/O power consumption of the chip, and the unit is W . The internal power dissipation of the chip is the IDD of the product

$\times VDD$, I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working, usually the value of this part is very small and can be

to ignore.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable temperature of the chip.

Junction temperature T_j .

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	θ/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	θ/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	θ/W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10%	θ/W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10%	θ/W

Table 4-1 Thermal resistance coefficient of each package

5 ordering information

Product number	HC32F460JEA QFN48TR	HC32F460JETA LQFP48	HC32F460KEUA QFN60TR	HC32F460KETA LQFP64	HC32F460PETB LQFP100	HC32F460PEHB VFBGA100	HC32F460JCTA LQFP48	HC32F460KCTA LQFP64	HC32F460PCTB LQFP100
Main frequency (MHz)	200	200	200	200	200	200	200	200	200
kernel	ARM Cortex-M4								
Flash (KB)	512	512	512	512	512	512	256	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5	VFBGA100 (7*7) e=0.5	LQFP48 (7*7) e=0.5	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
GPIO	38	38	50	52	83	83	38	52	83
Minimum working voltage	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Maximum working voltage	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
16-bit timer	11	11	11	11	11	11	11	11	11
Motor Control Timer	3	3	3	3	3	3	3	3	3
12-bit ADC conversion unit	2	2	2	2	2	2	2	2	2
12-bit ADC channel count	10	10	15	16	16	16	10	16	16
Comparators	3	3	3	3	3	3	3	3	3
Amplifier PGA	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I ² S	4	4	4	4	4	4	4	4	4
I ² C	3	3	3	3	3	3	3	3	3
UI(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
Full Speed USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
AES128	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
SHA256	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
WHITE	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
CRC	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
KEYSCAN	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
RTC	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
FLASH physical encryption	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
Shipping method	Tape	Plate	Tape	Plate	Plate	Plate	Plate	Plate	Plate

Before ordering, please contact the sales window for the latest mass production information.



Version Information & Contact Information

version date		Summary of revisions
Rev1.0	2019/11/12 Initial release	
Rev1.1	2020/1/10	<ul style="list-style-type: none"> ÿAdd 256KB product description in the full text; ÿAdd VFBGA package description in the full text; ÿModify the current max value of power-down mode at 105°C in the electrical characteristics; ÿUpdate the silk screen description
Rev1.2	2020/8/26	<ul style="list-style-type: none"> 1) Add the description of ultra-high-speed operation mode, update CoreMark/DMIPS, and add the description of ultra-high-speed mode. Update functional block diagram 2) Add 256KB model to pin configuration diagram 3) Add pad schematic diagram and package thermal resistance 4) Add BOR/PVD characteristics and current characteristics in ultra-high speed mode 5) Update
Rev1.3	2021/12/10	<ul style="list-style-type: none"> JTAG/SWJ debug port pins 1) Revise the statement, add A2/c1/c2 size of QFN48/60 in the package size, and modify the data retention period in the flash memory 2) External main clock crystal oscillator: (4-24MHz) changed to (4-25MHz) 3) Functional block diagram modification: USB_DMA -> USBFS_DMA; I2S_1 -> I2S_2; Add AOS 4) 1.4.6 Address <ul style="list-style-type: none"> 0x00000400H-0x0000041FH -> 0x0000_0400-0x0000_041F 0x00000408-0x0000041F -> 0x0000_0408-0x0000_041F 5) Add the introduction description of "Automatic Operation System (AOS)", update the description of "KeySCAN" 6) Correct the name and optimize the description 7) Modify the recommended configuration of bypass capacitors for analog power pins in the power scheme diagram, and delete the 10nF capacitor, the 10uF capacitor is changed to 1uF. 8) Add parameter items in the reset and power control module characteristic table: TIPVD1/TIPVD2/TINRST/TRSTBOR TRSTTAO->TRSTPOR 9) 3.3.12 Add description of CAN2.0B interface characteristics 10) In PLL characteristics, the Max value of fPLL_IN is changed from 24MHz to 25MHz, and Jitter characteristics are added 11) 3.3.16.1 The maximum value of fXTAL_EXT is changed to 25MHz 12) 3.3.16.2 Add external high-speed oscillator 13) 3.3.16.3 Add the precision index of the external low-speed oscillator XTAL32, modify the description of CL1 and CL2
Rev1.4	2022/3/9 Company	Logo update
Rev1.41	2022/3/29	<ul style="list-style-type: none"> 1) 3.3.13 USB interface characteristics RPD delete MAX, MIN value, add Typ value 15kÿ 3.3.16 ISU(XTAL) startup time delete maximum value, add typical value 2) 4.1 LQFP100/LQFP64/LQFP48 b MAX value changed to 0.27



If you have any comments or suggestions during the purchase and use, please feel free to contact us.

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