

Wave Digital Modeling of Nonlinear 3-terminal Devices for Virtual Analog Applications

Alberto Bernardini · Alessio E. Vergani ·
Augusto Sarti

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Abstract We propose a novel modeling method for circuits containing arbitrary nonlinear 3-terminal devices, which operates in the Wave Digital (WD) domain. This approach leads to the definition of a general and flexible WD model for 3-terminal devices, whose number of ports varies from 1 to 6. The generality of the method is confirmed by the fact that the WD models of 3-terminal devices already discussed in the literature can be seen as particular cases of the model that we present here. As examples of applications of our method, we develop WD models of the three most widespread types of transistors in audio circuitry, i.e., the MOSFET, the JFET and the BJT. These models are here designed to be used in Virtual Analog audio applications, therefore their derivation is aimed at minimizing computational complexity while avoiding implicit relations between port variables, as far as possible. Proposed MOSFET and JFET models are characterized by third-order polynomial equations, hence explicit closed-form wave scattering relations are obtained. On the other hand, the Ebers-Moll model describing the BJT results in transcendental equations in the WD domain that cannot be solved analytically. In order to cope with this problem, we propose a modified Newton-Raphson (NR) method for solving the implicit Ebers-Moll equations in the WD domain. Such iterative method exhibits a significantly higher robustness and convergence rate with respect to a traditional NR method, without compromising its efficiency. Finally, WD implementations of some audio circuits containing transistors are discussed.

Keywords Virtual Analog Modeling · Wave Digital Filters · Audio Signal Processing · Nonlinear Circuits

A. Bernardini and A. Sarti are with the Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB); Politecnico di Milano, Piazza L. Da Vinci 32, 20133 Milano, Italy (e-mail: [alberto.bernardini,augusto.sarti]@polimi.it). A. E. Vergani is with STMicroelectronics S.r.l., Via Olivetti 2, Agrate Brianza, MB 20864, Italy (e-mail: alessio-emanuele.vergani@st.com).

1 Introduction

Wave Digital (WD) Filter (WDF) theory [20] was introduced in the early 70s by Fettweis as a methodology for designing digital filters based on the discretization of passive analog filters. WDFs are designed starting from a port-wise consideration of the reference analog circuit that involves a linear transformation of each pair of port variables (port voltages and port currents) into a pair of wave variables (incident waves and reflected waves) with the introduction of a free parameter per port called port resistance. In the WD domain, the reference analog circuit is modeled as a structure made of input-output blocks; the topological connections are described using multi-port scattering junctions called adaptors, while the circuit elements become one-port or multi-port blocks characterized by scalar or vectorial scattering relations. Discrete-time implementations of circuits in the WD domain preserve the energetic properties of their analog counterpart, since the trapezoidal rule is typically employed for discretizing the time derivatives of dynamic (energy-storing) elements, e.g., capacitors and inductors [20]. For these reasons, in the more recent years, WDFs proved to be suitable for Sound Synthesis through physical modeling [31] and Virtual Analog modeling [5, 17]. While the literature on linear WDFs is well established, different methods are under study for modeling nonlinear WDFs in an unified fashion [1–4, 6, 7, 26–28, 32–34, 39]. In particular, different ad-hoc approaches exist for modeling nonlinear 3-terminal devices of audio gear (e.g., vacuum tubes or transistors) in the WD domain. One common approach is to model 3-terminal devices as 3-port elements, whose port terminals are the 3 terminals of the device (e.g., Grid, Cathode and Anode for triodes [15, 24, 29, 30] or Gate, Source and Drain for Junction gate Field-effect Transistors (JFETs) [23]) and ground as terminal in common to the 3 ports. Such WD models, however, are not usable when the reference circuit exhibits feedback between the terminals of the device. For this reason, in [9] a modified Ebers-Moll model, called Extended Ebers-Moll Model, is proposed for implementing the Bipolar Junction Transistor (BJT) in more complicated topologies. A different approach is used in [27, 39, 40], where the neither series nor parallel topological connections of the reference circuit are implemented using WD multi-port scattering junctions, called \mathcal{R} -type adaptors. In such cases, nonlinear 3-terminal devices are modeled with simple 2-port WD elements, since all the topological complexity is managed by the WD junctions. \mathcal{R} -type adaptors [10, 22, 25, 36–39] are extremely powerful, as they allow us to derive WD models of circuits with arbitrary topologies and multi-port elements in a systematic fashion. However, the fact that \mathcal{R} -type adaptors are often characterized by significantly big scattering matrices could negatively affect the computational cost of the resulting WD structures. Moreover, when a multi-port nonlinear element is connected to an \mathcal{R} -type adaptor through multiple ports delay-free loops are unavoidable. For these reasons, in some cases, WD models of 3-terminal devices with more than 2 ports can still be useful to reduce the complexity/dimensionality of \mathcal{R} -type adaptors. Such models should be built while honoring as much as possible the properties of modularity and

reusability of traditional WDFs, where the circuit elements and the topological connections are modeled in a rather independent fashion [20].

This paper offers a unified modeling strategy for the WD implementation of nonlinear 3-terminal devices in different topological configurations. The described modeling strategy is then applied to the derivation of WD models of the most common transistors in audio circuitry. Such models are developed to be used in Virtual Analog applications, where the digital models of nonlinear analog devices should be characterized by good accuracy, but also light computational weight. The paper is organized as follows. Section 2 proposes a general WD 6-port model applicable to arbitrary 3-terminal devices. We will show how the proposed 6-port model can be easily reduced to all the WD models of 3-terminal devices presented in the literature. The nonlinear part of the model is confined to the 2-dimensional nonlinear mapping characterizing the actual device, even when the number of ports of the chosen WD model is greater than 2. The rest of the paper provides a discussion on the WD realization of the three most widespread transistors in audio circuitry; the MOSFET, the JFET and the BJT. In particular, in Section 3, we derive explicit analytical WD models for MOSFET and JFET transistors. To the best of our knowledge, models of the MOSFET are not yet discussed in any publication on WDFs; while, the proposed JFET model is characterized by higher accuracy than the one already presented in the literature [23]. Conversely, numerous approaches for implementing the exponential Ebers-Moll model of the BJT in the WD domain are already discussed in the literature. In [9] approximations of the Ebers-Moll model are employed for deriving analytical WD scattering relations based on the Lambert Function; however, they might be inaccurate when both diodes are conducting at the same time. Instead, in [39] tabulations of the Ebers-Moll equations are performed; while in [27] the Newton-Raphson (NR) method is adopted. The iterative method in [27] is fast and accurate; however, convergence is not guaranteed. In Section 4 of this paper, we propose an improved NR method for implementing the Ebers-Moll model in the WD domain; the method, in fact, is characterized by higher robustness and efficiency with respect to the ones presented in the literature. Section 5 presents some examples of applications of the proposed models. We describe WD implementations of an overdrive guitar effect with three MOSFETs, a guitar preamplifier circuit with two JFETs and a common emitter amplifier with one BJT. Section 6 provides a final discussion on the presented results and concludes this paper.

2 A General Wave Digital Model for 3-terminal Devices

A generic 3-terminal device can be represented as in Fig. 1(a). As outlined in [14], the most general description of a 3-terminal nonlinear resistor is implicit and its characteristic is a 2-dimensional surface in a four-dimensional space. However, practical nonlinear memoryless models of the most widespread 3-terminal devices (e.g., transistors and vacuum tubes) are expressed in ex-

plicit form using 2-dimensional nonlinear functions with two scalar independent input variables [14]. In this Section we provide general formulas that describe nonlinear models of the sort in the WD domain. In the literature

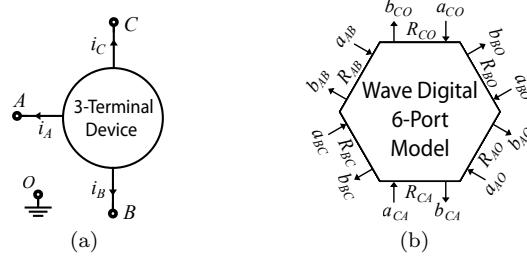


Fig. 1 A generic 3-terminal device (a) and a corresponding 6-port WD model (b).

on WDFs, some different WD models of nonlinear 3-terminal transistors and vacuum tubes with different port configurations have already been proposed [9, 15, 23, 24, 29, 39]. In the following, we present a 6-port WD model, which is applicable to general nonlinear 3-terminal devices and includes all the n -port configurations presented in the literature as particular cases, with $1 \leq n \leq 6$. The model will include the 3 terminals of the device and the ground node. In principle, it would be possible to include other nodes of the circuit and define n -port models with $n > 6$. This, however, would significantly undermine the modularity property typical of traditional WDFs, according to which all the elements of the circuit are modeled separately and independently from topological junctions called adaptors. We believe that the 6-port model presented in the following is a good compromise between modularity and generality, as it comprises only a potentially external node, i.e., the ground node, which is defined for the analysis of any circuit.

2.1 Definition of Wave Signals

The WD model is based on the following port-wise definition of wave signals

$$a = v + Ri , \quad b = v - Ri \quad (1)$$

where v is the port voltage, i is the port current, a is the *incident wave*, b is the *reflected wave*, R is a free parameter called *port resistance*. From (1) we can derive the following relations for computing the reflected waves

$$b = 2v - a , \quad (2)$$

$$b = a - 2Ri . \quad (3)$$

2.2 Kirchhoff representation of the 6-port Wave Digital Model

In [9] and [37, 39], it is shown how the WD scattering mapping of a one- or multi-port circuit element (e.g., a nonlinear device or a connection network) can be derived connecting *instantaneous Thévenin equivalents* to each port and solving the resulting circuit in the Kirchhoff domain. In particular, the voltage source and the series resistance of the Thévenin equivalent at each port are set equal to the incident wave and the port resistance, respectively; then, once a solution for port currents and/or port voltages is found equations in the form (2) or (3) are used for computing the reflected waves. The Kirchhoff representation of the proposed 6-port WD model of a general 3-terminal device with connected instantaneous Thévenin equivalents is shown in Fig. 2. Nodes are indicated with capital letters; A , B and

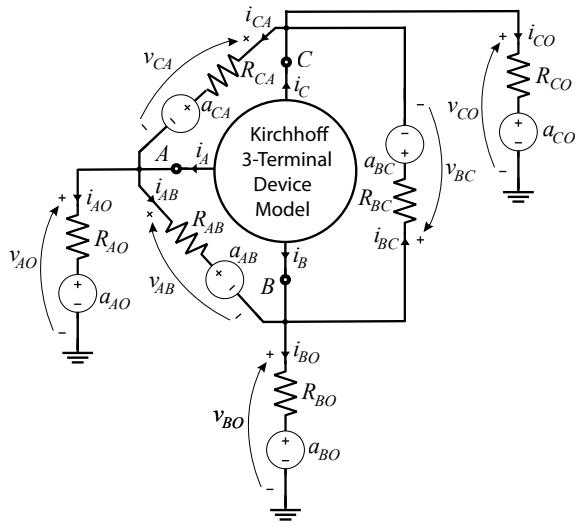


Fig. 2 Kirchhoff representation of the WD 6-port model of a generic 3-terminal device.

C indicate the nodes corresponding to the 3 terminals of the general device, while O indicates the ground node. Ports are identified by pairs of nodes, e.g., port AB is characterized by a port voltage v_{AB} , which is defined as $v_{AB} = v_A - v_B$, where v_A and v_B are the potentials at node A and B , respectively, a port current i_{AB} , whose polarity is indicated in Fig. 2, an incident wave a_{AB} , a reflected wave b_{AB} and a port resistance R_{AB} . Currents i_A , i_B and i_C are the currents flowing out from the 3 terminals of the device. According to this notation, we define the column vectors $\mathbf{i}_X = [i_A, i_B, i_C]^T$, $\mathbf{i}_{XY} = [i_{AB}, i_{BC}, i_{CA}]^T$, $\mathbf{i}_{XO} = [i_{AO}, i_{BO}, i_{CO}]^T$, $\mathbf{v}_{XY} = [v_{AB}, v_{BC}, v_{CA}]^T$, $\mathbf{v}_{XO} = [v_{AO}, v_{BO}, v_{CO}]^T$, $\mathbf{a}_{XY} = [a_{AB}, a_{BC}, a_{CA}]^T$, $\mathbf{a}_{XO} = [a_{AO}, a_{BO}, a_{CO}]^T$, $\mathbf{b}_{XY} = [b_{AB}, b_{BC}, b_{CA}]^T$ and $\mathbf{b}_{XO} = [b_{AO}, b_{BO}, b_{CO}]^T$, where the superscript T indicates the transposition operator. Such vectors and the diagonal matri-

ces $\mathbf{R}_{XY} = \text{diag}[R_{AB}, R_{BC}, R_{CA}]$ and $\mathbf{R}_{XO} = \text{diag}[R_{AO}, R_{BO}, R_{CO}]$ will be used in the derivation of the scattering relations characterizing the WD 6-port model of a generic 3-terminal device, represented in Fig. 1(b).

2.3 Definition of the Nonlinear Functions

The behavior of the 3-terminal device is described by the following equations

$$\mathbf{v}_{XY} = \mathbf{f}_v(\varphi), \quad \mathbf{i}_X = \mathbf{f}_i(\varphi), \quad (4)$$

where $\mathbf{f}_v(\varphi)$, $\mathbf{f}_i(\varphi)$ are two, generally nonlinear, functions and, with an abuse of notation, the vector $\varphi = [\varphi_1, \varphi_2]^T$ indicates a pair of independent input variables φ_1 and φ_2 (e.g., currents, voltages or dimensionless quantities). It is worth noticing that, according to Kirchhoff laws $v_{AB} + v_{BC} + v_{CA} = 0$ and $i_A + i_B + i_C = 0$, one of the three entries of the vector \mathbf{v}_{XY} can always be computed using a known linear combination of the other two and the same holds for the vector \mathbf{i}_{XY} . Functions $\mathbf{f}_i(\varphi)$ and $\mathbf{f}_v(\varphi)$ vary according to the actual 3-terminal device to be implemented. In most cases, it is possible to express \mathbf{i}_X as a nonlinear function $\mathbf{f}_i(\varphi)$ such that $\mathbf{f}_v(\varphi)$ reduces to a simple linear function (i.e., a matrix-by-vector multiplication); or, viceversa, it is possible to express $\mathbf{f}_v(\varphi)$ as a nonlinear function, such that $\mathbf{f}_i(\varphi)$ results to be linear.

2.4 Derivation of the Wave Scattering Relations

The analysis of the circuit in Fig. 2 leads to the formulation of the following mesh equations and node equations in matrix form

$$\mathbf{v}_{XO} = \mathbf{R}_{XO} \mathbf{i}_{XO} + \mathbf{a}_{XO} \quad (5)$$

$$\mathbf{v}_{XY} = \mathbf{R}_{XY} \mathbf{i}_{XY} + \mathbf{a}_{XY} \quad (6)$$

$$\mathbf{v}_{XY} = \mathbf{H} \mathbf{v}_{XO} \quad (7)$$

$$\mathbf{i}_X = \mathbf{i}_{XO} + \mathbf{H}^T \mathbf{i}_{XY} \quad (8)$$

where

$$\mathbf{H} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}.$$

Combining matrix equations (5), (6), (7), (8) and (4) we get the following matrix expression involving only incident waves, port resistances and the pair of independent variables φ

$$\begin{aligned} \mathbf{R}_{XO}^{-1} (\mathbf{H} \mathbf{R}_{XO} \mathbf{f}_i(\varphi) - (\mathbf{I} + \mathbf{H} \mathbf{R}_{XO} \mathbf{H}^T \mathbf{R}_{XY}^{-1}) \mathbf{f}_v(\varphi) + \\ + \mathbf{H} (\mathbf{a}_{XO} + \mathbf{R}_{XO} \mathbf{H}^T \mathbf{R}_{XY}^{-1} \mathbf{a}_{XY})) = \mathbf{0} \end{aligned} \quad (9)$$

where $\mathbf{0}$ is a 3×1 zero vector. It is worth noticing that, according to the considerations made in the previous Subsection, one of the three scalar equations

of the nonlinear system (9) is linearly dependent to the other two. For the sake of compactness, let us define function $\mathbf{g}(\varphi)$ as

$$\mathbf{g}(\varphi) = \mathbf{P}\mathbf{f}_i(\varphi) + \mathbf{K}\mathbf{f}_v(\varphi) + \tilde{\mathbf{a}} , \quad (10)$$

where

$$\mathbf{P} = \begin{bmatrix} P_{11} & P_{12} & P_{13} \\ P_{21} & P_{22} & P_{23} \\ P_{31} & P_{32} & P_{33} \end{bmatrix} = \mathbf{R}_{XO}^{-1} \mathbf{H} \mathbf{R}_{XO} , \quad (11)$$

$$\mathbf{K} = \begin{bmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{bmatrix} = -\mathbf{R}_{XO}^{-1} (\mathbf{I} + \mathbf{H} \mathbf{R}_{XO} \mathbf{H}^T \mathbf{R}_{XY}^{-1}) , \quad (12)$$

$$\tilde{\mathbf{a}} = [\tilde{a}_1, \tilde{a}_2, \tilde{a}_3]^T = \mathbf{R}_{XO}^{-1} \mathbf{H} (\mathbf{a}_{XO} + \mathbf{R}_{XO} \mathbf{H}^T \mathbf{R}_{XY}^{-1} \mathbf{a}_{XY}) , \quad (13)$$

such that we can rewrite (9) simply as

$$\mathbf{g}(\varphi) = \mathbf{0} . \quad (14)$$

Function $\mathbf{g}(\varphi)$ depends on the incident waves, the port resistances and the vector parameter φ ; however, only φ is indicated as input variable for the sake of brevity. How the nonlinear system (14) is solved strongly depends on the kind of nonlinearities \mathbf{f}_i and/or \mathbf{f}_v . As it will be shown in the next Sections, in some cases, closed-form solutions can be found; while, in some other cases, iterative solvers need to be used.

Solved (14) for φ , the reflected waves can be computed using the following closed form scattering relations, derived according to (2), (3) and (4)

$$\mathbf{b}_{XO} = \mathbf{a}_{XO} + 2\mathbf{R}_{XO} [\mathbf{i}_X + \mathbf{H}^T \mathbf{R}_{XY}^{-1} (\mathbf{a}_{XY} - \mathbf{v}_{XY})] , \quad (15)$$

$$\mathbf{b}_{XY} = 2\mathbf{v}_{XY} - \mathbf{a}_{XY} . \quad (16)$$

2.5 Derivation of Wave Digital n -port Models

Starting from (9), (15) and (16), which will be referred to as the 6-port model, general WD n -port models with $1 \leq n \leq 6$ can be derived. In fact, all models with $1 \leq n < 6$ can be considered as particular cases of the 6-port model, where open-circuits and/or short-circuits are connected to pairs of terminals of some ports. In particular, considering each instantaneous Thévenin equivalent in Fig. 2, under open-circuit conditions the Thévenin resistance (i.e., the port resistance of the WD model) is infinity, while, under short-circuit conditions, the Thévenin resistance and the Thévenin source (i.e., the incident wave in the WD model) are zero. In the light of this, the 6-port model, characterized by the vector equation $\mathbf{g}(\varphi) = \mathbf{0}$, is turned into a n -port model with n_o “open-circuited ports” and n_s “short-circuited ports”, such that $n + n_o + n_s = 6$, $0 \leq n_o < 6$ and $0 \leq n_s < 6$, by performing the following steps:

- take the limit of the vector function $\mathbf{g}(\varphi)$ as n_o port resistances go to infinity and n_s pairs of port resistances and incident waves go to zero and define the result as $\hat{\mathbf{g}}(\varphi)$;
- equate the expression $\hat{\mathbf{g}}(\varphi)$ resulting from the previous step to the zero vector $\mathbf{0}$, obtaining a nonlinear system of 3 equations, $\hat{\mathbf{g}}(\varphi) = \mathbf{0}$, which will be solved for φ ;
- eventually discard one equation of the derived nonlinear system, $\hat{\mathbf{g}}(\varphi) = \mathbf{0}$, since it always provides redundant information;
- derive the formulas for computing the reflected waves, as a simplified version of equations (15) and (16); performing the further following steps:
 - take the limit of the right side of equation (15) as n_o port resistances go to infinity and n_s pairs of port resistances and incident waves go to zero and define the result as $\hat{\mathbf{b}}_{XO}$;
 - equate the expression resulting from the previous step to \mathbf{b}_{XO} , i.e., $\mathbf{b}_{XO} = \hat{\mathbf{b}}_{XO}$;
 - select the scalar scattering relations for computing the needed reflected waves from the vector equations $\mathbf{b}_{XO} = \hat{\mathbf{b}}_{XO}$ and (16).

The above procedure for deriving n -port models can be performed, even using symbolic mathematical software, both before or after substituting the actual expressions of the nonlinear functions $\mathbf{f}_i(\varphi)$ and $\mathbf{f}_v(\varphi)$.

As an example, let us consider the circuit in Fig. 3(a). There are at least two different possible implementations of this circuit in the WD domain. These implementations are shown in Fig. 3(b) and Fig. 3(c). In Fig. 3(b), the 3-terminal device is modeled as a 4-port element, while, in Fig. 3(c), the same 3-terminal device is modeled as a 2-port element connected to a 6-port \mathcal{R} -type junction. Both the 4-port and the 2-port WD models for the 3-terminal device can be obtained as simplifications of the 6-port model characterized by eq. (14), following the previously described procedure.

The 4-port model is derived starting from the system of equations

$$\hat{\mathbf{g}}(\varphi) = \mathbf{0} \quad \text{where} \quad \hat{\mathbf{g}}(\varphi) = \lim_{(R_{BC}, R_{CA}) \rightarrow (\infty, \infty)} \mathbf{g}(\varphi) , \quad (17)$$

and removing one redundant equation, obtaining

$$\begin{bmatrix} 0 & -R_{BO} & R_{CO} \\ R_{AO} & 0 & -R_{CO} \end{bmatrix} \mathbf{f}_i(\varphi) + \begin{bmatrix} -\frac{R_{BO}}{R_{AB}} & 1 & 0 \\ -\frac{R_{BO}}{R_{AB}} & 0 & 1 \end{bmatrix} \mathbf{f}_v(\varphi) + \begin{bmatrix} 0 & -1 & 1 & \frac{R_{BO}}{R_{AB}} \\ 1 & 0 & -1 & \frac{R_{AO}}{R_{AB}} \end{bmatrix} \begin{bmatrix} a_{AO} \\ a_{BO} \\ a_{CO} \\ a_{AB} \end{bmatrix} = 0 . \quad (18)$$

Solved (18) for φ , the 4 reflected waves are computed using eq. (15) and a simplified version of eq. (16), i.e., $b_{AB} = 2v_{AB} - a_{AB}$.

Similarly, the 2-port model is derived, starting from the system of equations

$$\hat{\mathbf{g}}(\varphi) = \mathbf{0} \quad \text{where} \quad \hat{\mathbf{g}}(\varphi) = \lim_{(R_{AO}, R_{BO}, R_{CO}, R_{BC}) \rightarrow (\infty, \infty, \infty, \infty)} \mathbf{g}(\varphi) , \quad (19)$$

and removing one redundant equation, obtaining

$$\begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ \frac{1}{R_{AB}} & 0 & \frac{-2}{R_{CA}} \end{bmatrix} \mathbf{f}_i(\varphi) + \begin{bmatrix} \frac{1}{R_{AB}} & 0 & \frac{1}{R_{CA}} \\ \frac{-1}{R_{AB}} & \frac{-1}{R_{CA}} & 0 \\ \frac{-1}{R_{AB}} & \frac{2}{R_{CA}} & 0 \end{bmatrix} \begin{bmatrix} a_{AB} \\ a_{CA} \end{bmatrix} = 0 . \quad (20)$$

Solved (20) for φ , the 2 reflected waves are computed using $b_{AB} = 2v_{AB} - a_{AB}$ and $b_{CA} = 2v_{CA} - a_{CA}$.

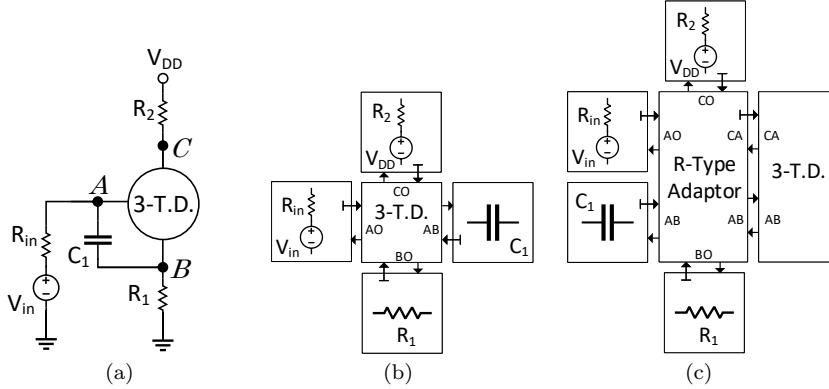


Fig. 3 Simple circuit with a generic nonlinear 3-terminal device (a). WD realization using a 4-port model of the 3-terminal device (b). WD realization using a 2-port model of the 3-terminal device and an \mathcal{R} -type adaptor (c).

3 Wave Digital Models of FET Transistors

In this Section, a method for implementing both MOSFET and JFET transistors in the WD domain is presented. A FET transistor is usually modeled considering the device in different possible operating regions (i.e., *cut-off region*, *linear or ohmic region*, *saturation region*) and describing its behavior in a case-by-case fashion. The derived WD models will be characterized by a linear equation describing the ohmic region and by third-order polynomial equations describing the other two operating regions. Closed-form formulas [13] will be adopted for solving the resulting system of equations (9). As examples of applications of the models discussed in this Section, WD realizations of audio circuits containing FET transistors will be presented in Section 5.

3.1 MOSFET Transistors

Fig. 4(a) shows a generic n-type MOSFET, whose three terminals are called *gate* (node A), *source* (node B) and *drain* (node C). A n-type MOSFET

model suitable for Virtual Analog applications is represented by the equivalent circuit in Fig. 4(b); the model is composed of an open circuit at the gate terminal and a current generator between drain and source. The current source

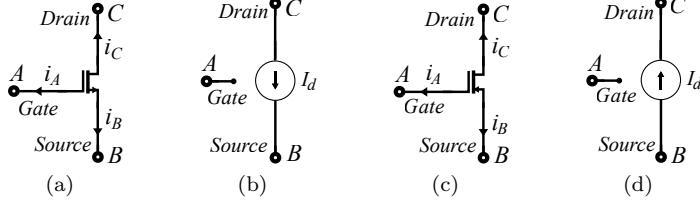


Fig. 4 Symbol of a n-type MOSFET (a) and corresponding macromodel (b). Symbol of a p-type MOSFET (c) and corresponding macromodel (d).

is characterized by the following three equations describing its behavior in the cut-off, ohmic and saturation operating regions, respectively,

$$I_d = 0, \quad \text{if } V_{ov} < 0 \quad (21)$$

$$I_d = \mu_n C_{ox} \frac{W}{L} (V_{ov} v_{CB} - \frac{v_{CB}^2}{2}) (1 + \lambda v_{CB}), \quad \text{if } V_{ov} > 0 \wedge v_{CB} < V_{ov} \quad (22)$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 (1 + \lambda v_{CB}), \quad \text{if } V_{ov} > 0 \wedge v_{CB} > V_{ov} \quad (23)$$

where the symbol \wedge is the logical AND, $V_{ov} = (v_{AB} - V_{th})$, v_{AB} is the gate-to-source voltage, V_{th} is the threshold voltage, $v_{CB} = -v_{BC}$ is the drain-to-source voltage, I_d is the current from drain to source, μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length, C_{ox} is the gate oxide capacitance per unit area and λ is the channel-length modulation parameter. V_{th} , μ_n , W , L , C_{ox} and λ depend on the actual considered MOSFET device and are assumed to be fixed and time-invariant.

Fig. 4(c), instead, shows a generic p-type MOSFET transistor, whose equivalent circuit model is represented in Fig. 4(d). The current source of the equivalent circuit is characterized by the following three equations describing its behavior in the cut-off, ohmic and saturation operating regions, respectively,

$$I_d = 0, \quad \text{if } V_{ov} < 0 \quad (24)$$

$$I_d = \mu_p C_{ox} \frac{W}{L} (V_{ov} v_{BC} - \frac{v_{BC}^2}{2}) (1 + \lambda v_{BC}), \quad \text{if } V_{ov} > 0 \wedge v_{BC} < V_{ov} \quad (25)$$

$$I_d = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} V_{ov}^2 (1 + \lambda v_{BC}), \quad \text{if } V_{ov} > 0 \wedge v_{BC} > V_{ov} \quad (26)$$

where the symbol \wedge is the logical AND, $V_{ov} = (v_{BA} - V_{th})$, $v_{BA} = -v_{AB}$ is the source-to-gate voltage, V_{th} is the threshold voltage, v_{BC} is the source-to-drain voltage, I_d is the current from source to drain, μ_p is the charge-carrier effective mobility, W is the gate width, L is the gate length, C_{ox} is the gate oxide

capacitance per unit area and λ is the channel-length modulation parameter. V_{th} , μ_p , W , L , C_{ox} and λ depend on the actual considered MOSFET device and are assumed to be fixed and time-invariant.

In the following part of this subsection, we will derive the WD model of the n-type MOSFET; however, practically the same modeling procedure can be performed also for the p-type MOSFET.

In order to derive the desired WD n-type MOSFET model, different parameterizations are usable. We choose to set $\varphi_1 = V_{ov}$ and $\varphi_2 = v_{CB}$, so that (21), (22) and (23) can be rewritten as follows

$$I_d = 0, \quad \text{if } \varphi_1 < 0 \quad (27)$$

$$I_d = \mu_n C_{ox} \frac{W}{L} (\varphi_1 \varphi_2 - \frac{\varphi_2^2}{2}) (1 + \lambda \varphi_2), \quad \text{if } \varphi_1 > 0 \wedge \varphi_2 < \varphi_1 \quad (28)$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \varphi_1^2 (1 + \lambda \varphi_2), \quad \text{if } \varphi_1 > 0 \wedge \varphi_2 > \varphi_1 \quad (29)$$

According to (27), (28) and (29), we can express (4) as

$$\mathbf{f}_i(\varphi) = \mathbf{i}_X = \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} I_d(\varphi_1, \varphi_2) \quad (30)$$

$$\mathbf{f}_v(\varphi) = \mathbf{v}_{XY} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} V_t \quad (31)$$

where the dependence of I_d from φ_1 and φ_2 is made explicit, expressing it as $I_d(\varphi_1, \varphi_2)$. Substituting (30) and (31) in (9), we obtain the following equation

$$\mathbf{P} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} I_d(\varphi_1, \varphi_2) + \mathbf{K} \left\{ \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} V_t \right\} + \tilde{\mathbf{a}} = 0. \quad (32)$$

(32) will be solved in a different way according to the considered operating region. In the following, a detailed analysis of the solution procedure for the cut-off, ohmic and saturation operating regions is provided.

3.1.1 Cut-Off Operating Region

The cut-off operating region is characterized by $I_d = 0$; therefore, substituting (27) in (32) a linear equation is obtained. It follows that, defined the vector \mathbf{u} and the matrix \mathbf{M} as

$$\mathbf{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \mathbf{K} \begin{bmatrix} V_t \\ 0 \\ -V_t \end{bmatrix} + \tilde{\mathbf{a}}, \quad (33)$$

$$\mathbf{M} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \\ M_{31} & M_{32} \end{bmatrix} = -\mathbf{K} \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -1 & 1 \end{bmatrix}, \quad (34)$$

the independent parameters φ_1 and φ_2 are given by

$$\begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} = \frac{1}{M_{11}M_{22} - M_{12}M_{21}} \begin{bmatrix} M_{22} & -M_{12} \\ -M_{21} & M_{11} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} . \quad (35)$$

It can be verified that, as long as the port resistances are positive real, the denominator term $M_{11}M_{22} - M_{12}M_{21}$ is always strictly negative.

3.1.2 Ohmic Operating Region

According to (22), the ohmic operating region is characterized by a nonlinear equation. Substituting (28) in (32) and defining the matrix \mathbf{E} as

$$\mathbf{E} = \begin{bmatrix} E_{11} & E_{12} \\ E_{21} & E_{22} \\ E_{31} & E_{32} \end{bmatrix} = \mu_n C_{ox} \frac{W}{L} \mathbf{P} \begin{bmatrix} 0 & 0 \\ 1 & -0.5 \\ -1 & 0.5 \end{bmatrix} \quad (36)$$

we get

$$\mathbf{u} = [\mathbf{M} - (\varphi_2 + \lambda\varphi_2^2) \mathbf{E}] \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} \quad (37)$$

where \mathbf{u} and \mathbf{M} have already been defined in (53) and (55), respectively. (37) is a nonlinear system with three scalar equations in two variables, φ_1 and φ_2 . As each of such three equations is a linear combination of the other two, we just focus on the first and the second ones, which can be rewritten as

$$\lambda E_{12}\varphi_2^3 + E_{12}\varphi_2^2 - M_{12}\varphi_2 + u_1 = \varphi_1 (\lambda E_{11}\varphi_2^2 + E_{11}\varphi_2 - M_{11}) , \quad (38)$$

$$\lambda E_{22}\varphi_2^3 + E_{21}\varphi_2^2 - M_{22}\varphi_2 + u_2 = \varphi_1 (\lambda E_{21}\varphi_2^2 + E_{21}\varphi_2 - M_{21}) . \quad (39)$$

Equation (38) can be also expressed as

$$\varphi_1 = \frac{\lambda E_{12}\varphi_2^3 + E_{12}\varphi_2^2 - M_{12}\varphi_2 + u_1}{\lambda E_{11}\varphi_2^2 + E_{11}\varphi_2 - M_{11}} \quad (40)$$

where the denominator is different from zero. Substituting (40) in (39), we obtain the following third order polynomial equation

$$\xi\varphi_2^3 + \delta\varphi_2^2 + \nu\varphi_2 + \rho = 0 , \quad (41)$$

where

$$\begin{aligned} \xi &= \lambda(M_{12}E_{21} + M_{21}E_{12} - M_{11}E_{22} - M_{22}E_{11}) \\ \delta &= M_{12}E_{21} + M_{21}E_{12} - M_{11}E_{22} - M_{22}E_{11} + \lambda(u_2E_{11} - u_1E_{21}) \\ \nu &= u_2E_{11} - u_1E_{21} + M_{11}M_{22} - M_{12}M_{21} \\ \rho &= u_1M_{21} - u_2M_{11} . \end{aligned}$$

Possible formulas [13] for expressing the roots of third order polynomials like (41) in closed-form are revised in Appendix A.

3.1.3 Saturation Operating Region

According to (23), the saturation operating region is also characterized by a nonlinear equation. Substituting (29) in (32) and defining the vector \mathbf{w} as

$$\mathbf{w} = \begin{bmatrix} w_1 \\ w_2 \\ w_3 \end{bmatrix} = -\frac{1}{2}\mu_n C_{ox} \frac{W}{L} \mathbf{P} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} \quad (42)$$

we get

$$\mathbf{u} = \mathbf{M} \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} - \varphi_1^2(1 + \lambda\varphi_2)\mathbf{w} \quad (43)$$

where \mathbf{u} and \mathbf{M} have already been defined in (53) and (55), respectively. (43) is a nonlinear system with three scalar equations in two variables, i.e., φ_1 and φ_2 . However, one of those three equations is a known linear combination of the other two; therefore, applying similar algebra to the one used for the ohmic case, we obtain

$$\varphi_2 = -\frac{w_1\varphi_1^2 - M_{11}\varphi_1 + u_1}{\lambda w_1\varphi_1^2 - M_{12}}$$

where the denominator is different from zero. Then, similarly to what done in the ohmic case, the following third order polynomial equation is obtained

$$\xi\varphi_1^3 + \delta\varphi_1^2 + \nu\varphi_1 + \rho = 0, \quad (44)$$

where

$$\begin{aligned} \xi &= \lambda(M_{11}w_2 - M_{21}w_1) \\ \delta &= \lambda(u_2w_1 - u_1w_2) + M_{22}w_1 - M_{12}w_2 \\ \nu &= M_{12}M_{21} - M_{11}M_{22} \\ \rho &= M_{22}u_1 - M_{12}u_2, \end{aligned}$$

which, again, can be solved in closed form using the formulas in Appendix A.

3.1.4 Implementation Discussion

Now that closed-form formulas for computing φ in each operating region have been presented, we will discuss how to exploit them in an actual implementation of the WD MOSFET model. The task is, given the input variables of the WD model, i.e., the incident waves, finding φ at each sampling step, such that the output variables, i.e., the reflected waves, can be computed by applying (15) and (16). Assuming the current operating region of the modeled device is known at any time instant, the task becomes simple; in fact, in the cut-off case equation (35) is used to directly compute φ , while in the ohmic case and in the saturation case the third order polynomial equations (41) and (44), respectively, need to be solved. In the two latter cases up to three candidate solutions for φ are computed, until the only valid solution, which matches the conditions on φ_1 and φ_2 in (27), (28) or (29), is found. In most practical applications, however, the current operating region of the device is not known a-priori. For

this reason, up to seven candidate solutions for φ are computed (one for the cut-off operating region, three for the ohmic operating region and three for the saturation operating region), until the solution that matches the conditions on φ_1 and φ_2 in (27), (28) or (29) is found. It is worth noticing that the case in which seven candidate solutions need to be checked to be valid is very unlucky since, especially dealing with periodic signals, predictors based on past visited operating regions can be used to select the order of the calculations of candidate solutions in a computationally convenient fashion. However, as we deal with closed-form formulas, the computation time required for computing φ in the worst case, i.e., the case with seven tries, can be estimated a-priori. In Virtual Analog applications, this is a considerable advantage of the proposed method based on closed-form formulas over other usable methods based on iterative solvers, whose computational load in the worst case is more difficult to be estimated a-priori.

3.2 JFET Transistors

Fig. 5(a) shows a generic n-type JFET transistor, whose three terminals are again called *gate* (node A), *source* (node B) and *drain* (node C). Only n-type JFET transistors are considered in this paper; however, applying the WD modeling approach described in this subsection also to p-type JFET transistors would be straightforward. A simplified, though suitable and fairly accurate, JFET model for Virtual Analog applications, is represented by the equivalent circuit in Fig. 5(b), which is composed of a large resistor R_{gate} between gate and ground and a current generator between drain and source, whose current I_d depends on the operating region. The presence of the large resistor R_{gate} in such a model is justified by the fact that the gate current I_g is very low and practically negligible with respect to I_d . A similar modeling approach in the contest of audio applications was applied to the JFET in [23].

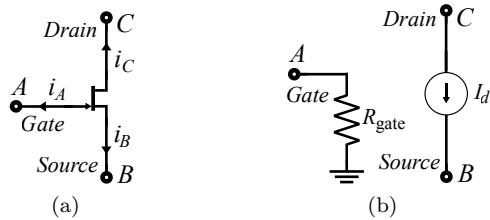


Fig. 5 Symbol of a n-type JFET (a) and corresponding macromodel (b).

In the *cut-off operating region* the condition $v_{AB} < V_p$ holds, where V_p is the so-called “pinch-off voltage”, which plays a role similar to the threshold voltage V_{th} in MOSFET transistors, but unlike V_{th} , is negative and, usually,

in the range $[-10, -0.3]$ V. In the cut-off operating region I_d is given by

$$I_d = 0 . \quad (45)$$

In the *ohmic operating region* the conditions $v_{AB} > V_p$ and $v_{CB} < v_{AB} - V_p$ hold and I_d is given by

$$I_d = \frac{2I_{S0}}{V_p^2} \left((v_{AB} - V_p)v_{CB} - \frac{v_{CB}^2}{2} \right) (1 + \lambda v_{CB}) , \quad (46)$$

where I_{S0} is the saturation current at zero gate-source voltage.

In the *saturation operating region* the conditions $v_{AB} > V_p$ and $v_{CB} > v_{AB} - V_p$ hold and I_d is given by

$$I_d = I_{S0} \left(1 - \frac{v_{AB}}{V_p} \right)^2 (1 + \lambda v_{CB}) . \quad (47)$$

Set $\varphi_1 = v_{AB} - V_p$ and $\varphi_2 = v_{CB}$, we can rewrite (45), (46) and (47) as

$$I_d = 0 , \quad \text{if } \varphi_1 < 0 \quad (48)$$

$$I_d = \frac{2I_{S0}}{V_p^2} \left(\varphi_1 \varphi_2 - \frac{\varphi_2^2}{2} \right) (1 + \lambda \varphi_2) , \quad \text{if } \varphi_1 > 0 \wedge \varphi_2 < \varphi_1 \quad (49)$$

$$I_d = I_{S0} \left(\frac{-\varphi_1}{V_p} \right)^2 (1 + \lambda \varphi_2) , \quad \text{if } \varphi_1 > 0 \wedge \varphi_2 > \varphi_1 . \quad (50)$$

According to (48), (49) and (50), we express (4) as

$$\mathbf{f}_i(\varphi) = \mathbf{i}_X = \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} I_d(\varphi_1, \varphi_2) \quad (51)$$

$$\mathbf{f}_v(\varphi) = \mathbf{v}_{XY} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} V_p \quad (52)$$

where, again, the dependence of I_d from φ_1 and φ_2 is made explicit, expressing it as $I_d(\varphi_1, \varphi_2)$. Substituting (51) and (52) in (9) an equation similar to (32) is easily obtained. The solution of such an equation can be performed using the same formulas (35), (41) and (44), provided that the vectors \mathbf{u} and \mathbf{w} and the matrices \mathbf{M} and \mathbf{E} are, this time, defined as

$$\mathbf{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \mathbf{K} \begin{bmatrix} V_p \\ 0 \\ -V_p \end{bmatrix} + \tilde{\mathbf{a}} , \quad (53)$$

$$\mathbf{w} = \begin{bmatrix} w_1 \\ w_2 \\ w_3 \end{bmatrix} = -\frac{I_{S0}}{V_p^2} \mathbf{P} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} , \quad (54)$$

$$\mathbf{M} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \\ M_{31} & M_{32} \end{bmatrix} = \mathbf{K} \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -1 & 1 \end{bmatrix}, \quad (55)$$

$$\mathbf{E} = \begin{bmatrix} E_{11} & E_{12} \\ E_{21} & E_{22} \\ E_{31} & E_{32} \end{bmatrix} = \frac{2I_{S0}}{V_p^2} \mathbf{P} \begin{bmatrix} 0 & 0 \\ 1 & -0.5 \\ -1 & 0.5 \end{bmatrix}. \quad (56)$$

4 Wave Digital Modeling of BJT Transistors

Fig. 6(a) shows a generic BJT transistor, whose three terminals are called *base* (node *A*), *emitter* (node *B*) and *collector* (node *C*). The most widespread large-signal model of the BJT is the Ebers-Moll Model (EMM) described in [19] and represented by the equivalent circuit in Fig. 6(b). The EMM is a good compromise between accuracy and simplicity; therefore, it is usually suitable for Virtual Analog audio applications [8, 9, 27]. The EMM is mathematically described by the following system of equations

$$\begin{cases} i_A + i_B + i_C = 0 \\ i_B = I_{s1} (e^{v_{AB}/(\eta_1 V_t)} - 1) - \alpha_r I_{s2} (e^{v_{AC}/(\eta_2 V_t)} - 1) \\ i_C = I_{s2} (e^{v_{AC}/(\eta_2 V_t)} - 1) - \alpha_f I_{s1} (e^{v_{AB}/(\eta_1 V_t)} - 1) \end{cases} \quad (57)$$

where i_A is the current flowing out of the base, i_B is the current flowing out of the emitter, i_C is the current flowing out of the collector, α_f is the forward common-base current gain, α_r is the reverse common-based current gain, v_{AB} is the base-to-emitter voltage, $v_{AC} = -v_{CA}$ is the base-to-collector voltage, V_t is the thermal voltage, I_{s1} is the saturation current of the base-emitter p-n junction, I_{s2} is the saturation current of the base-collector p-n junction, η_1 is the ideality factor of the base-emitter p-n junction and η_2 is the ideality factor of the base-collector p-n junction.

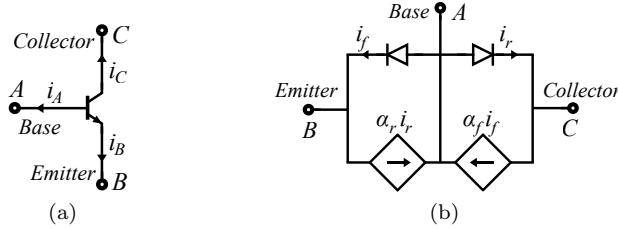


Fig. 6 Symbol of a BJT (a) and corresponding Ebers-Moll model (b).

Setting $\varphi_1 = v_{AB}$ and $\varphi_2 = v_{AC}$, we can express (4) as

$$\mathbf{f}_i(\varphi) = \mathbf{i}_X = \begin{bmatrix} \alpha_f - 1 & \alpha_r - 1 \\ 1 & -\alpha_r \\ -\alpha_f & 1 \end{bmatrix} \begin{bmatrix} I_{s1} (e^{\varphi_1/(\eta_1 V_t)} - 1) \\ I_{s2} (e^{\varphi_2/(\eta_2 V_t)} - 1) \end{bmatrix} , \quad (58)$$

$$\mathbf{f}_v(\varphi) = \mathbf{v}_{XY} = \begin{bmatrix} 1 & 0 \\ -1 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} . \quad (59)$$

After substituting (58) and (59) into (10), let us consider the following 2-dimensional nonlinear system,

$$\mathbf{g}_{nr}(\varphi) = \mathbf{0} , \quad (60)$$

obtained removing one redundant equation from the 3-dimensional system (14). Because of the exponentials in (58), the nonlinear system (60) is composed of two coupled transcendental implicit equations, therefore iterative solvers or tabulation methods are needed in order to solve (60) for φ .

According to the considerations in Subsection (2.4), the nonlinear system (60) varies depending on the number of ports n of the WD model. For instance, when we design a 2-port model with ports AB and CA , (60) reduces to (20).

In the following, we show how to solve (60) using iterative solvers based on the Newton-Raphson (NR) method that are arbitrarily accurate and generally more efficient than tabulation methods. The main drawback of such iterative methods is that convergence is not ensured. In this regard, we will propose a modification of the standard NR method exhibiting higher convergence rate and equal, or even higher, efficiency.

4.1 Newton-Raphson Method

The NR method applied to (60) is based on the following update equation

$$\varphi^{(k+1)} = \varphi^{(k)} - [\mathbf{J}(\varphi^{(k)})]^{-1} \mathbf{g}_{nr}(\varphi^{(k)}) , \quad (61)$$

where $\varphi^{(k)} = [\varphi_1^{(k)}, \varphi_2^{(k)}]^T$ and $\varphi^{(k+1)} = [\varphi_1^{(k+1)}, \varphi_2^{(k+1)}]^T$ indicate the values of φ evaluated at iterations k and $k+1$, respectively, $[\mathbf{J}(\varphi^{(k)})]^{-1}$ is the inverse matrix of the Jacobian of the vector function \mathbf{g}_{nr} evaluated at $\varphi^{(k)}$. Solving (60) using the NR method consists of:

- taking a suitable initial guess $\varphi^{(0)}$;
- repeating (61) up to convergence, i.e., up to the case in which $\|\varphi^{(k+1)} - \varphi^{(k)}\| < \epsilon_\varphi$ and $\|\mathbf{g}_{nr}(\varphi^{(k+1)})\| < \epsilon_g$, where ϵ_φ and ϵ_g are small positive scalar thresholds.

NR method convergence depends on the chosen initial guess $\varphi^{(0)}$. Moreover, when we deal with small or big numbers, numerical issues due to finite word-length representation might arise. In the following, a modification of the NR method applied to (60) that highly mitigates such problems is proposed.

4.2 Modified Newton-Raphson Method

The idea behind the proposed Modified NR (MNR) method is to control variables φ_1^k and φ_2^k iteration by iteration, forcing them to stay reasonably close to the desired solution. Hence, the update equation (61) is modified as follows

$$\tilde{\varphi}^{(k+1)} = \varphi^{(k)} - [\mathbf{J}(\varphi^{(k)})]^{-1} \mathbf{g}_{\text{nr}}(\varphi^{(k)}), \quad (62)$$

where $\tilde{\varphi}^{(k+1)} = [\tilde{\varphi}_1^{(k+1)}, \tilde{\varphi}_2^{(k+1)}]^T$, $\varphi^{(k)} = [\varphi_1^{(k)}, \varphi_2^{(k)}]^T$, and the two components of the vector $\varphi^{(k+1)}$ are given by

$$\varphi_1^{(k+1)} = \phi_1(\tilde{\varphi}^{(k+1)}) \quad , \quad \varphi_2^{(k+1)} = \phi_2(\tilde{\varphi}^{(k+1)}), \quad (63)$$

where ϕ_1 and ϕ_2 are compensation functions to be designed.

The role of compensation functions ϕ_1 and ϕ_2 is preventing overshooting. They could be designed in different ways and, in the most general case, they would both depend on $\tilde{\varphi}_1^{(k+1)}$ and $\tilde{\varphi}_2^{(k+1)}$, since the EMM describes a 2-dimensional nonlinearity. However, here we propose an effective design approach, which relies on the common lumped description of the EMM in Fig. 6(b), where the two exponential contributions of the two p-n junctions of the BJT are represented by two separated diodes. As a matter of fact, the EMM is a linear combination of two distinct exponential functions, which are two Shockley diode models. This fact is exploited in the proposed design approach, locally controlling the values of $\tilde{\varphi}_1^{(k+1)}$ and $\tilde{\varphi}_2^{(k+1)}$, which are the two voltages across the two diodes, in a decoupled fashion. It follows that compensation functions are built in such a way that ϕ_1 does not depend on $\tilde{\varphi}_2^{(k+1)}$ and ϕ_2 does not depend on $\tilde{\varphi}_1^{(k+1)}$. In particular, ϕ_1 is given by

$$\phi_1(\tilde{\varphi}^{(k+1)}) = \begin{cases} \tilde{\varphi}_1^{(k+1)} & , \text{ if } \tilde{\varphi}_1^{(k+1)} \leq \varphi_{1\text{thr}} \\ \eta_1 V_t \ln \left(1 + \frac{\rho_1(\tilde{\varphi}_1^{(k+1)})}{I_{s1}} \right) & , \text{ if } \tilde{\varphi}_1^{(k+1)} > \varphi_{1\text{thr}}, \end{cases} \quad (64)$$

where $\varphi_{1\text{thr}}$ is a positive threshold, greater than the desired solution φ_1 , and function ρ_1 is defined as

$$\rho_1(\tilde{\varphi}_1^{(k+1)}) = \frac{I_{s1} (e^{\varphi_{1\text{thr}}/(\eta_1 V_t)} - e^{\varphi_0/(\eta_1 V_t)})}{\varphi_{1\text{thr}} - \varphi_0} (\tilde{\varphi}_1^{(k+1)} - \varphi_0) + I_{s1} (e^{\varphi_0/(\eta_1 V_t)} - 1) \quad (65)$$

where φ_0 is a fixed coordinate such that $\varphi_0 < \varphi_{1\text{thr}}$, e.g., $\varphi_0 = 0$ V. Applying function ρ_1 to the input $\tilde{\varphi}_1^{(k+1)}$, we project the point $(\tilde{\varphi}_1^{(k+1)}, 0)$ onto the straight line passing through the two points $(\varphi_0, I_{s1} (e^{\varphi_0/(\eta_1 V_t)} - 1))$ and $(\varphi_{1\text{thr}}, I_{s1} (e^{\varphi_{1\text{thr}}/(\eta_1 V_t)} - 1))$ and we select the y -coordinate of the projection (i.e., a diode current value), which is returned as the output of ρ_1 . Then, the inverse of the exponential Shockley diode function, involving a natural logarithm, is applied to such an output, in order to compensate the nonlinearity effect that may cause divergence or numerical problems.

Choosing $\varphi_0 = 0$, we get an expression simpler than (64), as follows

$$\phi_1 \left(\tilde{\varphi}^{(k+1)} \right) = \begin{cases} \tilde{\varphi}_1^{(k+1)} & , \text{ if } \tilde{\varphi}_1^{(k+1)} \leq \varphi_{1\text{thr}} \\ \eta_1 V_t \ln \left(1 + \frac{\tilde{\varphi}_1^{(k+1)}}{\varphi_{1\text{thr}}} (e^{\varphi_{1\text{thr}}/(\eta_1 V_t)} - 1) \right) & , \text{ if } \tilde{\varphi}_1^{(k+1)} > \varphi_{1\text{thr}} . \end{cases} \quad (66)$$

Similarly, ϕ_2 is given by

$$\phi_2 \left(\tilde{\varphi}^{(k+1)} \right) = \begin{cases} \tilde{\varphi}_2^{(k+1)} & , \text{ if } \tilde{\varphi}_2^{(k+1)} \leq \varphi_{2\text{thr}} \\ \eta_2 V_t \ln \left(1 + \frac{\tilde{\varphi}_2^{(k+1)}}{\varphi_{2\text{thr}}} (e^{\varphi_{2\text{thr}}/(\eta_2 V_t)} - 1) \right) & , \text{ if } \tilde{\varphi}_2^{(k+1)} > \varphi_{2\text{thr}} , \end{cases} \quad (67)$$

where $\varphi_{2\text{thr}}$ is a positive threshold, similar to $\varphi_{1\text{thr}}$.

4.3 NR method and MNR method: a performance comparison

In this subsection, we provide a performance comparison between the traditional NR method and the MNR method used for implementing the EMM in the WD domain. The parameters of the EMM are set as follows: $I_{s1} = 1.005 \times 10^{-14} \text{ A}$, $I_{s2} = 1.333 \times 10^{-14} \text{ A}$, $\alpha_f = 0.995$, $\alpha_r = 0.75$, $V_t = 25.7 \text{ mV}$, $\eta_1 = 1$ and $\eta_2 = 1$. Without loss of generality, let us assume that the BJT is modeled in the WD domain as a 2-port. The two ports of the WD model are AB and CA , as in equations (19) and (20).

Before comparing the performance of traditional NR and MNR, we need a strategy for checking whether, given a pair of incident waves a_{AB} and a_{CA} and a pair of port resistances R_{AB} and R_{CA} , the pair of reflected waves b_{AB} and b_{CA} (returned when one of the two considered methods converges) is correct. In order to do so, let us set the voltages across the two diodes of the EMM, i.e., v_{AB} and v_{AC} , to certain values (which are inside specific ranges that we will define later). Then, we are able to find the corresponding currents of the EMM i_B and i_C , using (57). Such data are sufficient for deriving the Kirchhoff port variables of the 2-port model, i.e., v_{AB} , $i_{AB} = -i_B$, $v_{CA} = -v_{AC}$ and $i_{CA} = i_C$. The corresponding WD port variables can easily be computed as $a_{AB} = v_{AB} + R_{AB}i_{AB}$, $b_{AB} = v_{AB} - R_{AB}i_{AB}$, $a_{CA} = v_{CA} + R_{CA}i_{CA}$ and $b_{CA} = v_{CA} - R_{CA}i_{CA}$. It follows that we have all the ingredients for testing the accuracy of the two iterative methods; given a_{AB} , a_{CA} , R_{AB} and R_{CA} , we can verify whether the returned reflected waves are equal to b_{AB} and b_{CA} .

Let us now choose the ranges of values for the main variables involved in the WD model, such that we can test all the combinations of such values and evaluate both the accuracy and the convergence rate of the two methods. The ranges are a rough estimate of the possible values that variables can assume during a generic simulation of an audio circuit containing the modeled BJT. The chosen ranges are exaggerated in order to test the two methods also in borderline cases. The considered variables are: the initial guesses of the iterative methods φ_1^0 and φ_2^0 , the parameters $\varphi_1 = v_{AB}$ and $\varphi_2 = v_{AC}$

Table 1 Comparison between NR Method and MNR Method

	NR Method	MNR Method
Convergence Rate	74.26 %	100 %
Average Number of Iterations when there is convergence	8.92	7.26

from which Kirchhoff and WD port variables can be derived according to the aforementioned procedure, and the reference port resistances R_{AB} and R_{CA} . Values of variables are chosen as follows:

- $\{\varphi_1^0, \varphi_2^0, \varphi_1, \varphi_2\} \in [-20 \text{ V}, 0.8 \text{ V}]$; for each variable $\varphi_1^0, \varphi_2^0, \varphi_1$ and φ_2 we pick 4 uniformly distributed points in the sub-range $[-20 \text{ V}, 0.3 \text{ V}]$ and 6 uniformly distributed points in the sub-range $(0.3 \text{ V}, 0.8 \text{ V}]$;
- $\{R_{AB}, R_{CA}\} \in [10^{-1} \Omega, 10^6 \Omega]$; for both R_{AB} and R_{CA} variables we pick 8 logarithmically spaced points.

It follows that both the NR algorithm and the MNR algorithm are executed $(4 + 6)^4 \times 8^2 = 640000$ times, always with different combinations of values. $\epsilon_\varphi = \epsilon_g = 10^{-8} \text{ V}$, $\varphi_{1\text{thr}}$ is set such that $I_{s1}(e^{\varphi_{1\text{thr}}/(\eta_1 V_t)} - 1) = 1 \text{ A}$, i.e., $\varphi_{1\text{thr}} = 0.8283 \text{ V}$, while $\varphi_{2\text{thr}}$ is set such that $I_{s2}(e^{\varphi_{2\text{thr}}/(\eta_2 V_t)} - 1) = 1 \text{ A}$, i.e., $\varphi_{2\text{thr}} = 0.8211 \text{ V}$. If the number of iterations of a simulation exceeds 1000, we deduce the algorithm is diverging. Table 1 shows the obtained results. It is worth noticing that the proposed MNR method always converges to the correct solution, unlike the NR method. Moreover, the MNR method needs a lower average number of iterations to converge with respect to the NR method.

5 Examples of Applications

5.0.1 Example of Application of the Wave Digital MOSFET Model

Let us consider the schematics of the overdrive guitar effect presented in [16]. The schematics are redrawn in Fig. 7. The overdrive guitar effect circuit is constituted of three MOSFET amplification stages and a tone stack. The parameters of each of the three p-type MOSFET elements, called T_1 , T_2 and T_3 , are the following: $\mu_p C_{ox} \frac{W}{L} = 1.6 \text{ mA/V}^2$, $V_{th} = 1 \text{ V}$ and $\lambda = 0 \text{ V}^{-1}$. The other circuit parameters are set as: $R_{in} = 1 \text{ k}\Omega$, $V_{DD} = -9 \text{ V}$, $R_1 = 1.5 \text{ M}\Omega$, $R_2 = 3.3 \text{ M}\Omega$, $R_3 = 1.5 \text{ M}\Omega$, $R_4 = 10 \text{ k}\Omega$, $R_5 = 3.3 \text{ M}\Omega$, $R_6 = 1.5 \text{ M}\Omega$, $R_7 = 10 \text{ k}\Omega$, $R_8 = 3.3 \text{ M}\Omega$, $R_9 = 1.5 \text{ M}\Omega$, $R_{10} = 33 \text{ k}\Omega$, $R_{11} = 1 \text{ M}\Omega$, $R_{D1} = 3.9 \text{ k}\Omega$, $R_{D2} = 3.9 \text{ k}\Omega$, $R_{D3} = 3.9 \text{ k}\Omega$, $R_{S1} = 1 \text{ k}\Omega$, $R_{S2} = 1 \text{ k}\Omega$, $R_{S3} = 1 \text{ k}\Omega$, $C_1 = 0.1 \mu\text{F}$, $C_2 = 0.1 \mu\text{F}$, $C_3 = 0.1 \mu\text{F}$, $C_4 = 0.1 \mu\text{F}$, $C_5 = 3.3 \text{ nF}$, $C_6 = 0.01 \mu\text{F}$, $C_{S1} = 4.7 \mu\text{F}$, $C_{S2} = 4.7 \mu\text{F}$, $C_{S3} = 4.7 \mu\text{F}$ and $C_{in} = 0.1 \mu\text{F}$. Potentiometers R_{gain} , R_{tone} and R_{volume} are simply modeled using pairs of resistors such that $R_{gain} = R_{gain1} + R_{gain2} = 100 \text{ k}\Omega$,

$R_{\text{tone}} = R_{\text{tone1}} + R_{\text{tone2}} = 100 \text{ k}\Omega$ and $R_{\text{volume}} = R_{\text{volume1}} + R_{\text{volume2}} = 100 \text{ k}\Omega$. Discretization is performed using a sampling frequency $F_s = 1/T_s = 96 \text{ kHz}$, where T_s is the sampling step in seconds.

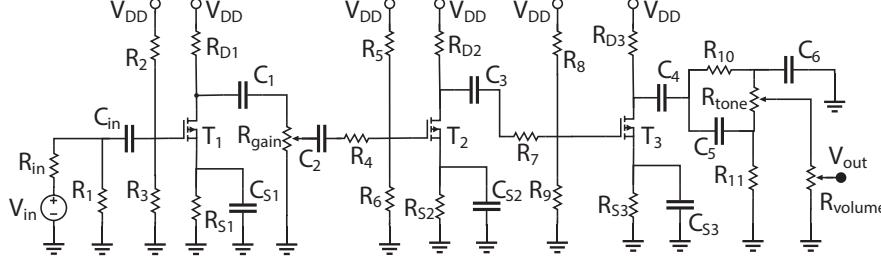


Fig. 7 Obsidian overdrive guitar effect circuit presented in [16].

Since MOSFET devices are modeled using an open-circuit, as described in Subsection 3.1 and highlighted in Fig. 4(b), the schematics in Fig. 7 can also be described as the cascade of three separated subcircuits, which will be called *stages*. The input signal of the second stage is controlled by the output signal of the first stage and, similarly, the input signal of the third stage is controlled by the output signal of the second stage. The WD realization of the schematics in Fig. 7 is characterized by three WD structures, one per stage, and each WD structure contains one nonlinear MOSFET element modeled as a 3-port. According to the conventions of Section 2, the 3 used ports are AO , BO and CO . It follows that separated connection trees are connected to each port of MOSFET elements. Fig. 8(a), Fig. 8(b) and Fig. 8(c) represent the WD implementation of first, second and third stages, respectively. All linear elements are adapted according to traditional WDF theory [20]. For the WD realization of the first and second stages, interconnections of traditional series and parallel adaptors [21] are used. For the WD realization of the third stage, instead, also a 8-port \mathcal{R} -type adaptor is employed. The \mathcal{R} -type adaptor is characterized by the following scattering matrix [25]

$$\mathbf{S} = 2\mathbf{Q}^T (\mathbf{Q}\mathbf{R}_{\mathcal{R}}^{-1}\mathbf{Q}^T)^{-1} \mathbf{Q}\mathbf{R}_{\mathcal{R}}^{-1} - \mathbf{I}, \quad (68)$$

where \mathbf{I} is the 8×8 identity matrix and

$$\mathbf{Q} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & -1 & 0 & -1 & -1 \\ 0 & 0 & 1 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & -1 \end{bmatrix}. \quad (69)$$

Since all linear elements of the WD structure are adapted, the diagonal matrix of port resistances is given by

$$\mathbf{R}_{\mathcal{R}} = \text{diag}[R_{\text{adapt}}, R_{10}, T_s/(2C_5), R_{\text{tone1}}, R_{\text{tone2}}, R_{11}, T_s/(2C_6), R_{\text{volume}}], \quad (70)$$

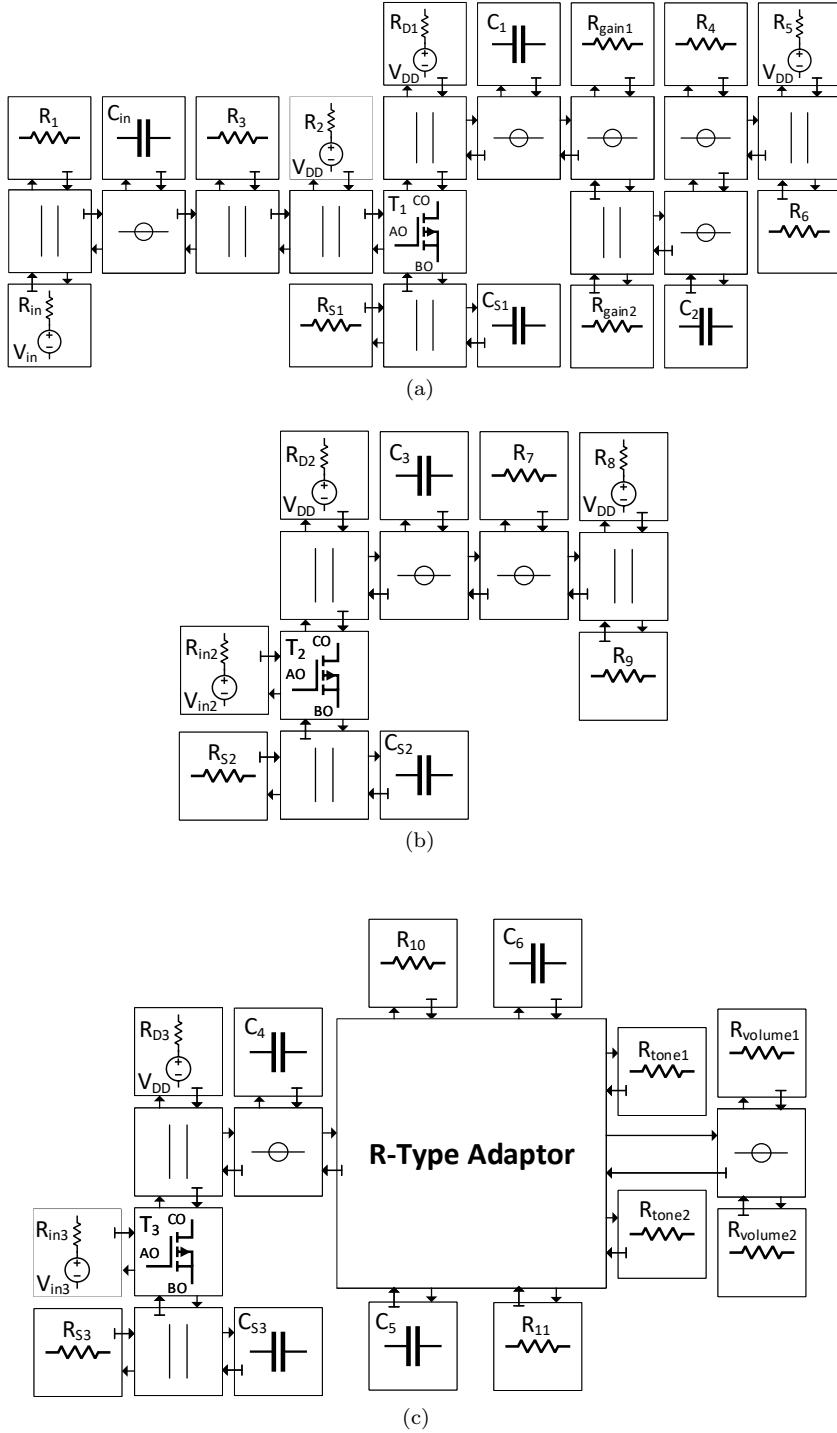


Fig. 8 WD realization of the circuit represented in Fig. 7. WD structures implementing the first, the second and the third amplification stages of the overdrive guitar effect are represented in (a), (b) and (c), respectively.

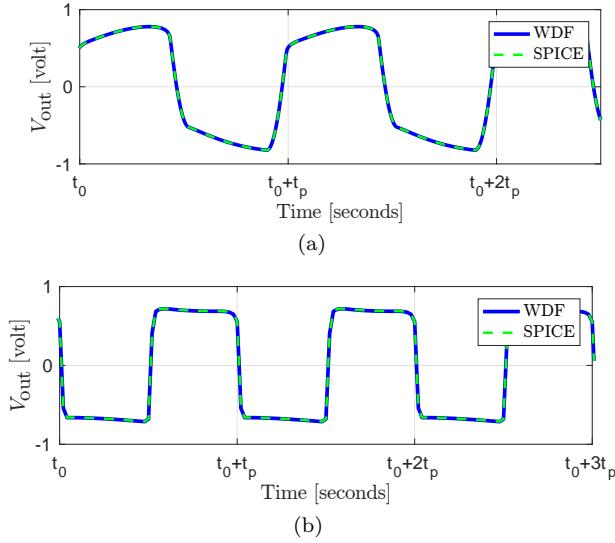


Fig. 9 Overdrive guitar effect circuit. Comparison between V_{out} signals by WD structure and Spice obtained from two simulations with different settings of parameters. Simulation parameters in (a) are: $V_0 = 100 \text{ mV}$, $f_p = 1/t_p = 500 \text{ Hz}$, $R_{\text{gain}2} = 0.75 \times R_{\text{gain}}$, $R_{\text{tone}2} = 0.5 \times R_{\text{tone}}$ and $R_{\text{volume}2} = 0.5 \times R_{\text{volume}}$. Simulation parameters in (b) are: $V_0 = 500 \text{ mV}$, $f_p = 1/t_p = 2 \text{ kHz}$, $R_{\text{gain}2} = 0.5 \times R_{\text{gain}}$, $R_{\text{tone}2} = 0.5 \times R_{\text{tone}}$ and $R_{\text{volume}2} = 0.5 \times R_{\text{volume}}$.

where the port resistance R_{adapt} is set in such a way that the first diagonal entry of \mathbf{S} goes to zero, i.e., the port of the \mathcal{R} -type adaptor on the left (see Fig. 8(c)) is made reflection-free.

The link of the first stage to the second stage is modeled as a Thévenin equivalent with voltage source $V_{\text{in}2}$ and series resistance $R_{\text{in}2}$, as shown in Fig. 8(b). The correct value of the voltage source can be easily set, imposing $V_{\text{in}2}$ equal to the voltage across resistor R_6 . The value of the series resistance $R_{\text{in}2}$, instead, can be set arbitrarily (e.g., $R_{\text{in}2} = 1 \text{ k}\Omega$), because no current flows through the gate of the MOSFET T_2 with terminals A , B and C , as defined in Subsection 3.1. This means that, according to the models in Fig. 4(b) and in Fig. 1(a), $i_A = 0 \text{ A}$ and, as a consequence, in this case, $i_{AO} = i_A = 0 \text{ A}$. It follows that the value of $R_{\text{in}2}$ does not affect the behavior of the second stage. Similar considerations hold for the link of the second stage to the third stage, modeled as a Thévenin equivalent with voltage source $V_{\text{in}3}$ and series resistance $R_{\text{in}3}$, as shown in Fig. 8(b). $V_{\text{in}3}$ is set equal to the voltage across R_9 , while $R_{\text{in}3}$ can be set to an arbitrary resistance value (e.g., $R_{\text{in}3} = 1 \text{ k}\Omega$).

The schematics in Fig. 7 are simulated with Spice using the Schichman-Hodges model [35] also described in [12, p. 206], for the three MOSFET transistors. We define the input signal as a sinusoid $V_{\text{in}}(t) = V_0 \sin(2\pi f_p t)$, where V_0 is the amplitude gain and f_p is the fundamental frequency. The output signal V_{out} obtained with Spice is compared to the same signal obtained with the described WD implementation. Fig. 9(a) shows one of such comparisons,

when $V_0 = 100$ mV, $f_p = 500$ Hz, $R_{\text{gain}2} = 0.75 \times R_{\text{gain}}$, $R_{\text{tone}2} = 0.5 \times R_{\text{tone}}$ and $R_{\text{volume}2} = 0.5 \times R_{\text{volume}}$. Results in Fig. 9(b), instead, are obtained setting $V_0 = 500$ mV, $f_p = 2$ kHz, $R_{\text{gain}2} = 0.5 \times R_{\text{gain}}$, $R_{\text{tone}2} = 0.5 \times R_{\text{tone}}$ and $R_{\text{volume}2} = 0.5 \times R_{\text{volume}}$. Both Fig. 9(a) and Fig. 9(b) show a very good matching between Spice and the WD implementation.

5.0.2 Example of Application of the Wave Digital JFET Model

Let us consider the guitar preamplifier circuit shown in Fig. 10 also discussed in [23]. Model parameters of JFET transistors T_1 and T_2 , are $I_{S0} = 0.6$ mA, $V_p = -0.8$ V, $\lambda = 0$ V $^{-1}$ and $R_{\text{gate}} = 1$ G Ω . The other circuit parameters are set as: $V_{\text{DD}} = 9$ V, $R_{\text{in}} = 1$ Ω , $R_{G1} = 1$ M Ω , $R_{I1} = 64$ k Ω , $R_{D1} = 15$ k Ω , $R_{S1} = 1.5$ k Ω , $R_1 = 47$ k Ω , $R_{\text{gain}} = 500$ k Ω , $R_{I2} = 64$ k Ω , $R_{D2} = 15$ k Ω , $R_{S2} = 1.5$ k Ω , $R_2 = 100$ k Ω , $R_{\text{tone}} = 1$ M Ω , $R_{\text{volume}} = 500$ k Ω , $C_{\text{in}} = 1$ μF , $C_1 = 0.1$ nF, $C_2 = 1$ μF , $C_3 = 1$ μF , $C_4 = 0.16$ nF, $C_{S1} = 1$ μF and $C_{S2} = 1$ μF . We define the input signal as a sinusoid $V_{\text{in}}(t) = V_0 \sin(2\pi f_p t)$, where V_0 is the amplitude gain and f_p is the fundamental frequency. Discretization is performed using a sampling frequency $F_s = 1/T_s = 48$ kHz.

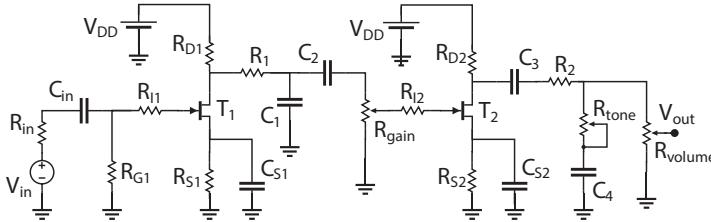


Fig. 10 Guitar preamplifier circuit discussed in [23].

The proposed WD realization of the circuit in Fig. 10 is shown in Fig. 11. JFET devices are implemented as 3-port WD elements according to the model presented in Subsection 3.2. Following the conventions of Section 2, the 3 used ports are called *AO*, *BO* and *CO*. As shown in Fig. 5(b), resistance R_{gate} is a linear subpart of the JFET model, separable from the rest. As a consequence, port *AO* of the 3-port WD JFET element can be made reflection free, properly setting $R_{AO} = R_{\text{gate}}$. Such a property is exploited in the proposed WD implementation in Fig. 11, where port *AO* of T_2 is adapted. It follows that, in this very particular case, contrary to what usually happens, we are able to accommodate two nonlinear 3-port JFET elements in the same WD structure without creating any delay-free loop, i.e., implicit equation.

Plots at the top of Fig. 12(a) and Fig. 12(b) show the comparison between the signal V_{out} of the proposed WD realization and the one in [23]. Both WD implementations are also compared with a ground-truth obtained by Spice simulation where the JFET transistors are emulated using the model described in [12, p. 176]. Plots at the bottom of Fig. 12(a) and Fig. 12(b) show the errors

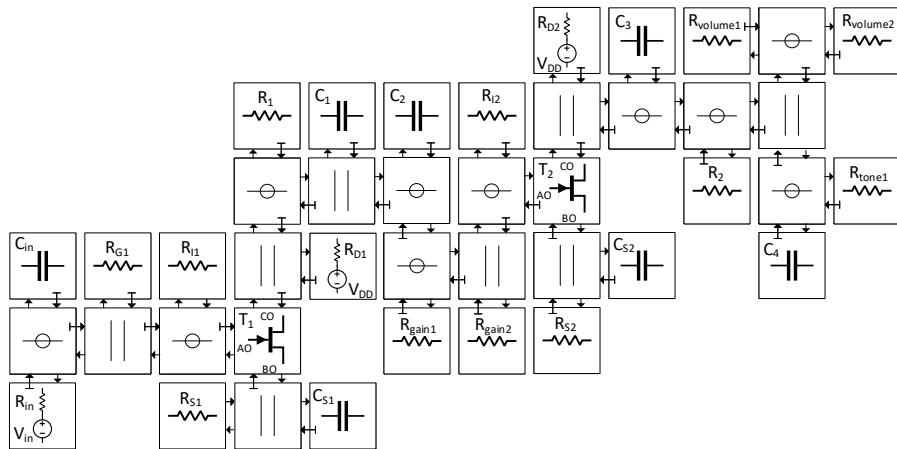


Fig. 11 WD realization of the guitar preamplifier circuit shown in Fig. 10.

of the two WD implementations with respect to Spice. We notice that the error of the proposed WD implementation is generally lower. The main reason is that WD JFET model presented in [23] makes use of a fictitious delay element for solving computability issues. We can conclude that the proposed WD JFET model, beside being an explicit model like the one presented in [23], it is more accurate, at the cost of a slightly higher computational complexity.

5.0.3 Example of Application of the Wave Digital BJT Model

Let us consider the common emitter amplifier implemented in [27] and reported in Fig. 13(a). The BJT transistor T_1 is described using the EMM discussed in Section 4; the EMM parameters are set as in Subsection 4.3, except for the thermal voltage which is set to $V_t = 25.868$ mV. The other circuit parameters are set as follows: $B_1 = 18$ V, $R_{in} = 1$ k Ω , $C_{in} = 50$ μ F, $R_1 = 27.35$ k Ω , $R_2 = 2.65$ k Ω , $R_E = 220$ Ω , $C_E = 100$ μ F, $R_C = 1.78$ k Ω , $C_2 = 10$ μ F and $R_L = 1$ k Ω . We define the input signal as a sinusoid $V_{in}(t) = V_0 \sin(2\pi f_p t)$, where V_0 is the amplitude gain and f_p is the fundamental frequency. Discretization is performed using a sampling frequency $F_s = 1/T_s = 96$ kHz.

In the WD realization of the common emitter amplifier presented in [27], the BJT is implemented as a 2-port WD element and a 8-port \mathcal{R} -type adaptor is employed. In the WD realization of the same circuit shown in Fig. 13(b), instead, the BJT T_1 is implemented as a 3-port WD element, such that only interconnections of series and parallel 3-port adaptors are employed and the use of the 8-port \mathcal{R} -type adaptor is avoided. The approach used for implementing the WD structure in Fig. 13(b) is very similar to the one proposed in [15], where a circuit containing one nonlinear vacuum tube triode, modeled as a 3-port WD element, is considered. While in [15] a local iterative solver based on the secant method is used for computing the waves reflected from the

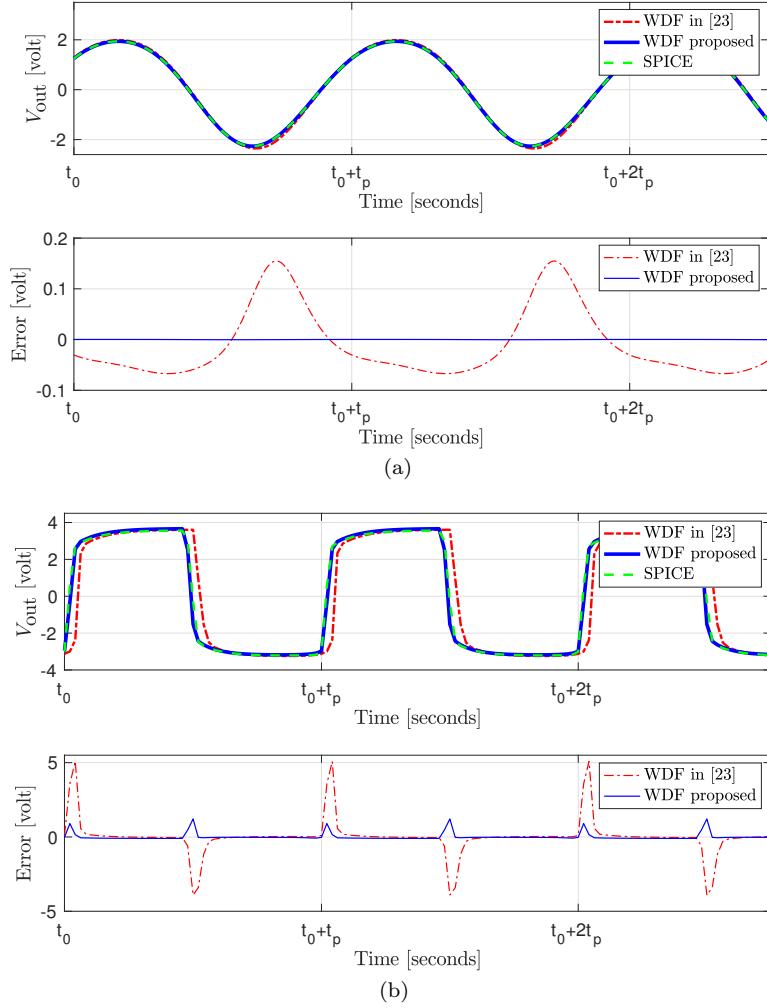


Fig. 12 Preamplifier circuit. V_{out} signals and relative errors between WD implementations and Spice obtained from two simulations with different settings of parameters. Simulation parameters in (a) are: $V_0 = 50$ mV, $f_p = 1/t_p = 300$ Hz, $R_{gain2} = 0.5 \times R_{gain}$, $R_{tone1} = 0.5 \times R_{tone}$ and $R_{volume2} = 0.99 \times R_{volume}$. Simulation parameters in (b) are: $V_0 = 500$ mV, $f_p = 1$ kHz, $R_{gain2} = 0.5 \times R_{gain}$, $R_{tone1} = 0.5 \times R_{tone}$ and $R_{volume2} = 0.99 \times R_{volume}$.

WD nonlinear triode, in this case we use the local iterative solver based on the MNR method described in Subsection 4.2 for solving the scattering relations of the WD nonlinear BJT. Following the conventions of Section 2, the 3 ports of the BJT in Fig. 13(b) are called *AO*, *BO* and *CO*.

Fig. 14 shows that the signal V_{out} of the WD implementation closely matches the same signal resulting from a Spice simulation of the circuit in Fig. 13(b). In this case $f_p = 1$ KHz and $V_0 = 0.1$ V. In Table 2 we show the results of other simulations where different values of f_p and V_0 are tested,

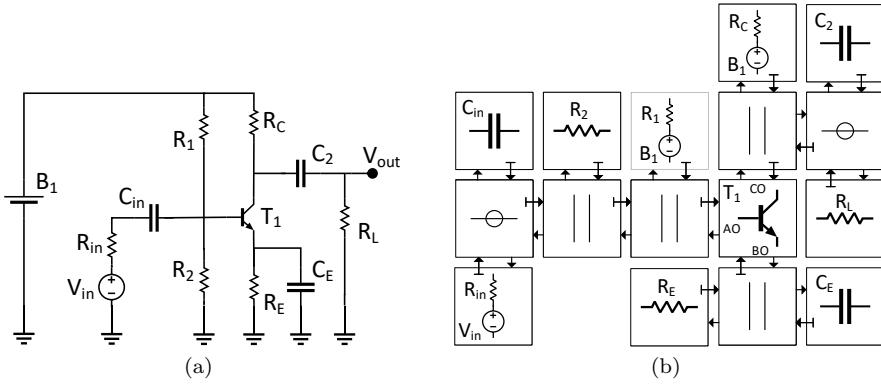


Fig. 13 Common emitter amplifier circuit (a) and its WD realization (b).

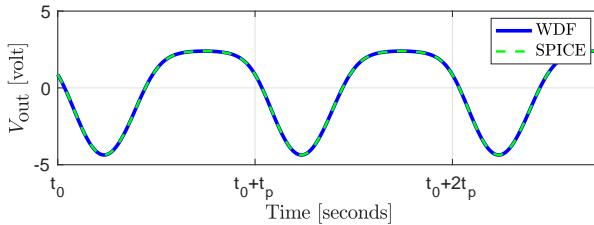


Fig. 14 Common emitter amplifier. Comparison between V_{out} signals by WD implementation and Spice. $V_0 = 100$ mV and $f_p = 1/t_p = 1$ kHz.

along with a comparison (in terms of minimum, maximum and average number of iterations) between WD implementations using the traditional NR method described in Subsection 4.1 for solving the BJT scattering relations and WD implementations based on the MNR method presented in Subsection 4.2. Parameters ϵ_φ , ϵ_g , $\varphi_{1\text{thr}}$ and $\varphi_{2\text{thr}}$ are set as specified in Subsection 4.3. We notice that the number of iterations needed by the MNR method to converge is always lower or equal to the one required by the NR method. More importantly, the MNR method always converged, while the NR method diverged in two cases, i.e., the ones in which the number of iterations is indicated with “N/A”. Table 2 in this article resembles Table 3 in [27], where it is shown that the NR solver used in [27] for the WD implementation of the same circuit does not converge with certain input signals, i.e., the simulation in which $f_p = 1$ kHz and $V_0 = 1$ V and the simulation in which $f_p = 10$ kHz and $V_0 = 1$ V. It is worth pointing out that in [27] a Newton’s method with backtracking [18, pp. 111-154], [11] is proposed for attenuating problems of divergence affecting the NR solver. Table 3 in [27] shows that divergence is prevented using the Newton’s method with backtracking when $f_p = 1$ kHz and $V_0 = 1$ V, while even the Newton’s method with backtracking diverges when $f_p = 10$ kHz and $V_0 = 1$ V.

Table 2 NR method vs. MNR method used in the WD structure in Fig. 13(b).

		NR Method			MNR Method		
		Number of Iterations			Number of Iterations		
f_p [Hz]	V_0 [V]	Min	Max	Avg	Min	Max	Avg
100	0.01	1	2	1.83	1	2	1.83
	0.1	2	3	2.44	2	3	2.44
	1	2	19	2.36	2	15	2.35
1k	0.01	2	3	2.75	2	3	2.75
	0.1	2	4	3.02	2	4	3.02
	1	N/A	N/A	N/A	2	13	3.02
10k	0.01	3	3	3	3	3	3
	0.1	3	5	4.33	3	5	4.33
	1	N/A	N/A	N/A	2	17	5.96

6 Final Discussion, Conclusion and Future Work

In this article we proposed a general n -port ($1 \leq n \leq 6$) WD model for nonlinear 3-terminal devices. The 2-port WD models of 3-terminal devices are perhaps the most practical ones in most situations. However, as we showed in examples of applications, resorting to alternate port configurations can still be advantageous, since sometimes the use of \mathcal{R} -type adaptors can be avoided or the number of their ports can be reduced.

In this regard, as an example, let us consider the two different WD implementations of the same circuit in Fig. 3(b) and Fig. 3(c) and assume that the 3-terminal device is a FET modeled as in Section 3. Since the considered WD models of FET devices are explicit, the WD structure in Fig. 3(b), where the FET is modeled as a 4-port WD element, does not exhibit delay-free loops and it can be implemented without iterative solvers. The WD structure in Fig. 3(c), instead, is characterized by delay-free loops involving waves at ports CA and AB , because the 2-port nonlinear WD element is connected to the \mathcal{R} -type adaptor through a double port connection. Therefore, the use of iterative methods, or other computationally costly strategies like multi-dimensional look-up tables, is unavoidable for the implementation of the WDF in Fig. 3(c).

In this article, we also presented WD models of the three most widespread transistors in audio circuitry: the MOSFET, the JFET and the BJT. Such WD models have been designed to meet, as much as possible, both the accuracy requirements and the computational cost requirements typical of Virtual Analog applications. The proposed MOSFET and JFET models are characterized by explicit scattering relations, while the BJT model employs a 2-dimensional Modified Newton-Raphson solver, which is more robust and equally or more efficient than NR solvers presented in the literature.

All considered WD models of 3-terminal devices are memoryless. As a future work, it is worth developing multi-port models with memory effect.

Appendix A: Let us consider a 3rd grade equation in the canonical form

$$\xi x^3 + \delta x^2 + \nu x + \rho = 0$$

where $\xi \neq 0$ and x is the unknown variable. The 3 solutions in closed form are

$$\begin{aligned} x_1 &= s + t - \frac{\delta}{3\xi} \\ x_2 &= -\frac{1}{2}(s + t) - \frac{\delta}{3\xi} + \frac{\sqrt{3}}{2}(s - t)j \\ x_3 &= -\frac{1}{2}(s + t) - \frac{\delta}{3\xi} - \frac{\sqrt{3}}{2}(s - t)j \end{aligned}$$

where j is the imaginary unit and

$$\begin{aligned} s &= \sqrt[3]{\frac{r}{2} + \sqrt{\frac{q^3}{27} + \frac{r^2}{4}}} \quad , \quad t = \sqrt[3]{\frac{r}{2} - \sqrt{\frac{q^3}{27} + \frac{r^2}{4}}} \quad , \\ q &= \frac{3\xi\nu - \delta^2}{3\xi^2} \quad , \quad r = \frac{9\xi\delta\nu - 27\xi^2\rho - 2\delta^3}{27\xi^3} \quad . \end{aligned}$$

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