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Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers: supplementary material

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This document provides supplementary information to "Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers," http://dx.doi.org/10.1364/optica.3.000064, including electrostatic MEMS actuator design, low loss multimode interference crossing design, simulations for fabrication error tolerance study, fabrication process, and measurement of passive optical test structures. © 2016 Optical Society of America

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Section I. Electrostatic MEMS Actuator Design

The 64 x 64 switch consists of 4,096 unit cells. The schematic of a unit cell is depicted in Fig. 1b in the main text. Each unit cell contains two vertically actuated adiabatic waveguide couplers connected by a 90-degree waveguide bend. They are actuated using parallel-plate-type electrostatic actuators with folded spring suspensions. The actuator is depicted in Fig. S1(a). The actuators are designed for digital actuation, exploiting the pull-in effect of the electrostatic actuator. Cross-sectional views of the switch in both OFF and ON states are depicted in Fig. S1(b). The mechanical stoppers (also labelled as dimples) precisely define the coupling distance in the ON state (125 nm), while the OFF state distance is defined by the rest-position of the actuator, which is controlled by the thickness of the sacrificial layer (900 nm).

The design parameters of the actuator include the actuation voltage, the actuation speed, and the geometrical constraints of the optical layout, and the manufacturing tolerances, in particular the photolithography resolution. The actuation voltage needs to be reasonably low to avoid breakdown and to enable the use of standard driving circuitry. With these criteria we design for an actuation voltage of 25 V. To obtain the fastest switching time, we set the corresponding mechanical resonance frequency as high as possible.

For a parallel-plate electrostatic actuator, the pull-in voltage V_{PI} and the mechanical resonance frequency f_0 are given by Equation (S1) and (S2) respectively:

$$V_{PI} = \sqrt{\frac{8kd_0^3}{27\varepsilon A}} \quad \textbf{(S1)}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \quad \textbf{(S2)}$$

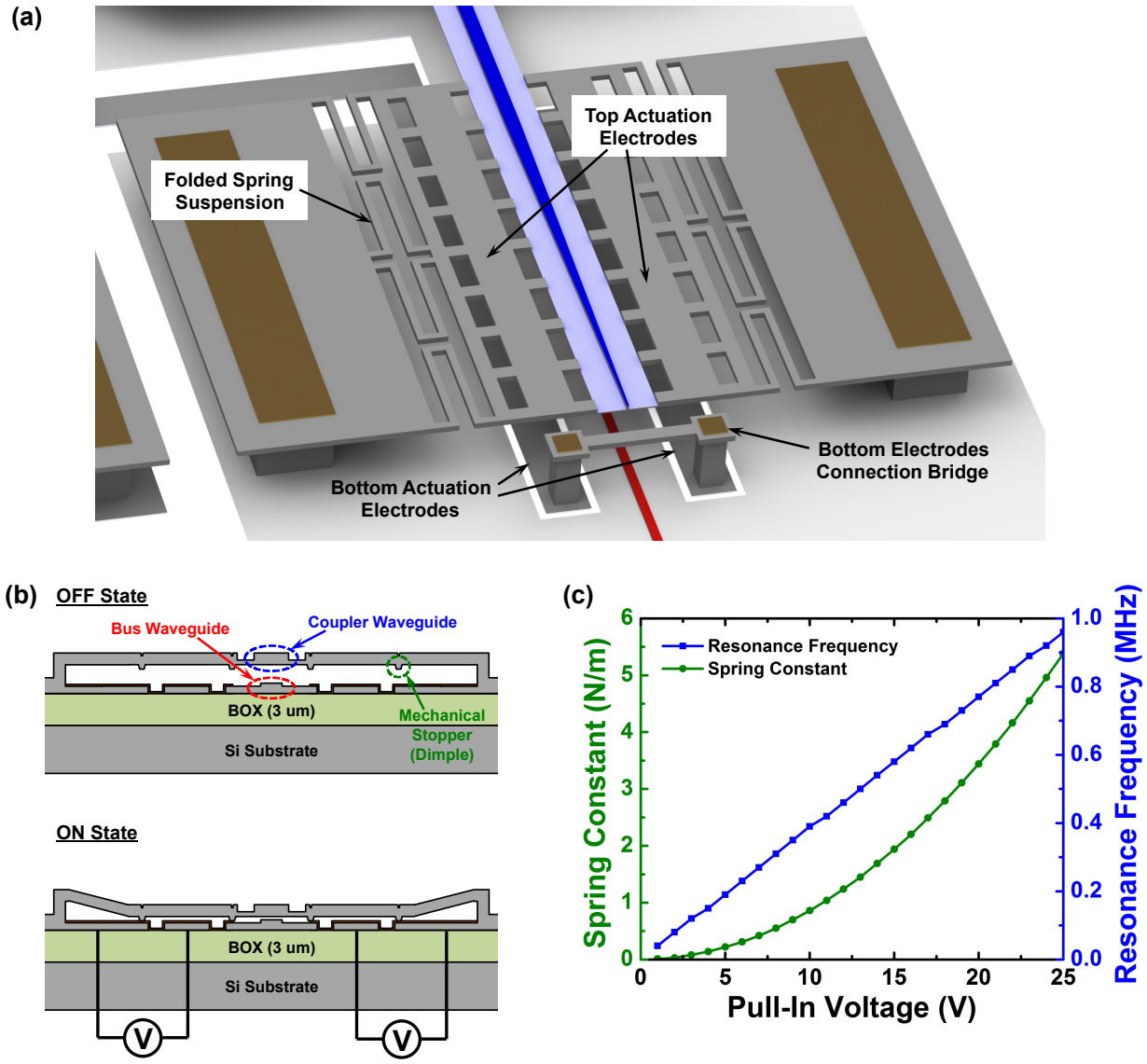

Fig. S1. Electrostatic MEMS actuator design. (a) Schematic of the actuator. (b) Cross sections of the actuator in ON and OFF states. (c) Calculated spring constant and resonance frequency as functions of pull-in voltage.

where k is the spring stiffness, d_0 the initial gap distance, A the actuation electrode area, ε the permittivity and m the actuated mass. For low actuation voltage, we first maximize the electrostatic actuator area, limited by the optical design and layout constraints. The electrode area of one actuator is 2 x 35 µm x 3 µm. The initial gap distance d_0 of 900 nm is chosen to ensure zero optical coupling (-60 dB) in the OFF state. With d_0 and A defined, the remaining free design parameter is the spring stiffness k. A low spring stiffness will allow for low actuation voltages, but at the same time, the resonance frequency will be low, and the restoring spring force $F = kx$ will be limited. The restoring spring force needs to be sufficient to overcome the adhesion at the interface between the poly-silicon dimple and the landing site, preventing in-use stiction of the MEMS structures. While quantitative prediction of the adhesion effect is difficult, the following preventive measures were implemented in order to minimize the stiction: (1) the dimple area is kept to a minimal size (dimple diameter is 500nm, limited by our lithography capabilities); (2) the landing site and the dimple are kept at the same potential (common ground) at all times; (3) the alumina ALD layer provides a hard surface coating in order to reduce surface wear [1].

The spring stiffness can be expressed as function of the design pull-in voltage:

$$k = \frac{27 V_{PI}^2 \varepsilon A}{8 d_0^3} \qquad \textbf{(S3)}$$

Figure S1(c) shows the spring constant and the corresponding resonance frequency versus pull-in voltage for the area and gap distance given above. The spring constants are in the range of 1–5 N/m for actuation voltages below 25 V. Experimentally, we observe that for spring constants below 1 N/m, the adhesion force at the dimple/landing site interface is larger than the restoring spring force, and the actuator is permanently stuck. We choose folded-spring suspensions to achieve a compact layout and relief of any residual stress in the deposited polysilicon layer. Eight folded springs with an unfolded length of 20 µm and a width of 500 nm each are attached to the actuator. With a poly-Si thickness of 300 nm, the total spring stiffness amounts to 4.1 N/m in this design. This corresponds to a pull-in voltage of 22 V and an estimated resonance frequency of 840 kHz.

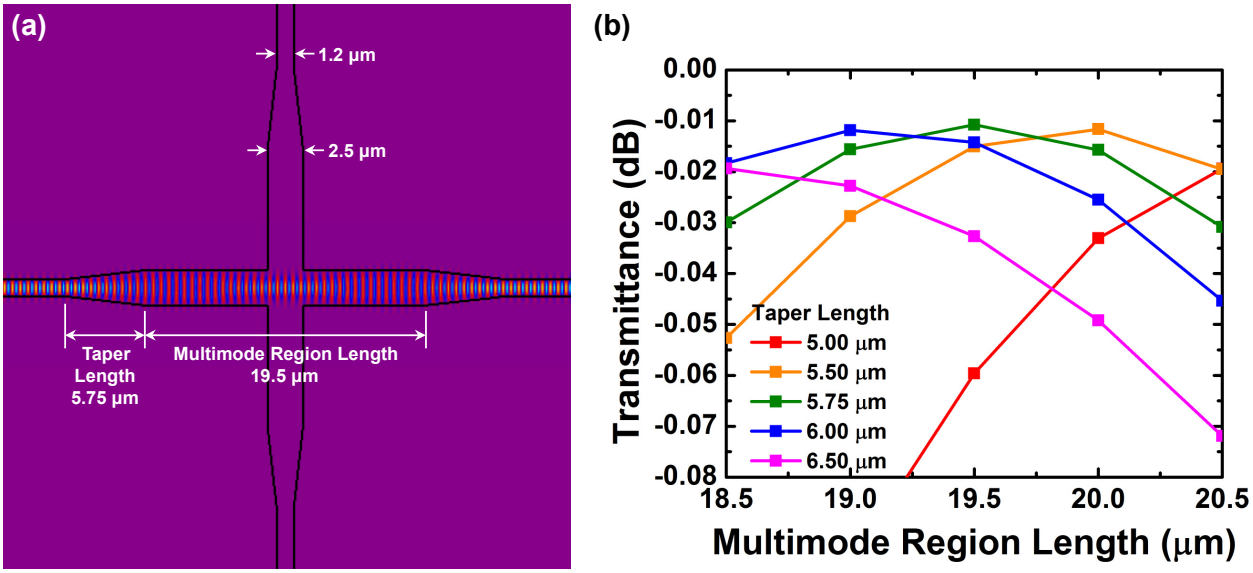

Fig. S2. MMI crossing design. (a) Optical mode profile of the designed MMI crossing. (b) Simulations of insertion loss with various taper and multimode region lengths. The lowest loss of 0.011 dB is obtained with 5.75 μm taper length and 19.5 μm multimode region length.

Section II. Low Loss Multimode Interference Crossing Design

Light propagates through multiple crossings in our switch architecture although it needs to pass through only one switching element (a pair of adiabatic couplers). Therefore, low loss crossings are essential components to keep the overall insertion loss low. Here, multimode interference (MMI) structures are used to achieve ultra low insertion loss.

The MMI crossing uses the interference of two or more optical modes to focus light at the center of the intersection. The length of the multimode region is determined by the beat length among the modes. Previously, MMI crossings on silicon photonics platform have been demonstrated with compact footprints (< 10x10 μm^2) and decent optical losses (0.017~0.2 dB) [2–7]. Here, we aim at much lower optical loss by using smaller effective index difference for the MMI, at the expense of larger footprint. Our waveguides and MMI crossings are defined by 60 nm-deep partial etch on a 220 nm-thick silicon layer.

The physical dimensions and the optical mode profile of our crossing design are shown in Fig. S2(a). We choose 1.2 μm for the width of the input and output waveguides to support a single even mode. The width is subsequently tapered to 2.5 μm to excite two even modes. The taper length and the multimode region length were optimized by parameter variation to minimize the insertion loss as shown in Fig. S2(b). The insertion loss of the optimum design with a taper length of 5.75 μm and a multimode region length of 19.5 μm is calculated to be 0.011 dB and the crosstalk is less than -70 dB.

Section III. Simulations for Fabrication Error Tolerance Study

One of the key challenges of large-scale photonic integrated circuits is the fabrication precision and yield. Our 64x64 switch has 8,192 adiabatic couplers. It is important to design couplers with high fabrication tolerance as fine-tuning individual couplers will be prohibitively expensive and consume too much power.

Fortunately, the adiabatic couplers have large fabrication tolerance and operate over a broad optical bandwidth, unlike normal directional couplers, which are highly sensitive to physical dimensions such as waveguide width, gap spacing, and coupler length. For example, the adiabatic coupler shows an acceptable coupling performance (insertion loss < 0.2 dB) with ±50 nm variation around the optimum spacing (125 nm) as shown in Fig. 2d in the main text. The transfer characteristics of adiabatic couplers for various taper lengths is plotted in Fig. S3(a). Efficient coupling is achieved for couplers that are longer than 25 μm. We chose 30 μm to obtain an extra safety margin.

Because the polysilicon coupler waveguide layer is deposited using low-pressure chemical vapor deposition (LPCVD), some thickness variation is possible. As depicted in Fig. S3(b), the coupling loss is less than 0.2 dB for coupler waveguide thickness variation of ±40 nm. It is also verified that the adiabatic coupler works well as long as etch depth is controlled within ±40 nm variation from its design target [Fig. S3(c)].

We also investigated the effect of the alignment error between the bus and the coupler waveguides. No significant performance degradation was observed with ±100 nm alignment offset, which can be easily achieved using standard lithography equipment such as steppers.

Section IV. Fabrication Process

The fabrication process flow is illustrated in Fig. S4. We start with a silicon-on-insulator (SOI) wafer with a 220 nm-thick silicon device layer and a 3 μm-thick buried oxide (BOX) layer. First, the bus waveguides and actuation electrodes are patterned by 60 nm-deep shallow etch and 220 nm-deep full etch on the silicon layer. Then, a 10 nm-thick aluminum oxide layer is deposited by atomic layer deposition (ALD). The purpose of this aluminum oxide layer is to protect the BOX layer from undercut during the final release etch. However, subsequent thermal processes at high temperature degrade the aluminum oxide layer, resulting in increased optical loss. Therefore, the aluminum oxide on top of waveguides is selectively removed by wet etching (in BHF). Next, a 1.5 μm-thick low temperature oxide (LTO) is deposited, followed by chemical mechanical polishing (CMP) to planarize the LTO surface and reduce the LTO thickness to 1 μm. Circular holes are etched into LTO with a partial etch depth (175 nm) to create mechanical dimple stoppers. The etch depth at this step defines the gap

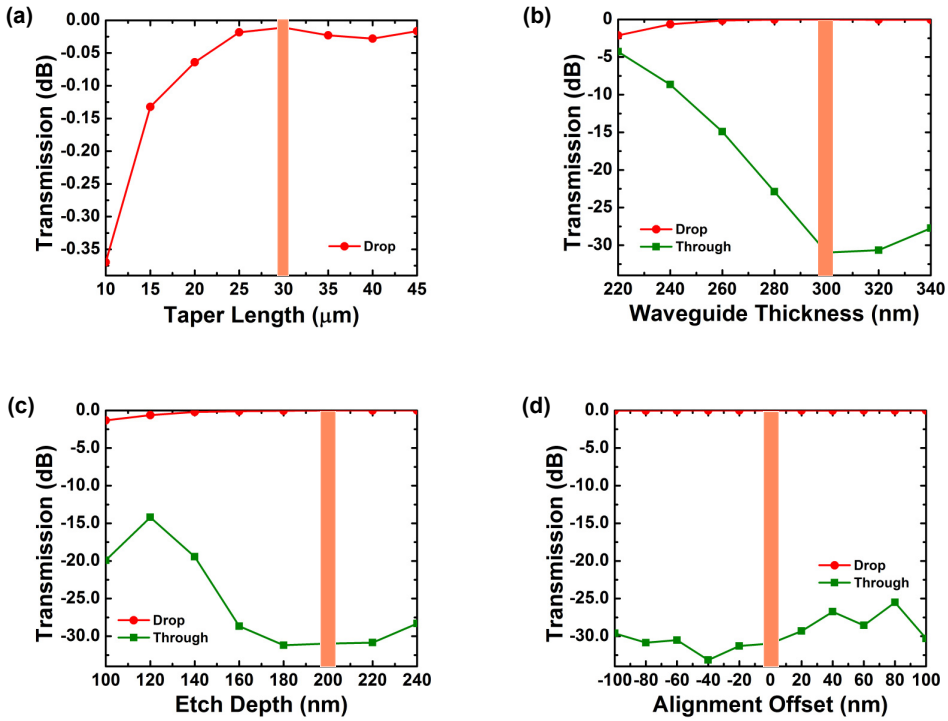

Fig. S3. Simulations for fabrication imperfection tolerance. (a) Optical transmission as a function of adiabatically tapered coupler lengths. (b) Optical transmissions as a function of thickness of the coupler waveguide. (c) Optical transmissions as a function of the etch depth of poly-silicon coupler waveguide. (d) Optical transmissions as a function of alignment offset between coupler waveguide and bus waveguide. The selected design parameter is highlighted with an orange bar in each plot.

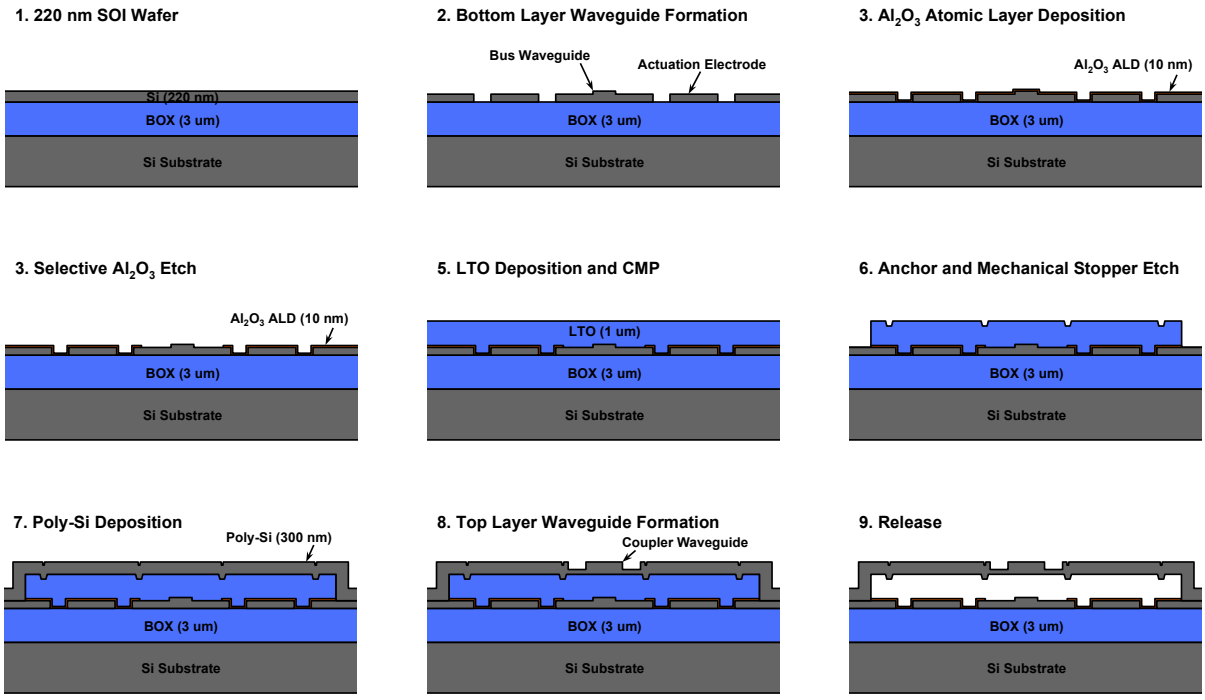

Fig. S4. Fabrication process.

distance (125 nm) in the ON state. Another full LTO etch stopping at silicon layer is performed for mechanical anchors. For the coupler waveguide, a 300 nm-thick amorphous silicon layer is deposited by LPCVD at 570 °C, followed by two annealing steps of 12 hours at 600 °C and 1 hour at 900 °C. Then, the adiabatic couplers and actuators are patterned by 200 nm-deep partial etch and 300 nm-deep full etch. Metal contacts are created by metal evaporations (30 nm-thick chrome and 150 nm-thick gold) and

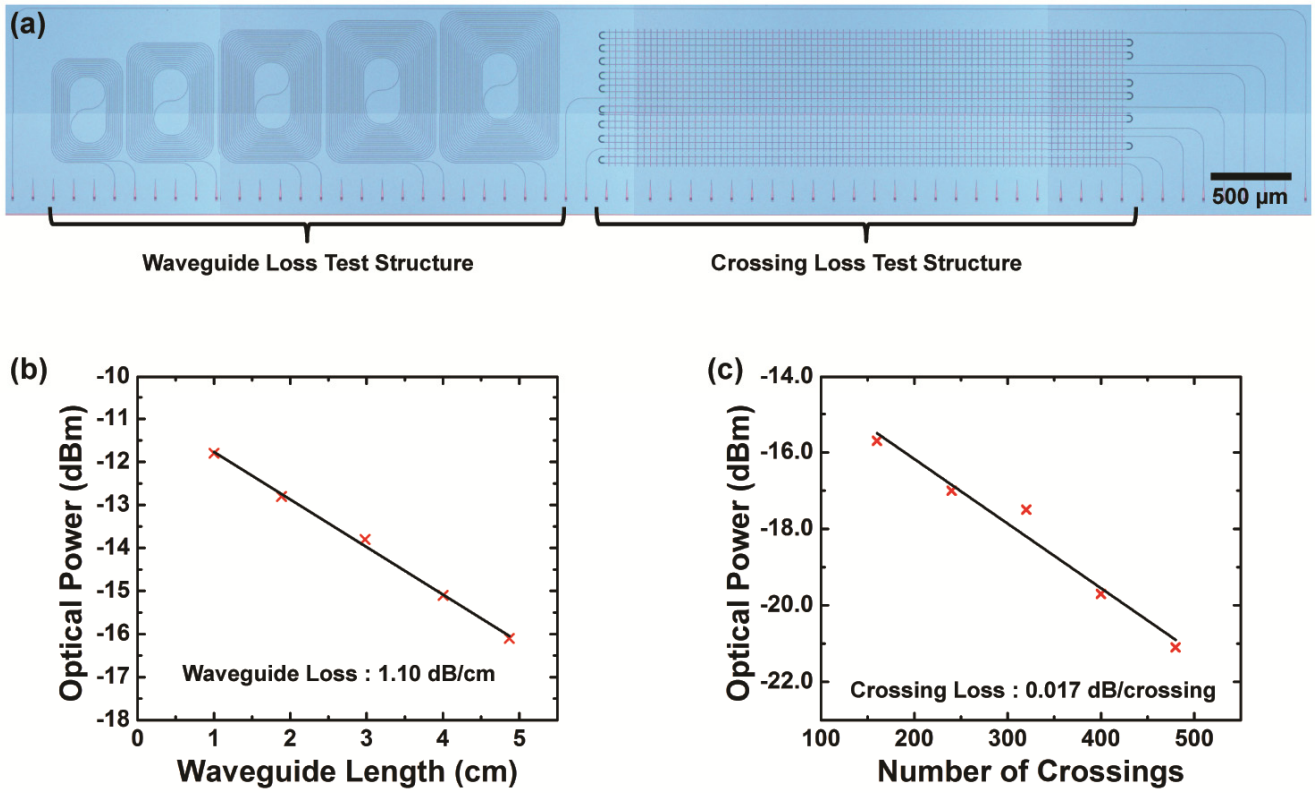

Fig. S5. Passive optical test structures. (a) Microscope image of the test structures. 600 nm-wide ridge waveguide spirals with various lengths is shown at left and waveguides with various numbers of MMI crossings at right. (b) Measured propagation loss versus waveguide length. The measured propagation loss is 1.1 dB/cm. (c) Measured insertion loss versus the number of the MMI crossings. The measured insertion loss is 0.017 dB/crossing.

subsequent lift-off process. Finally, the device is released in vapor HF.

Section V. Measurement of Passive Optical Test Structures

In order to measure the passive optical losses (waveguide propagation loss and crossing insertion loss), we designed passive test structures for a cut-back method [Fig. S5(a)]. For the waveguide propagation loss, 600 nm-wide ridge waveguide spirals having various lengths were measured. The propagation loss was estimated to be 1.1 dB/cm as shown in Fig. S5(b). Then, the waveguide crossing loss was measured from waveguides with various numbers of crossings [Fig. S5(c)]. The measured crossing loss and crosstalk are 0.017 dB/crossing and -55 dB, respectively. The unit cell loss can be inferred from these measured values. Since one unit cell consists of a 70 μm-long ridge waveguide and a MMI crossing, the estimated unit cell loss is 0.025 dB (= 1.1 dB/cm x 70 μm + 0.017 dB).

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