**Optimization of Bistable Silicon Photonic MEMS Switch Architectures**

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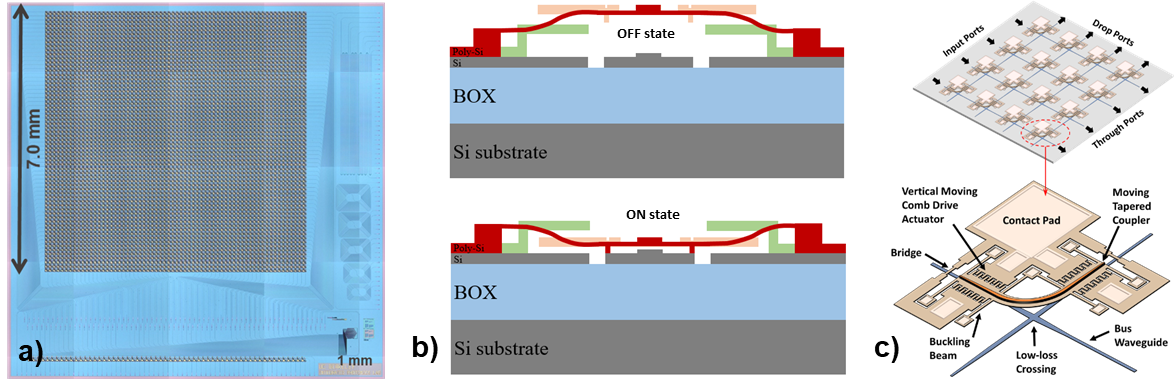
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*Project Type: Semester Project Section: Microengineering*

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*Submission of Final Report: 11.06.2021 Presentation at Group Meeting: TBD*

Silicon Photonic MEMS Switches have recently been shown to be an excellent contender for large-scale photonic integrated circuit switch matrices, for the use in next-generation data centers, telecommunication infrastructure, as well as in space telecommunications [1]. In particular, the possibility to include mechanical bistability, provides access to mechanically stable, unique non-volatile optical configuration states, which has the potential to drastically reduce the power consumption in optical switches [2]. An example of a previously fabricated 64 x 64 silicon photonic MEMS switch is shown in Figure 1a, with the bistability mechanism shown in Figure 1b, and the architecture and unit cell depicted schematically in Figure 1c.



The bistability mechanism introduces additional constraints on the design. In particular, it would be beneficial, to only exploit uni-axial stress states by implementing **suspensions aligned in one direction only**. At the same time, a minimization of the unit cell size is desired, to **reduce overall footprint** and to **increase the actuation speed**. Finally, the optical switch matrix architecture should result in **lowest optical loss** possible, and allow for row-column addressing at the same time.

The goal of this project is to investigate optimized silicon photonic MEMS switch architectures according to the above optimization criteria, and to draft the corresponding photonic chip layouts in an actual microfabrication design framework. The project provides ample design freedom and opportunities for creative solutions. The student will dive into the exciting topic of photonic integrated circuits, investigate cutting edge photonic MEMS switches and we will provide integration in a dynamic team of photonic MEMS enthusiasts.

[1] T.-J. Seok, et al. (2016), Optica, (<https://doi.org/10.1364/OPTICA.3.000064>)

[2] H Sattari et al. (2019) Proc. SPIE 10931D (<https://doi.org/10.1117/12.2507192>).

**Proposed Project Timeline and Content of the Project:**

*Preparation Phase:*

* Study of Silicon Photonic MEMS Literature.

*Layout Analysis*

* Detailed understanding of the current design framework (and the tightly linked microfabrication process)

*Design Exploration and Architecture Analysis*

* Explore Design Space for Various Unit Cell Design Variations
* Propose at least 3 optimized switch designs.
* Extraction of Scaling Properties (Footprint, Optical Loss, etc.)
* For at least 1 Optimized Design: Determination of Buckling States in FEM Simulation
* For at least 1 Optimized Design: Determination of Resonance Frequency in FEM Simulation
  + if time permits, assessment of dynamic behavior according to dedicated model (tbd)
* Comparison and assessment of design and architectures.
* For 1 optimized design: Layout Drafting, and Finalization in ASML Stepper Framework

*Reporting:*

* **TBD – Mid-term project presentations**
* **TBD – Final presentation** at the Quack Group Meeting (exact date to be defined, but before 28.6.2021).
* **11.06.2021 – Date of Submission of Final Report**

The dates are as from the academic calendar on 4 January 2021, which should correspond to the official dates. However, the official dates are communicated by the Service Académique (SAC). It is the student’s responsibility to respect the deadlines and the administrative formalities of the reporting to the Service Académique (notably on isa.epfl.ch).