

# **Systematic Design of Analog CMOS Circuits with LUTs using open-source tools and PDKs**

## **Part I (c)**

\* Most slides are borrowed or adapted from B. Murmann

# Appendix

# MOS Device Capacitances

source: Razavi

A circuit perspective:

NOTE:

*we are interested  
only in modeling the  
caps for  $V_{GB} > V_{FB}$   
(no accumulation)*

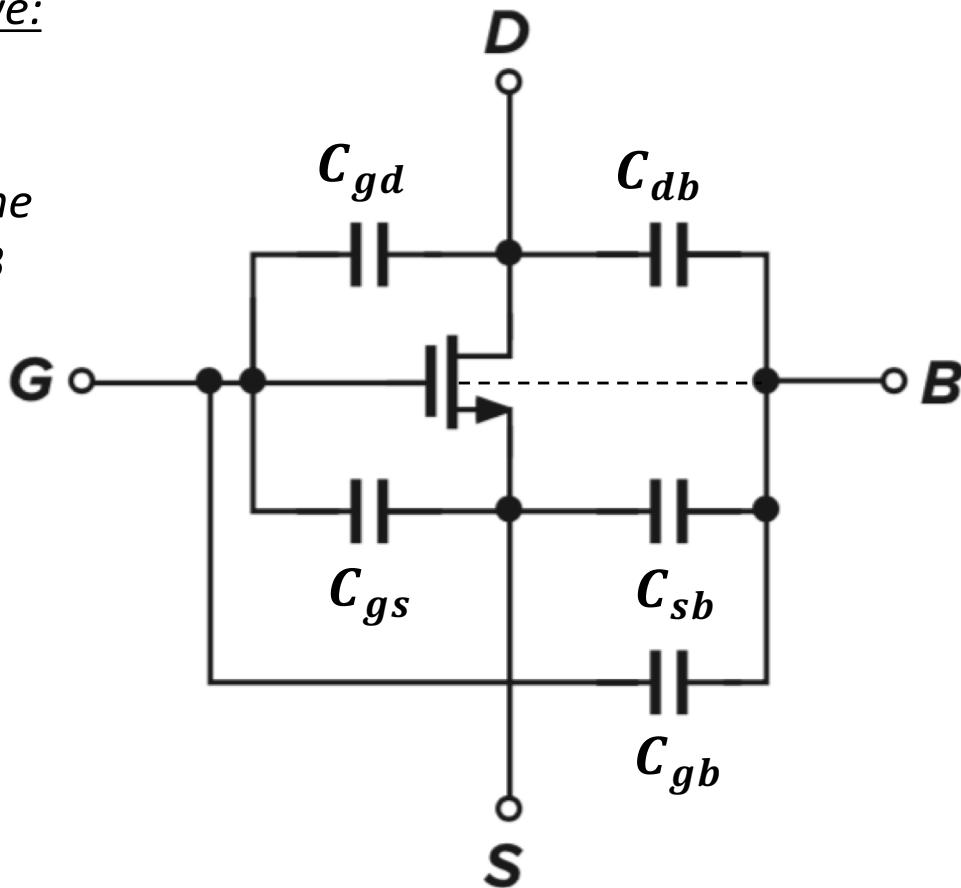
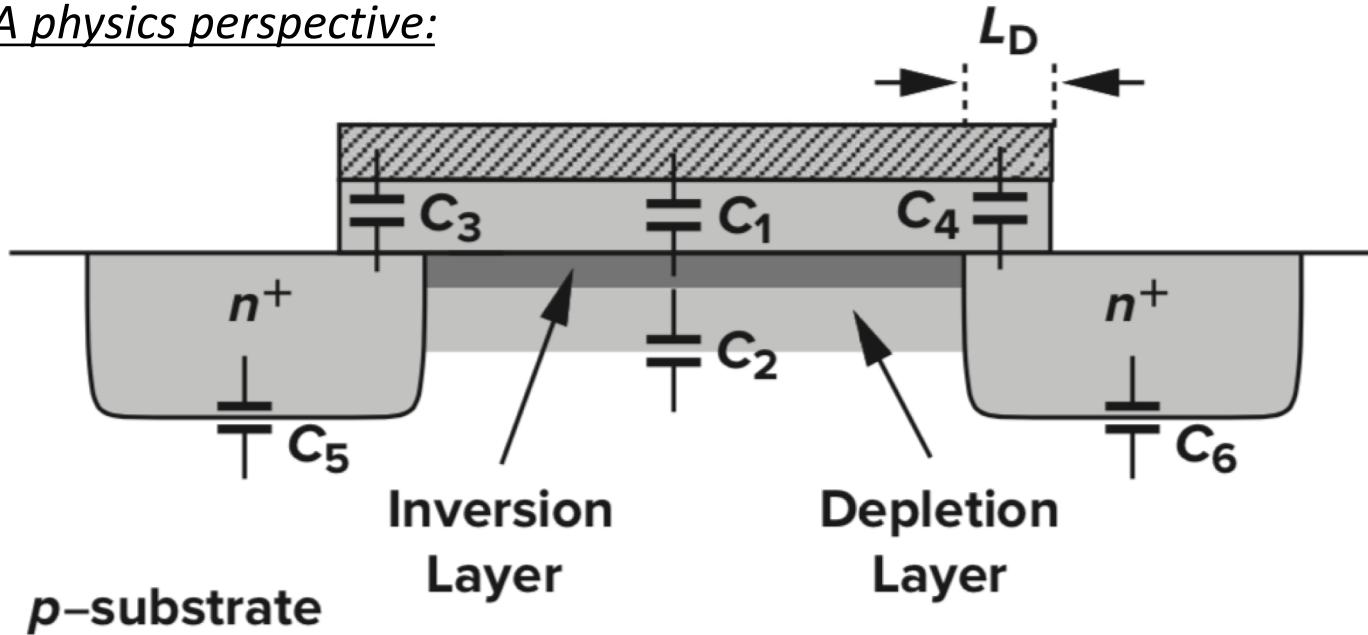


Figure 2.31 MOS capacitances.

# MOS Device Capacitances

A physics perspective:

source: Razavi

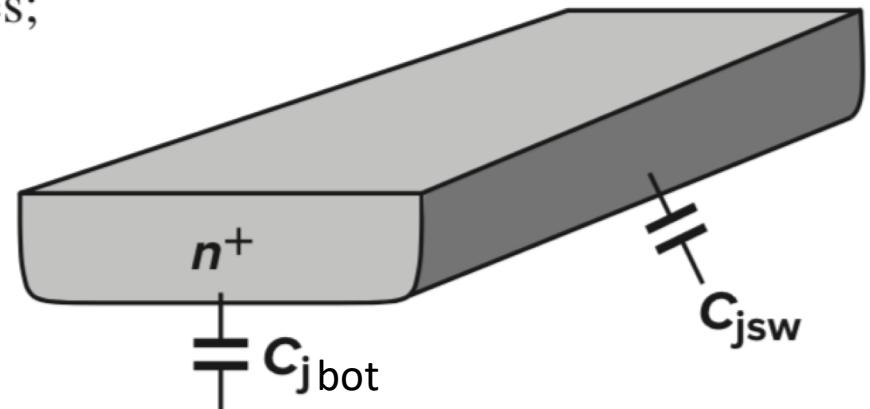


**NOTE:**

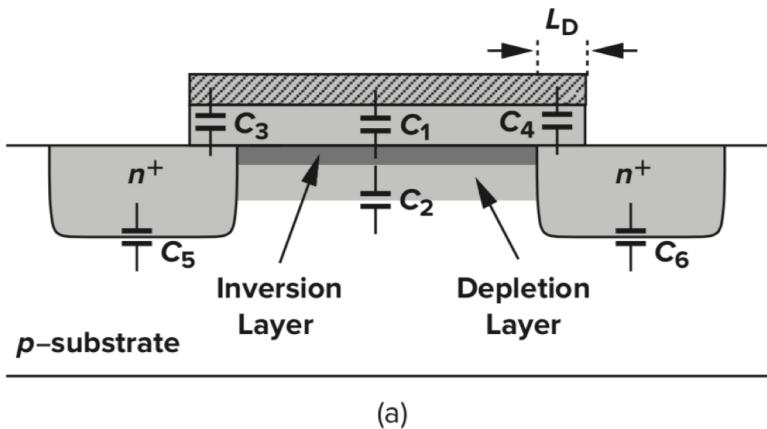
*we are interested  
only in modeling the  
caps for  $V_{GB} > V_{FB}$   
(no accumulation)*

(a) MOS device capacitances;

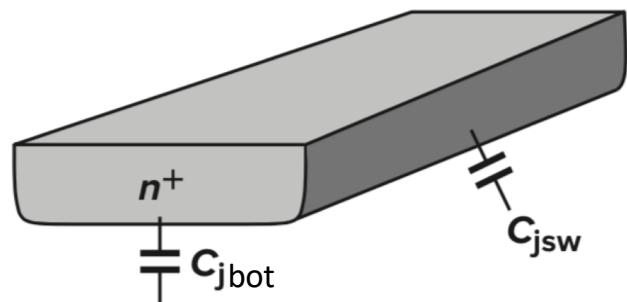
(b) decomposition of S/D junction capacitance  
into bottom-plate and sidewall components.



# S/D junction capacitances



*source: Razavi*



$$C_5 \equiv C_{sb}$$

$$C_6 \equiv C_{db}$$

$$C_{db} = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PB}\right)^{MJSW}}$$

$$C_{sb} = \frac{AD \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VSB}{PB}\right)^{MJSW}}$$

$$AD = W \cdot L_{DIF}$$

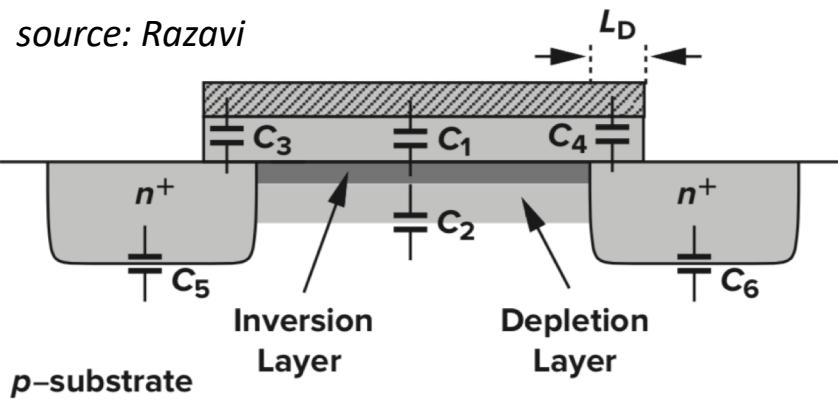
$$PD = W + 2 \cdot L_{DIF}$$

$$AS = W \cdot L_{DIF}$$

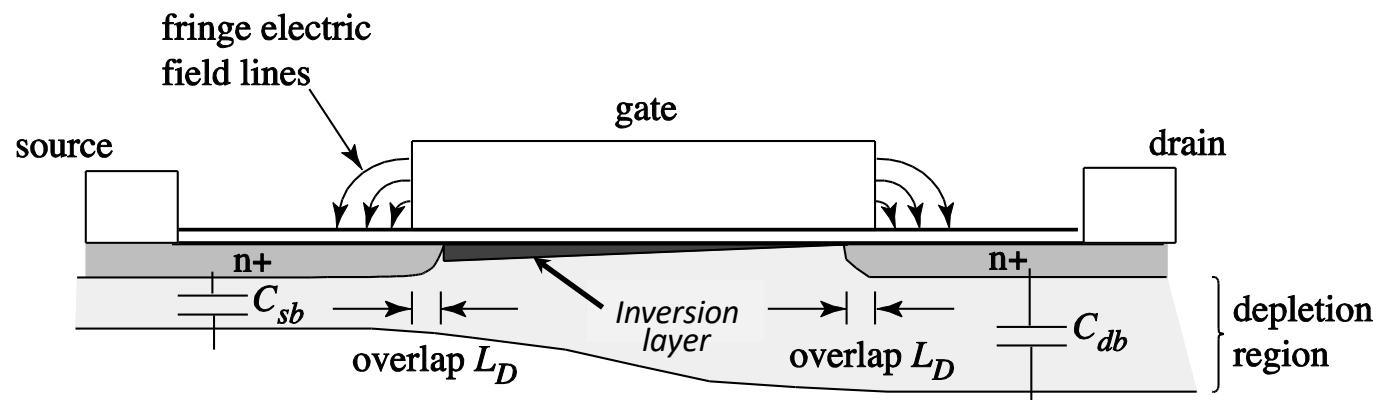
$$PS = W + 2 \cdot L_{DIF}$$

$$ACM = 3 \rightarrow L_{DIF} = 2 \cdot HDIF$$

# Overlap capacitances



source: Razavi



source: Murmann

$$C_{ovl,s} = C'_{ox} WL_D + C_{s,fringe} = C'_{ovl,s} \cdot W = CGSO \cdot W$$

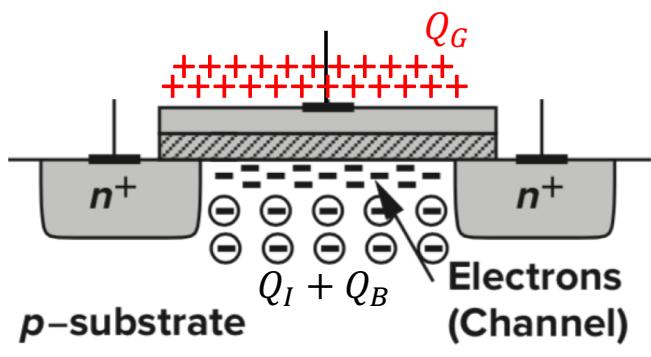
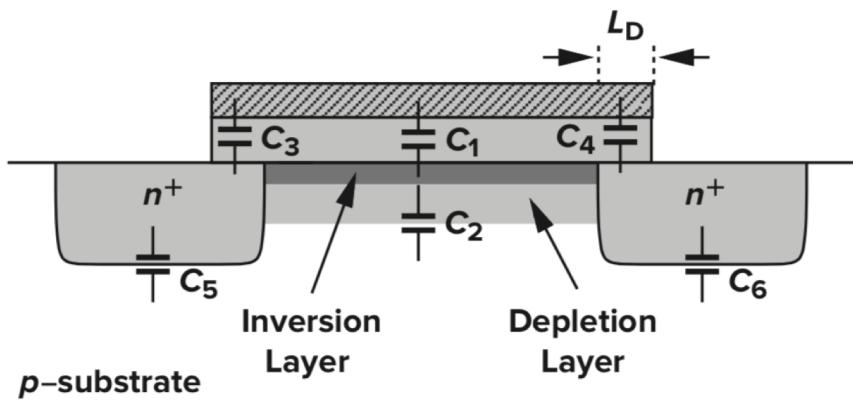
$$C_{ovl,d} = C'_{ox} WL_D + C_{d,fringe} = C'_{ovl,d} \cdot W = CGDO \cdot W$$

$$C'_{ox} = \frac{\epsilon_{ox}}{TOX} \quad \epsilon_{ox} = \epsilon_0 \cdot k_{ox} = 8.85 \cdot 10^{-12} \frac{F}{m} \cdot 3.9 \approx 34.52 \cdot 10^{-12} \frac{F}{m}$$

Example:

$$TOX = 4.1 \cdot 10^{-9} m \rightarrow C'_{ox} \approx 8.42 \cdot 10^{-3} F/m^2 = 8.42 fF/\mu m^2$$

# Capacitances between gate and substrate



*Charge neutrality:*

$$Q_G + Q_I + Q_B = 0$$

Here the “story” gets more complicated:

- Assuming  $V_{GB} > V_{FB}$ , before the channel forms (and in practice as long as the inversion charge is negligible compared to the depletion charge) we have:  
 $\Delta Q_G = -\Delta Q_B$  and  $\Delta Q_I = 0$  and  $\Delta V_{GB} = \Delta V_{ox} + \Delta \psi_s$   
 Therefore:

$$\frac{-\Delta Q_B}{\Delta V_{GB}} = \left( \frac{1}{C_{ox}} + \frac{1}{C_b} \right)^{-1}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} WL = C'_{ox} WL \equiv C_1$$

$$C_b = \frac{\epsilon_s}{d_B} WL \equiv C_2$$

$$d_B \approx \sqrt{\frac{2\epsilon_s}{qN_A} \left( -\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}} \right)}$$

The charge in the channel comes from the drain and the source:  $\Delta Q_I = \Delta Q_D + \Delta Q_s$

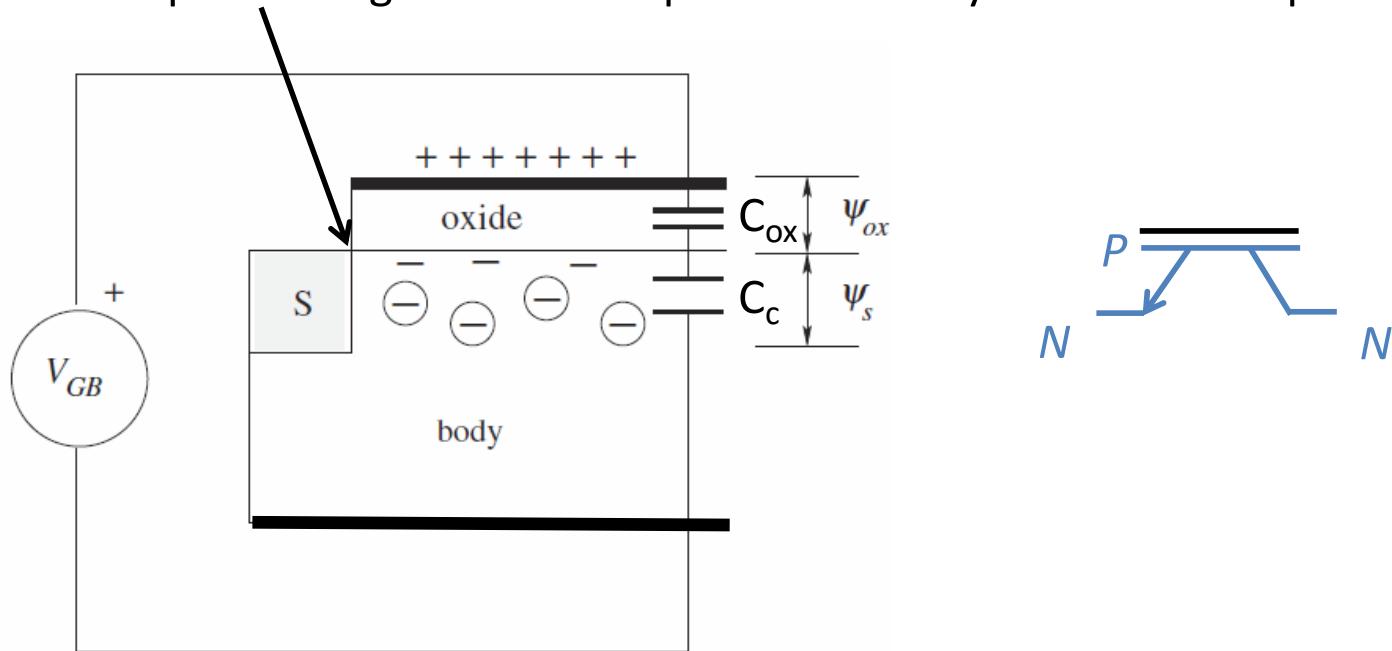
$$\frac{-\Delta Q_s}{\Delta V_{GS}} = 0$$

$$\frac{-\Delta Q_D}{\Delta V_{GD}} = 0$$

# Weak Inversion Operation

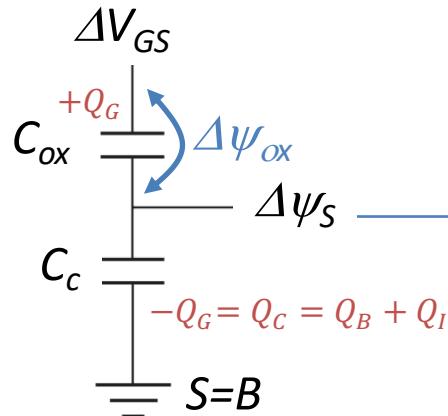
- Physics of the MOST is governed by a “floating base BJT” model
- The amount of electrons injected into a given point of the body depends on the potential present at that given point

Potential at this point is higher than the potential at any other surface point



D.L. Pulfrey, Understanding Modern Transistors and Diodes,  
Cambridge University Press, 2010.

Total drain current dashed line



# Capacitive Divider

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_c + C_{ox}} = \frac{1}{n}$$

*Only a fraction of the controlling voltage applied at the gate reaches the surface of the semiconductor*

- n is called “subthreshold slope”
- $n \approx 1.45$  for the nMOS device in our technology
- Using a more precise approach (e.g. see Tsividis) we can find that the final expression for the drain current becomes:

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}-V_T}{n\phi_t}} \left( 1 - e^{-\frac{V_{DS}}{\phi_t}} \right) \quad I_{D0} = \mu(n-1)C'_{ox}\phi_t^2$$

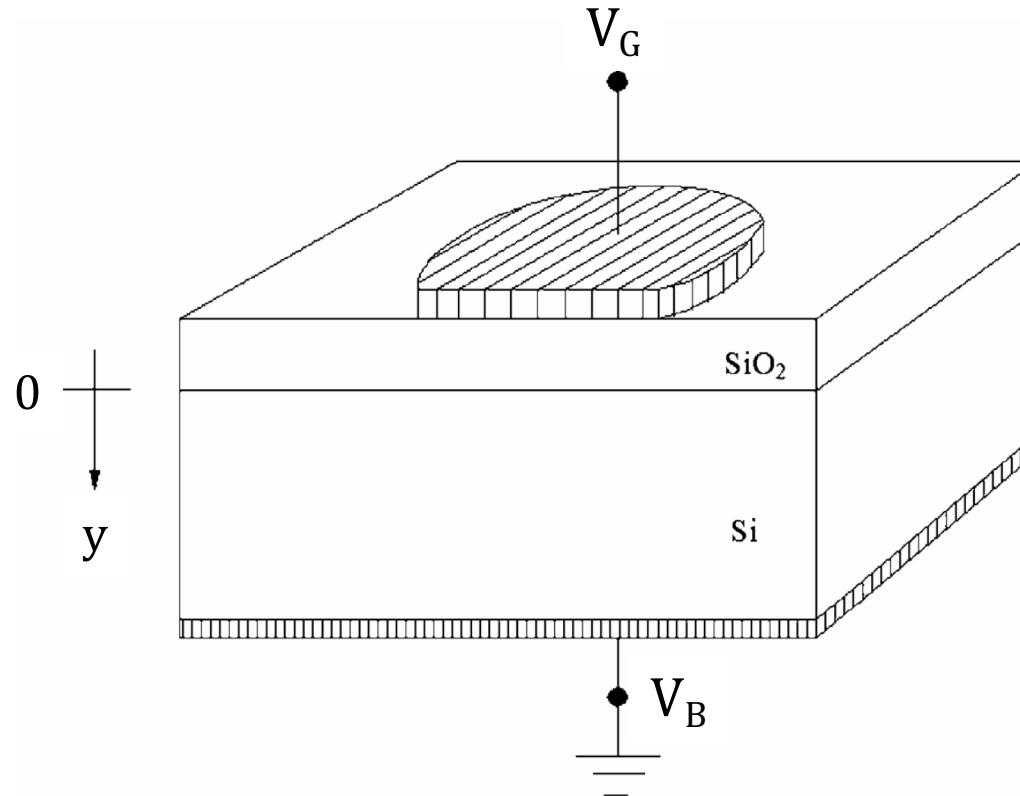
$I_{D0} \approx 0.43 \mu\text{A}$  for the nMOS device in our technology

- The fact that the current becomes independent of  $V_{DS}$  for  $V_{DS} > 3\phi_t$  ( $\approx 78$  mV) means that, unlike in strong inversion, in weak inversion the  $V_{DS}$  required to force the MOS to operate as a current source is independent of the overdrive (in other words  $V_{DS,\text{sat}}$  for a MOS in weak inversion is about  $3\phi_t$ )

# MOS “core” structure

source: Pierret

The semiconductor is sufficiently thick so that, regardless of the applied voltage  $V_{GB}$ , a field free region (the so called Si-Bulk, a.k.a. quasi neutral region) is encountered before reaching the back contact



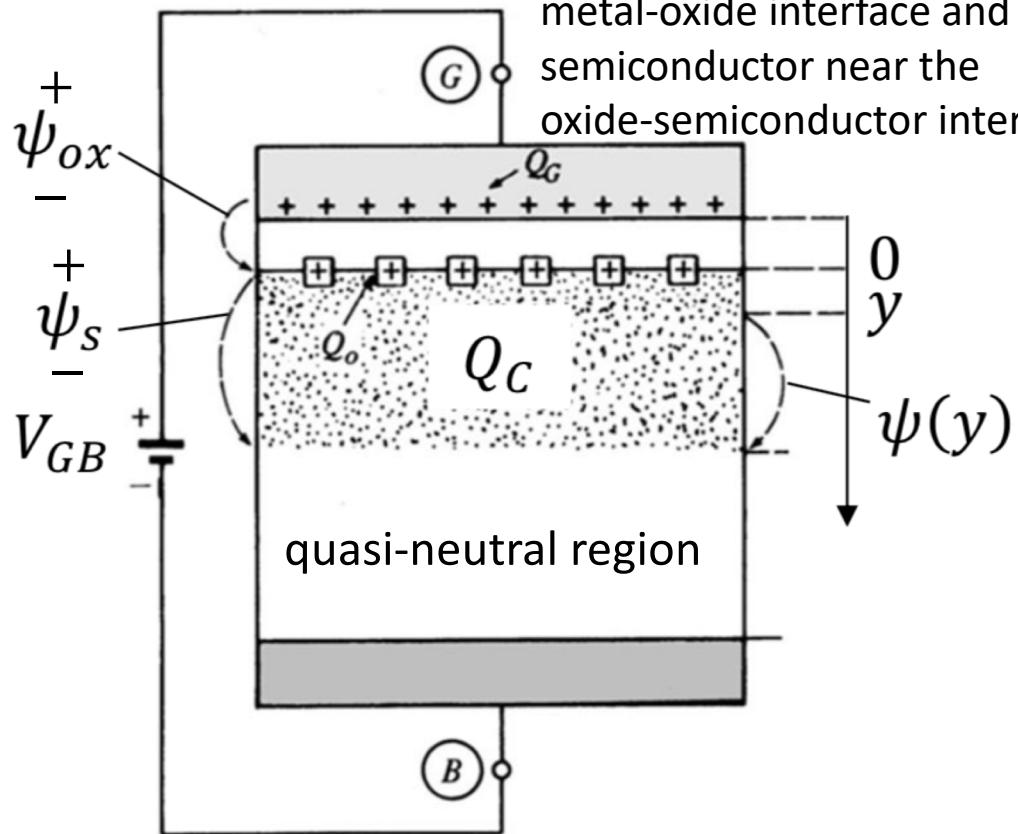
The metal-oxide-semiconductor capacitor (MOS-C)

# MOS “core” structure

source: Tsividis

**MOS “core” = Two-terminal MOS structure**

Biasing the MOS-C, charge appears in the metal near the metal-oxide interface and in the semiconductor near the oxide-semiconductor interface



top plate      bottom plate

$$Q'_G + Q'_0 + Q'_C = 0$$

(Charge balance)

$$\Delta Q'_G + \Delta Q'_C = 0$$

$$V_{GB} = \psi_{ox} + \psi_s + \phi_{MS}$$

(Potential balance)

$$\Delta V_{GB} = \Delta \psi_{ox} + \Delta \psi_s$$

NOTE:  $Q'_C = Q'_B + Q'_I$

# Inversion channel in the MOS “core”

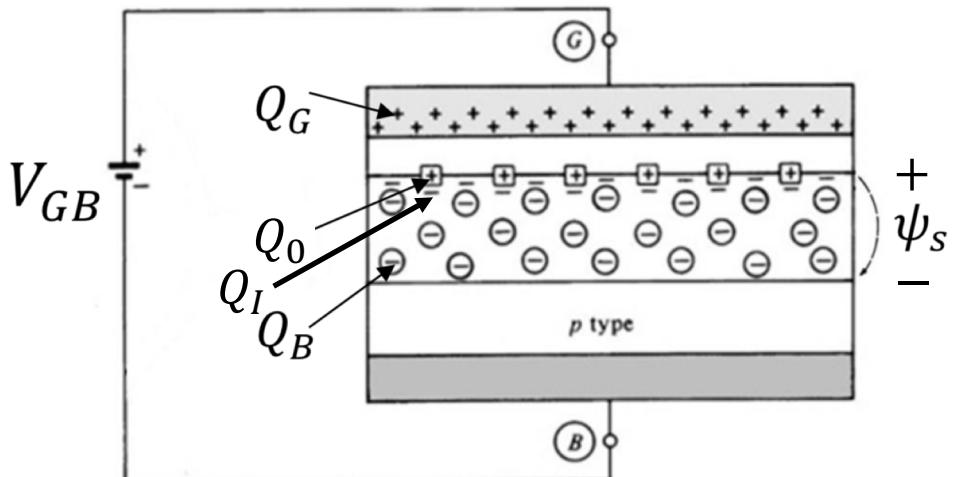
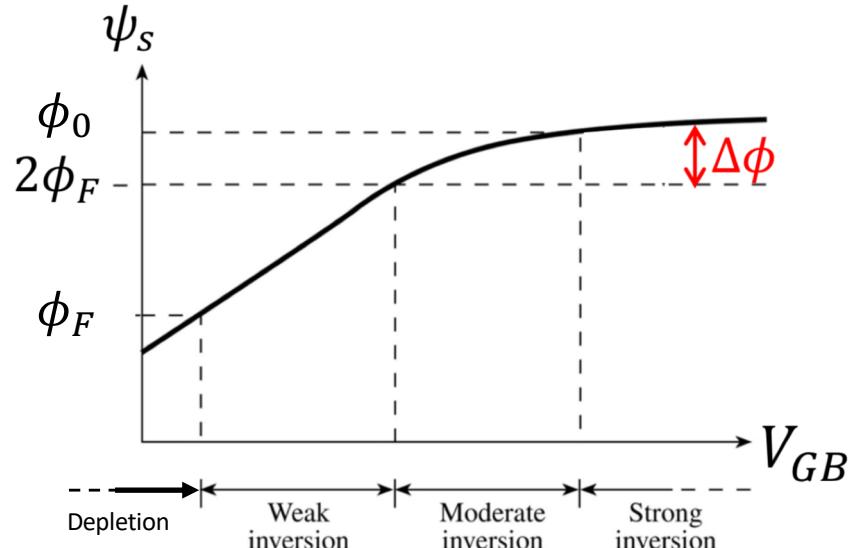
source: Tsividis

$$Q'_I = -C'_{ox}(V_{GB} - V_{FB} - \gamma\sqrt{\psi_s} - \psi_s)$$

NOTE:  
to find  $Q_I$  we need to find  $\psi_s$

Inverting the channel requires that the difference between the applied voltage  $V_{GB}$  and the other voltage terms is positive (there is an “offset”).

Note that  $\psi_s$  depends on  $V_{GB}$

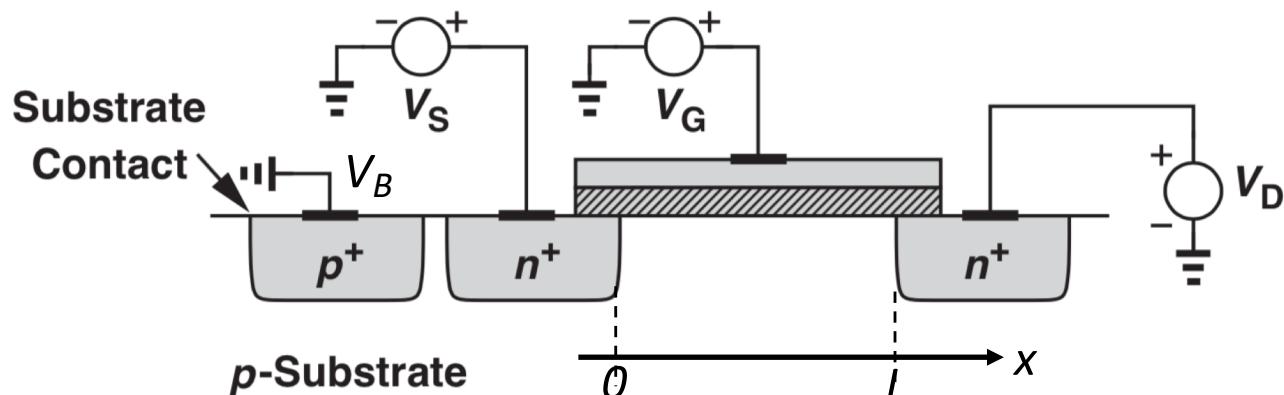


# Four-terminal nMOS structure

As we add more terminals and start to apply different voltages to them the physics of the MOS structure gets more complicated and we expect the voltage along the channel to vary (and with it the surface potential  $\psi_s$  and  $Q'_I$ )

*$\psi_s$  (and  $\psi_{ox}$ ) varies along  $x$*

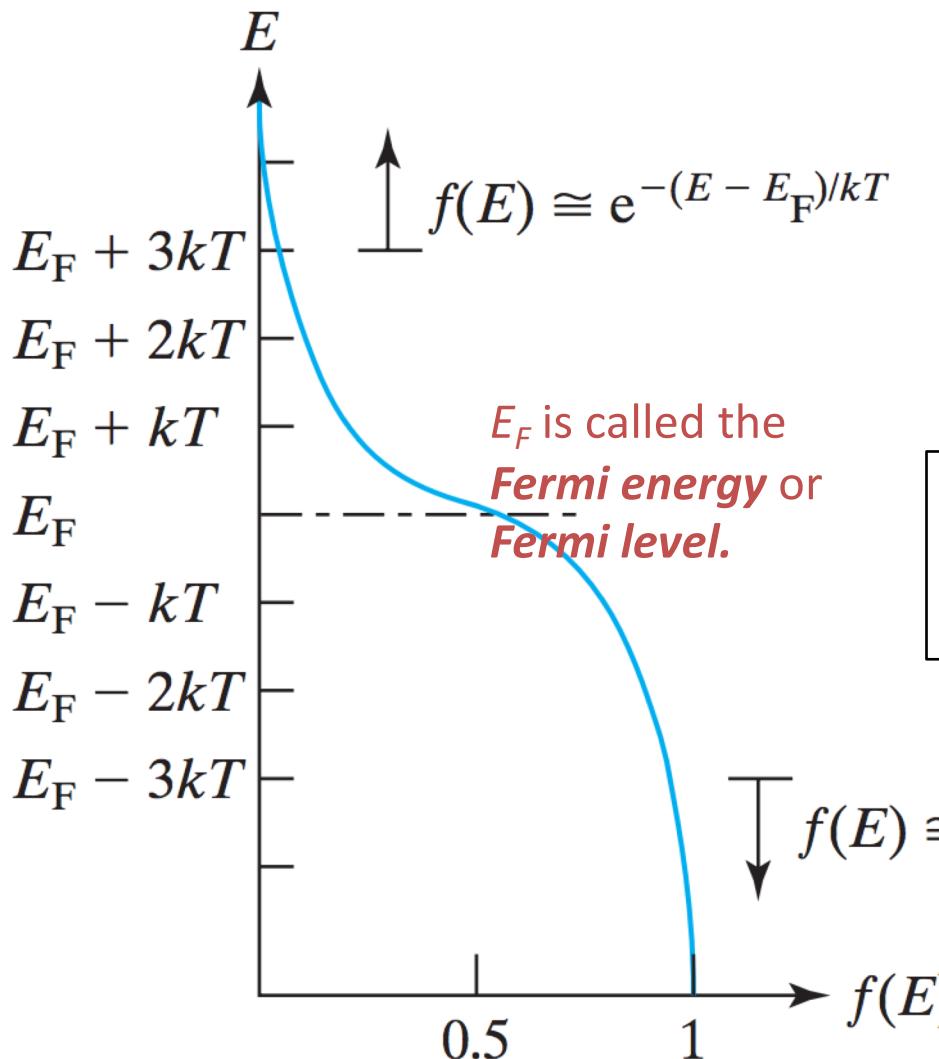
$$V_{GB} = V_{GS} - V_{SB}$$



source: Razavi

# Fermi Function

source: C. Hu



$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

$f(E)$  = Probability of an Energy State Being Occupied by an Electron

NOTE:  $\exp(3) \approx 20$

Boltzmann approximation:

$$E - E_F \gg KT \rightarrow f(E) \approx e^{-(E-E_F)/KT}$$

$$E - E_F \ll -KT \rightarrow f(E) \approx 1 - e^{-(E_F-E)/KT}$$

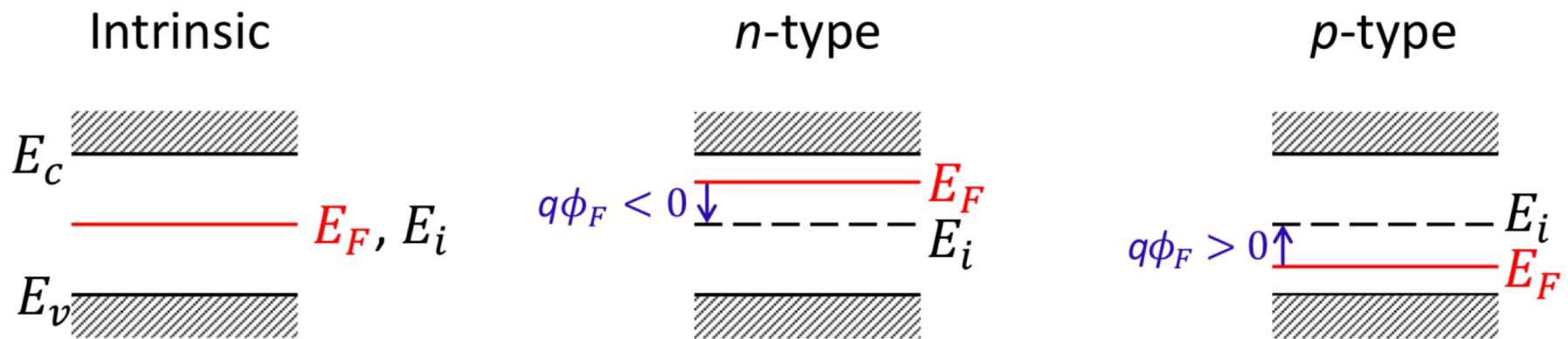
$$f(E) \approx 1 - e^{-(E_F - E)/kT}$$

**Remember:** there is only one Fermi-level in a system at equilibrium

# Equilibrium

source: Tsividis

Equilibrium = No energy exchange with external world = No current flow



$E_F$ : Fermi energy level,  $E_i$ : Intrinsic energy level,  $q$ : electron charge magnitude ( $1.602 \times 10^{-19}$  C),  $k$ : Boltzmann constant ( $1.3807 \times 10^{-23}$  C · V/K),  $T$ : absolute temperature,  $\phi_F$ : Fermi potential,  $\phi_t$ : thermal voltage

Fermi-Dirac Statistic reduces to Maxwell-Boltzmann:  $\phi_F \equiv (E_i - E_F)/q$ ,  $\phi_t \equiv kT/q$

$$p_o = n_i e^{(E_i - E_F)/(kT)} = n_i e^{\phi_F/\phi_t}$$

$$n_o = n_i e^{(E_F - E_i)/(kT)} = n_i e^{-\phi_F/\phi_t}$$

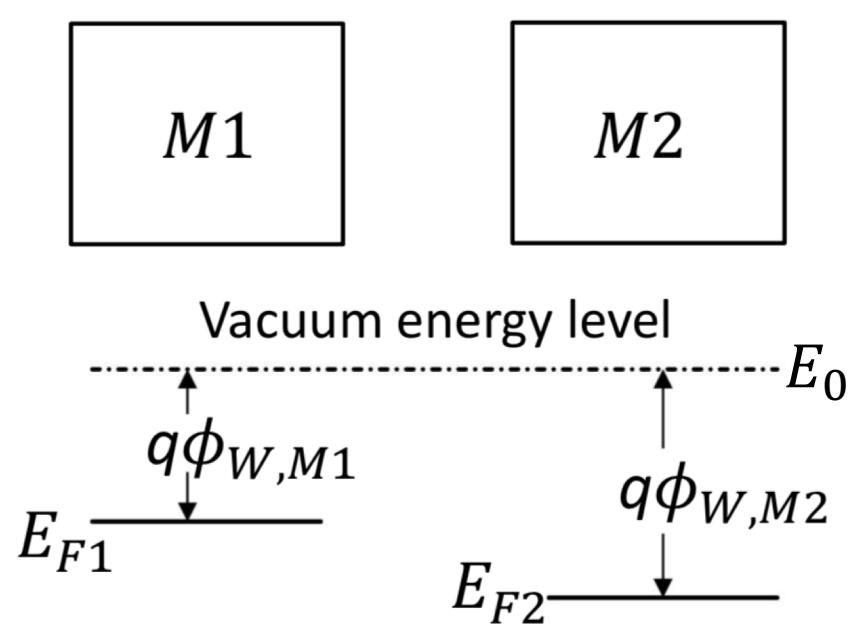
# Contact Potentials

source: Tsividis

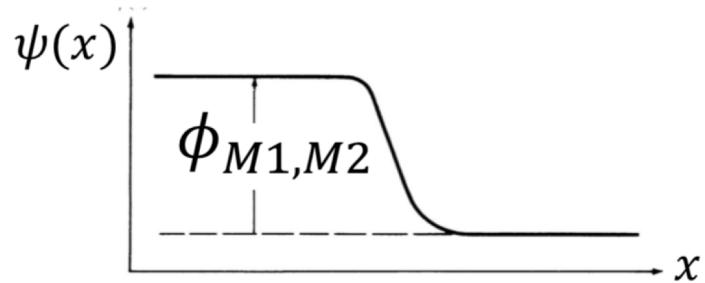
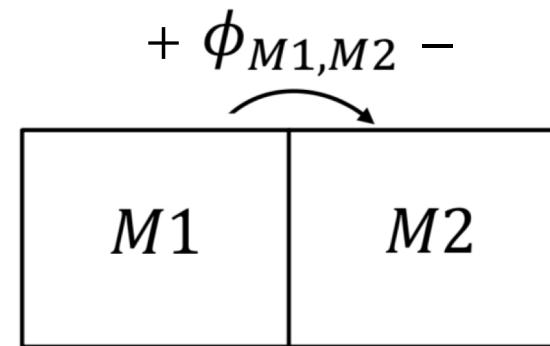
- Consider the junction of two different neutral materials M1 and M2.
- When the two materials are brought together, at first carriers diffuse from one material to the other because the concentration of these carriers is, in general, different in M1 and M2, and no opposing field exists in the initially neutral material.
- However, as each charge carrier crosses the junction, it leaves behind a net charge of the opposite polarity, and an electric field is thus established in the vicinity of the junction, which tends to inhibit the movement of carriers.
- Eventually, The field intensity increases to the point that it counteracts the tendency of carriers to diffuse, and a balance is achieved at which there is no more net carrier movement.
- An electrostatic potential change is then encountered when going from one material, through the junction, to the other material. The total potential drop in going from M1 to M2 is called the contact potential of material M1 to material M2 and is denoted by  $\phi_{M1,M2}$

# Contact Potentials

source: Tsividis



$q\phi_{W,Mi}$ : Work function of material Mi

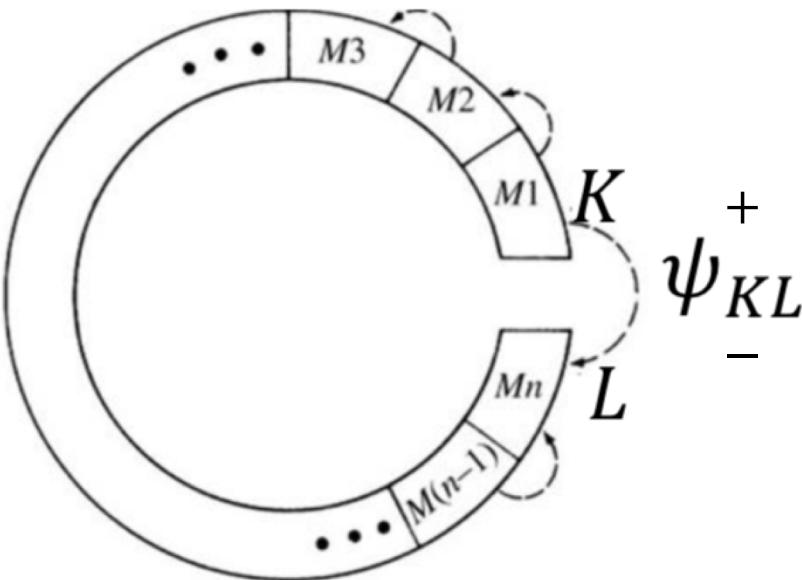


Contact potential of M1 to M2:  
$$\phi_{M1,M2} = \phi_{W,M2} - \phi_{W,M1}$$

# Several materials in series

source: Tsividis

No matter how many materials are in the loop, the electrostatic potential difference between its two ends depends only on the first and last material

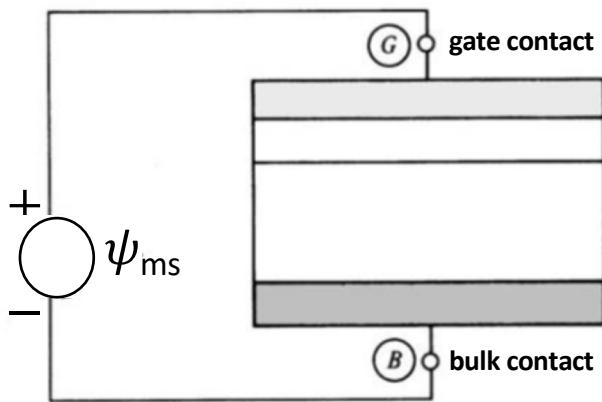
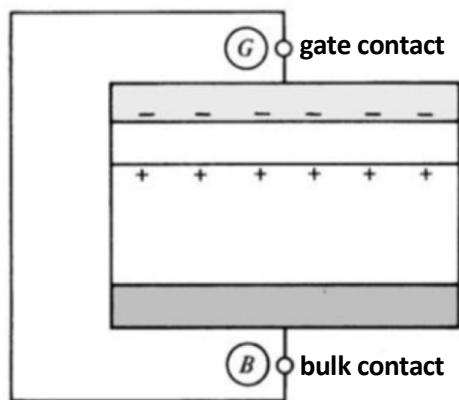
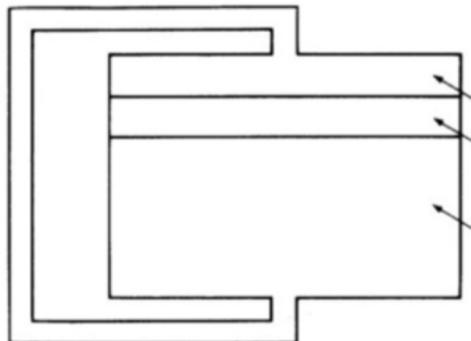


$$\psi_{KL} = (\phi_{W,M2} - \phi_{W,M1}) + (\phi_{W,M3} - \phi_{W,M2}) + \dots$$

$$\psi_{KL} = \phi_{W,Mn} - \phi_{W,M1}$$

# Flatband

source: Tsividis



- (a) Assume the gate is made of the same p-type semiconductor material as the substrate, and the same material is also used to connect the gate to the substrate. In the semiconductor, to each hole correspond a negatively charged acceptor atom from which the hole has originated. The material is neutral everywhere. Then no field can exist in the oxide, and there is no reason for carriers to be attracted toward the oxide-semiconductor interface.
- (b) Now assume the gate is made of a material that is not the same as the material of the substrate. The gate terminal is shorted to the body terminal with a wire. Going from the gate, through the external connection, to the bulk and taking into account that the sum of the encountered contact potentials depends only on the first and last material, the existence of a non zero potential between the gate and the bulk causes net charge to appear on both sides of the oxide
- (c) These net charges disappear if the total potential from the gate contact, through the external connection, to the bulk contact equals zero. This is possible if an external voltage source is applied

# Flatband

source: C. Hu

- If we assume there is electric charge  $Q_0$  trapped at the interface then the value of  $V_{GB}$  for flatband condition has to “neutralize” also the voltage induced by the presence of  $Q_0$  not just the metal-oxide contact potential  $\phi_{MS}$

$$V_{FB} = \phi_{MS} - \frac{Q_0}{C_{ox}} \quad \text{Flatband Voltage}$$

- KVL making the effect of  $Q_0$  explicit:

$$V_{GB} = \phi_{MS} - \frac{Q_0}{C_{ox}} + \psi_s + \psi_{ox} \equiv V_{FB} + \psi_s + \psi_{ox}$$

# Threshold condition

source: C. Hu

- If we decide that the level of inversion at which  $n_{\text{surface}}$  is about  $N_A$  is “satisfactory” (**a poor choice**), we see that we need to apply a value of  $V_{GB}$  equal to:

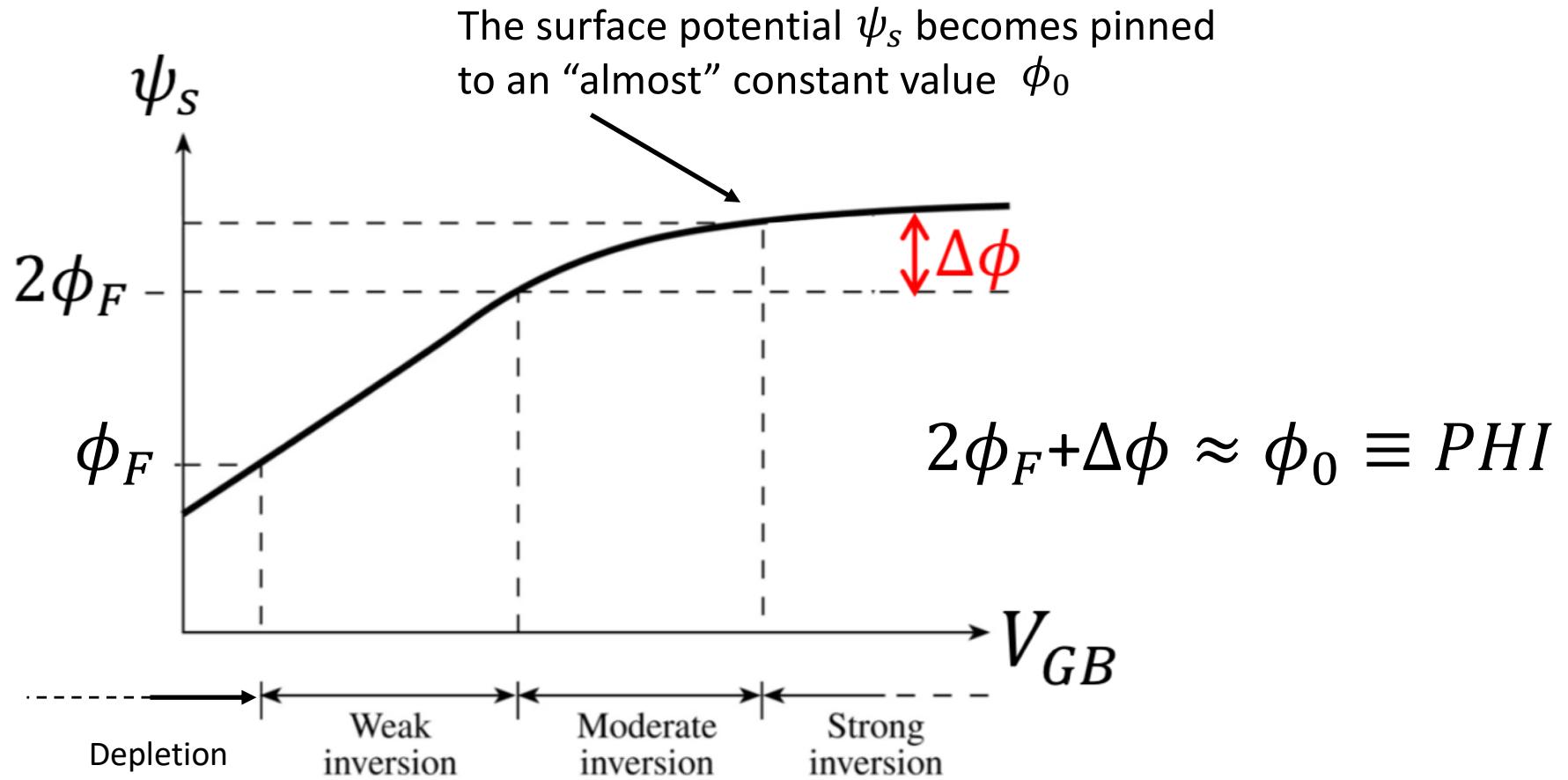
$$\psi_s = 2\phi_F$$

$$V_{GB} = V_{FB} + \psi_s + \psi_{ox} = V_{FB} + 2\phi_F + \underbrace{\frac{\sqrt{qN_A 2\epsilon_s 2\phi_F}}{C'_{ox}}}_{= \psi_{ox}} \equiv V_{t0}$$

$$V_{t0} \equiv V_{FB} + 2\phi_F + \underbrace{\frac{\sqrt{qN_A 2\epsilon_s}}{C'_{ox}} \sqrt{2\phi_F}}_{\equiv \gamma}$$

# Strong Inversion

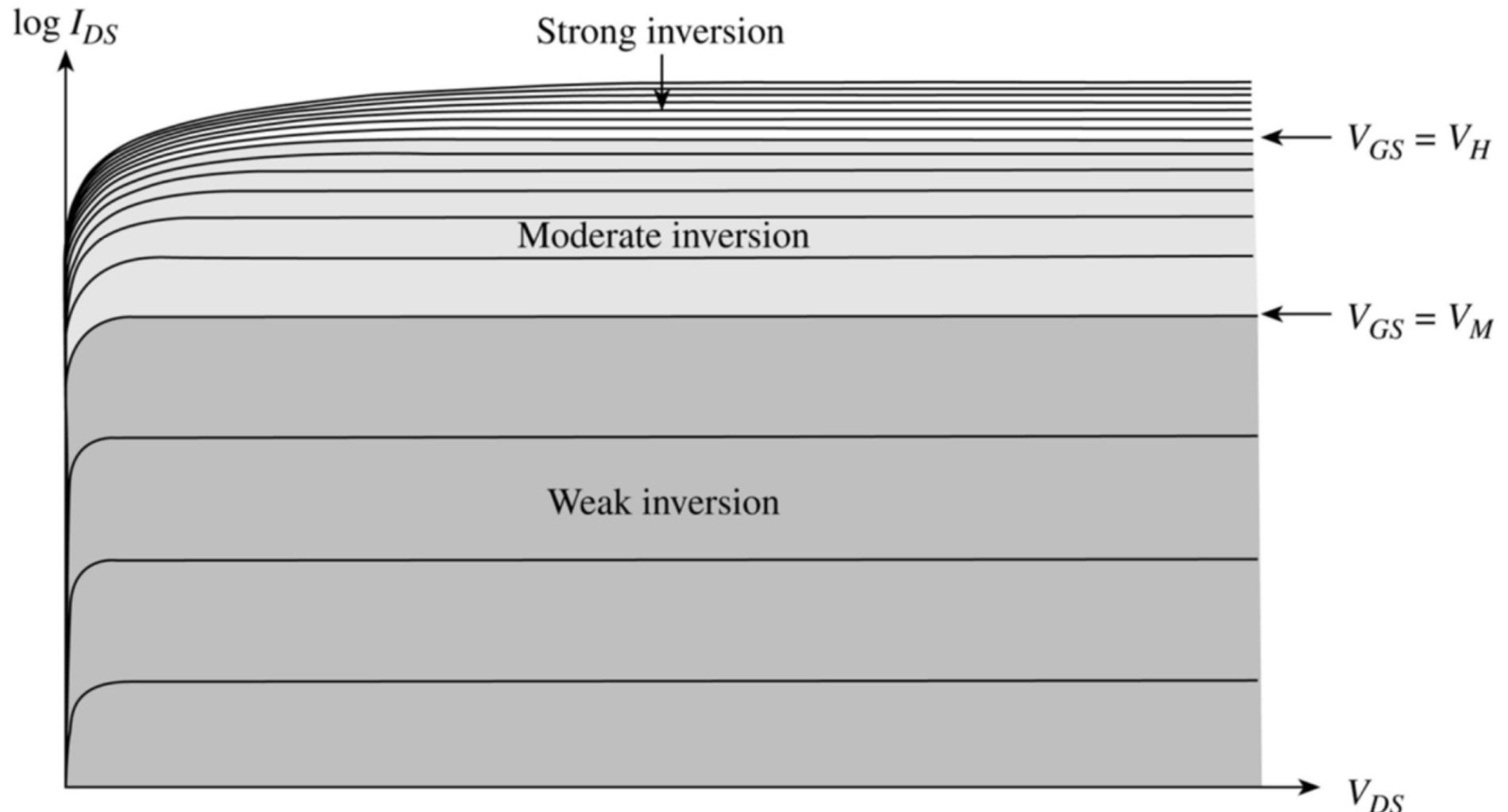
source: Tsividis



*Therefore, in all previous equations, just replace  $\psi_s$  with  $\phi_0$*

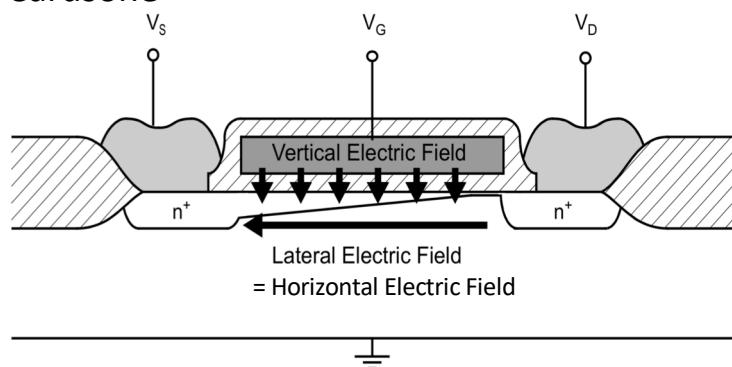
# Long Channel MOST

source: Tsividis

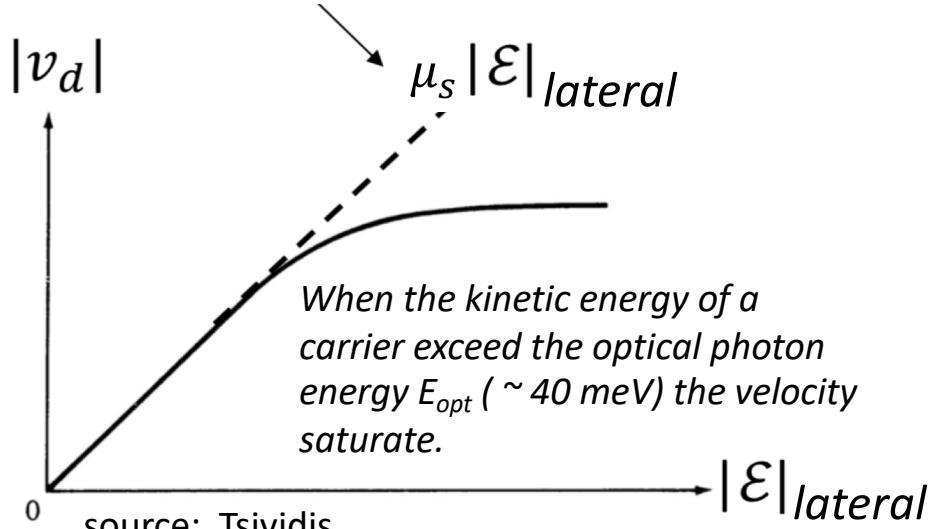


# Mobility issues (1)

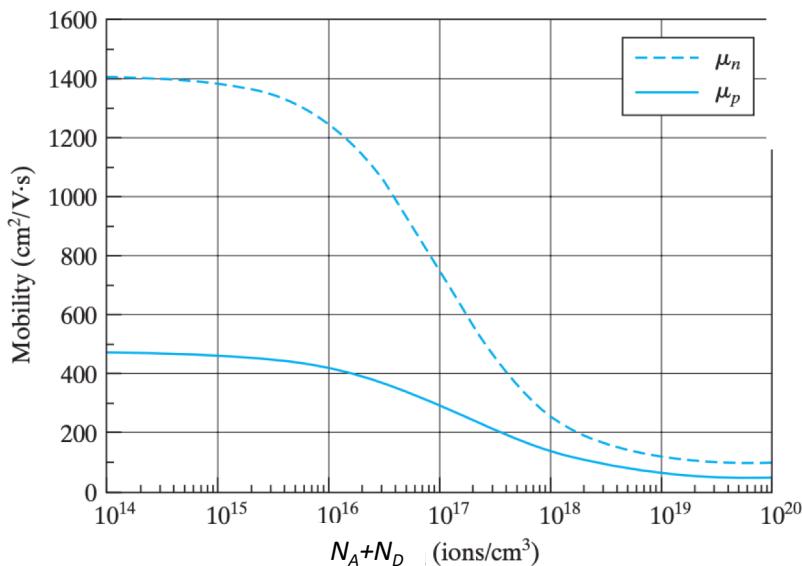
source: Carusone



$\mu_s$  = surface mobility of at “low-field”



source: Hu



source: Tsividis

$$v_{sat-holes} \approx 6 \times 10^6 \frac{\text{cm}}{\text{s}}$$

$$v_{sat-electrons} \approx 8 \times 10^6 \frac{\text{cm}}{\text{s}}$$

## Mobility Issues:

- Mobility degradation (vertical field)
- Velocity saturation (lateral field)

**FIGURE 2-5** The electron and hole mobilities of silicon at 300 K. At low dopant concentration, the electron mobility is dominated by phonon scattering; at high dopant concentration, it is dominated by impurity ion scattering. (After [3].)

# Mobility issues (2)

Mobility degradation from vertical field:

$$\mu_s = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)}$$

$\mu_0$  mobility with zero vertical field

$$\theta \propto \frac{1}{t_{ox}}$$

Velocity saturation from horizontal field:

$$v_d = \frac{\mu_s \mathcal{E}_{lateral}}{1 + \frac{\mathcal{E}_{lateral}}{\mathcal{E}_c}}$$

The critical electric field  $\mathcal{E}_c$  is defined as the field at which the drift velocity becomes  $v_{sat}/2$

- For  $\mathcal{E}_{lateral} \ll \mathcal{E}_c \Rightarrow v_d \approx \mu_s \mathcal{E}_{lateral}$
- For  $\mathcal{E}_{lateral} = \mathcal{E}_c \Rightarrow v_d = \frac{\mu_s \mathcal{E}_c}{2} = \frac{v_{sat}}{2}$
- For  $\mathcal{E}_{lateral} \gg \mathcal{E}_c \Rightarrow v_d \approx v_{sat}$

This behavior can also be modeled in terms of an effective mobility  $\mu_{eff}$   
 $\Rightarrow v_d = \mu_{eff} \mathcal{E}_{lateral}$

# Mobility issues (3)

$$\mu_{eff} = \frac{\mu_s}{1 + \alpha \varepsilon_{lateral}}$$

$$v_d = \mu_{eff} \varepsilon_{lateral} = \frac{\mu_s}{1 + \alpha \varepsilon_{lateral}} \varepsilon_{lateral}$$

Since for  $\varepsilon_{lateral} \rightarrow \infty \Rightarrow v_d \approx v_{sat} \leftrightarrow \alpha = \mu_s/v_{sat} (= \frac{1}{\varepsilon_c})$

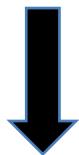
$$\mu_{eff} = \frac{\mu_s}{1 + \frac{\mu_s}{v_{sat}} \varepsilon_{lateral}}$$

To verify that it works substitute in the expression of  $v_d$ :

$$v_d = \frac{\mu_s}{1 + \frac{\mu_s}{v_{sat}} \varepsilon_{lateral}} \varepsilon_{lateral} = \frac{\mu_s}{1 + \varepsilon_{lateral}/\varepsilon_c} \varepsilon_{lateral}$$

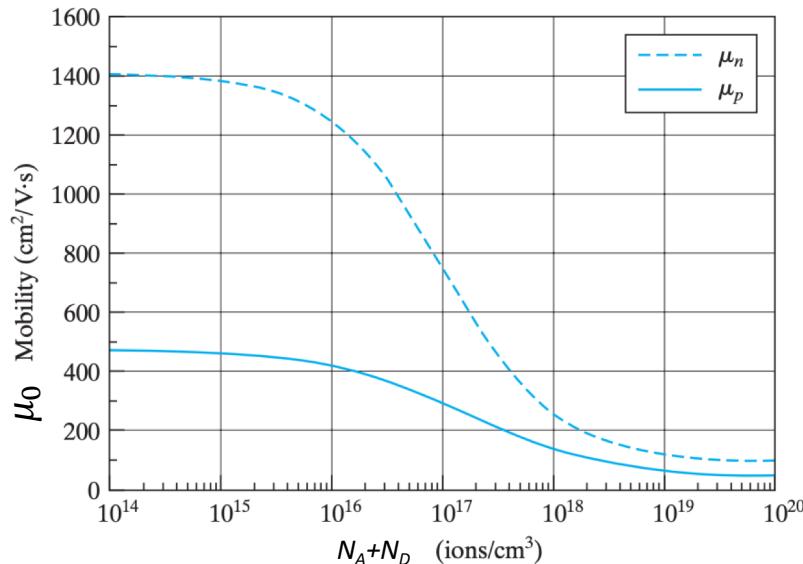
- For  $\varepsilon_{lateral} \ll \varepsilon_c = \frac{v_{sat}}{\mu_s} \Rightarrow v_d \approx \mu_s \varepsilon_{lateral}$
- For  $\varepsilon_{lateral} = \varepsilon_c \Rightarrow v_d = \frac{v_{sat}}{2}$
- For  $\varepsilon_{lateral} \gg \varepsilon_c \Rightarrow v_d \approx v_{sat}$

# Mobility issues (4)



*Finally, putting all together:*

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_T) + \frac{\mu_0}{v_{sat}} \epsilon_{lateral}}$$



**FIGURE 2–5** The electron and hole mobilities of silicon at 300 K. At low dopant concentration, the electron mobility is dominated by phonon scattering; at high dopant concentration, it is dominated by impurity ion scattering. (After [3].)

# Semiconductor Theory: References

