

Systematic Design of Analog CMOS Circuits with LUTs using open-source tools and PDKs

Part II (d)

LVS using magic VLSI and netgen

2025.11

Create the following script **lvs**:

```
/foss/designs/gf180-2025/ring > cat lvs
#!/usr/bin/env python3
import os, sys

if len(sys.argv) != 3:
    print(' LVS: you must specify two netlist filenames to compare! ')
    sys.exit(1)

os.system('netgen -batch lvs {} {} \
/foss/pdks/gf180mcuD/libs.tech/netgen/gf180mcuD_setup.tcl'.format(sys.argv[1], sys.argv[2]))
sys.exit(0);
```

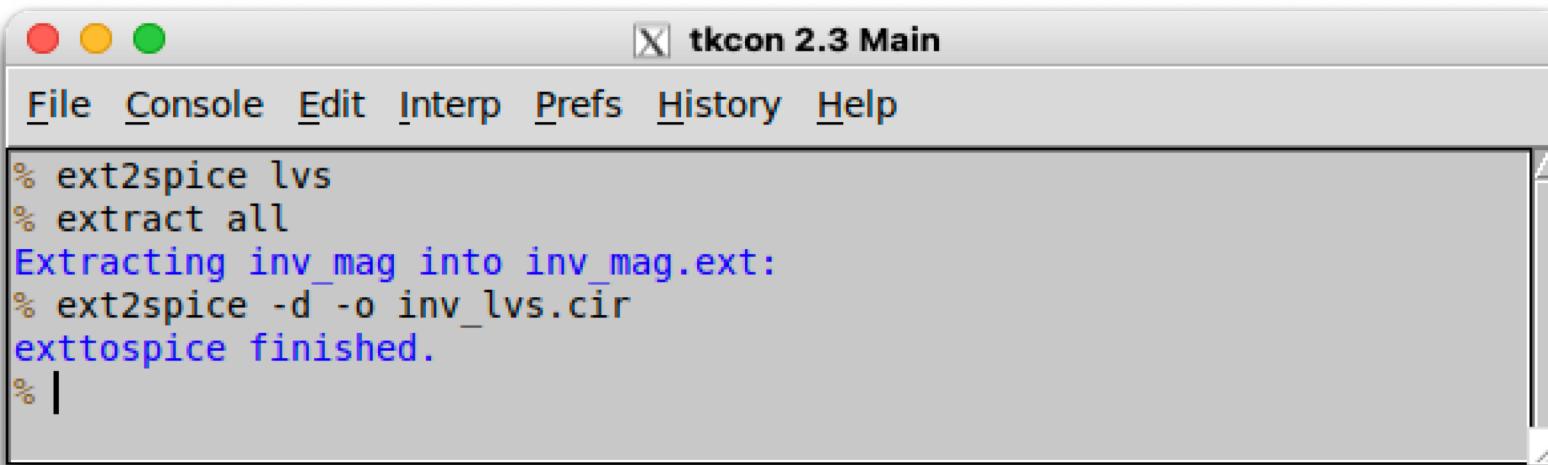
Make the script **lvs** executable:

```
/foss/designs/gf180-2025/ring > chmod ug+x lvs
```

LVS using magic VLSI and netgen

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```
/foss/designs/gf180-2025/ring > magic inv_mag.mag
```



The screenshot shows a terminal window titled "tkcon 2.3 Main". The window has standard OS X-style red, yellow, and green close buttons at the top left. The menu bar includes "File", "Console", "Edit", "Interp", "Prefs", "History", and "Help". The main text area contains the following command-line session:

```
% ext2spice lvs
% extract all
Extracting inv_mag into inv_mag.ext:
% ext2spice -d -o inv_lvs.cir
exttospice finished.
%
```

```
/foss/designs/gf180-2025/ring > cat inv_lvs.cir
* NGSPICE file created from inv_mag.ext - technology: gf180mcuD

.subckt inv_mag vo vi vss vdd
X0 vo vi vdd vdd pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
X1 vo vi vss vss nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
.ends
```

Tweaking the layout's netlist

```
/foss/designs/gf180-2025/ring > cat inv_lvs.cir
* NGSPICE file created from inv_mag.ext - technology: gf180mcuD

*****.subckt inv_mag vo vi vss vdd
M0 vo vi vdd vdd pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
M1 vo vi vss vss nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
*****.ends
```

Tweaking the schematic's netlist

```
/foss/designs/gf180-2025/ring > cat inv.spice
** sch_path: /foss/designs/gf180-2025/ring/inv.sch
.subckt inv vdd vi vo vss
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
.ends
```

```
/foss/designs/gf180-2025/ring > cp inv.spice inv.cir
```

Modify `inv.cir` as follows:

```
/foss/designs/gf180-2025/ring > cat inv.cir
** sch_path: /foss/designs/gf180-2025/ring/inv.sch
*****.subckt inv vdd vi vo vss
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
*****.ends
```

Comparing the netlists

2025.11

```
/foss/designs/gf180-2025/ring > ./lvs inv_lvs.cir inv.cir
```

```
/foss/designs/gf180-2025/ring > cat comp.out
```

Subcircuit summary:

Circuit 1: inv_lvs.cir

pfet_03v3 (1)

nfet_03v3 (1)

Number of devices: 2

Number of nets: 4

Circuit 2: inv.cir

pfet_03v3 (1)

nfet_03v3 (1)

Number of devices: 2

Number of nets: 4

Netlists match uniquely.

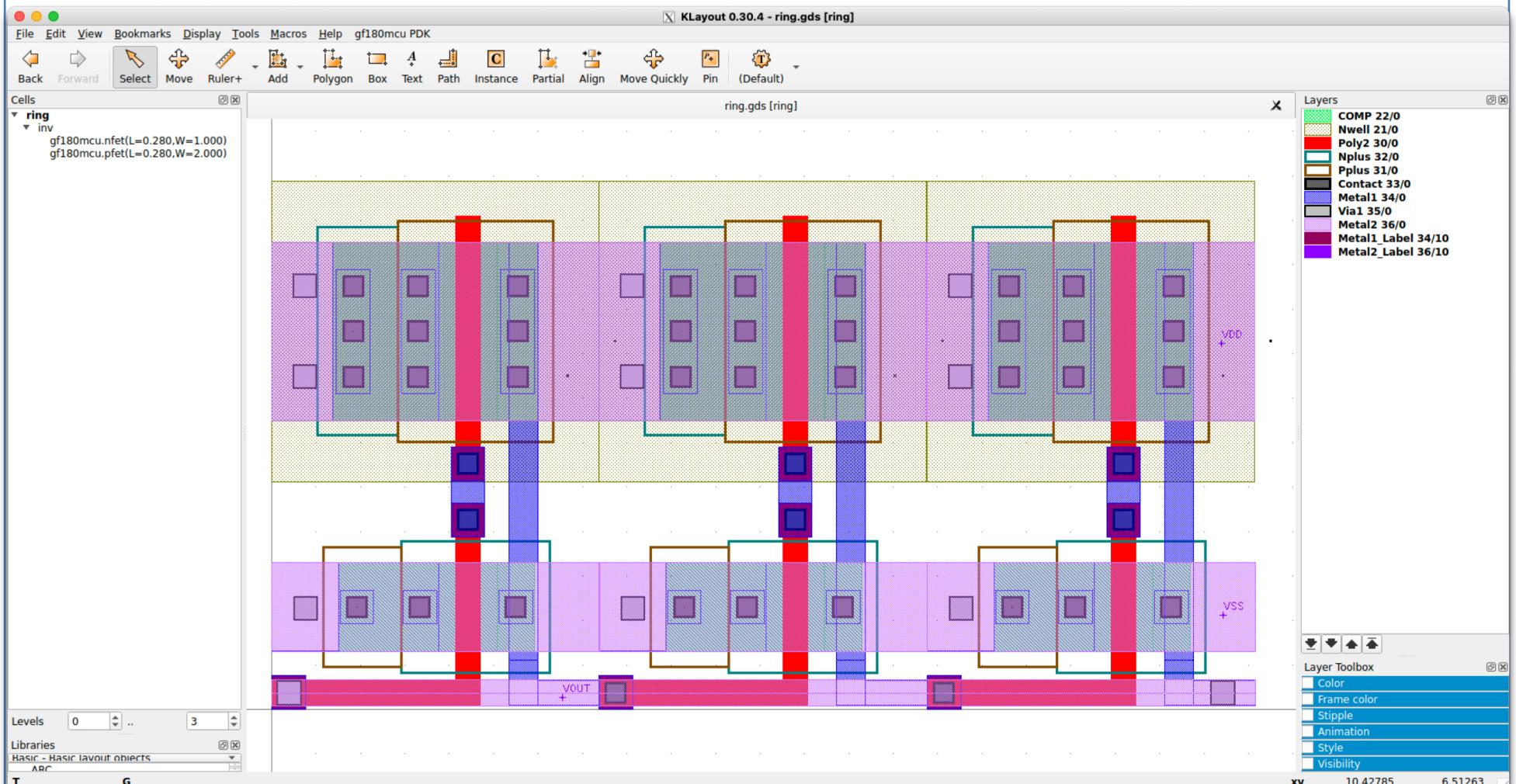
Cells have no pins; pin matching not needed.

Device classes inv_lvs.cir and inv.cir are equivalent.

Final result: Circuits match uniquely.

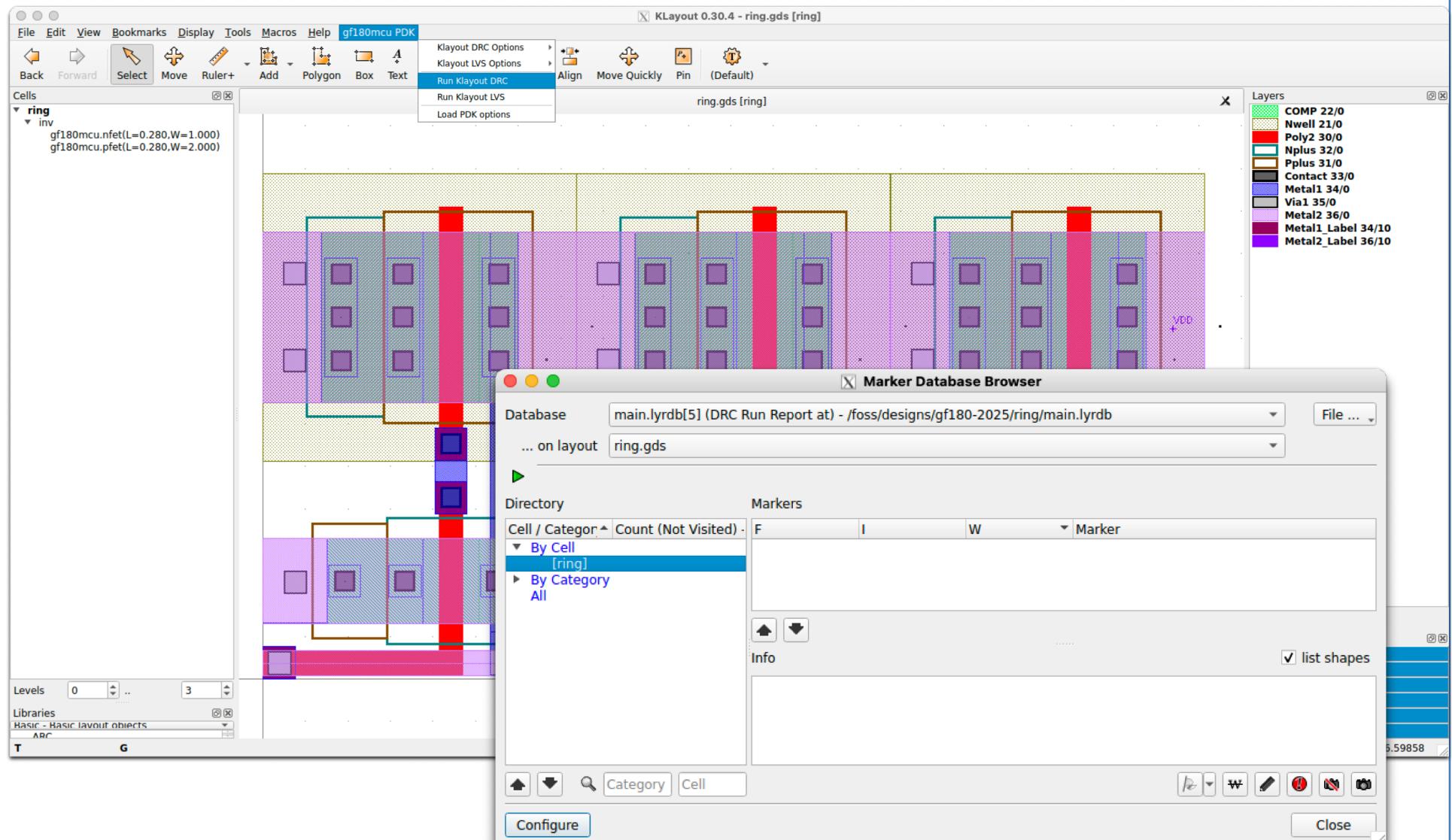
2025.09

Hierarchical Layout using klayout



2025.09

DRC with KLayout

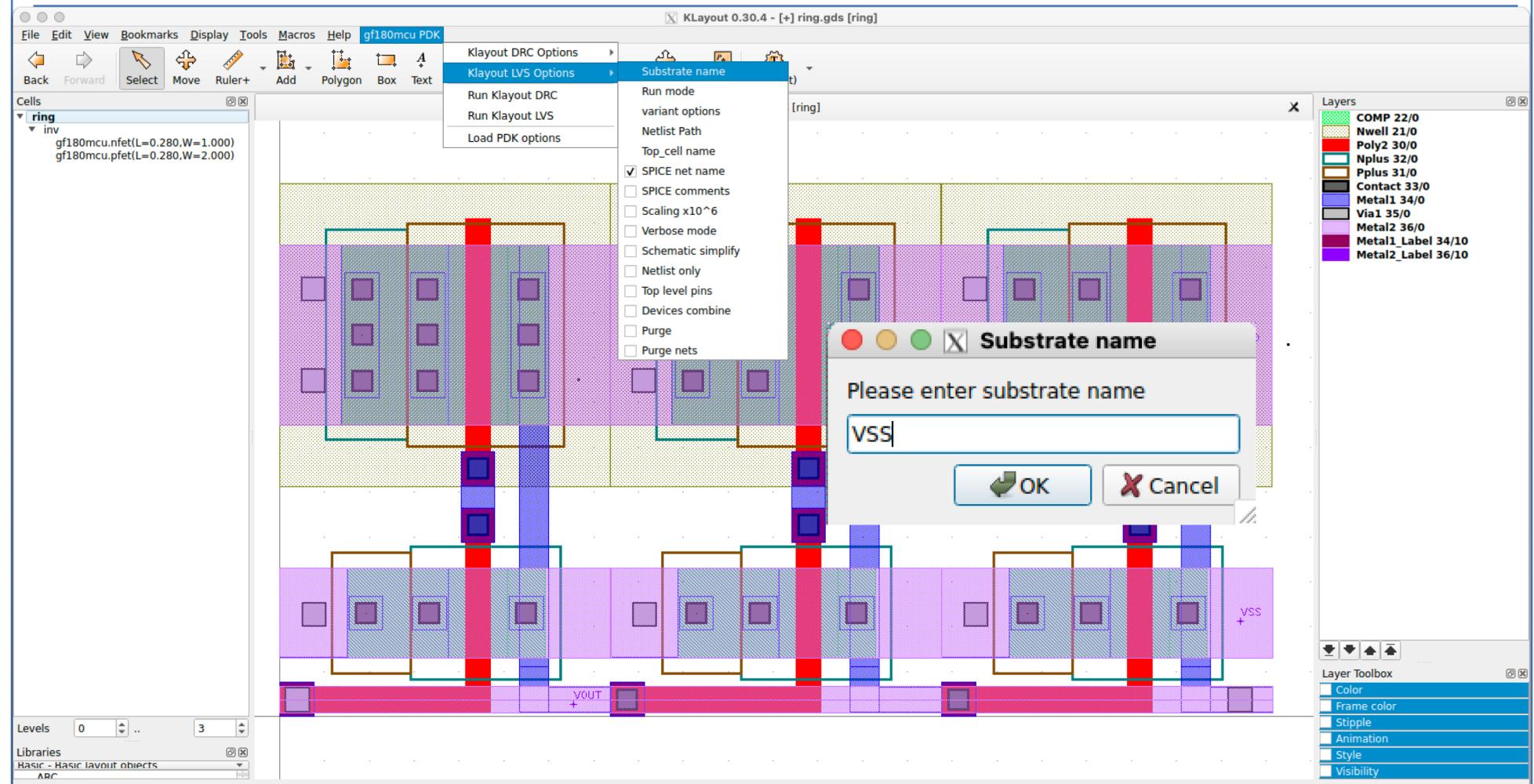


claudio talarico

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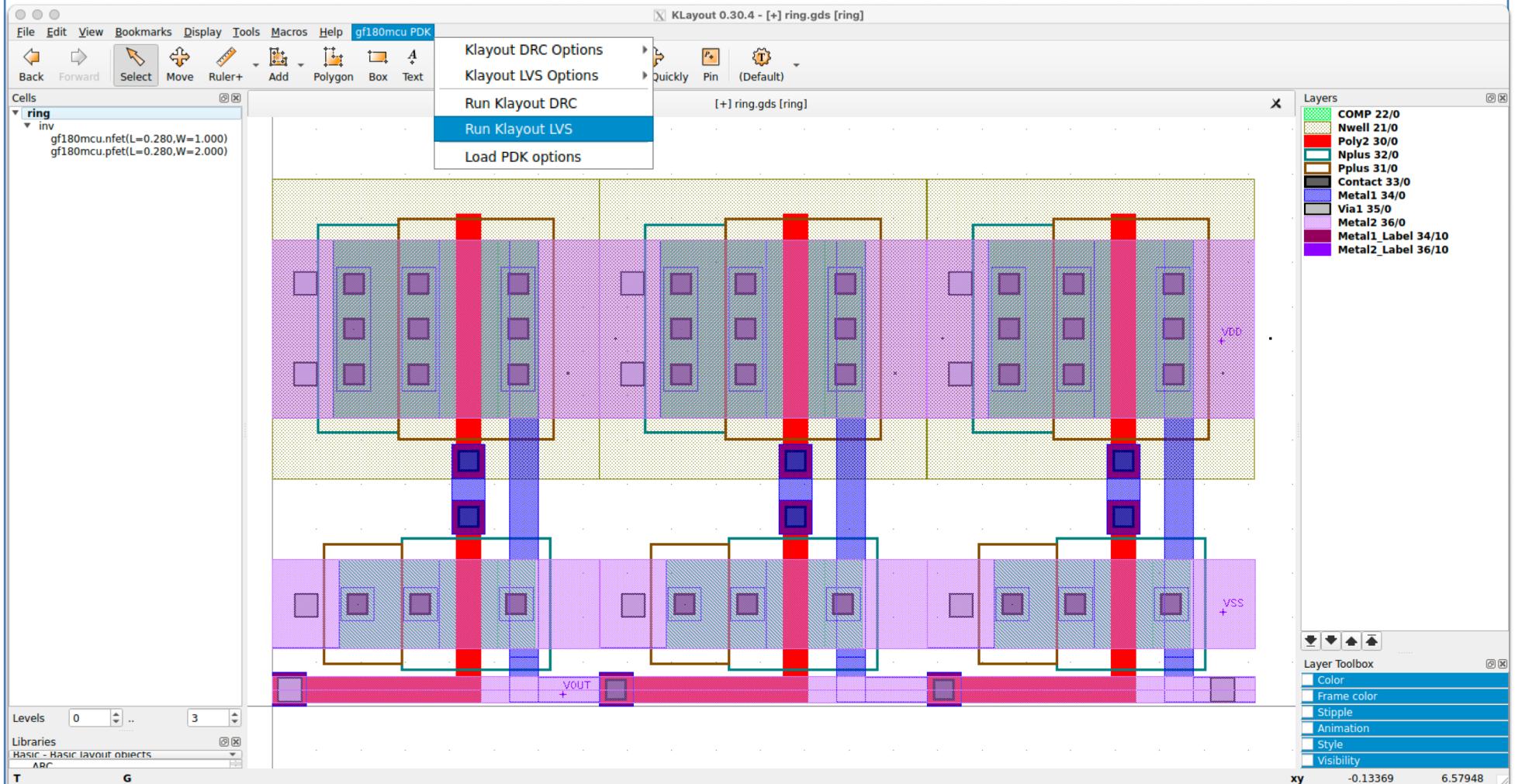
2025.09

LVS with klayout



2025.09

LVS with KLayout



Netlist Database Browser

Netlist LVS
... on layout ring.gds

Find text ...

Netlist Schematic Cross Reference Log

Circuits ring ↔ RII

Objects	Layout	Reference
ring ↔ RING	ring	RING
↳ Pins		
↳ VDD	VDD (7)	VDD (7)
↳ VOUT	VOUT (5)	VOUT (5)
↳ VSS	VSS (7)	VSS (7)
↑ Nets		
↑ \$2 ↔ NET1	\$2 (4)	NET1 (4)
↑ \$3 ↔ NET2	\$3 (4)	NET2 (4)
↑ VDD	VDD (7)	VDD (7)
↑ VOUT	VOUT (5)	VOUT (5)
↑ VSS	VSS (7)	VSS (7)
↳ Devices		
↳ nfet_03v3	\$4 / nfet_03v3 [L=0.28, 'INV1.1 / NFET_03V3 [L=0.28, W=1]	
↳ nfet_03v3	\$5 / nfet_03v3 [L=0.28, 'INV2.1 / NFET_03V3 [L=0.28, W=1]	
↳ nfet_03v3	\$6 / nfet_03v3 [L=0.28, 'INV3.1 / NFET_03V3 [L=0.28, W=1]	
↳ pfet_03v3	\$1 / pfet_03v3 [L=0.28, 'INV1.2 / PFET_03V3 [L=0.28, W=2]	
↳ pfet_03v3	\$2 / pfet_03v3 [L=0.28, 'INV2.2 / PFET_03V3 [L=0.28, W=2]	
↳ pfet_03v3	\$3 / pfet_03v3 [L=0.28, 'INV3.2 / PFET_03V3 [L=0.28, W=2]	

Configure Probe Net Lock Close

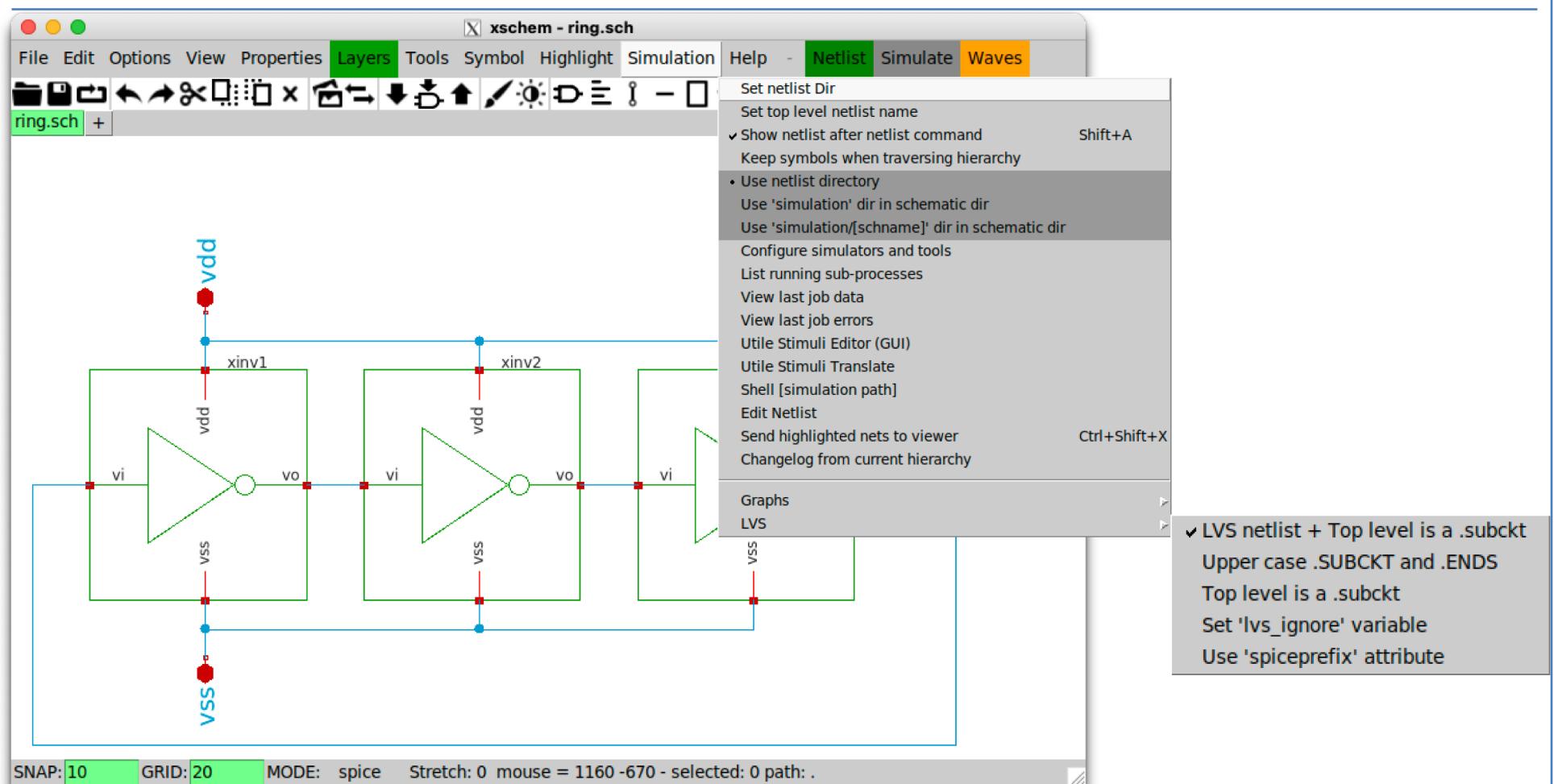
Netlist extracted from the Layout

```
/foss/designs/gf180-2025/ring > cat ring_extracted.cir
* Extracted by KLayout with GF180MCU LVS runset on : 18/12/2025 19:06

.SUBCKT ring VOUT VSS VDD
M$1 \$2 VOUT VDD VDD pfet_03v3 L=0.28U W=2U AS=1.3P AD=1.3P PS=5.3U PD=5.3U
M$2 \$3 \$2 VDD VDD pfet_03v3 L=0.28U W=2U AS=1.3P AD=1.3P PS=5.3U PD=5.3U
M$3 VOUT \$3 VDD VDD pfet_03v3 L=0.28U W=2U AS=1.3P AD=1.3P PS=5.3U PD=5.3U
M$4 \$2 VOUT VSS VSS nfet_03v3 L=0.28U W=1U AS=0.61P AD=0.61P PS=3.22U PD=3.22U
M$5 \$3 \$2 VSS VSS nfet_03v3 L=0.28U W=1U AS=0.61P AD=0.61P PS=3.22U PD=3.22U
M$6 VOUT \$3 VSS VSS nfet_03v3 L=0.28U W=1U AS=0.61P AD=0.61P PS=3.22U PD=3.22U
.ENDS ring
```

Netlist extracted from the Schematic

```
/foss/designs/gf180-2025/ring > xschem ring.sch
```



Netlist extracted from the Schematic

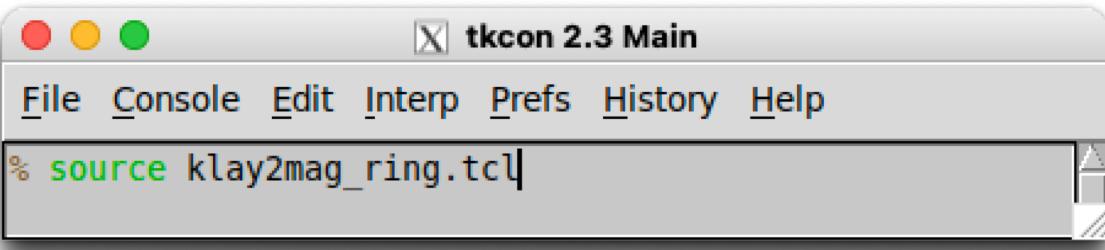
```
/foss/designs/gf180-2025/ring > cat ring.spice
** sch_path: /foss/designs/gf180-2025/ring/ring.sch
.subckt ring vdd vout vss
*.PININFO vdd:B vss:B vout:0
xinv1 vdd vout net1 vss inv
xinv2 vdd net1 net2 vss inv
xinv3 vdd net2 vout vss inv
.ends

* expanding symbol: inv.sym # of pins=4
** sym_path: /foss/designs/gf180-2025/ring/inv.sym
** sch_path: /foss/designs/gf180-2025/ring/inv.sch
.subckt inv vdd vi vo vss
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
.ends
```

NOTE: the order of the pins in the top-level subckt is not the same as in the netlist extracted from the layout though KLayout

LVS using netgen and magic

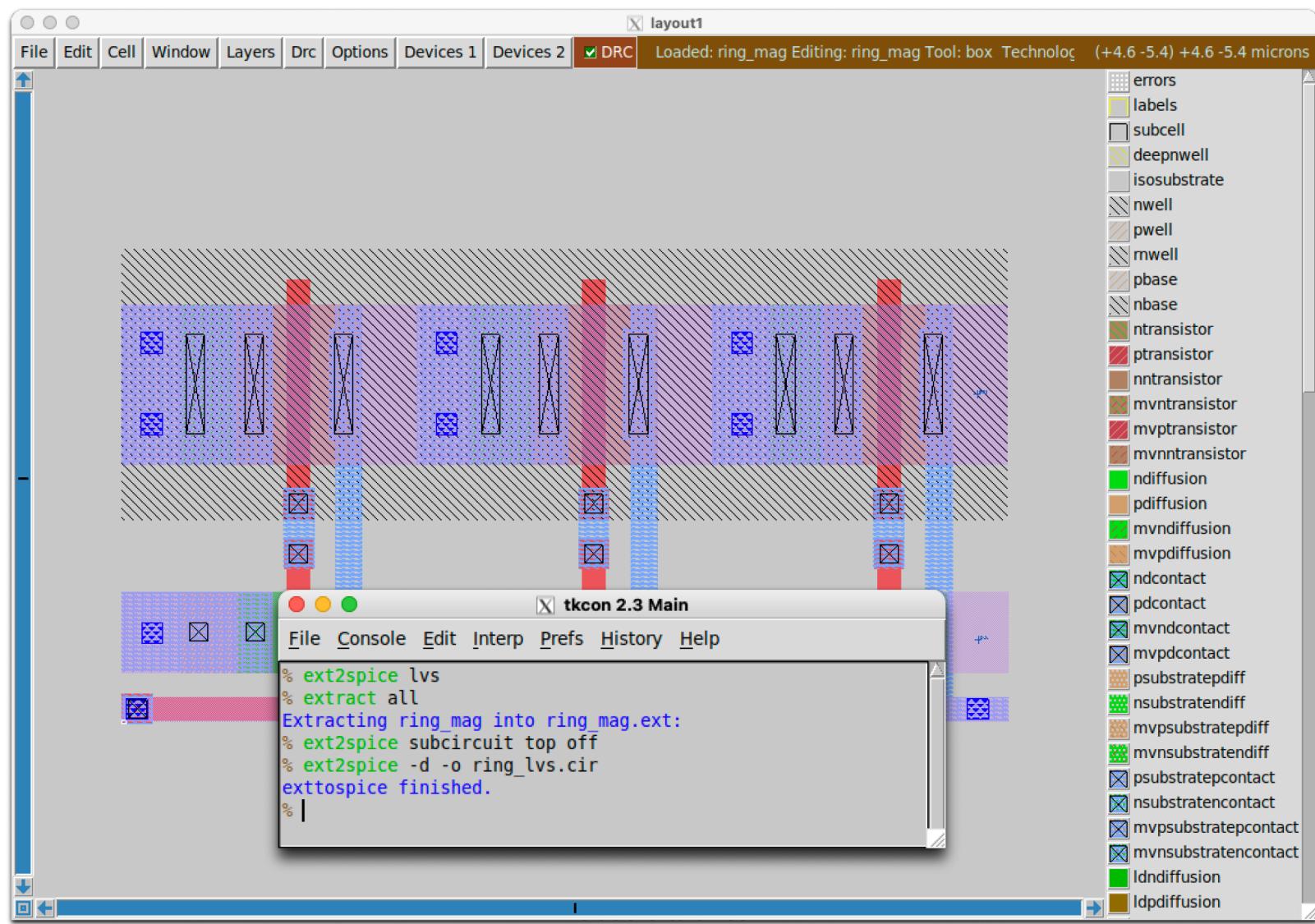
```
/foss/designs/gf180-2025/ring > magic
```



```
/foss/designs/gf180-2025/ring > cat klay2mag_ring.tcl
# klay2mag_ring.tcl
grid 0.005u 0.005u
snap user
gds read ring.gds
load ring
select top cell
expand
flatten ring_mag
load ring_mag
select top cell
cellname create ring_mag
save ring_mag.mag
quit -noprompt
```

LVS using netgen and magic

```
/foss/designs/gf180-2025/ring > magic ring_mag.mag
```



Netlist extracted from the layout using magic

```
/foss/designs/gf180-2025/ring > cat ring_lvs.cir
* NGSPICE file created from ring_mag.ext - technology: gf180mcuD

.subckt ring_mag VDD VOUT VSS
X0 VOUT a_1208_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
X1 a_1208_130# a_470_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
X2 a_1208_130# a_470_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
X3 a_470_130# VOUT VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
X4 VOUT a_1208_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
X5 a_470_130# VOUT VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
.ends
```

Tweaking ring_lvs.cir

```
/foss/designs/gf180-2025/ring > cat ring_lvs.cir
* NGSPICE file created from ring_mag.ext - technology: gf180mcuD

*****.subckt ring_mag VDD VOUT VSS
MX0 VOUT a_1208_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
MX1 a_1208_130# a_470_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
MX2 a_1208_130# a_470_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
MX3 a_470_130# VOUT VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
MX4 VOUT a_1208_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
**devattr s=52000,1060 d=52000,1060
MX5 a_470_130# VOUT VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
**devattr s=24400,644 d=24400,644
*****.ends
```

Tweaking the netlist extracted from the schematic

```
/foss/designs/gf180-2025/ring > cat ring.spice
** sch_path: /foss/designs/gf180-2025/ring/ring.sch
.subckt ring vdd vout vss
*.PININFO vdd:B vss:B vout:0
xinv1 vdd vout net1 vss inv
xinv2 vdd net1 net2 vss inv
xinv3 vdd net2 vout vss inv
.ends

* expanding symbol: inv.sym # of pins=4
** sym_path: /foss/designs/gf180-2025/ring/inv.sym
** sch_path: /foss/designs/gf180-2025/ring/inv.sch
.subckt inv vdd vi vo vss
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
.ends
```

```
/foss/designs/gf180-2025/ring > cp ring.spice ring.cir
```

Tweaking the netlist extracted from the schematic

- Modify `ring.cir` as follows:

```
/foss/designs/gf180-2025/ring > cat ring.cir
** sch_path: /foss/designs/gf180-2025/ring/ring.sch
*****.subckt ring vdd vout vss
*.PININFO vdd:B vss:B vout:0
xinv1 vdd vout net1 vss inv
xinv2 vdd net1 net2 vss inv
xinv3 vdd net2 vout vss inv
*****.ends

* expanding symbol: inv.sym # of pins=4
** sym_path: /foss/designs/gf180-2025/ring/inv.sym
** sch_path: /foss/designs/gf180-2025/ring/inv.sch
.subckt inv vdd vi vo vss
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
.ends
```

Comparing the netlists

```
/foss/designs/gf180-2025/ring > ./lvs ring.cir ring_lvs.cir
```

```
/foss/designs/gf180-2025/ring > cat comp.out
Flattening unmatched subcell inv in circuit ring.cir (0)(3 instances)
```

Subcircuit summary:

Circuit 1: ring.cir

nfet_03v3 (3)

pfet_03v3 (3)

Number of devices: 6

Number of nets: 5

Circuit 2: ring_lvs.cir

nfet_03v3 (3)

pfet_03v3 (3)

Number of devices: 6

Number of nets: 5

Resolving symmetries by property value.

Resolving symmetries by pin name.

Resolving symmetries by net name.

Netlists match with 3 symmetries.

Cells have no pins; pin matching not needed.

Device classes ring.cir and ring_lvs.cir are equivalent.

Final result: Circuits match uniquely.

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PEX (parasitic extraction)

- The IIC_OSIC_TOOLS echo system provides a script to extract parasitic using magic

```
/foss/designs/gf180-2025 > sak-pex.sh
```

PEX script using Magic-VLSI (DIC@JKU)

```
Usage: /foss/tools/sak/sak-pex.sh [-d] [-m mode] [-s mode] [-n <subcktname>] [-w <workdir>] <cellname>
```

```
-m Select PEX mode (1 = C-decoupled, 2 = C-coupled [default], 3 = full-RC)
-s Subcircuit definition in PEX netlist (1 = include subcircuit definition [default], 0 = no subcircuit)
-n name of PEX subcircuit (default is <cellname>)
-w Set <workdir> working directory
-d Enable debug information
```

Running the pex script

```
/foss/designs/gf180-2025/ring > sak-pex.sh -d -s 1 -m 1 -w results ring
```

```
/foss/designs/gf180-2025/ring > cat results/pex_ring.tcl
crashbackups stop
drc off
gds read ring.gds
load ring
select top cell
flatten ring_flat
load ring_flat
cellname delete ring
cellname rename ring_flat ring
select top cell
extract path /foss/designs/gf180-2025/ring/results
ext2spice lvs
extract no coupling
ext2spice cthresh 0.01
ext2spice -p /foss/designs/gf180-2025/ring/results -o /foss/designs/gf180-2025/ring/results/ring.pex.spice.tmp
quit -noprompt
```

The pex netlist

```
/foss/designs/gf180-2025/ring > cp results/ring.pex.spice ring.pex.spc
```

```
/foss/designs/gf180-2025/ring > cat ring.pex.spc
* PEX produced on Thu Dec 18 11:01:03 PM CET 2025 using
* /foss/tools/sak/iic-pex.sh with m=1 and s=1
* NGSPICE file created from ring.ext - technology: gf180mcuD

.subckt ring VDD VOUT VSS
X0 VOUT a_1208_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
X1 a_1208_130# a_470_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X2 a_1208_130# a_470_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
X3 a_470_130# VOUT VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X4 VOUT a_1208_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X5 a_470_130# VOUT VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
C0 VOUT VSS 2.28632f
C1 VDD VSS 6.94136f
C2 a_1208_130# VSS 1.45559f
C3 a_470_130# VSS 1.45559f
.ends
```

Modify the pex netlist

- Modify the name of the subcircuit in the ring.pex.spc netlist as follows:

```
* PEX produced on Thu Dec 18 11:01:03 PM CET 2025 using
* /foss/tools/sak/iic-pex.sh with m=1 and s=1
* NGSPICE file created from ring.ext - technology: gf180mcuD

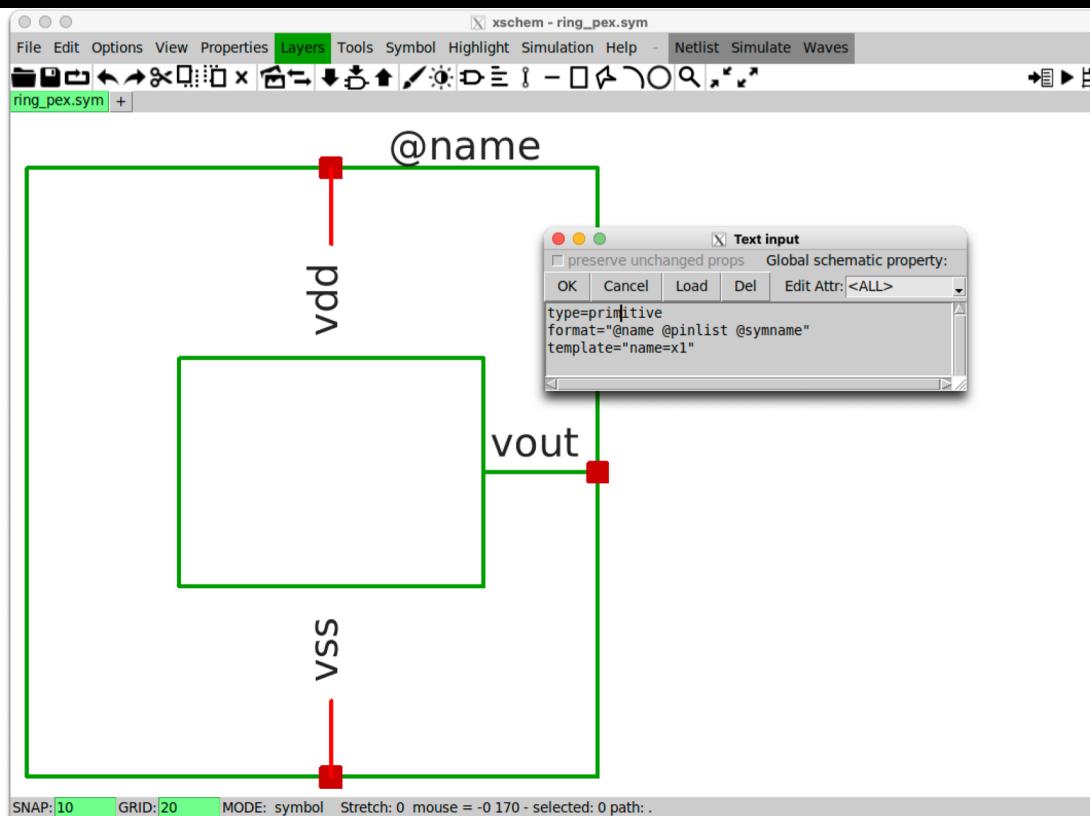
.subckt ring_pex VDD VOUT VSS
X0 VOUT a_1208_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
X1 a_1208_130# a_470_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X2 a_1208_130# a_470_130# VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
X3 a_470_130# VOUT VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X4 VOUT a_1208_130# VDD VDD pfet_03v3 ad=1.3p pd=5.3u as=1.3p ps=5.3u w=2u l=0.28u
X5 a_470_130# VOUT VSS VSS nfet_03v3 ad=0.61p pd=3.22u as=0.61p ps=3.22u w=1u l=0.28u
C0 VOUT VSS 2.28632f
C1 VDD VSS 6.94136f
C2 a_1208_130# VSS 1.45559f
C3 a_470_130# VSS 1.45559f
.ends
```

Post-Layout Simulation

- Create a symbol for the post-layout simulation
- Open the symbol and change the type from **subcircuit** to **primitive**

```
/foss/designs/gf180-2025/ring > cp ring.sym ring_pex.sym
```

```
/foss/designs/gf180-2025/ring > xschem ring_pex.sym
```



Post-Layout Simulation

```
/foss/designs/gf180-2025/ring > cp ring_tb.sch ring_pex_tb.sch
```

- Open and Edit the post-layout testbench as follows:

The screenshot shows the xschem software interface with the file "ring_pex_tb.sch" open. The top menu bar includes File, Edit, Options, View, Properties, Layers (selected), Tools, Symbol, Highlight, Simulation, Help, Netlist, Simulate, and Waves. The left pane displays the SPICE netlist:

```
MODELS
.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064.ngspice typical

NGSPICE
.control
save all

** Define transient params
let fsig = 1e9
let tper = 1/fsig
let tstop = 3*tper
let tstep = 0.001*tper

** Simulations
tran $&tstep $&tstop

** Plots
setplot tran1
let vout = v(out)
meas tran tosc trig v(out) val=0.5*3.3 rise=4 TARG v(out) val=0.5*3.3 rise=5
plot vout

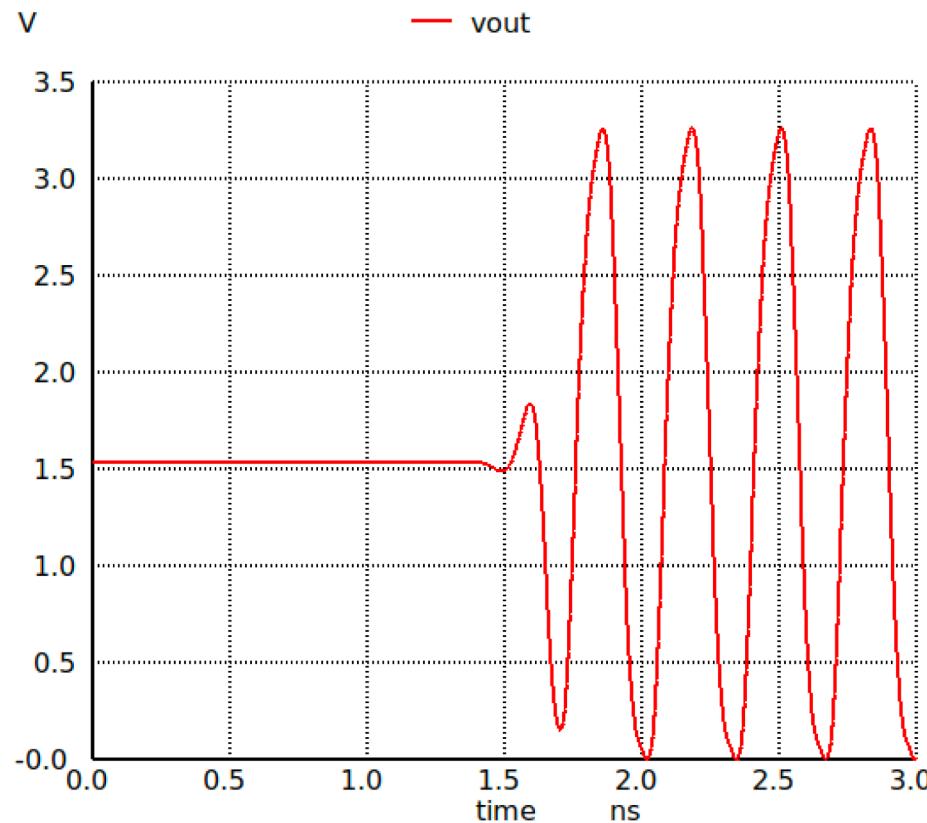
echo $plots
.endc

include
.inclu ./.ring.pex.spc
```

The right pane shows a schematic diagram of a ring oscillator. It consists of four NMOS transistors arranged in a square loop. The top transistor has its drain connected to the top node of the loop and its source connected to ground (GND). The bottom transistor has its drain connected to the bottom node of the loop and its source connected to VSS. The left transistor has its drain connected to the left node of the loop and its source connected to VDD. The right transistor has its drain connected to the right node of the loop and its source connected to GND. The output node of the rightmost transistor is labeled "out". A voltage source "V1" is connected between the top node and the bottom node, with its value set to 3.3. The top and bottom nodes are also connected to VDD and VSS respectively.

Make sure
to use the
ring_pex.sym

Post-Layout Simulation Result



Pre-Layout

$tosc = 2.376660e-10$ s

Post-Layout

$tosc = 3.252879e-10$ s