

# **Systematic Design of Analog CMOS Circuits with LUTs using open-source tools and PDKs**

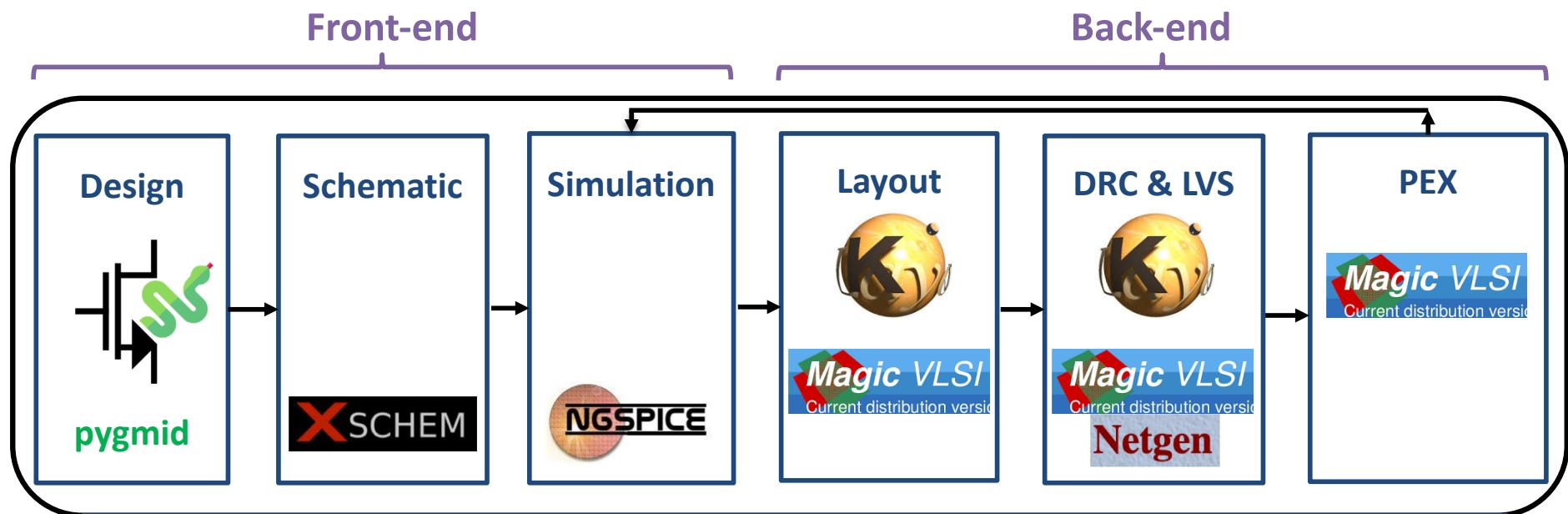
## **Part II (a)**

This presentation:

<https://github.com/claudiotalarico/workshop-analog-2025>

<https://github.com/claudiotalarico/workshop-analog-2025/tree/main/gf180-2025>

# Analog Flow



Tools ecosystem: IIC-OSIC-TOOLS **JYU**  
JOHANNES KEPLER  
UNIVERSITÄT LINZ

PDK: **GLOBAL FOUNDRIES**  
**gf180mcuD**

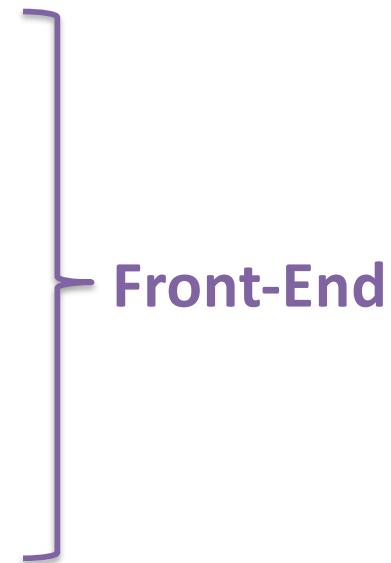
# What's next ?

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- Assumption:
  - We have a design that meets specs.
    - example: ring oscillator
- Goal:
  - Walk through all steps required to complete the analog flow

# Outline

- **Analog Flow**
  - Design ✓
  - Schematic - xschem
    - inv.sch, inv.sym
    - ring.sch, ring.sym ← Hierarchical
  - Simulation - xschem + ngspice
    - inv\_tb.sch
    - ring\_tb.sch
  - Generate schematic's netlists (for later to run LVS) – xschem + ngspice
    - inv.spice
    - ring.spice



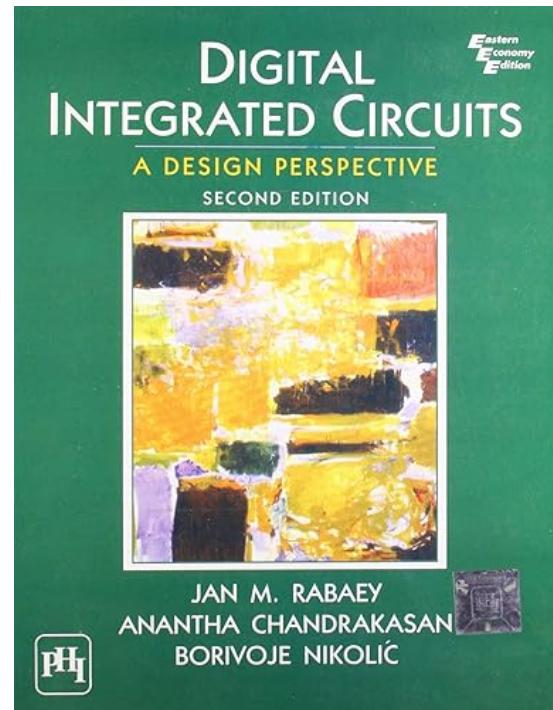
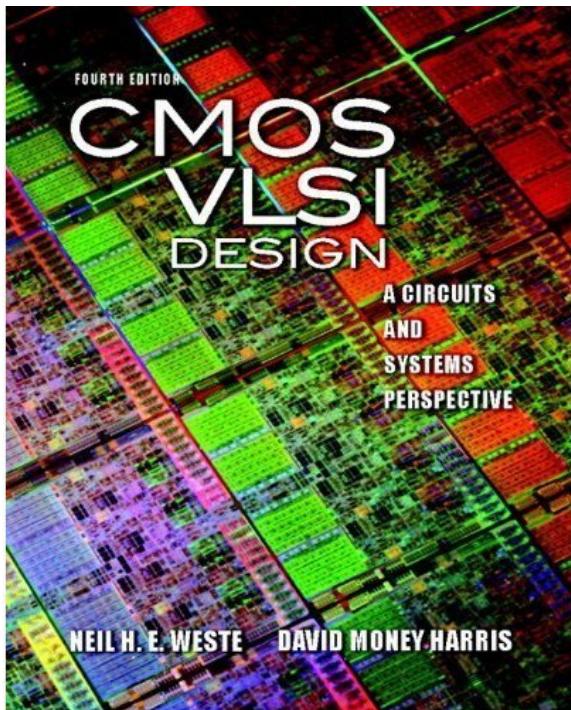
# Outline

- **Analog Flow**
  - **Layout**
    - with KLayout - inv.gds, ring.gds (hierarchical)
    - with magic VLSI (inv\_mag.mag, ring\_mag.mag)
  - **DRC**
    - with KLayout
    - with magic VLSI
  - **LVS**
    - with KLayout
      - inv.spice, inv\_extracted.cir
      - ring.spice, ring\_extracted.cir
    - with Netgen (tweak the netlists)
      - inv.cir, inv\_lvs.cir
      - ring.cir, ring\_lvs.cir
  - **PEX**
    - with magic VLSI (with IIC\_OSIC\_TOOLS script /foss/tools/sak/sak-pex.sh)
      - pex\_ring.tcl, ring.pex.spice (generated automatically running sak-pex.sh)
      - pex\_ct.tcl (edited manually and run through magic VLSI), ring.pex.spc
  - **Post-Layout simulation - xschem + ngspice**
    - ring\_pex.sym, tb\_ring\_pex.sch, ring.pex.spc

Back-End

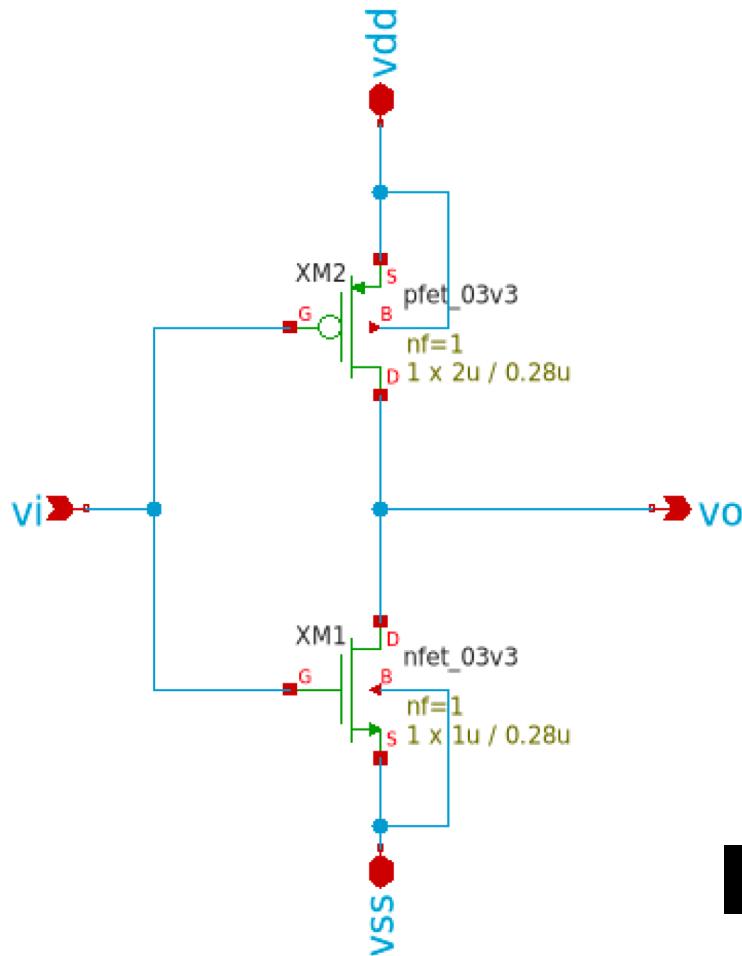
# References

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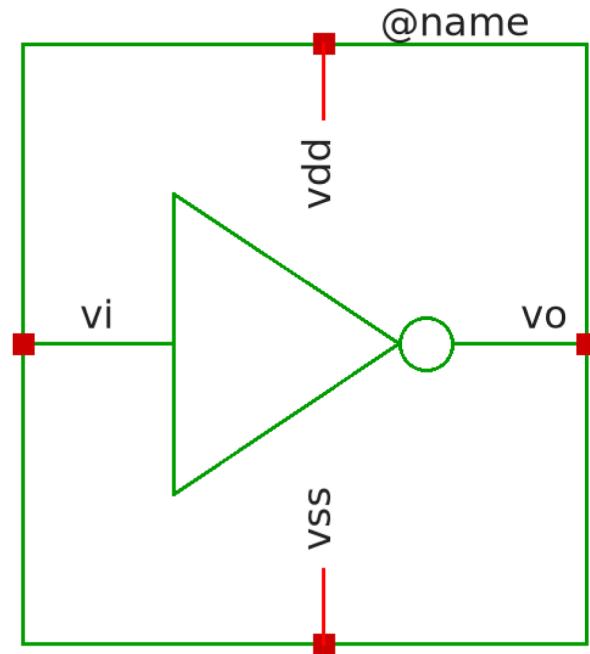
# Basic Building Block: The CMOS Inverter

Simple CMOS Inverter



source: M. Koefinger at

`/foss/examples/demo_gf180mcuD/ana >`



`/foss/designs/gf180-2025/ring > xschem inv.sym`

`/foss/designs/gf180-2025/ring > xschem inv.sch`

## NGSPICE

```
.control
save all

** Define input signal
* let fsig = 1e3 ; too slow
let fsig = 1e9
let tper = 1/fsig
let tfr = 0.01*tper
let ton = 0.5*tper-2*tfr
let tofs = tper

** Define transient params
let tstop = 4*tper
let tstep = 0.001*tper

** Set Sources
alter @VIN[DC] = 0.0
alter @VIN[PULSE] = [ 0 3.3 $&tofs $&tfr $&ton $&tper 0 ]

** Simulations
op
dc vin 0 3.3 0.01
tran $&tstep $&tstop

** Plots
setplot dc1
let vout = v(out)
let dvout = deriv(v(out))
plot v(in) vout
meas dc VSW find v(in) when v(out)=1.65
meas dc VIL find v(in) when dvout=-1 cross=1
meas dc VIH find v(in) when dvout=-1 cross=2
meas dc VOH find v(out) when dvout=-1 cross=1
meas dc VOL find v(out) when dvout=-1 cross=2

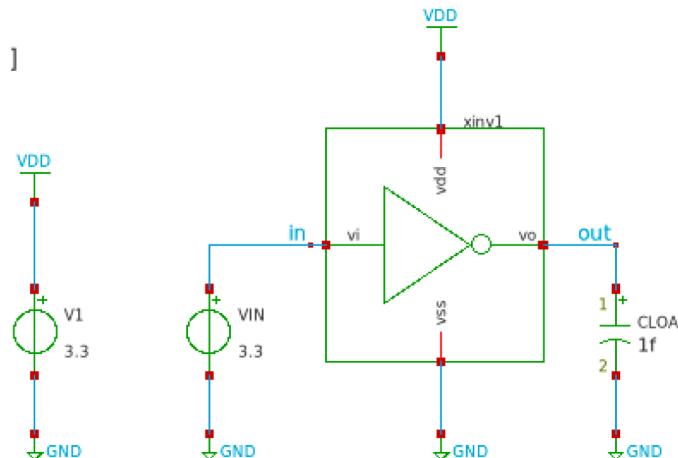
setplot tran1
let vout = v(out)
let vin = v(in)
let ivdd = -v1#branch*1e4
meas tran tpLH trig v(in) val=1.65 fall=2 TARG v(out) val=1.65 rise=2
meas tran tpHL trig v(in) val=1.65 rise=2 TARG v(out) val=1.65 fall=2
meas tran trise trig v(out) val=0.1*3.3 rise=2 TARG v(out) val=0.9*3.3 rise=2
meas tran tfall trig v(out) val=0.9*3.3 fall=2 TARG v(out) val=0.1*3.3 fall=2
plot ivdd
plot vin+4 vout

setplot op1
write inv_tb.raw
echo $plots
.endc
```

## MODELS

```
.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064.ngspice typical
```

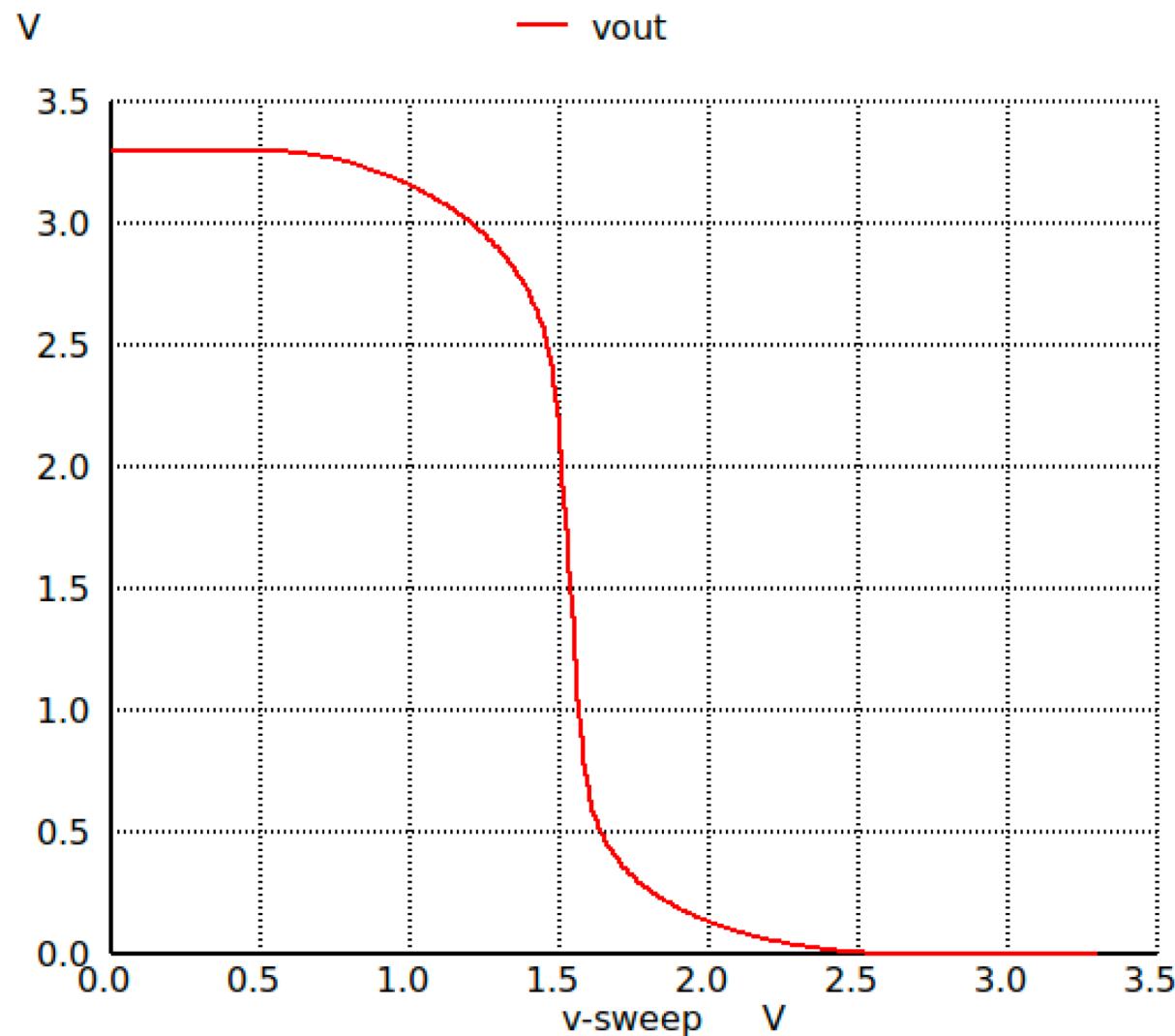
→ Annotate OP



Not a good setup for measuring the dynamic parameters

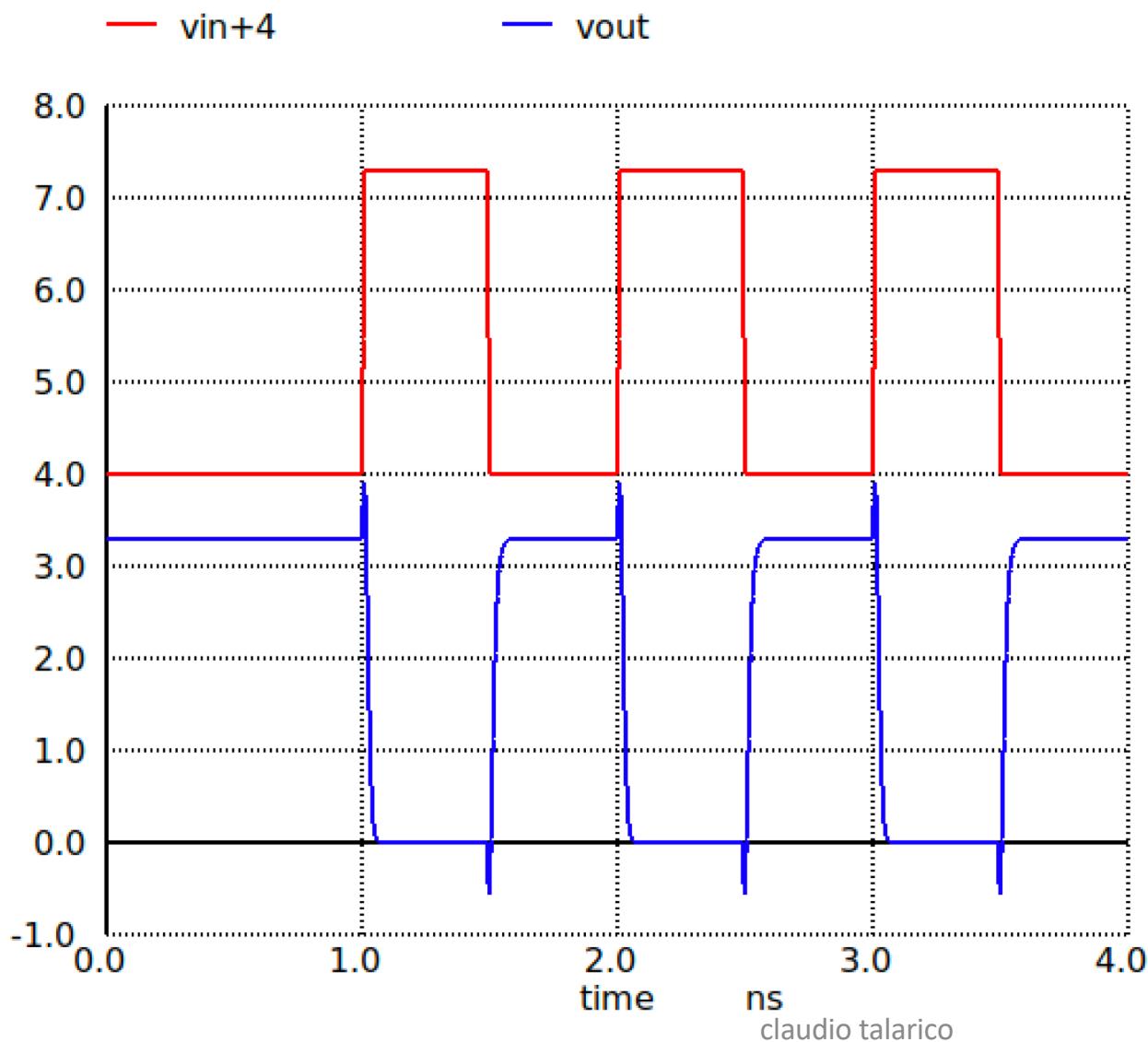
/foss/designs/gf180-2025/ring > xschem inv\_tb.sch

# DC Analysis



vsw = 1.525452e+00  
vil = 1.204496e+00  
vih = 1.775522e+00  
voh = 3.001193e+00  
vol = 2.865048e-01

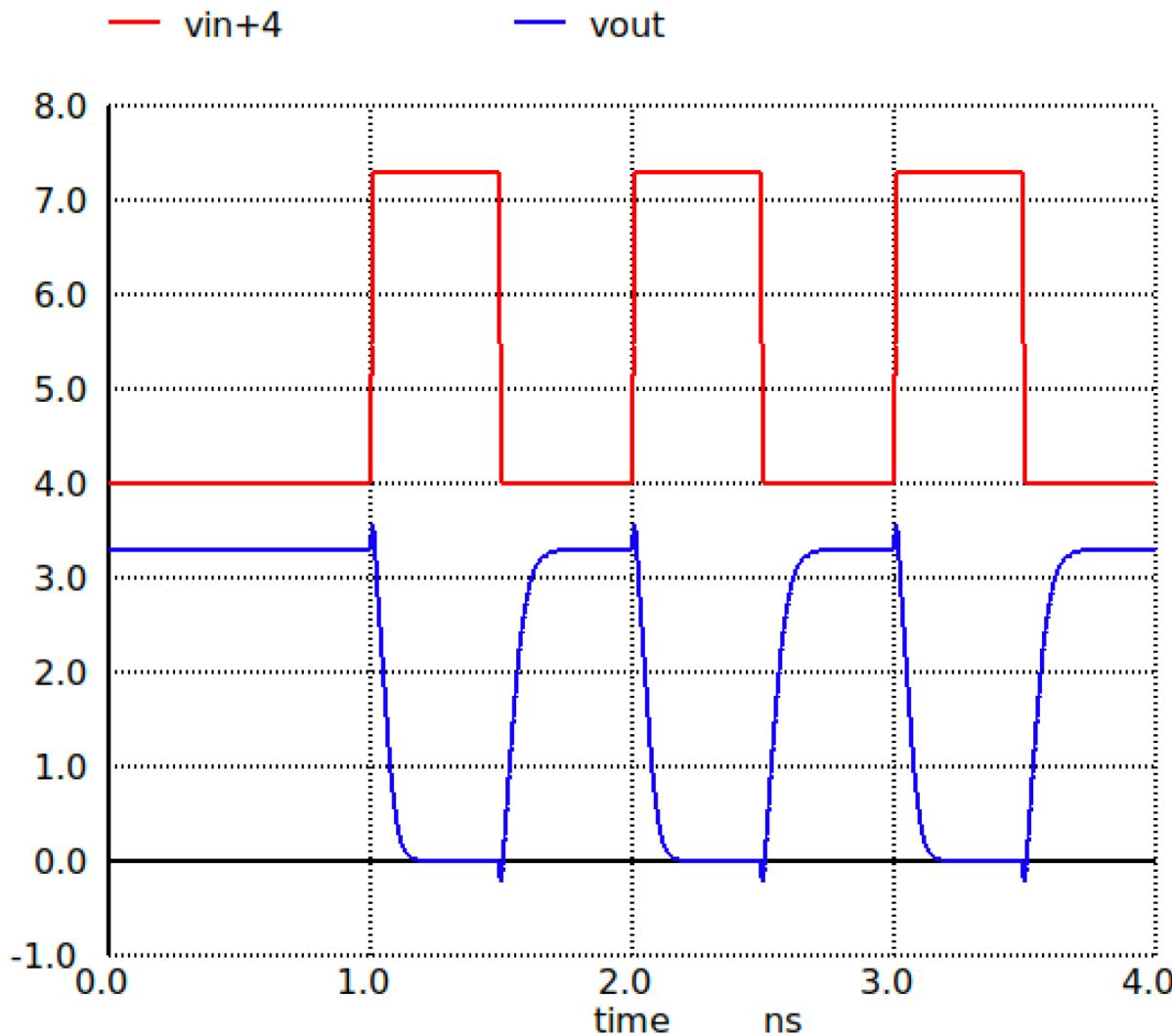
# TRAN Analysis



$$C_{LOAD} = 1fF$$

$t_{plh} = 2.159973e-11$   
 $t_{phl} = 2.184482e-11$   
 $t_{rise} = 3.079366e-11$   
 $t_{fall} = 2.385487e-11$

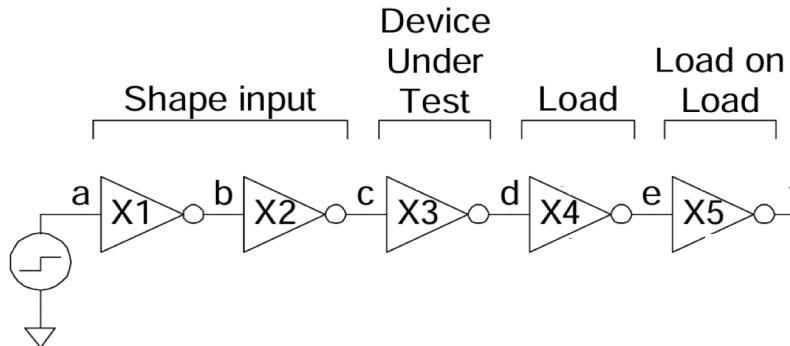
# TRAN Analysis



$$C_{LOAD} = 10 \text{ fF}$$

$$\begin{aligned} t_{plh} &= 5.449427 \times 10^{-11} \\ t_{phl} &= 5.245359 \times 10^{-11} \\ t_{rise} &= 9.867376 \times 10^{-11} \\ t_{fall} &= 8.110537 \times 10^{-11} \end{aligned}$$

# A more realistic setup for the TRAN Analysis



```
/foss/designs/gf180-2025/ring > xschem inv_tb_dynamic.sch
```

```
NGSPICE
.control
save all

** Define input signal
let fsig = 1e9
let tper = 1/fsig
let tfr = 0.01*tper
let ton = 0.5*tper-2*tfr
let tofs = tper

** Define transient params
let tstop = 4*tper
let tstep = 0.001*tper

** Set Sources
alter @VIN[PULSE] = [ 0 3.3 $&tofs $&tfr $&ton $&tper 0 ]

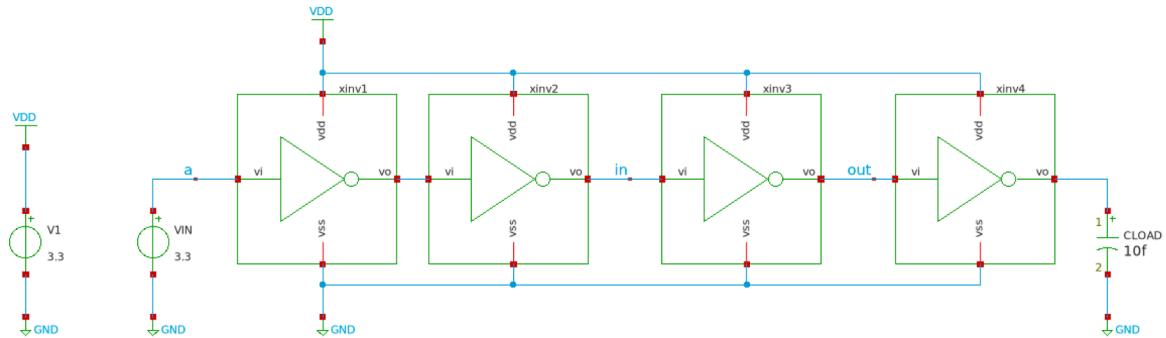
** Simulations
tran $&tstep $&tstop

** Plots
setplot tranl
let vout = v(out)
let vin = v(in)
meas tran tpLH trig v(in) val=1.65 fall=2 TARG v(out) val=1.65 rise=2
meas tran tpHL trig v(in) val=1.65 rise=2 TARG v(out) val=1.65 fall=2
meas tran trise trig v(out) val=0.1*3.3 rise=2 TARG v(out) val=0.9*3.3 rise=2
meas tran tfall trig v(out) val=0.9*3.3 fall=2 TARG v(out) val=0.1*3.3 fall=2
plot vout vin + 4

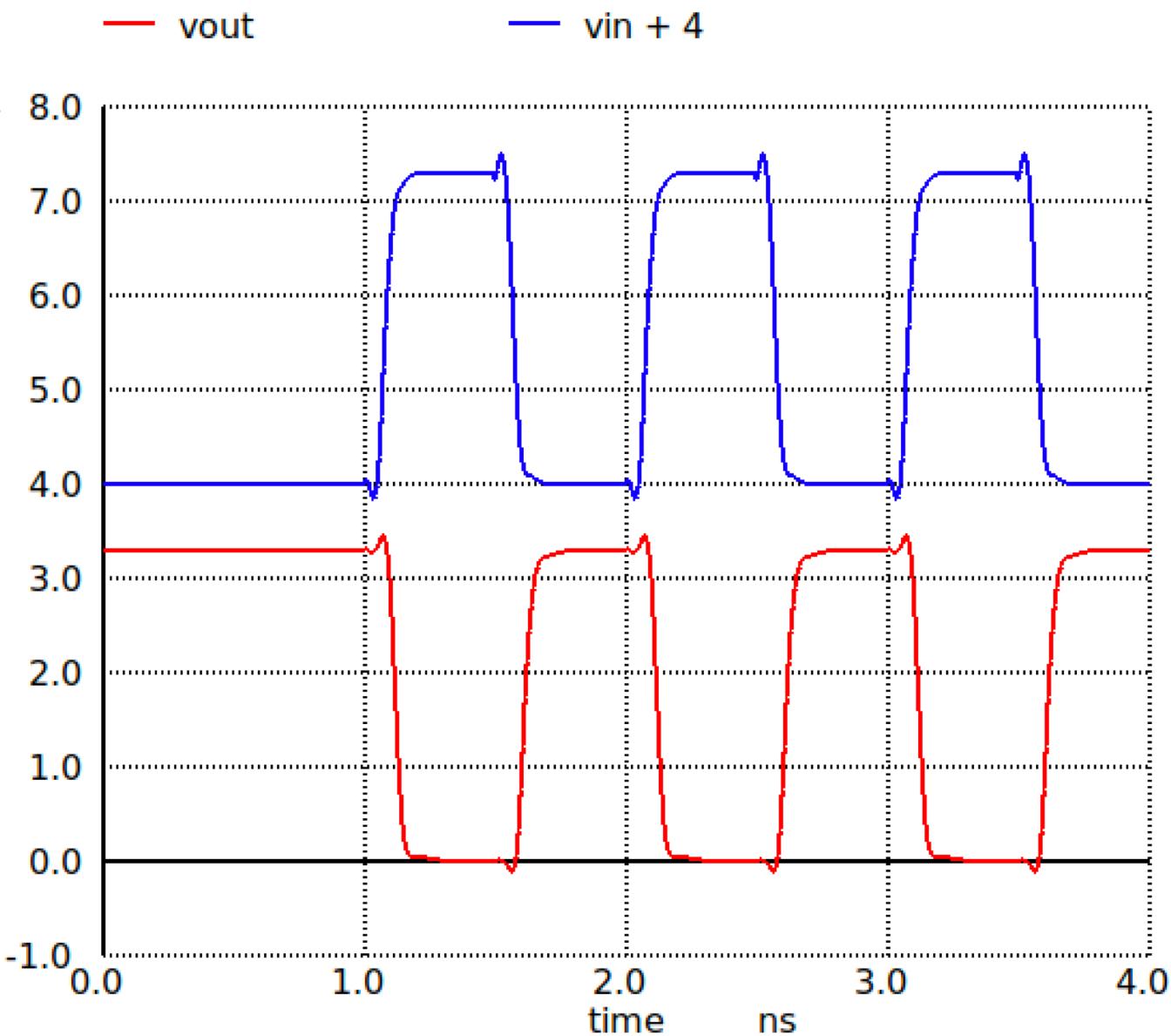
echo $plots
.endc
```

## MODELS

```
.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064.ngspice typical
```



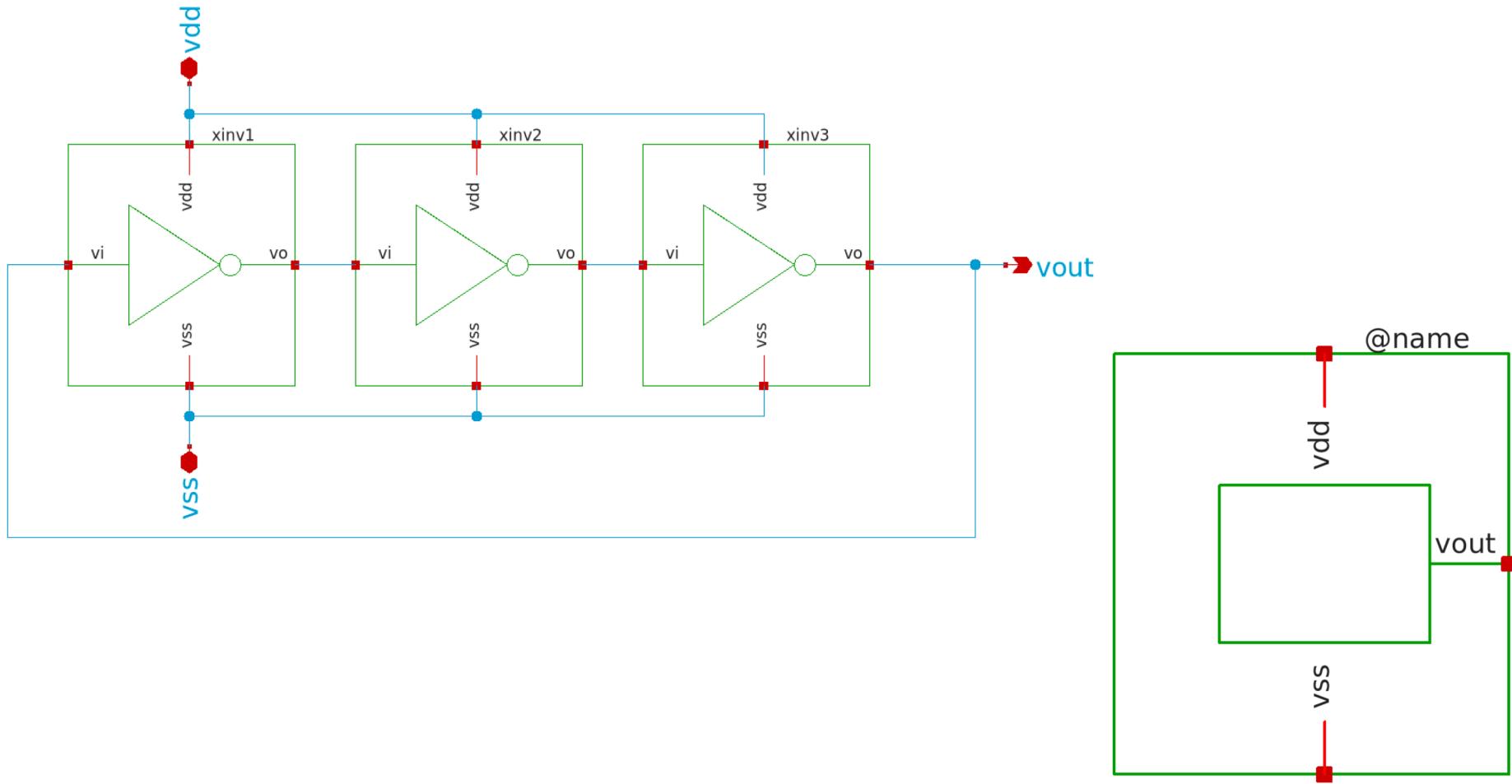
**tplh** = 4.209099e-11  
**tphl** = 4.004589e-11  
**trise** = 6.055123e-11  
**tfall** = 5.089469e-11



tplh = 4.209099e-11  
tphl = 4.004589e-11  
trise = 6.055123e-11  
tfall = 5.089469e-11

# Ring Oscillator

/foss/designs/gf180-2025/ring > xschem ring.sch



/foss/designs/gf180-2025/ring > xschem ring.sym

# Ring Oscillator: Testbench

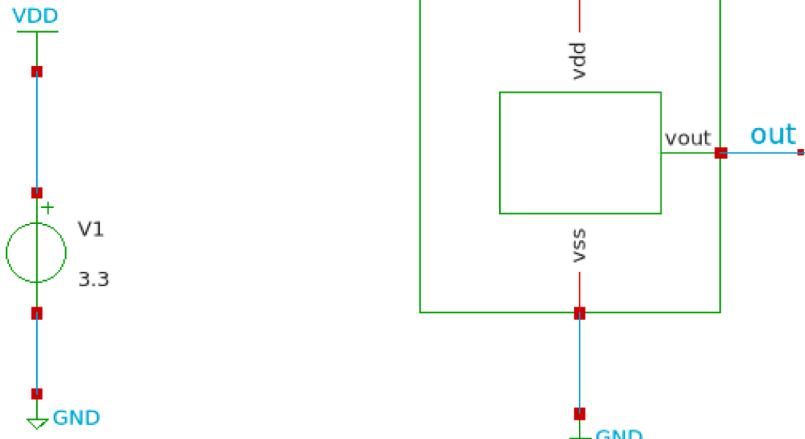
```
/foss/designs/gf180-2025/ring > xschem ring_tb.sch
```

## MODELS

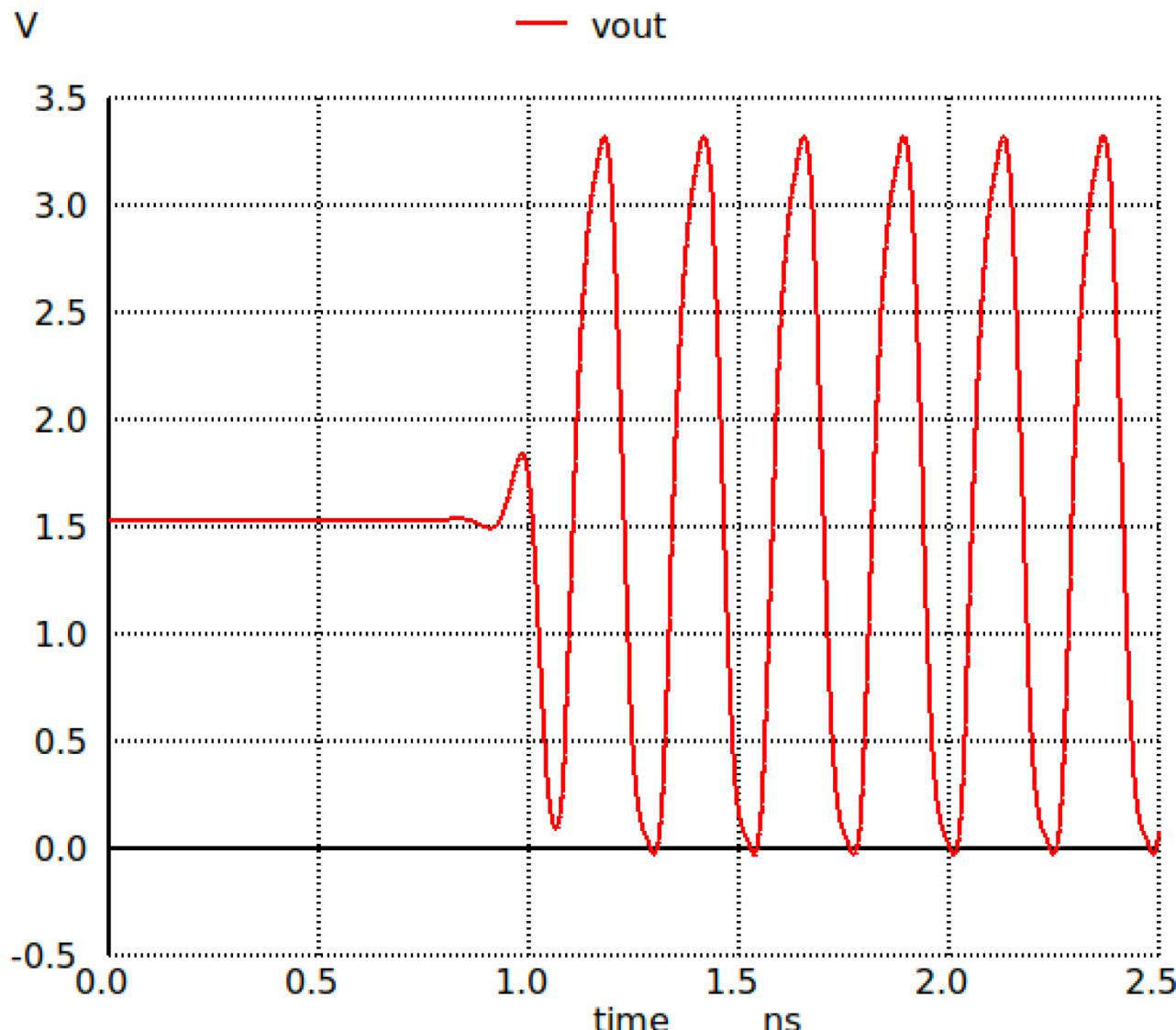
```
.include $::180MCU_MODELS/design.ngspice  
.lib $::180MCU_MODELS/sm141064.ngspice typical
```

## NGSPICE

```
.control  
save all  
  
** Define transient params  
let fsig = 1e9  
let tper = 1/fsig  
let tstop = 2.5*tper  
let tstep = 0.001*tper  
  
** Simulations  
tran $tstep $tstop  
  
** Plots  
setplot tran1  
let vout = v(out)  
meas tran tosc trig v(out) val=0.5*3.3 rise=4 TARG v(out) val=0.5*3.3 rise=5  
plot vout  
  
echo $plots  
.endc
```



# Ring Oscillator: Simulation



Simulation Measurement:

$$t_{osc} = 2.376660e-10$$

Estimate:

$$t_{osc} = N \cdot (t_{pHL} + t_{PLH}) \\ \approx 2.464106e-10$$

$$N = 3$$

$$tplh = 4.209099e-11$$

$$tphl = 4.004589e-11$$

% Error =

$$= \left| \frac{\text{measured} - \text{theoretical}}{\text{theoretical}} \right| \times 100 \\ \cong 3.94 \%$$

# KLayout

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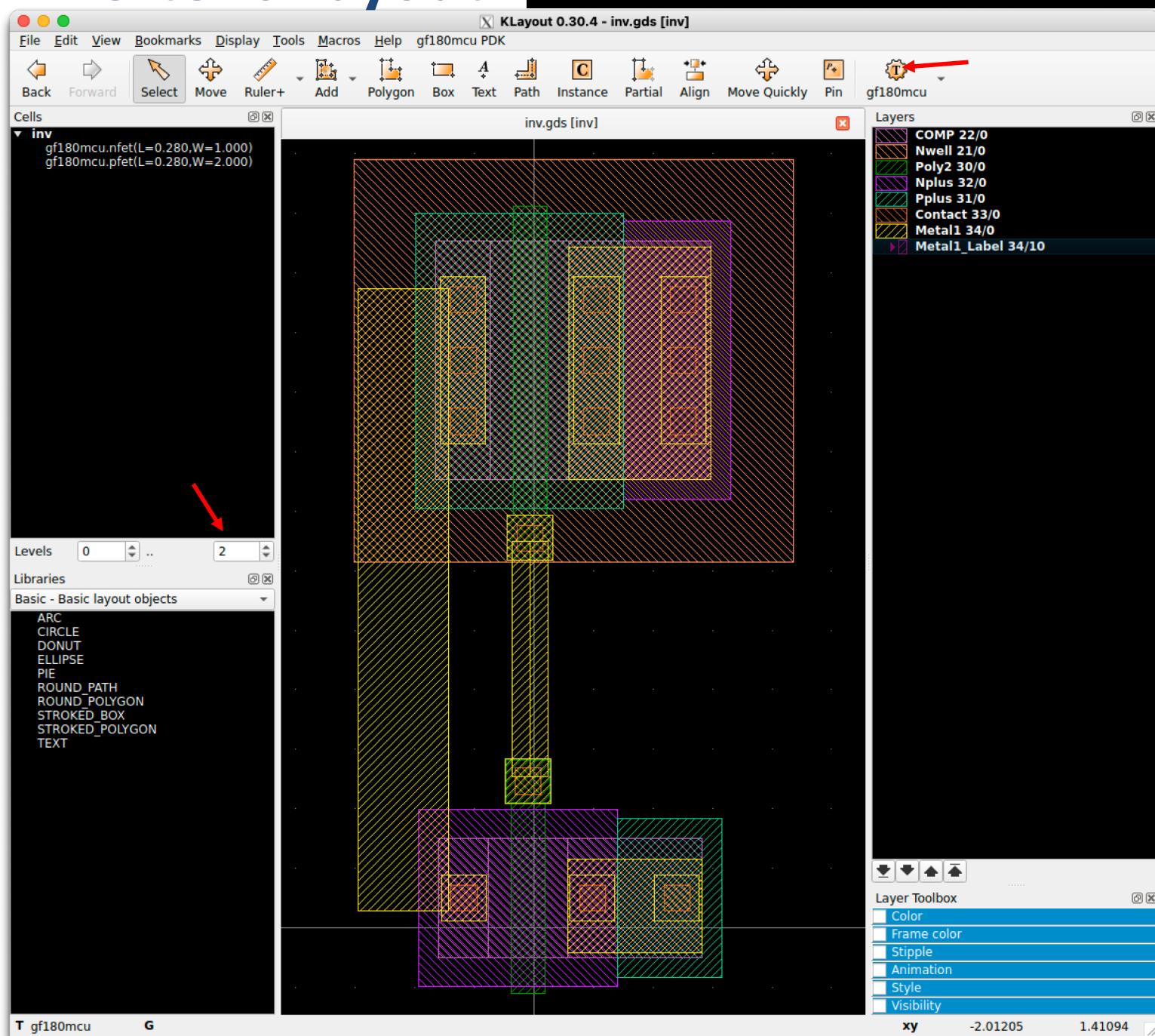
- **KLayout:** Layout Viewer And Editor  
<https://www.klayout.de/doc.html>
- gf180mcu  
<https://gf180mcu-pdk.readthedocs.io/en/latest>



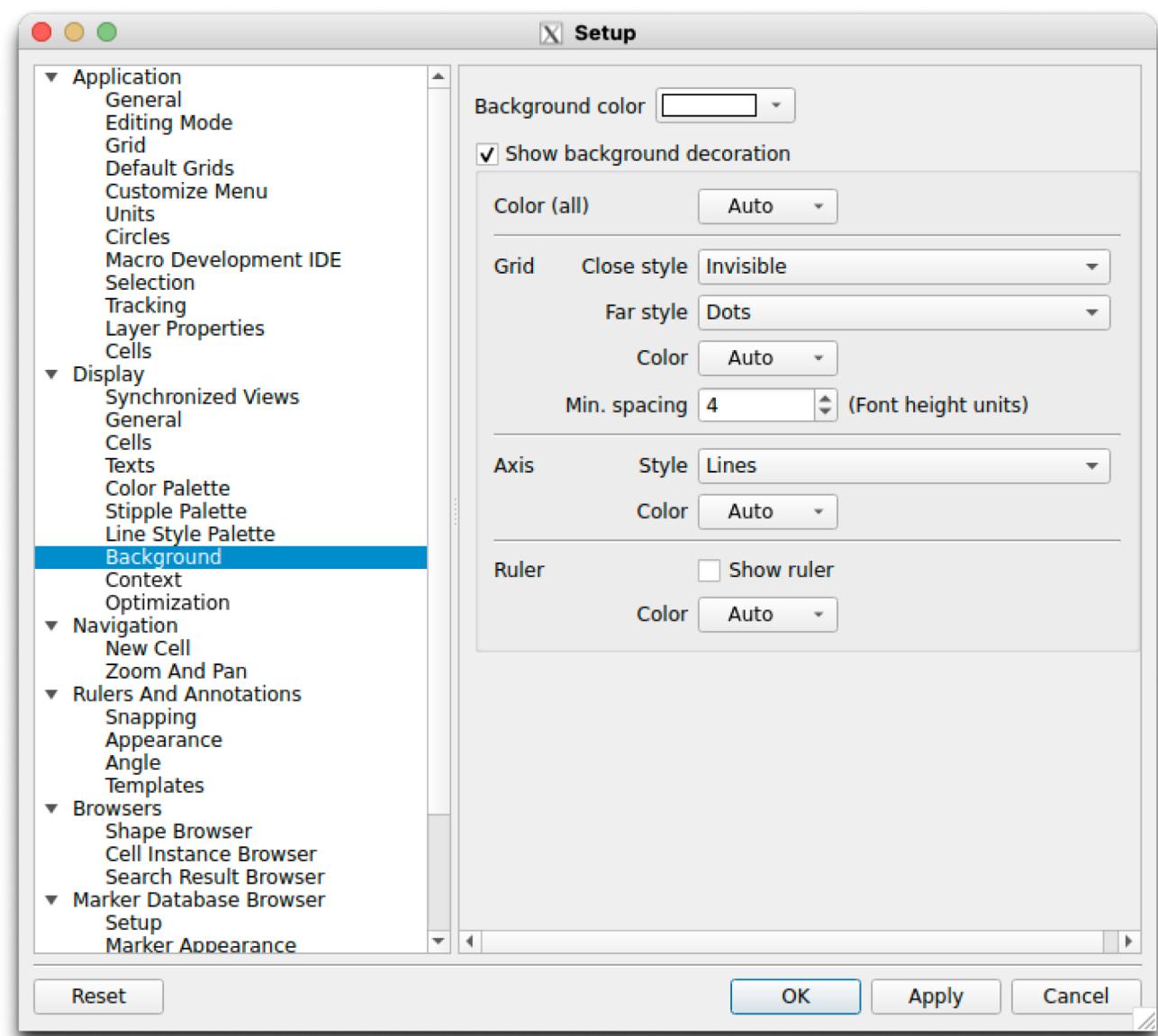
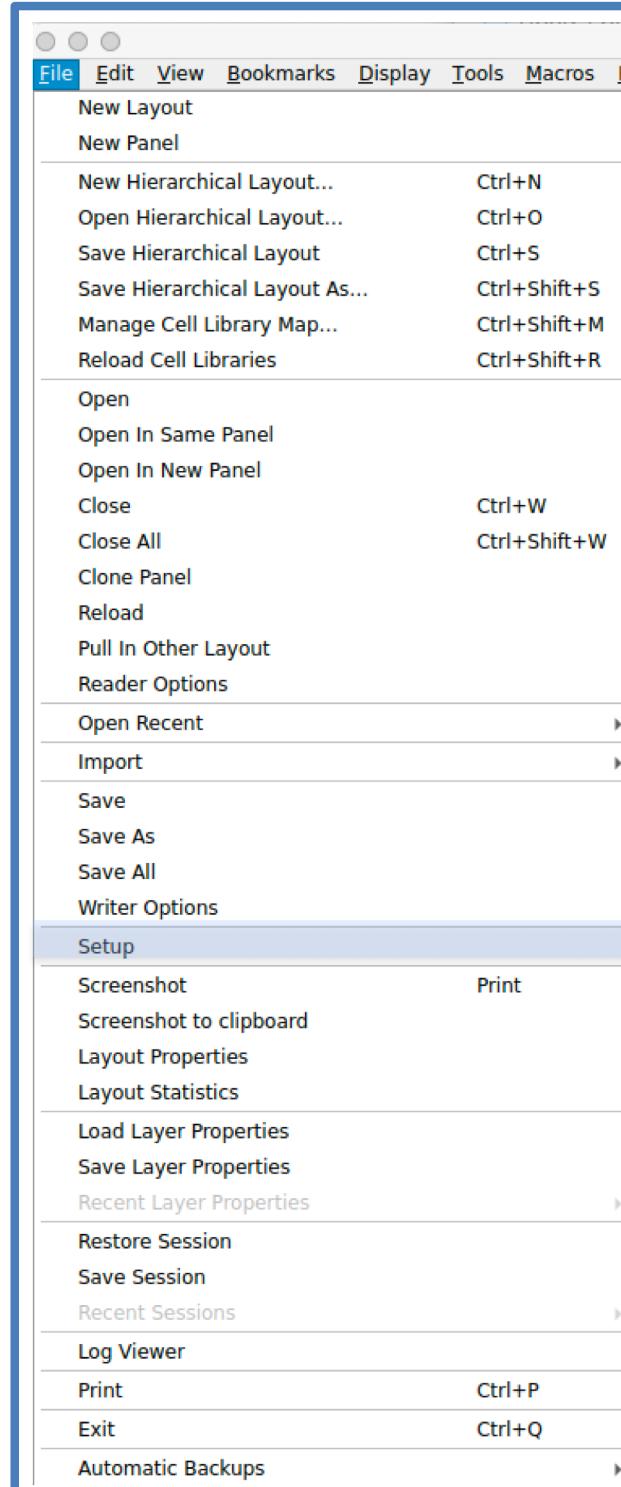
```
/foss/designs/gf180-2025/ring > echo $IIC_OSIC_TOOLS_VERSION
2025.11
/foss/designs/gf180-2025/ring > klayout -v
KLayout 0.30.4
/foss/designs/gf180-2025/ring > cat /headless/.bashrc | grep 'alias ke'
alias ke='klayout -e'
/foss/designs/gf180-2025/ring > klayout -h
...
```

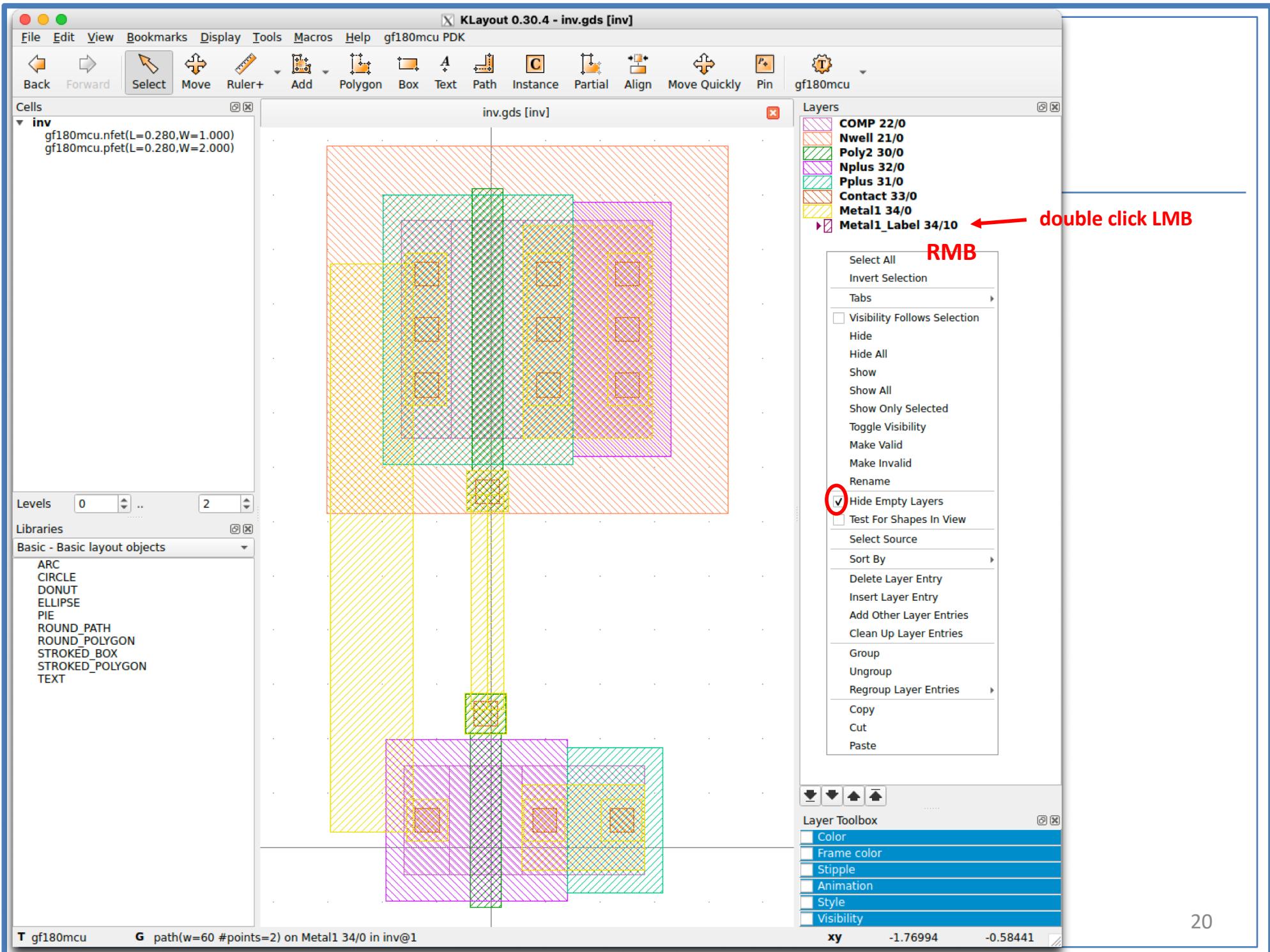
# Inverter's Layout

/foss/designs/gf180-2025/ring > ke inv.gds

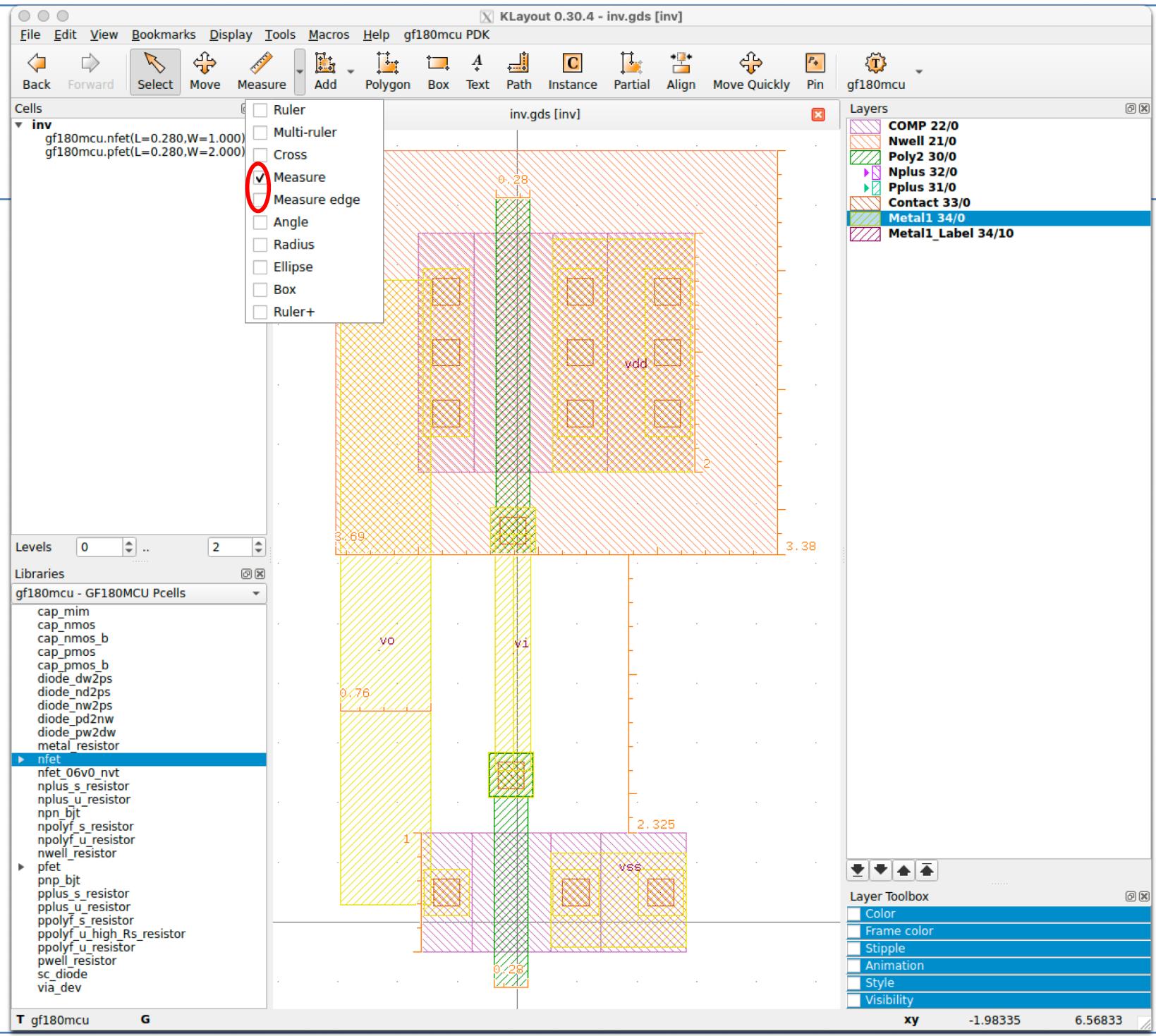


# Changing Background Color





# Dissecting the Layout

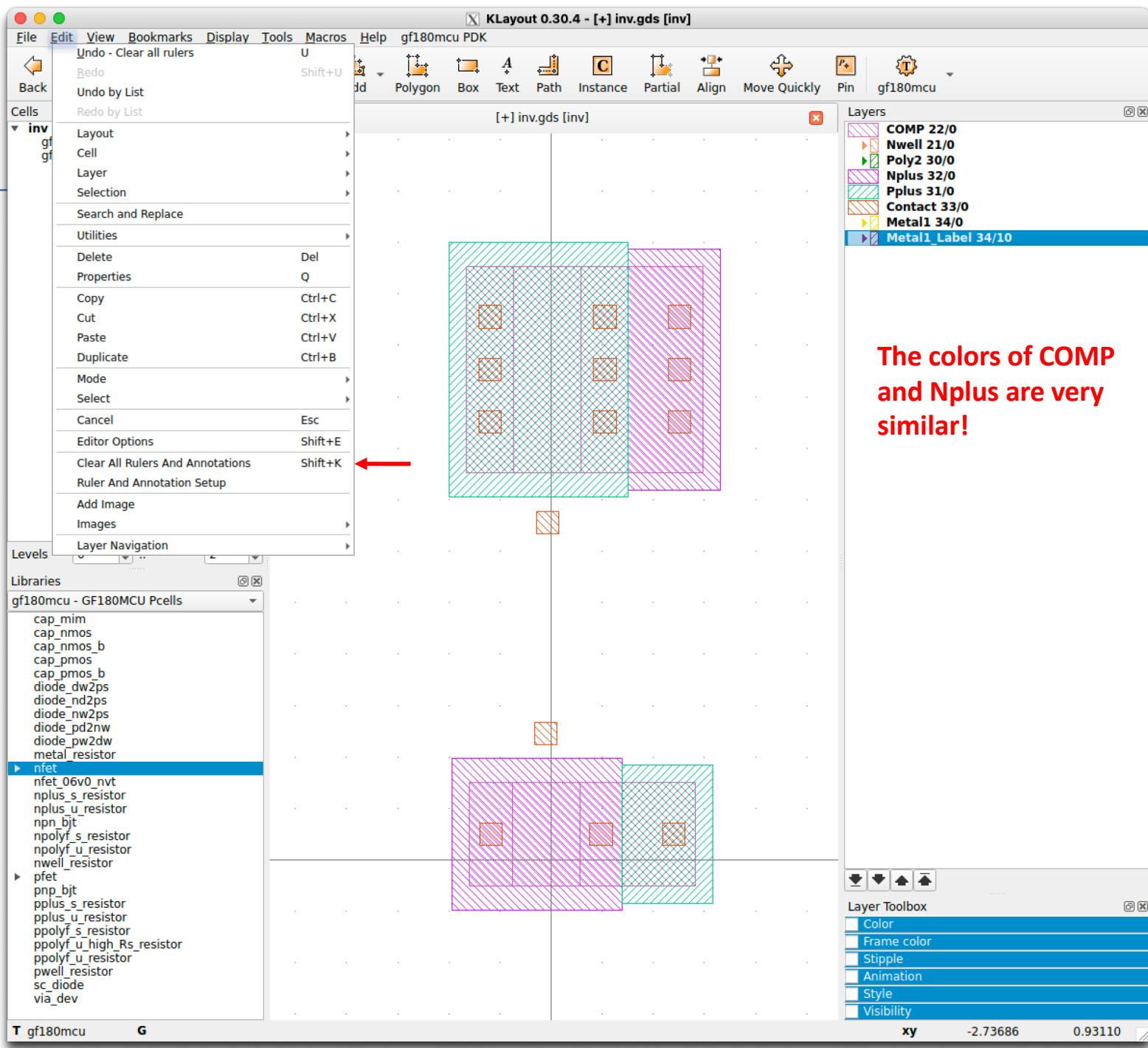


# Drawn layer definition and abbreviation

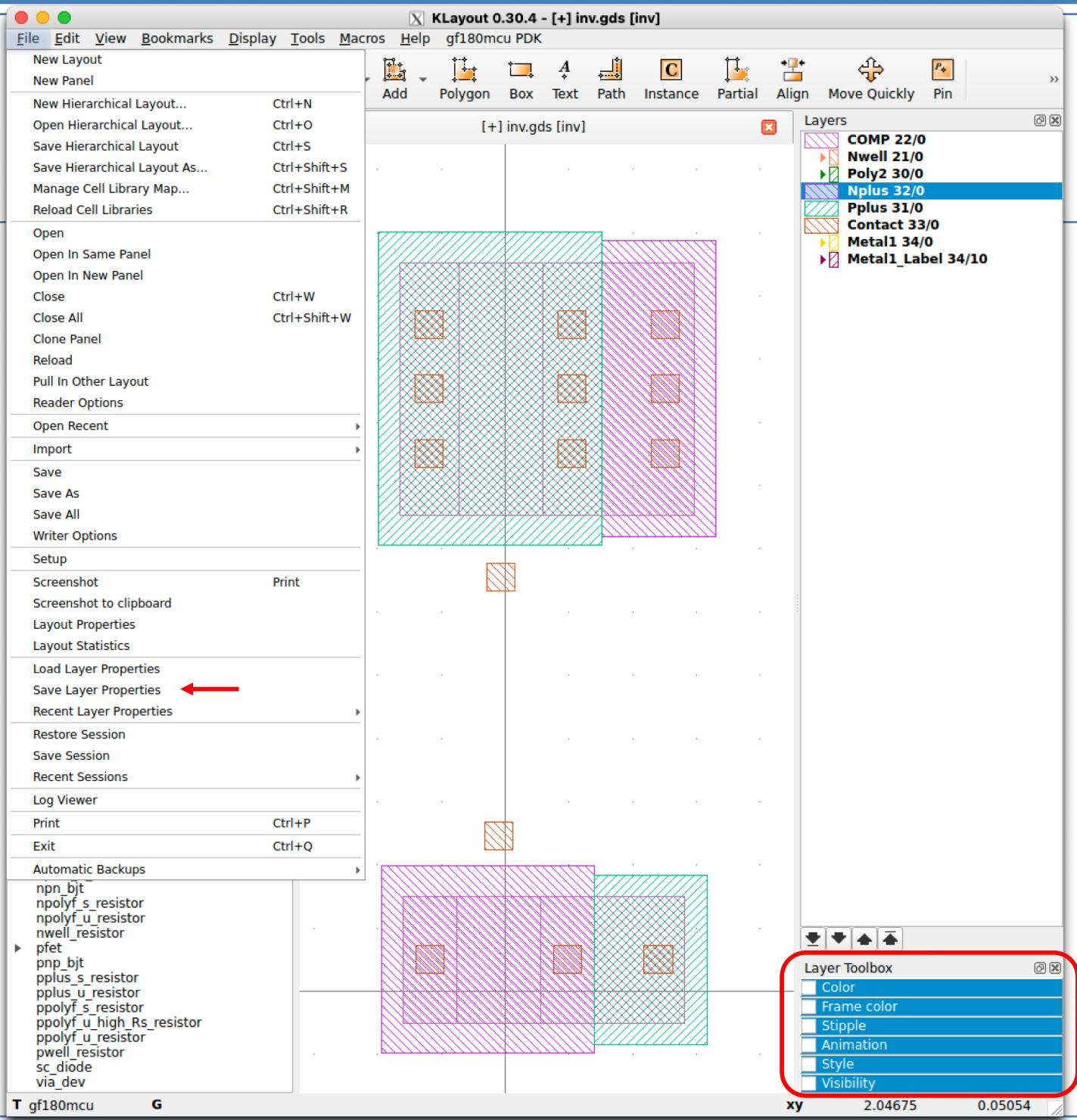
[https://gf180mcu-pdk.readthedocs.io/en/latest/physical\\_verification/design\\_manual/drm\\_04\\_1.html](https://gf180mcu-pdk.readthedocs.io/en/latest/physical_verification/design_manual/drm_04_1.html)

Layer Name	Purpose	GDS #	Data Type
COMP	Diffusion for device and interconnect	22	0
Nwell	Nwell Implant	21	0
Poly2	Poly2 gate and interconnect	30	0
Nplus	Nplus Implant	32	0
Pplus	Pplus Implant	31	0
Contact	Metal1 to Active or Poly2 contact	33	0
Metal1	Metal1 Interconnect	34	0
Metal1_Label	LABEL drawn at Metal1 layer	34	10
Via1	Metal2 to Metal1 contact	35	0
Metal 2	Metal2 Interconnect	36	0
Metal2_Label	LABEL drawn at Metal2 layer	36	10

# Dissecting the Layout

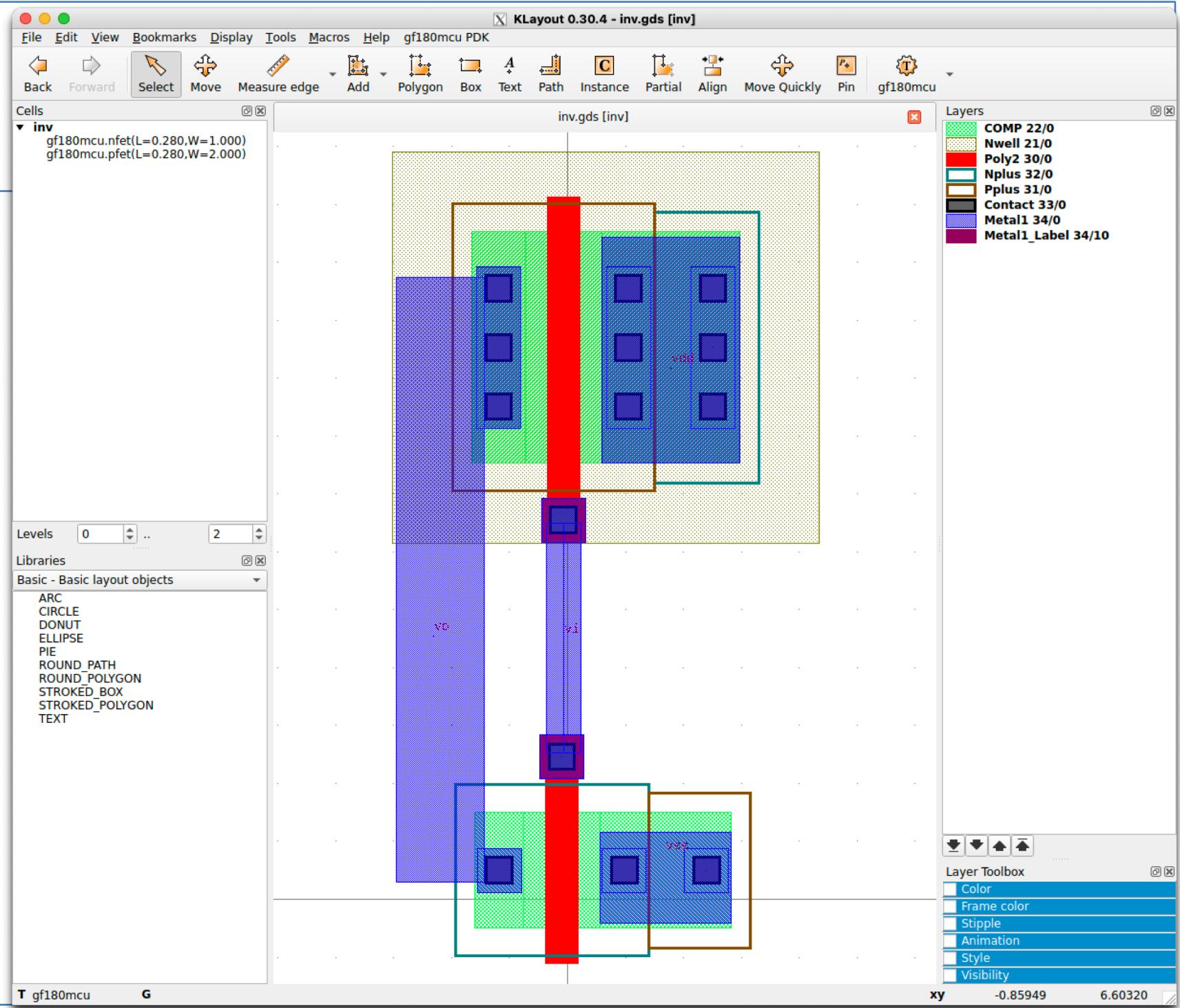


# Changing the layers properties

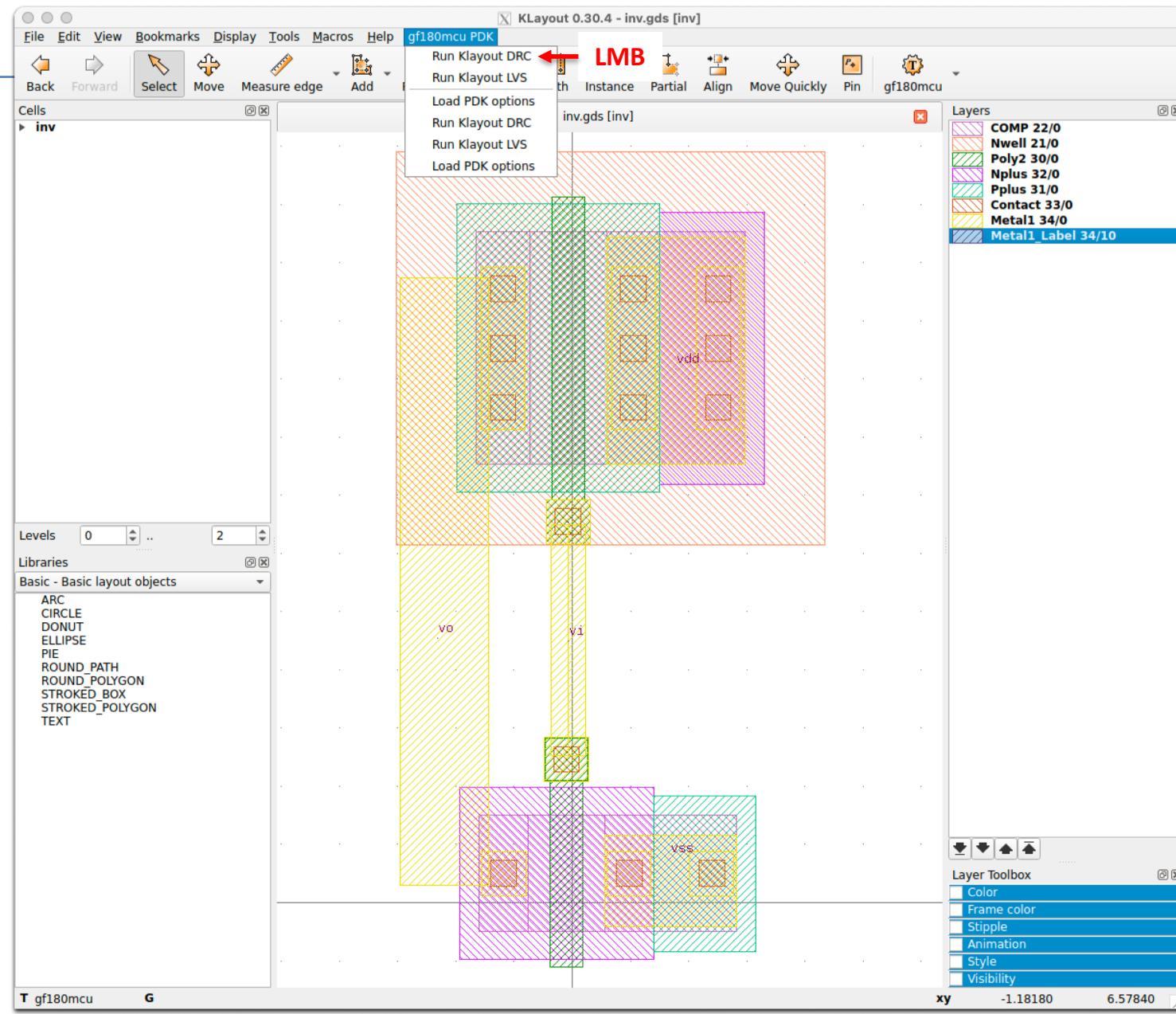


source: Peter Kinget

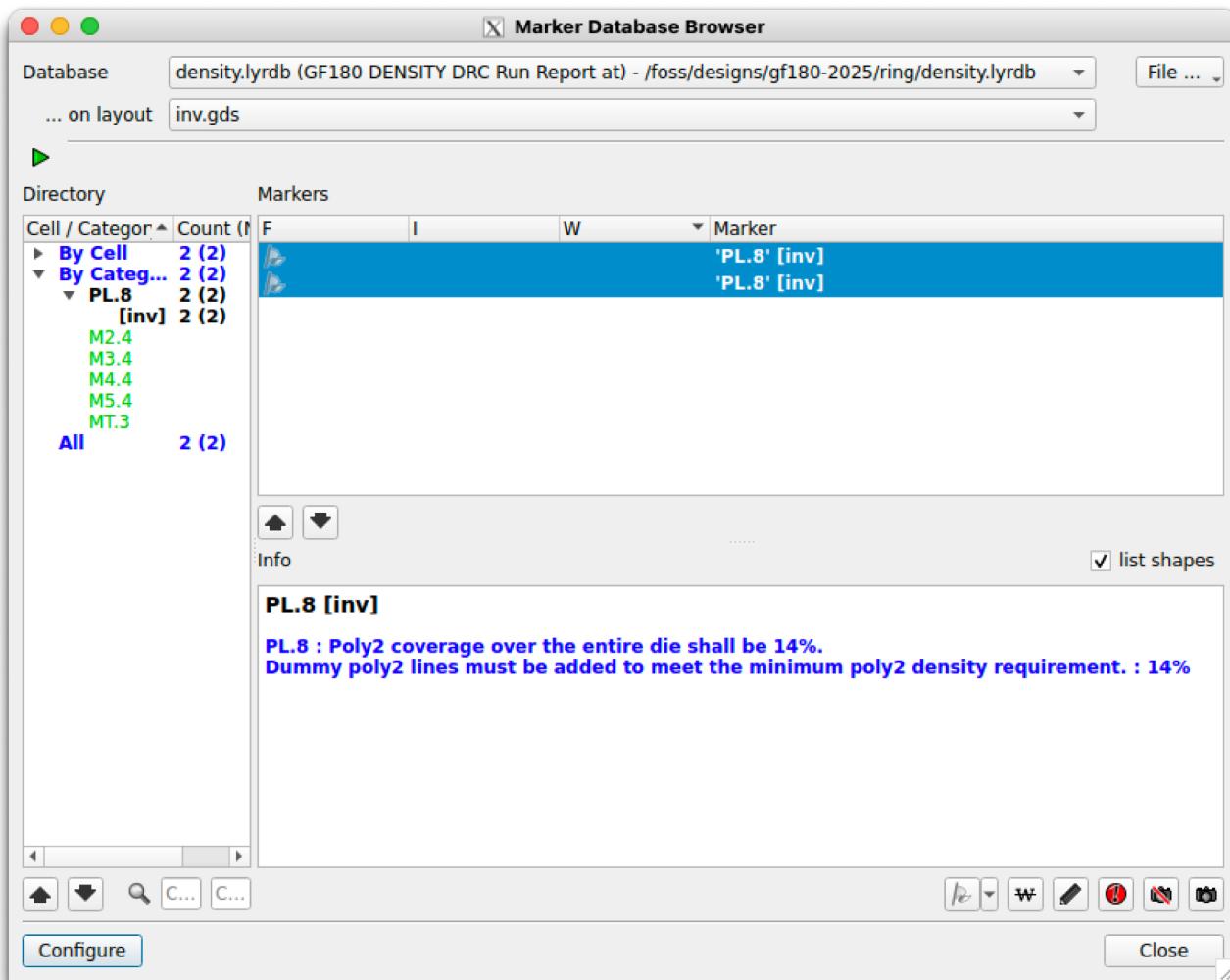
/foss/designs/gf180-2025/ring > ke -l gf180mcu\_Pk.lyp inv.gds



# DRC using KLayout



# DRC errors



There are DRC density violations ?!?

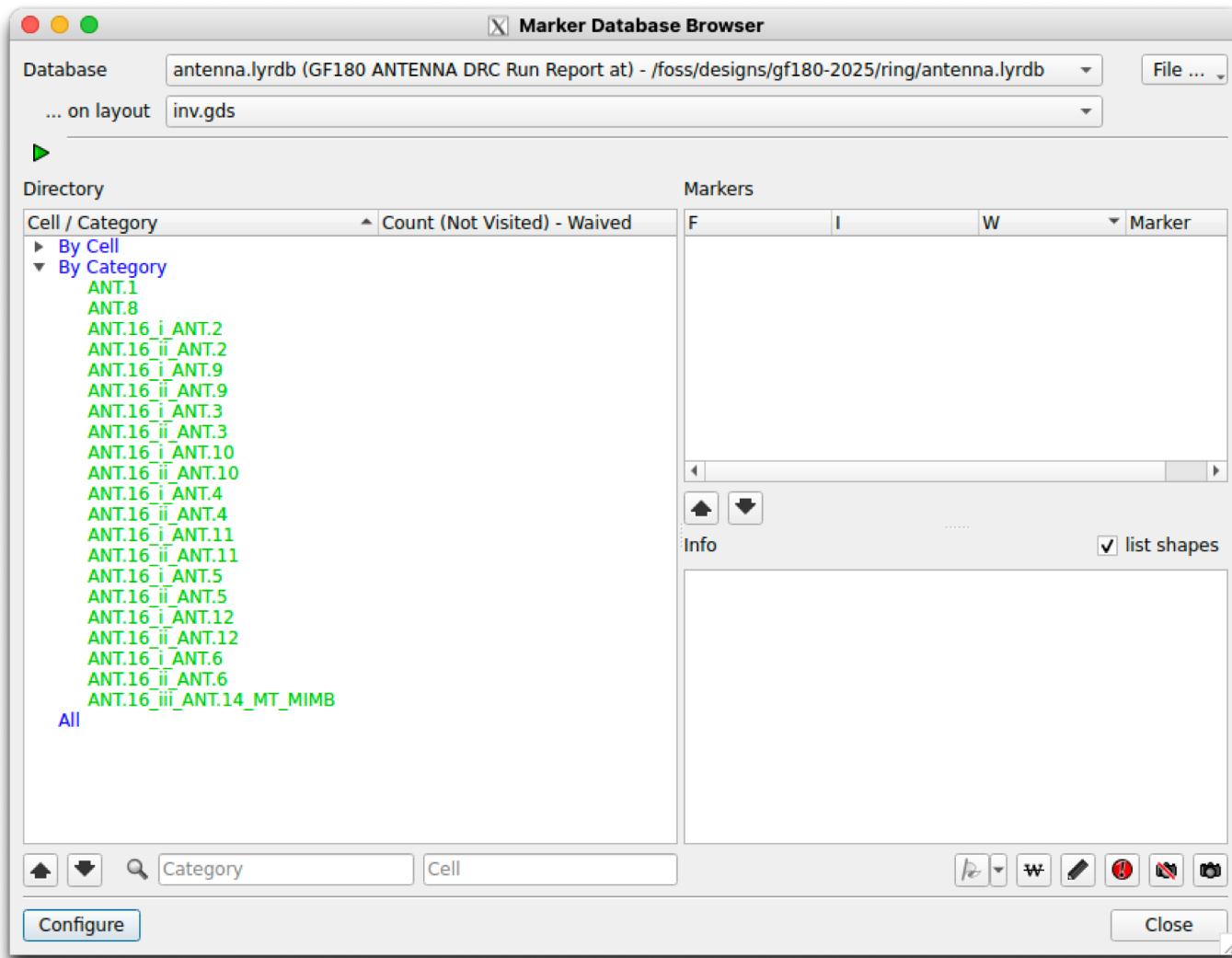
Usually, density rules are checked late in the layout process (after routing).

Sometimes the foundry provides you some script to fix them.

Should we neglect the issue ?!?

**density.lyrdb**

# DRC errors



No Antenna Ratio Rules violations!

antenna.lyrdb

# What is a DRC density error ?

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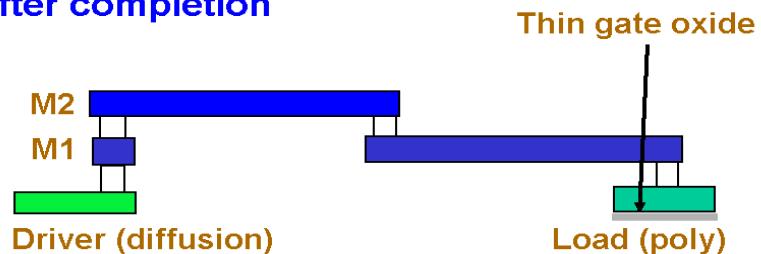
- A DRC density error in chip design means your layout doesn't meet foundry requirements for metal/poly coverage in an area, often due to too much or too little conductive material, causing issues with wafer yield.
- Chemical-mechanical polishing (CMP) demands consistent surface density across each layer. Uneven pattern densities can cause over- or under-polishing, leading to metal/poly deformation (a.k.a. dishing) or dielectric erosion.
- Uneven density causes sagging (low density) or stress (high density) in dielectric layers, so it affects lithography
- You fix it by adding dummy fill, adjusting routing, or modifying cell placement to balance density.

# What is an antenna ratio violation ?

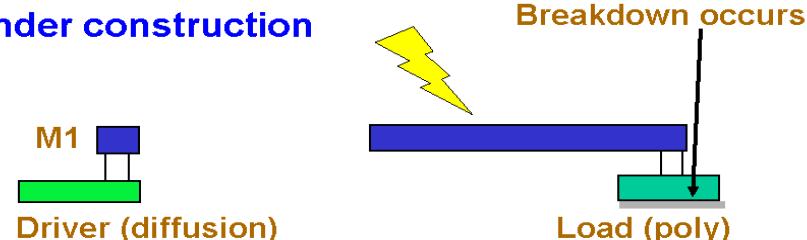
source: Wikipedia

- **The antenna effect**, more formally **plasma induced gate oxide damage**, is an effect that can potentially cause reliability problems during manufacturing. During plasma etching, a long metal wire (antenna) can collect excessive electrical charge, causing a high voltage spike that can break down the thin gate oxide of the connected transistor and lead to chip failure

(a) After completion



(b) Under construction



antenna ratio = metal area / gate area

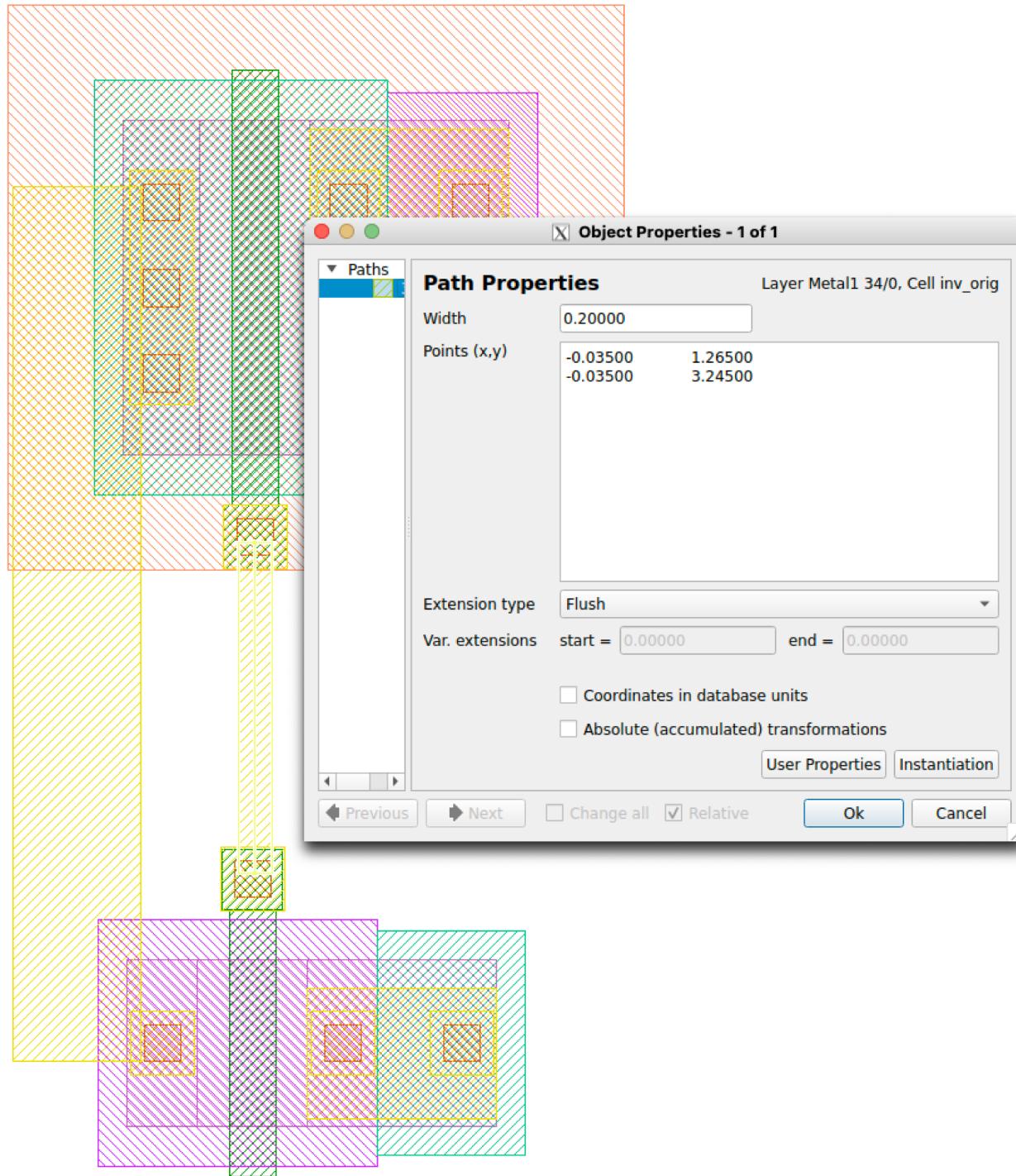
# Can we trust the DRC result ?

- Let's violate a rule on purpose and see what happen.

7.13 Metaln (where n = 1 to 5)

Metaln RULES		
RULE NO.	DESCRIPTION	LAYOUT RULE
Layer	Mn – Metaln (where n = 1 to 5)	
Mn.1	Width	0.23 (n = 1) 0.28 (2 <= n <= 5)
Mn.2a	Space	0.23 (n = 1) 0.28 (2 <= n <= 5)
Mn.2b	Space to wide Metaln (length & width > 10µm)	0.3
Mn.3	Minimum Metaln area	0.1444 um <sup>2</sup>
Mn.4	Metaln coverage over the entire die shall be >30% (Refer to section 13.0 for Dummy Metal fill guidelines. Customer needs to ensure enough dummy metal to satisfy Metaln coverage)	

[https://gf180mcu-pdk.readthedocs.io/en/latest/physical\\_verification/design\\_manual/drm\\_07\\_14.html](https://gf180mcu-pdk.readthedocs.io/en/latest/physical_verification/design_manual/drm_07_14.html)



Reduce width  
of metal1  
that connects the  
gates to 0.2 um  
(the min width  
is 0.23 um)

# Disaster !!!

Instead of checking the main rules the tool checks only density and antenna rules

The screenshot shows the 'Marker Database Browser' window with the following details:

- Database:** density.lyrdb (GF180 DENSITY DRC Run Report at) - /foss/designs/gf180-2025/ring/density.lyrdb
- ... on layout:** inv.gds
- Directory:** Cell / Category ▲ Count (Not Visited) - Waived
  - ▶ By Cell 2 (2)
  - ▼ By Categ... 2 (2)
    - ▶ PL.8 2 (2)
      - M3.4
      - M4.4
      - M5.4
      - MT.3
  - All 2 (2)
- Markers:** A table showing markers for cell PL.8.

F	I	W	Marker
PL.8	PL.8	PL.8	'PL.8' [inv]
PL.8	PL.8	PL.8	'PL.8' [inv]
- Info:** PL.8 [inv]

PL.8 : Poly2 coverage over the entire die shall be 14%.  
Dummy poly2 lines must be added to meet the minimum poly2 density requirement. : 14%
- Buttons:** Category, Cell, Configure, Close.

# DRC and LVS with KLayout

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- For the gf180mcuD technology, with IIC\_OSIC\_TOOLS\_VERSION 2025.11, KLayout has issues running LVS
- DRC has also issues ! It runs density and antenna checks, but does not check the main rules !
  - 2025.11 uses KLayout 0.30.4
- Work around: use **2025.07 or 2025.09**
  - 2025.07 uses KLayout 0.30.2
  - 2025.09 uses KLayout 0.30.4