

# **Systematic Design of Analog CMOS Circuits with LUTs using open-source tools and PDKs**

**Part II (e)**

# Aside: Post Processing Ngspice's Simulations with Python

```
/foss/designs/gf180-2025/ring > xschem inv_tb_stat_enh.sch
```

## NGSPICE

```
.control
option num_digit = 3
set wr_singlescale
set wr_vecnames
save all

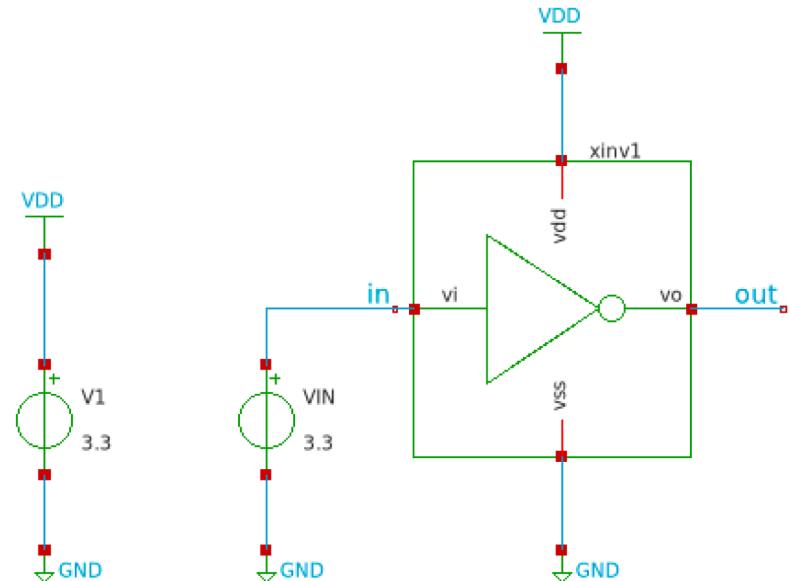
** Simulation (DC Sweep)
dc vin 0 3.3 0.01

** Plots
let vout = v(out)
let dvout = deriv(v(out))
plot v(in) vout
meas dc VSW find v(in) when v(out)=1.65
meas dc VIL find v(in) when dvout=-1 cross=1
meas dc VIH find v(in) when dvout=-1 cross=2
meas dc VOH find v(out) when dvout=-1 cross=1
meas dc VOL find v(out) when dvout=-1 cross=2

wrdata inv_tb_stat_enh.txt v(in) v(out) VSW VIL VIH VOH VOL
echo $plots
.endc
```

## MODELS

```
.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064.ngspice typical
```



# Aside: Post Processing Ngspice's Simulations with Python

```
/foss/designs/gf180-2025/ring > jupyter notebook pp_inv_tb_stat_enh.ipynb
```

## Post Process ngspice's Simulation Results with Python

### Import packages

```
import matplotlib.pyplot as plt  
import numpy as np  
import pandas as pd  
✓ 0.7s
```

### Load the simulation's data

```
df = pd.read_csv('./inv_tb_stat_enh.txt', sep='\\s+')  
  
par_names = df.columns.to_list()  
print(par_names)  
✓ 0.0s  
['v-sweep', 'v(in)', 'v(out)', 'VSW', 'VIL', 'VIH', 'VOH', 'VOL']
```

## Extract and massage the data

```
df = df.apply(pd.to_numeric)

vin = df[["v(in)"]]
vout = df[["v(out)"]]

VSW = df[["VSW"]]
VSW = VSW.to_numpy()
VSW = VSW[0,0]

VOH = df[["VOH"]]
VOH = VOH.to_numpy()
VOH = VOH[0,0]

VIL = df[["VIL"]]
VIL = VIL.to_numpy()
VIL = VIL[0,0]

VOL = df[["VOL"]]
VOL = VOL.to_numpy()
VOL = VOL[0,0]

VIH = df[["VIH"]]
VIH = VIH.to_numpy()
VIH = VIH[0,0]

print(VSW)
print(VOH)
print(VIL)
print(VIH)
```

[3] ✓ 0.0s

```
... 1.525452
    3.001193
    1.204496
    1.775522
```

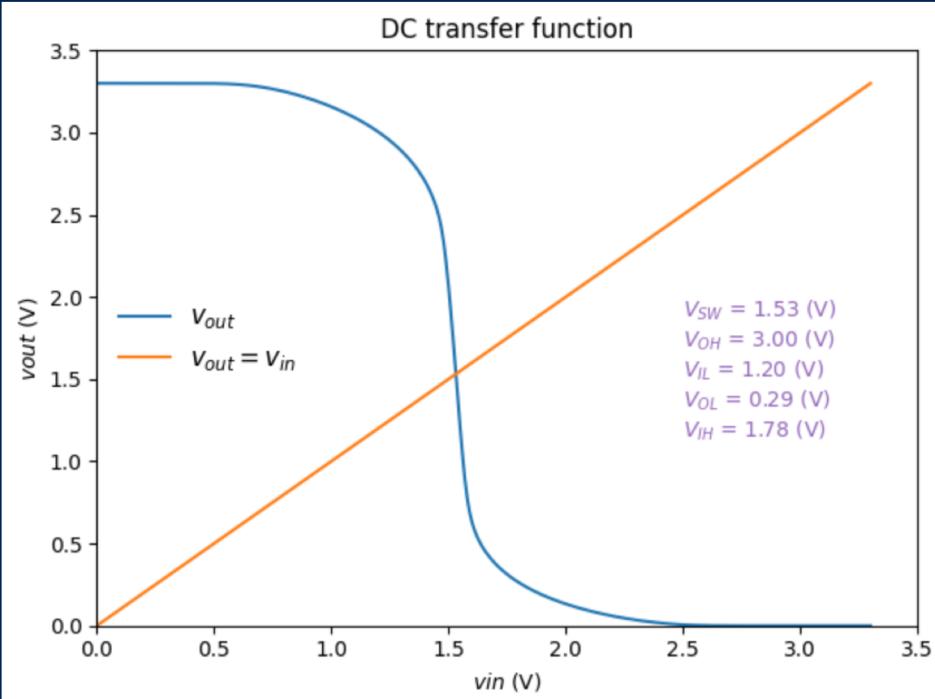
## Plot

```
fig1 = plt.figure()
plt.plot(vin,vout,label="$v_{out}$")
plt.plot(vin,vin,label="$v_{out}=v_{in}$")
plt.xlabel("$vin$ (V)")
plt.ylabel("$vout$ (V)")
plt.title("DC transfer function")
plt.ylim(0,3.5)
plt.xlim(0,3.5)
plt.legend(loc='center left',frameon=False,fontsize=12)
str1 = f" = {VSW:.2f} (V)"
str2 = f" = {VOH:.2f} (V)"
str3 = f" = {VIL:.2f} (V)"
str4 = f" = {VOL:.2f} (V)"
str5 = f" = {VIH:.2f} (V)"
plt.annotate("$V_{SW}" + str1 + '\n' + "$V_{OH}" + str2 + '\n' +
"$V_{IL}" + str3 + '\n' + "$V_{OL}" + str4 + '\n' +
"$V_{IH}" + str5,
xy=(2.5,2.0), ha='left',va='top',color='tab:purple')
fig1.tight_layout()
plt.savefig("./Plot_inv_tb_stat_enh.png")
plt.show()
```

[4]

✓ 0.4s

...



# Appendix

- Efabless videos – 2023  
[https://www.youtube.com/@efabless\\_channel/videos](https://www.youtube.com/@efabless_channel/videos)
- gf180mcu tutorial part 1 - intro  
[https://www.youtube.com/watch?v=\\_spkK77JeqY](https://www.youtube.com/watch?v=_spkK77JeqY)
- gf180mcu tutorial part 2 - volare  
<https://www.youtube.com/watch?v=btB5Qov8MEs>
- gf180mcu tutorial part 3 – xschem  
<https://www.youtube.com/watch?v=hweOEznql-M>
- gf180mcu tutorial part 4 – symbol creation  
<https://www.youtube.com/watch?v=TJ71K0e-DvA>
- gf180mcu tutorial part 5 – symbol finishing  
<https://www.youtube.com/watch?v=XNUbrxx771w>
- gf180mcu tutorial part 6 – ngspice  
<https://www.youtube.com/watch?v=HaowKMUeOsQ>
- gf180mcu tutorial part 7 – preparing klayout  
<https://www.youtube.com/watch?v=KtegPMeYu2Q>
- gf180mcu tutorial part 8 – klayout  
<https://www.youtube.com/watch?v=MwwiYSQ2JX8>
- gf180mcu tutorial part 9 – DRC  
<https://www.youtube.com/watch?v=UeyEeScHZB0>
- gf180mcu tutorial part 10 - LVS  
[https://www.youtube.com/watch?v=\\_SGbifHECc0](https://www.youtube.com/watch?v=_SGbifHECc0)

# Appendix

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- GF180MCU Tutorial - Single Video  
<https://www.youtube.com/watch?v=USCmZuREMTE&t=1731s>
- Bradley Minch  
<https://www.youtube.com/@bminch>
- ENGR3426: MADVLSI Tutorials  
[https://www.youtube.com/playlist?list=PLgsDG5BJZpBTEUaxjfYUiMPpUPU\\_vQpr](https://www.youtube.com/playlist?list=PLgsDG5BJZpBTEUaxjfYUiMPpUPU_vQpr)
- IIC-OSIC-TOOLS  
<https://www.youtube.com/@IIC-OSIC-TOOLS>
- Tutorial Using Klayout with gf180mcu (part 4)  
<https://www.youtube.com/watch?v=vamfMryYPS4&t=617s>

# Appendix

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- Chipalooza 2024 – Tim Edwards
- Chipalooza - Analog and Mixed-Signal Design Launch  
[https://www.youtube.com/watch?v=DQ6\\_AuMmijw](https://www.youtube.com/watch?v=DQ6_AuMmijw)
- workshop #1 (schematic and simulation) - <https://www.youtube.com/watch?v=dzmQlIRxqks>
- workshop #2 (layout and extraction) -  
[https://www.youtube.com/watch?v=ObFrLI1lqxQ&list=PLZuGFJzpFksALPQKbX88\\_HvwNdGMgzoxy&index=12&t=28s](https://www.youtube.com/watch?v=ObFrLI1lqxQ&list=PLZuGFJzpFksALPQKbX88_HvwNdGMgzoxy&index=12&t=28s)
- workshop #3 - (physical verification) - <https://www.youtube.com/watch?v=PCpsgkmM6u4>
- Analog layout of an op-amp using the Magic VLSI tool – Tim Edwards  
[https://www.youtube.com/watch?v=XvBpqKwzrFY&list=PLZuGFJzpFksALPQKbX88\\_HvwNdGMgzoxy&index=2&t=5523s](https://www.youtube.com/watch?v=XvBpqKwzrFY&list=PLZuGFJzpFksALPQKbX88_HvwNdGMgzoxy&index=2&t=5523s)

# Appendix: looking at the layout of a standard cells

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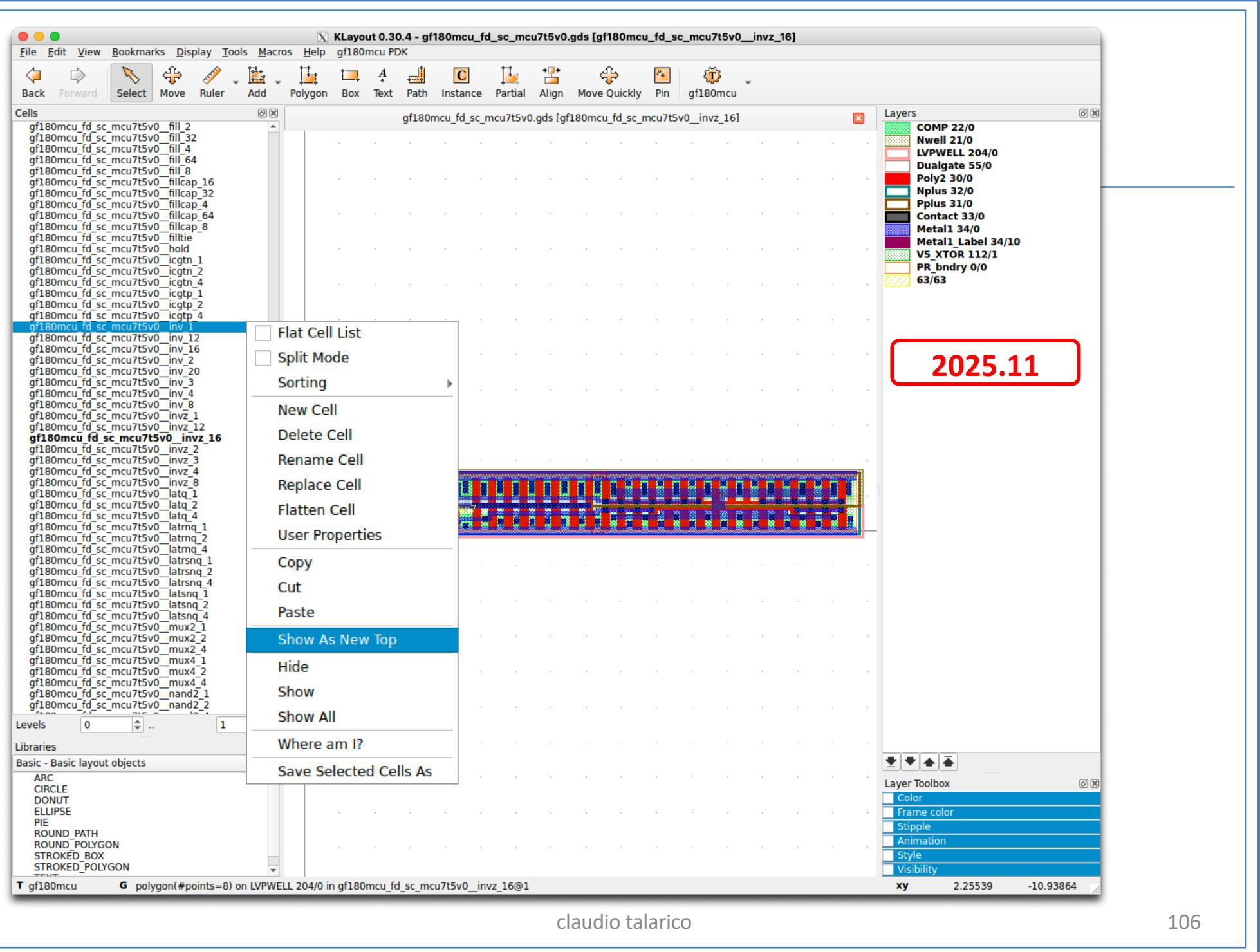
From location: **/foss/designs/gf180-2025/ring >**

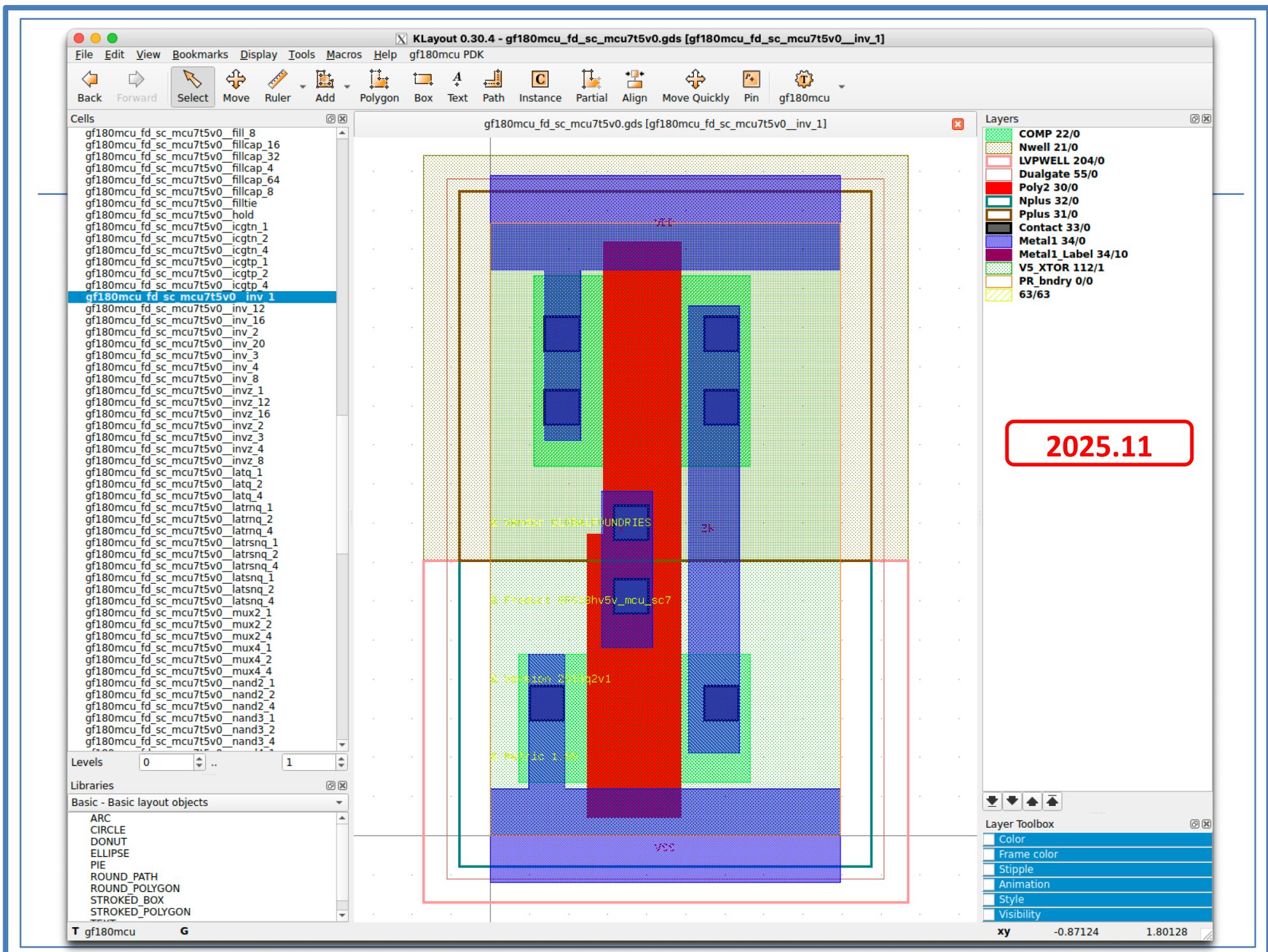
Run the following commands:

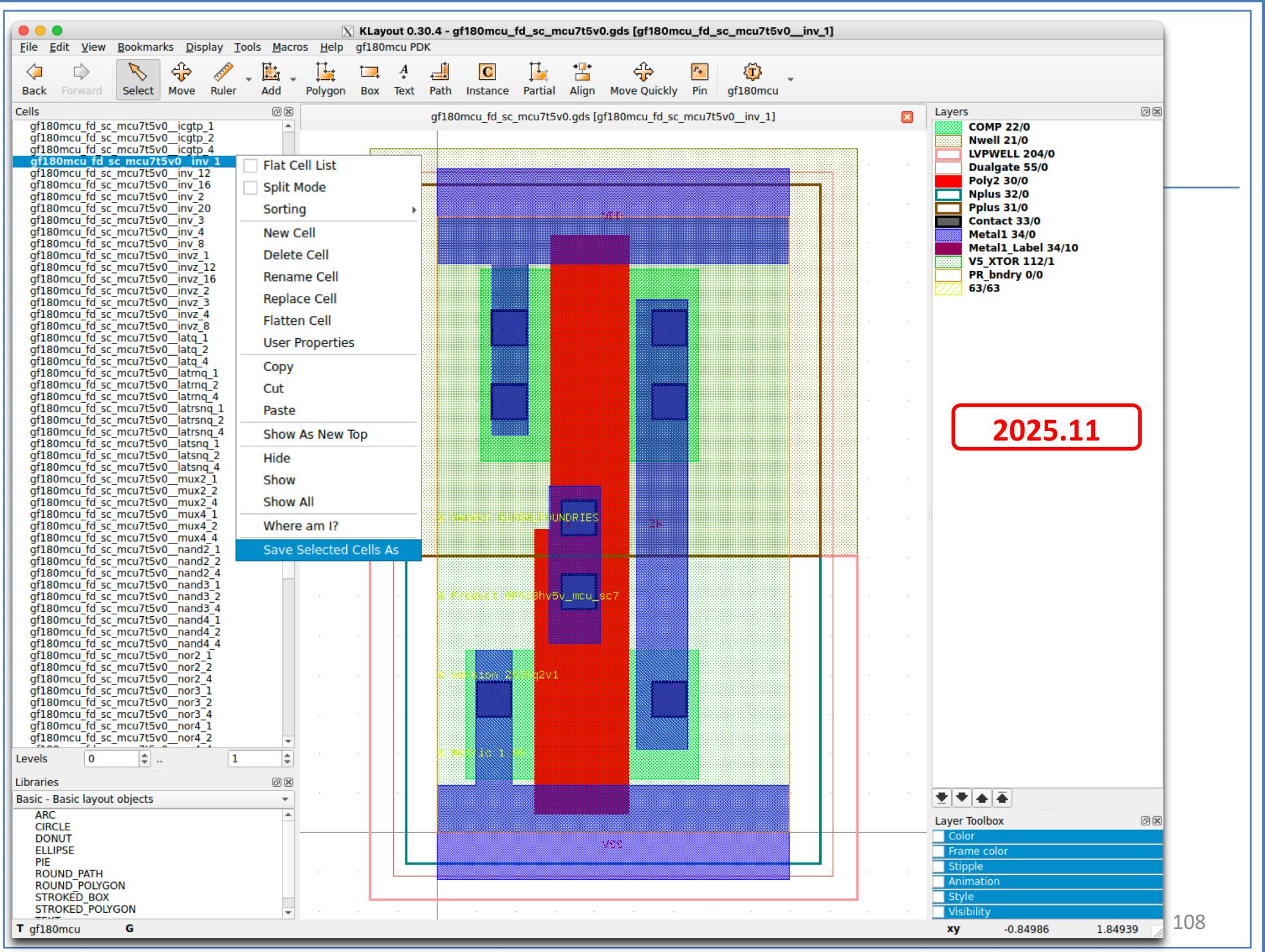
```
cp $PDK_ROOT/$PDK/libs.ref/gf180mcu_fd_sc_mcu7t5v0/gds/gf180mcu_fd_sc_mcu7t5v0.gds .
```

```
ke -l gf180mcu_PK.lyp gf180mcu_fd_sc_mcu7t5v0.gds
```

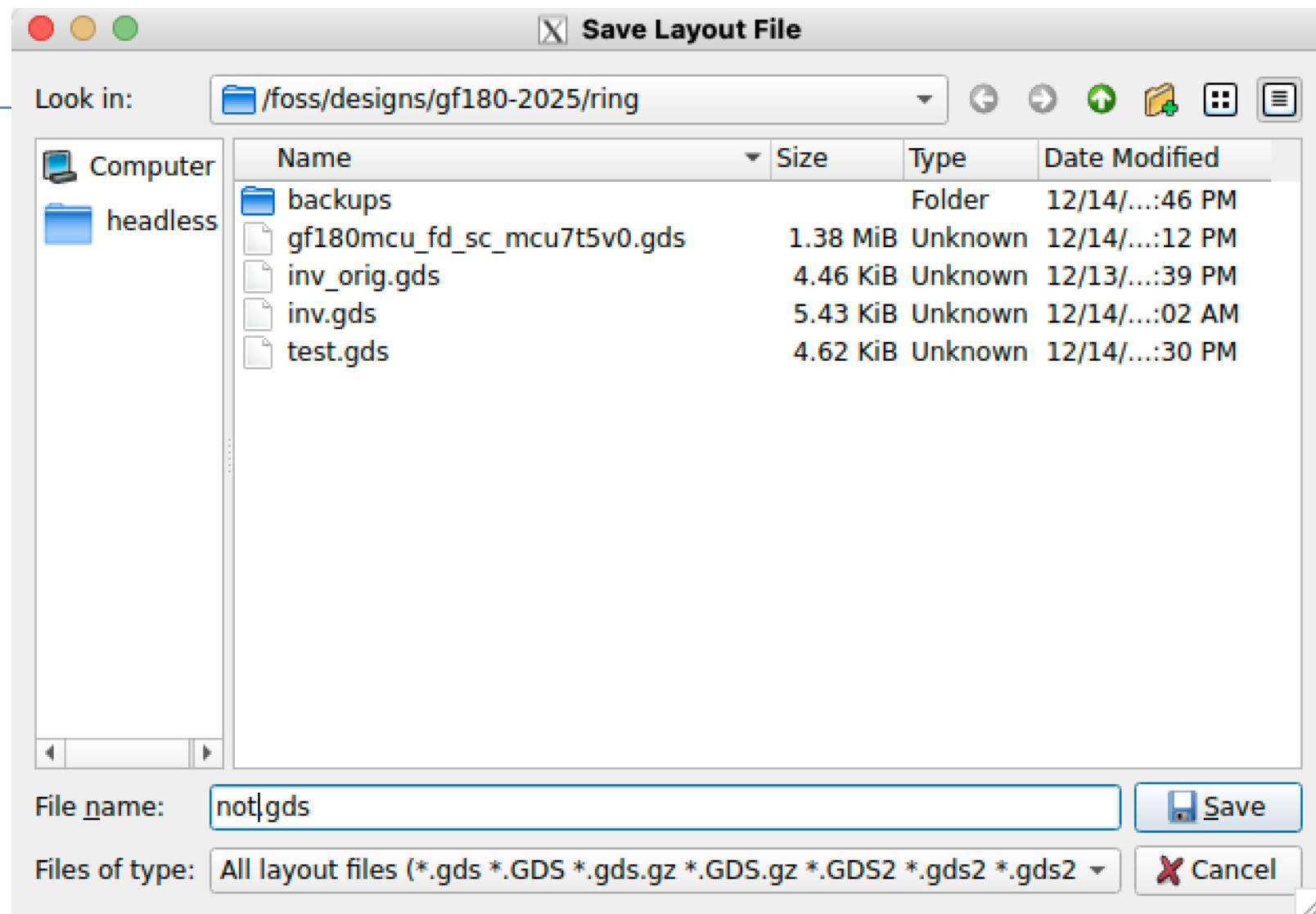
```
echo $IIC_OSIC_TOOLS_VERSION  
2025.11
```



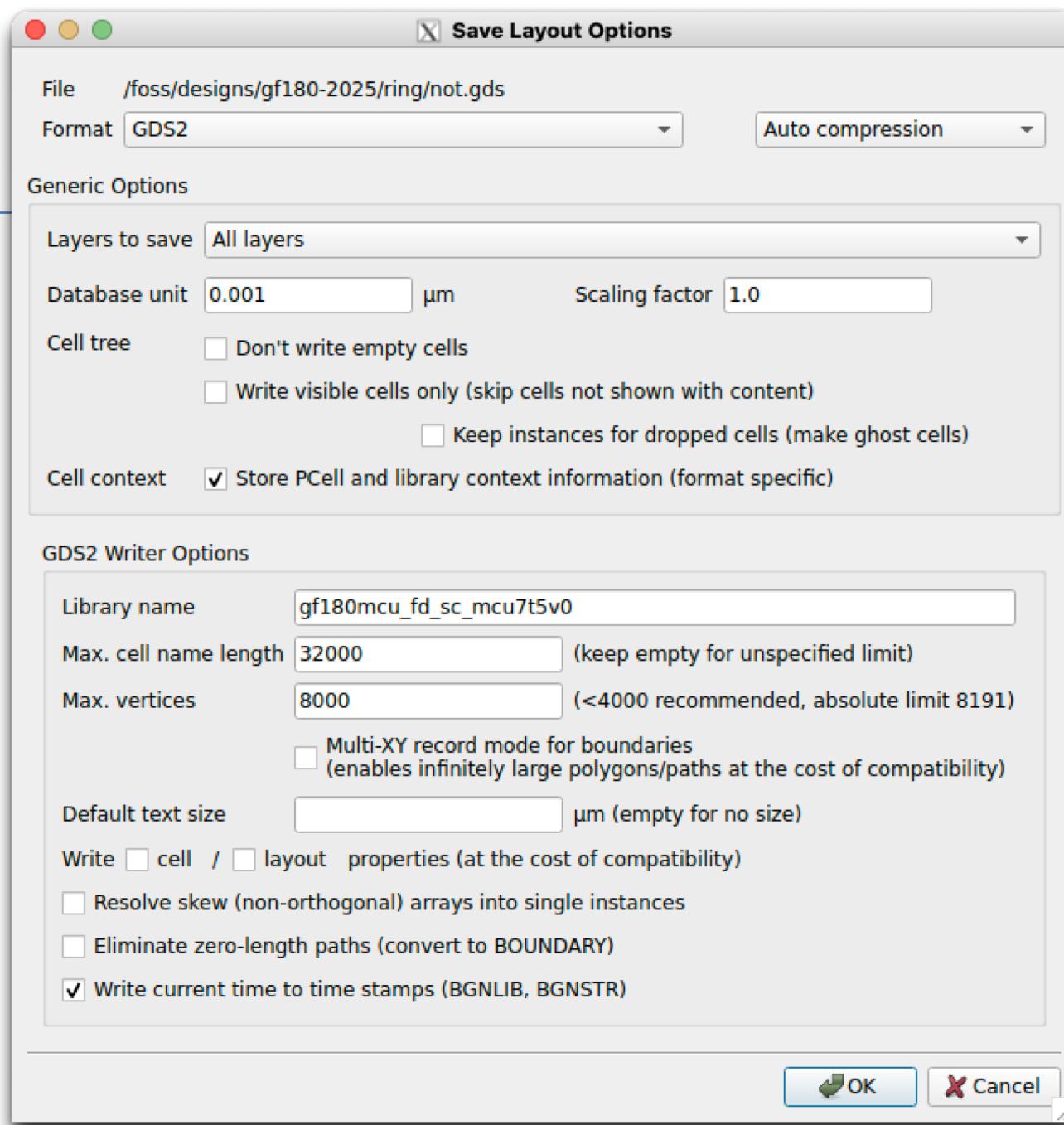




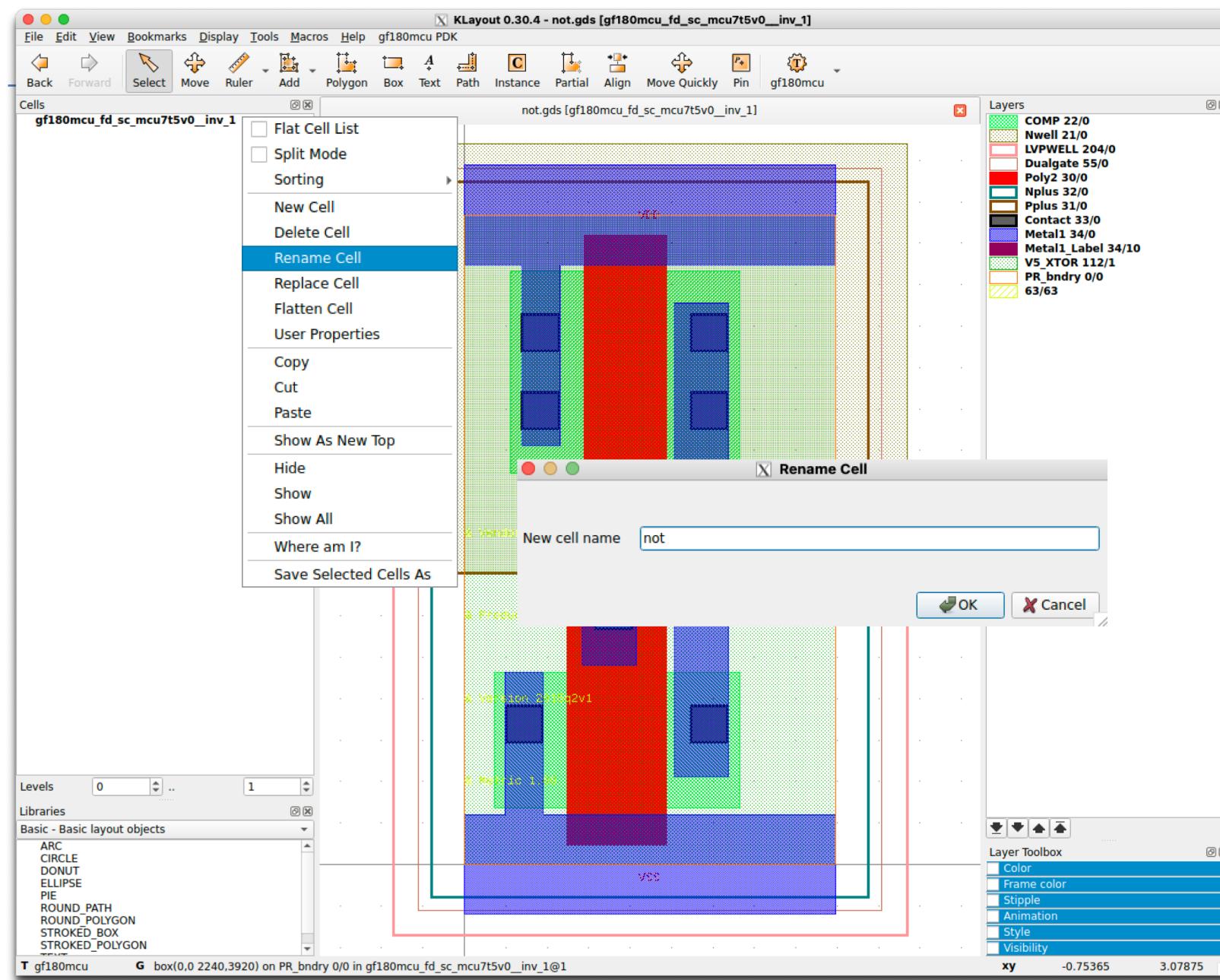
2025.11



2025.11

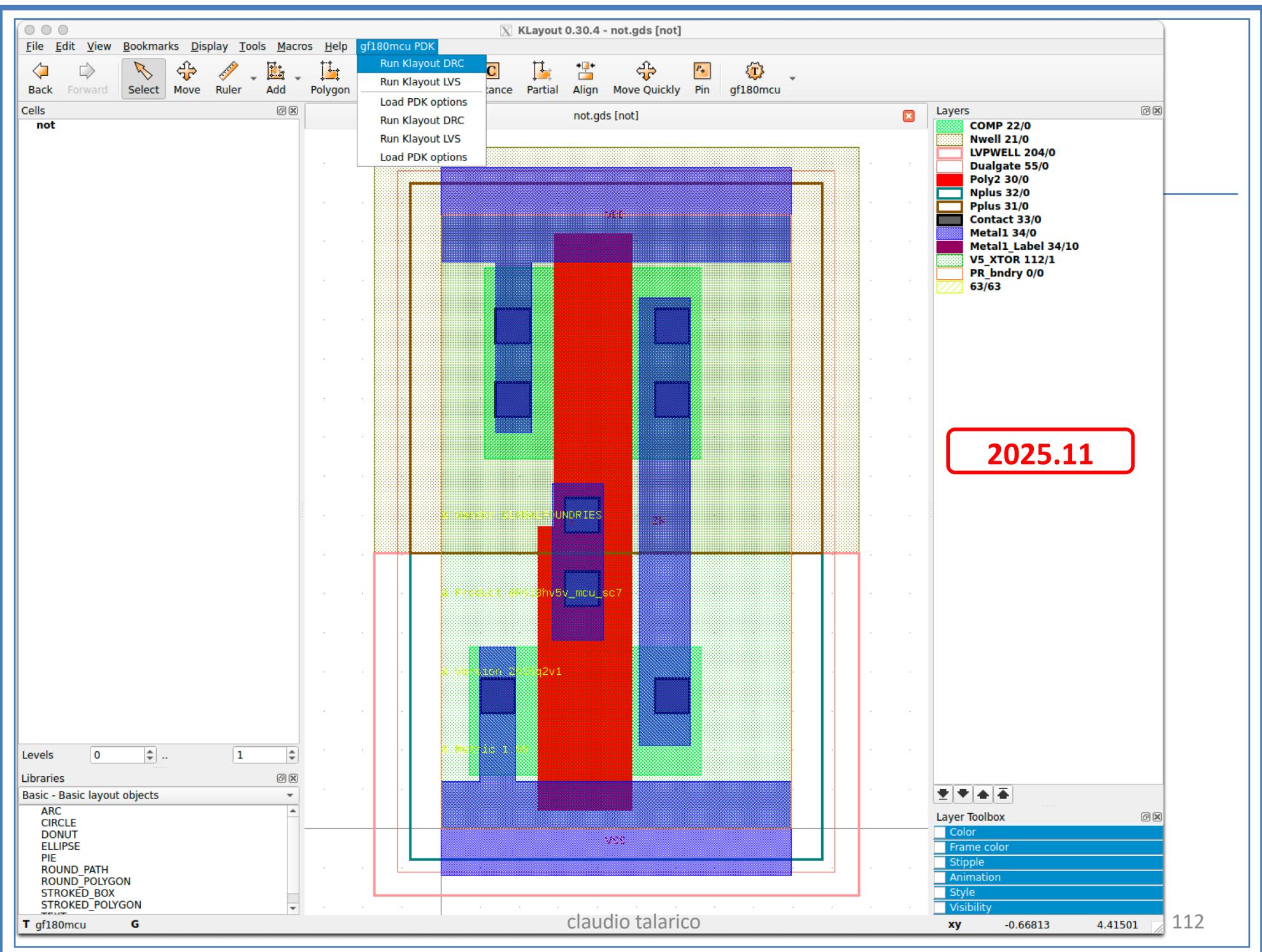


```
/foss/designs/gf180-2025/ring > ke -l gf180mcu_PK.lyp not.gds
```

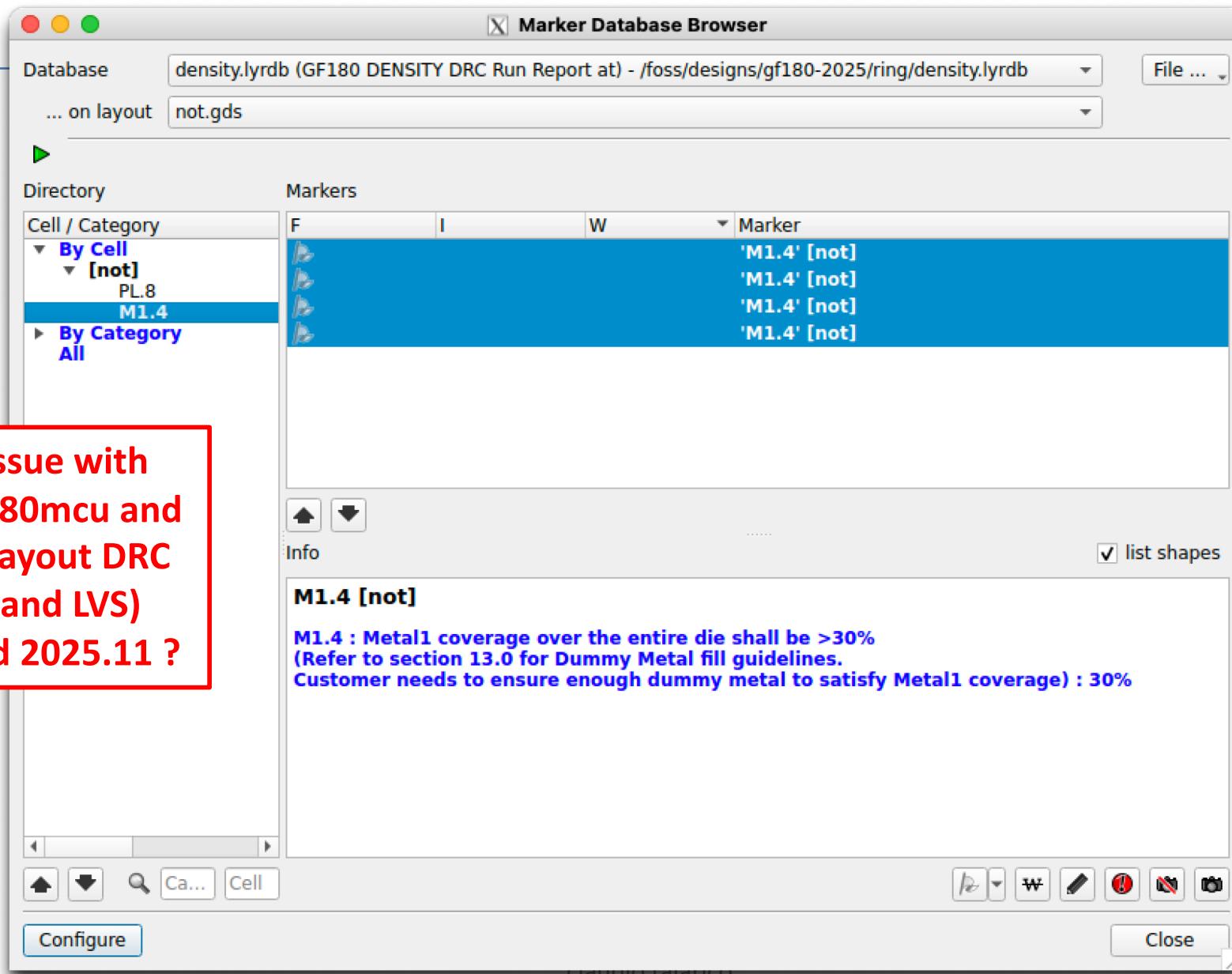


2025.11

111



# The standard cell has both Poly and M1 density violations



# Appendix: inv\_orig using 2025.07

LMB

/foss/designs/gf180-2025/ring > xschem inv\_orig.sch

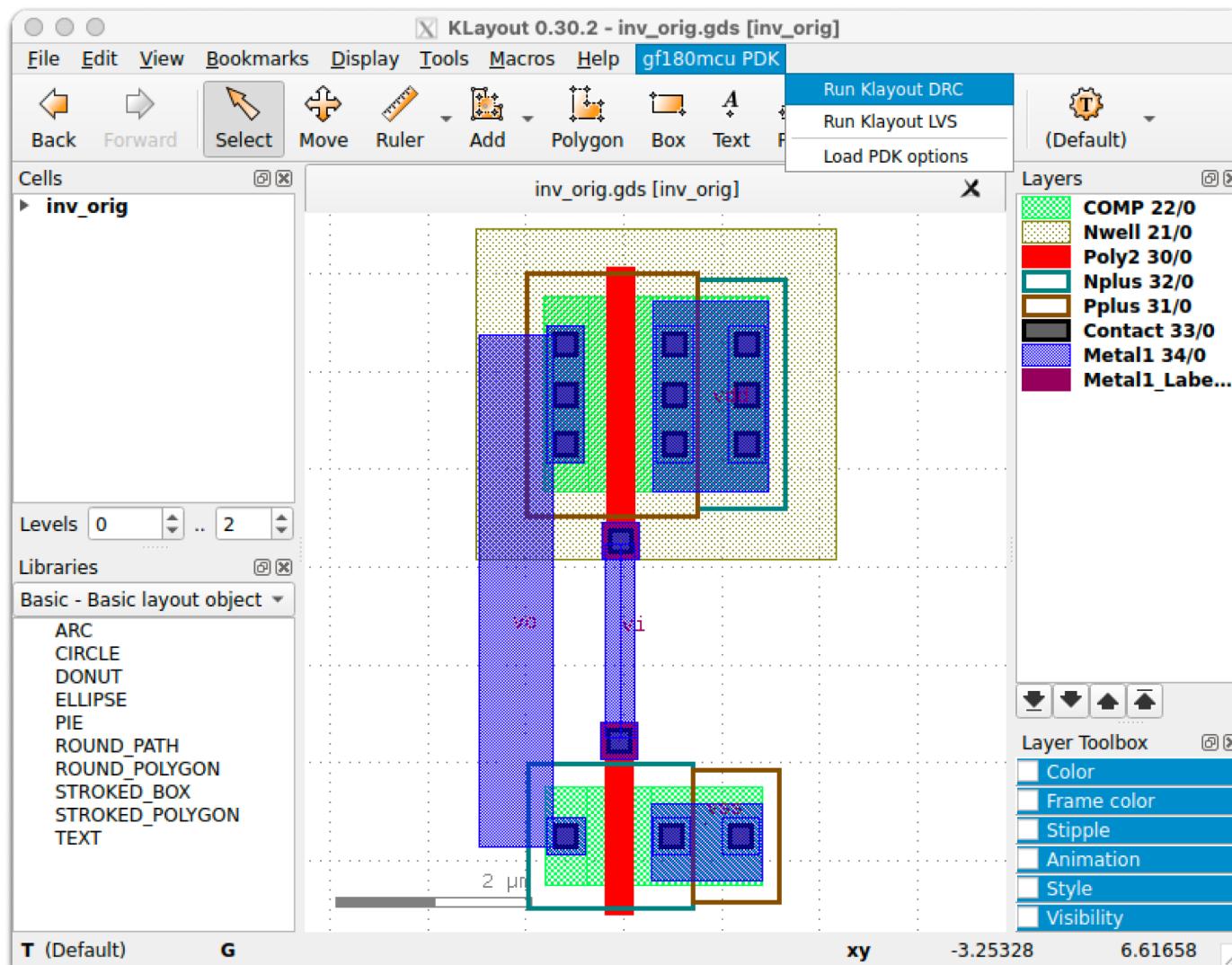
The screenshot shows the xschem application window titled "xschem - inv\_orig.sch". The menu bar includes File, Edit, Options, View, Properties, Layers (highlighted in green), Tools, Symbol, Highlight, Simulation, Help, Netlist, Simulate, and Waves. A red arrow points from the text "LMB" to the "Netlist" menu item. The "Netlist" menu is open, displaying options such as "Set netlist Dir", "Set top level netlist name", "Show netlist after netlist command", "Keep symbols when traversing hierarchy", "Use netlist directory", "Use 'simulation' dir in schematic dir", "Use 'simulation/[schname]' dir in schematic dir", "Configure simulators and tools", "List running sub-processes", "View last job data", "View last job errors", "Utile Stimuli Editor (GUI)", "Utile Stimuli Translate", "Shell [simulation path]", "Edit Netlist", "Send highlighted nets to viewer", and "Changelog from current hierarchy". The keyboard shortcut "Shift+A" is listed next to "Set netlist Dir". Below the menu is a toolbar with icons for zoom, orientation, and other functions. The main workspace displays a schematic diagram of a single NMOS inverter (M1) with its source connected to VSS. The drain terminal is labeled "D" and the gate terminal is labeled "G". The channel width is specified as "nf=1" and the channel length as "1 x 1u / 0.28u". The netlist output is shown in a terminal window:

```
/foss/designs/gf180-2025/ring > cat inv_orig.spice
** sch_path: /foss/designs/gf180-2025/ring/inv_orig.sch
.subckt inv_orig vdd vss vi vo
*.PININFO vdd:B vss:B vi:I vo:0
M1 vo vi vss vss nfet_03v3 L=0.28u W=1u nf=1 m=1
M2 vo vi vdd vdd pfet_03v3 L=0.28u W=2u nf=1 m=1
.ends
```

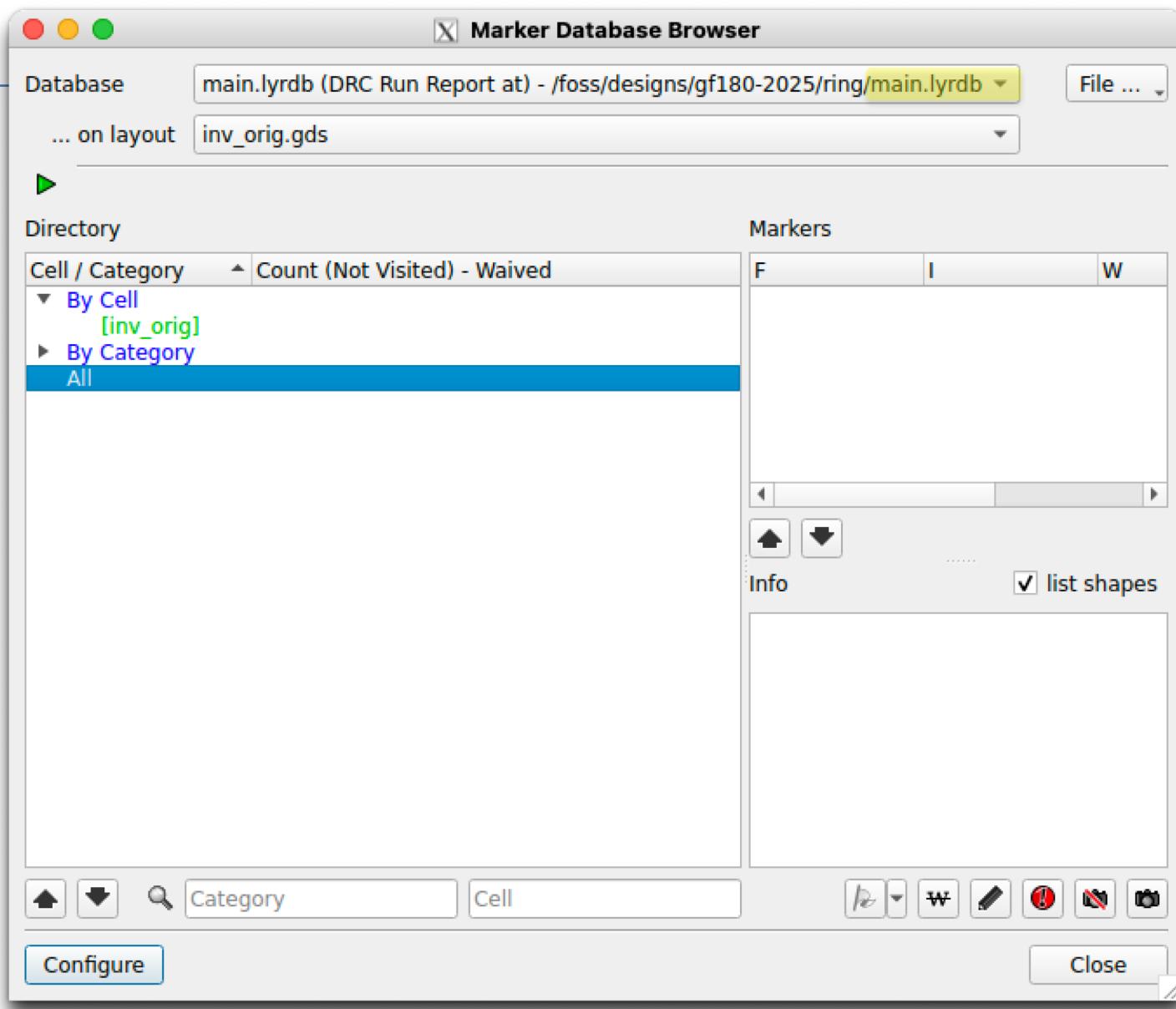
A context menu is open over the inverter symbol, listing options: "LVS netlist + Top level is a .subckt", "Upper case .SUBCKT and .ENDS", "Top level is a .subckt", "Set 'lvs\_ignore' variable", and "Use 'spiceprefix' attribute". The status bar at the bottom shows "SNAP: 10 GRID: 20 MODE: spice Stretch: 0 810 -110 - select". The footer of the slide contains the text "Claudio Talarico" and the page number "114".

# Appendix: inv\_orig using 2025.07

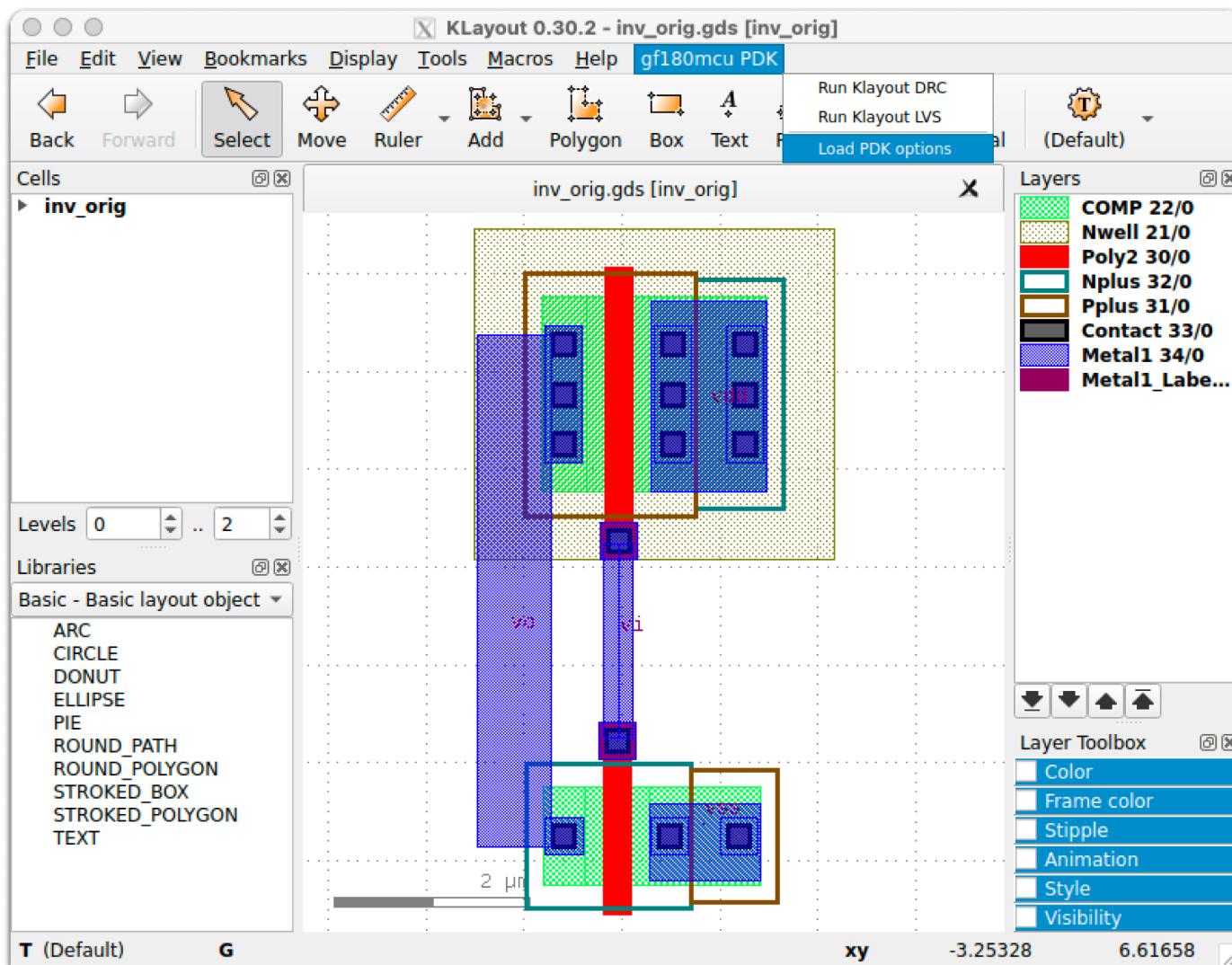
```
/foss/designs/gf180-2025/ring > ke -l gf180mcu_PK.lyp inv_orig.gds
```



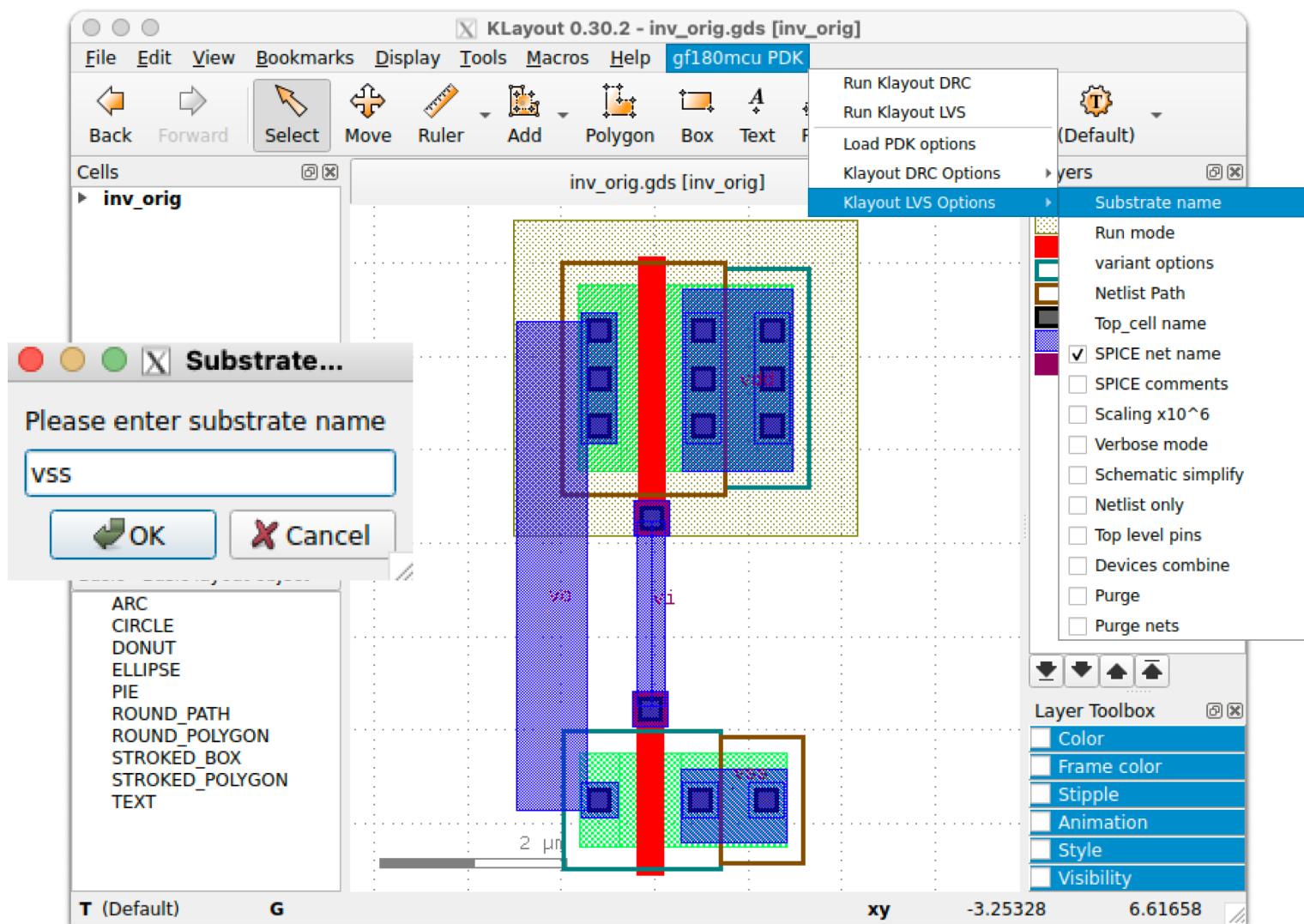
# Appendix: inv\_orig using 2025.07



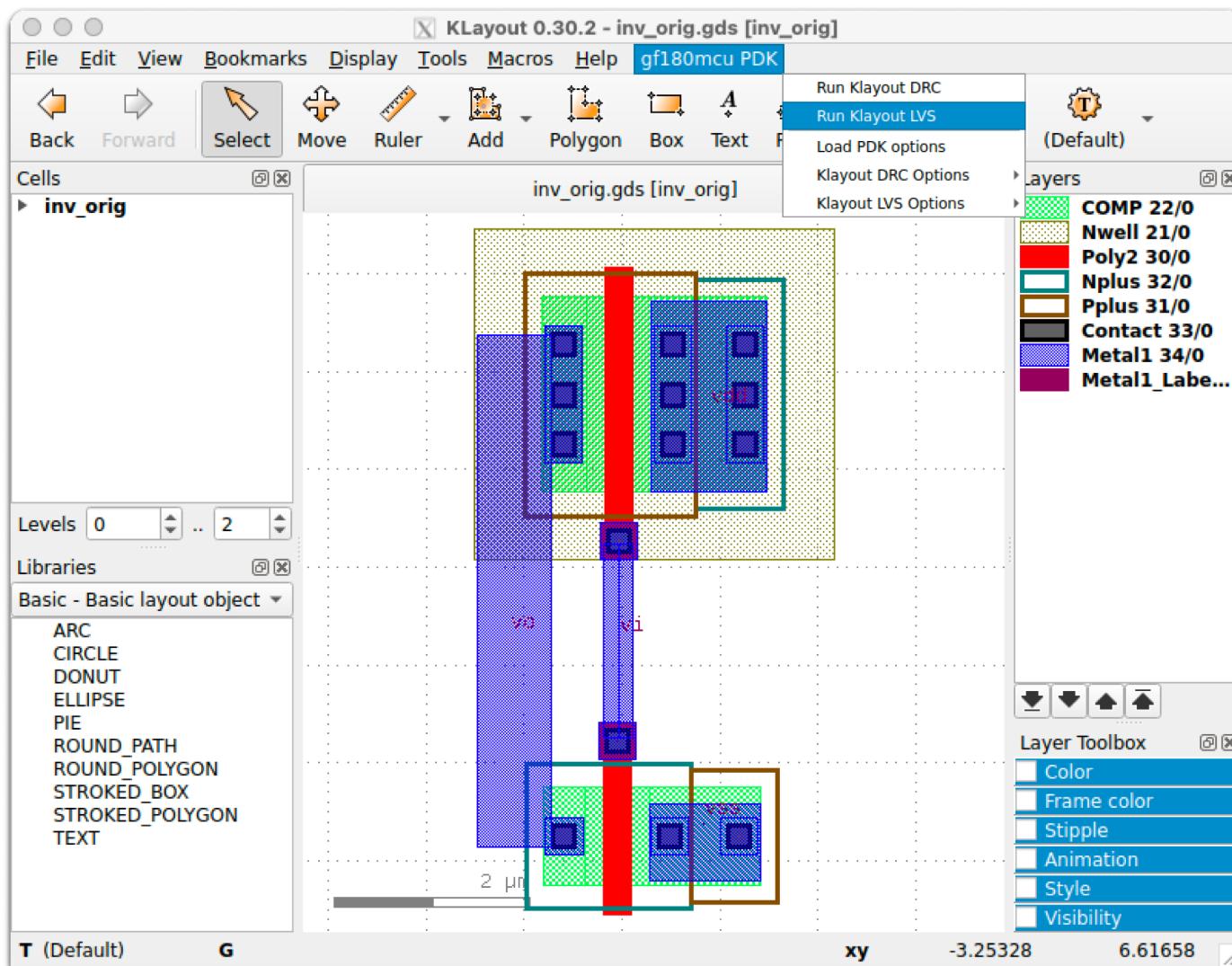
# Appendix: inv\_orig using 2025.07



# Appendix: inv\_orig using 2025.07



# Appendix: inv\_orig using 2025.07



# Appendix: inv\_orig using 2025.07

The screenshot shows the Netlist Database Browser window with the following details:

- Netlist:** LVS
- ... on layout:** inv\_orig.gds
- Cross Reference Tab:** Selected
- Circuits:** inv\_orig
- Objects:** A table showing the cross reference between the circuit objects and their corresponding layout and reference names.

Objects	Layout	Reference
inv_orig ↔ INV_OF	inv_orig	INV_ORIG
↳ Pins		
↳ vdd ↔ VDD	vdd (3)	VDD (3)
↳ vi ↔ VI	vi (3)	VI (3)
↳ vo ↔ VO	vo (3)	VO (3)
↳ vss ↔ VSS	vss (3)	VSS (3)
↑ Nets		
↑ vdd ↔ VDD	vdd (3)	VDD (3)
↑ vi ↔ VI	vi (3)	VI (3)
↑ vo ↔ VO	vo (3)	VO (3)
↑ vss ↔ VSS	vss (3)	VSS (3)
↳ Devices		
↳ nfet_03v3	\$2 / nfet_03v3 [L=0.28, '1 / NFET_03V3 [L=0.28, W=1]	
↳ pfet_03v3	\$1 / pfet_03v3 [L=0.28, '2 / PFET_03V3 [L=0.28, W=2]	

- Buttons:** Configure, Probe Net, Lock, Close

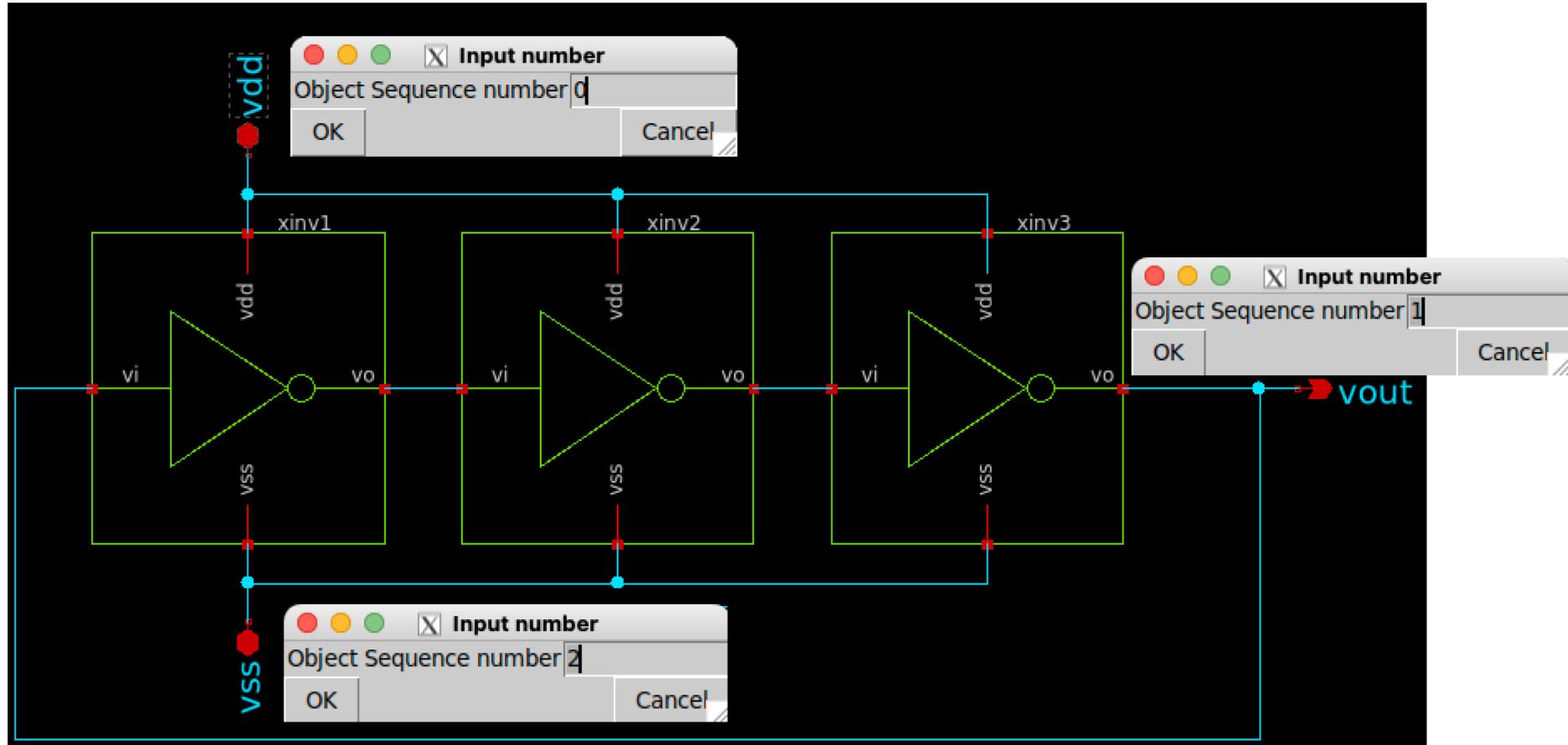
# Appendix: inv\_orig using 2025.07

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```
/foss/designs/gf180-2025/ring > cat inv_orig_extracted.cir
* Extracted by KLayout with GF180MCU LVS runset on : 16/12/2025 05:05

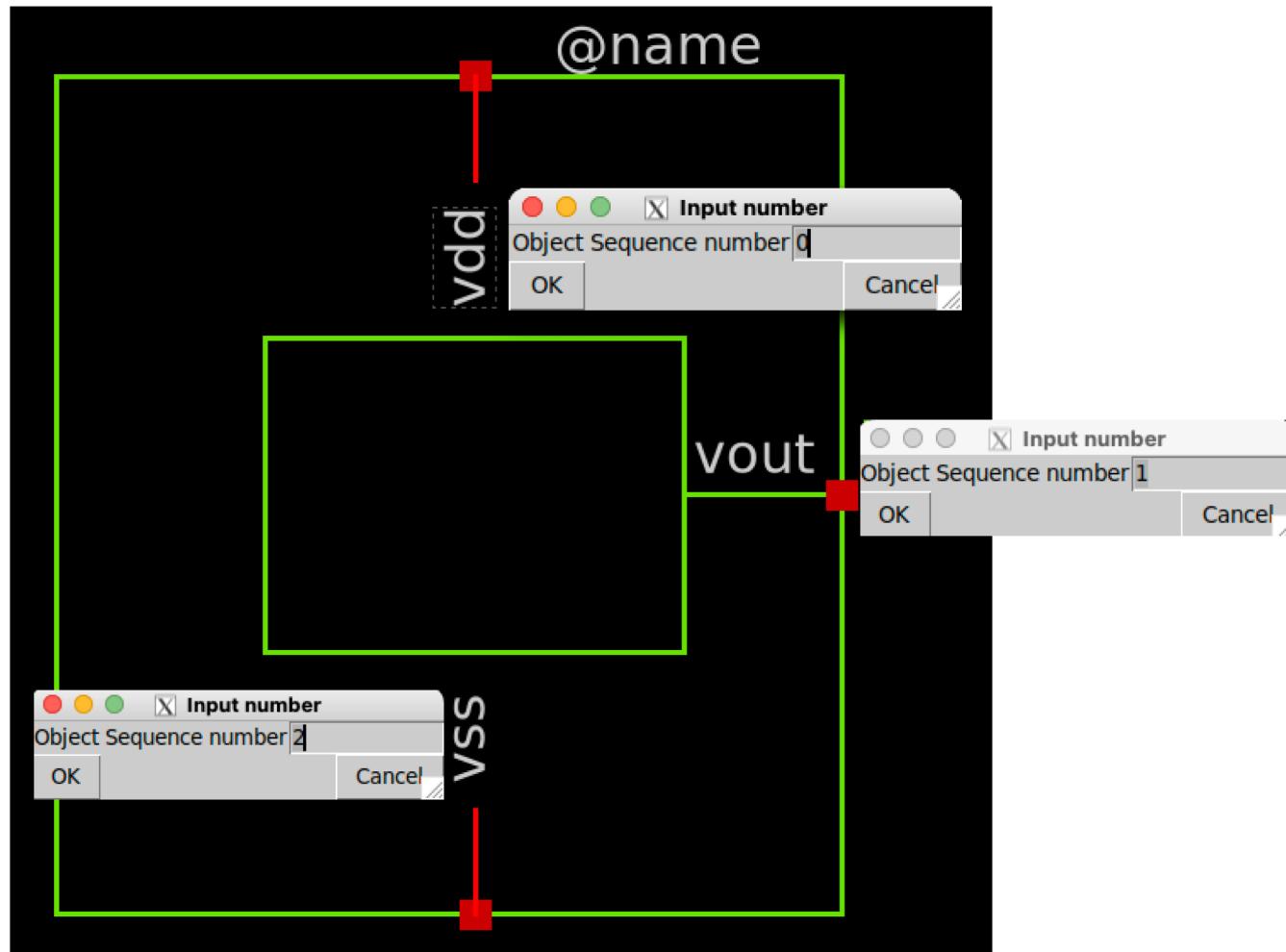
.SUBCKT inv_orig vdd vo vss vi
M$1 vdd vi vo vdd pfet_03v3 L=0.28U W=2U AS=1.3P AD=1.3P PS=5.3U PD=5.3U
M$2 vss vi vo vss nfet_03v3 L=0.28U W=1U AS=0.61P AD=0.61P PS=3.22U PD=3.22U
.ENDS inv_orig
```

# Changing the order of the pins in the schematic and its associate symbol



- Click on the first pin, then hit shift-s and number it 0.
- Repeat the process for each of the pins
- `.subckt ring vdd vout vss`

# Changing the order of the pins in the schematic and its associate symbol



- Click on the first pin, then hit shift-s and number it 0.
- Repeat the process for each of the pins