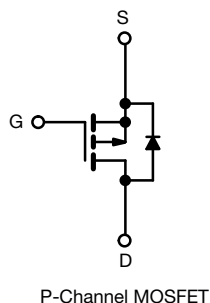
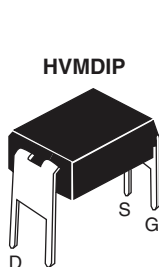


Power MOSFET



FEATURES

- For automatic insertion
- Compact, end stackable
- Fast switching
- Low drive current
- Easy paralleled
- Excellent temperature stability
- P-channel versatility
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness.

The p-channel HVMDIPs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common n-channel HVMDIPs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-channels HVMDIPs are intended for use in power stages where complementary symmetry with n-channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

PRODUCT SUMMARY

V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.50
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	3.8	
Q_{gd} (nC)	4.1	
Configuration	Single	

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD9010PbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	- 50	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	- 8.8	
Linear derating factor		0.01	W/ $^\circ\text{C}$
Inductive current, clamped	$L = 100\ \mu\text{H}$ see fig. 14	I_{LM}	A
Inductive current, unclamped (avalanche current)	see fig. 15	I_L	
Maximum power dissipation	$T_C = 25^\circ\text{C}$	P_D	W
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	For 10 s	300 ^d	

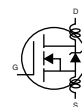

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = -25$ V, starting $T_J = 25^\circ\text{C}$, $L = 52$ mH, $R_g = 25\ \Omega$, $I_{AS} = -2.0$ A (see fig. 12)
- $I_{SD} \leq -4.0$ A, $dI/dt \leq 75$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

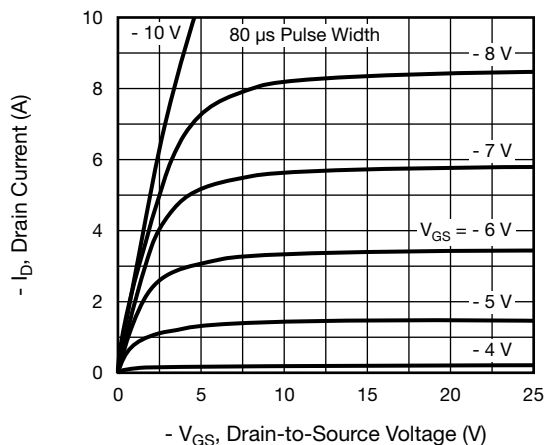
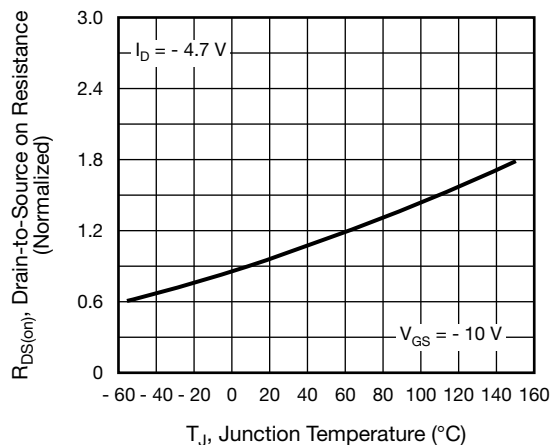
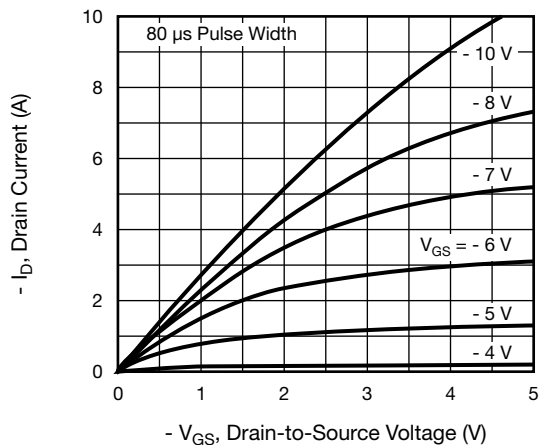
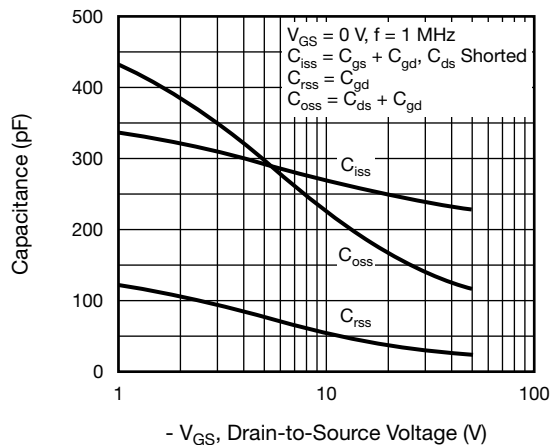
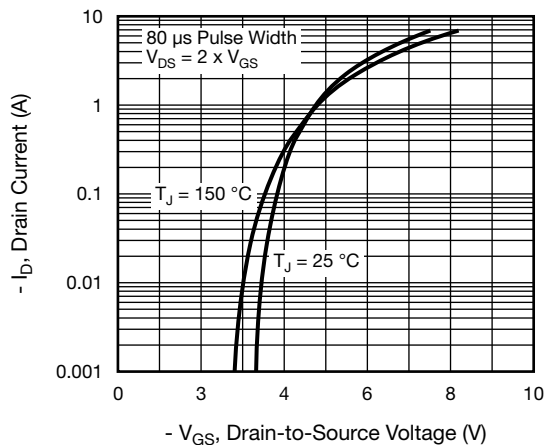
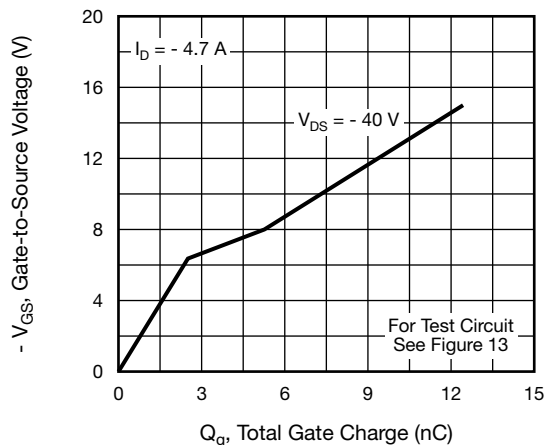
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

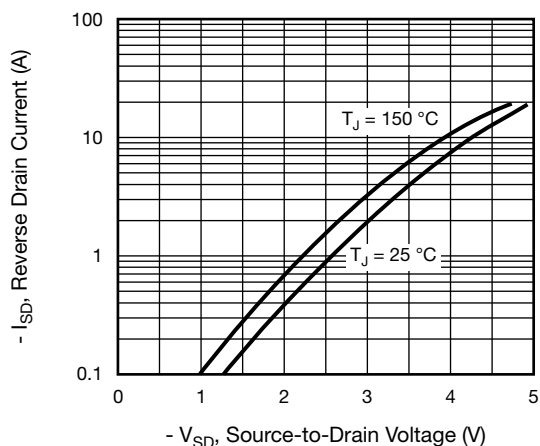
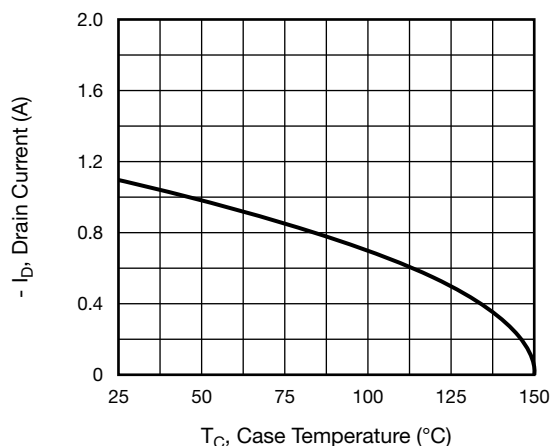
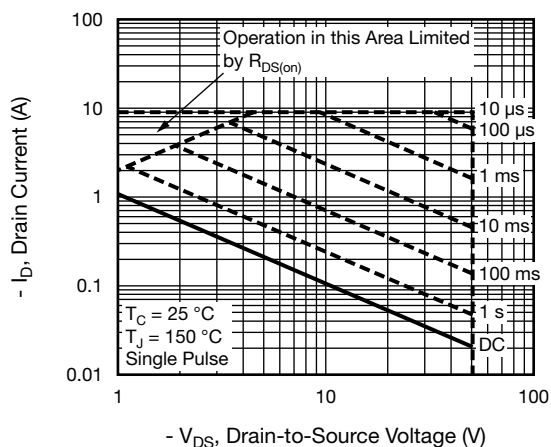
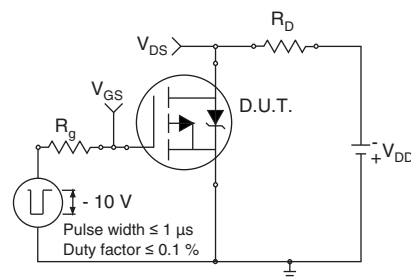
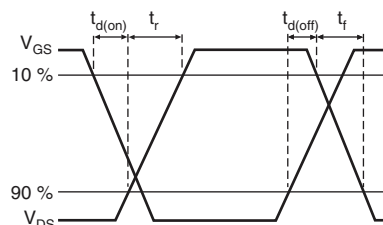
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 50	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.091	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 50 V, V _{GS} = 0 V		-	-	- 250	μA
		V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 125 °C		-	-	- 1000	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V	V _{DS} > I _{D(on)} × R _{DS(on)} max.	- 1.1	-	-	A
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 0.58 A ^b	-	0.35	0.50	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 20 V, I _D = - 2.4 A		1.7	2.5	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	240	-	pF
Output Capacitance	C _{oss}			-	160	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 4.7 A, V _{DS} = 0.8 V see fig. 6 and 13 ^b	-	7.2	11	nC
Gate-Source Charge	Q _{gs}			-	2.5	3.8	
Gate-Drain Charge	Q _{gd}			-	2.7	4.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 25 V, I _D = - 4.7 A R _g = 24 Ω, R _D = 5.6 Ω, see fig. 10 ^b		-	6.1	9.2	ns
Rise Time	t _r			-	47	71	
Turn-Off Delay Time	t _{d(off)}			-	13	20	
Fall Time	t _f			-	39	59	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.1	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 8.8	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 0.7 A, V _{GS} = 0 V ^b		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 4.7 A, dI/dt = 100 A/μs ^b		33	75	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.090	0.22	0.52	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

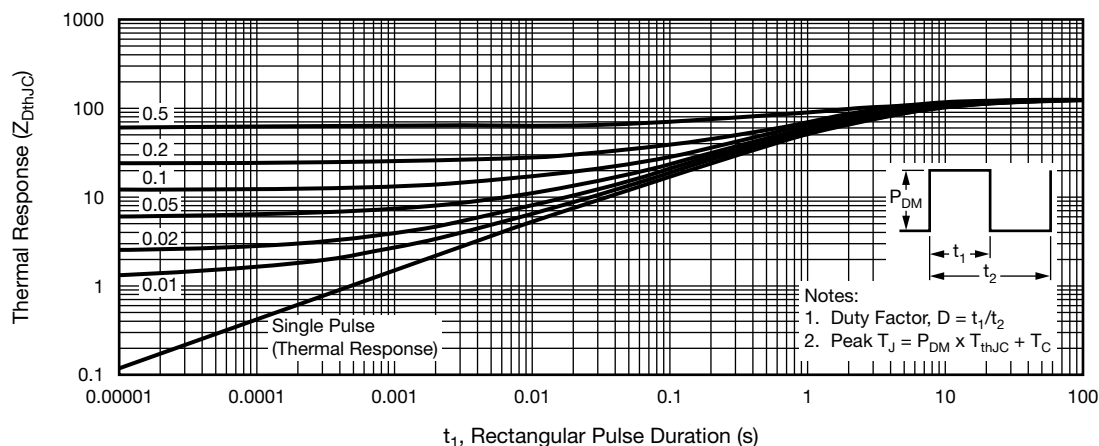
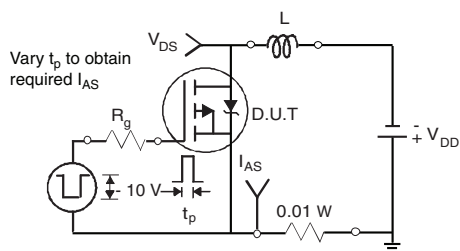
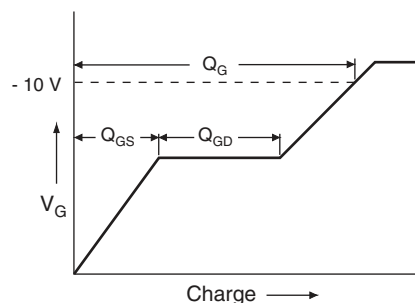
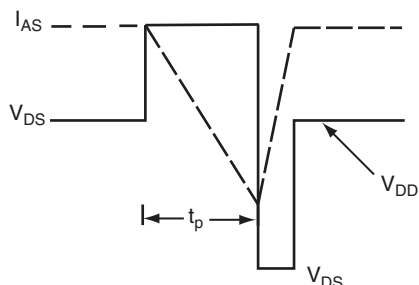
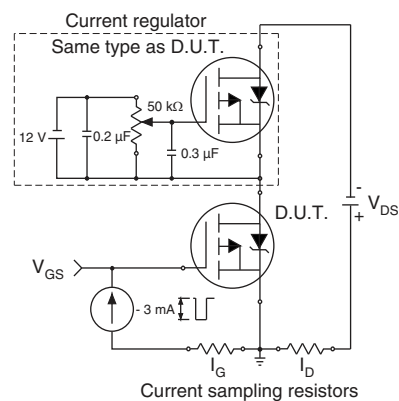
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 13a - Basic Gate Charge Waveform

Fig. 12b - Unclamped Inductive Waveforms

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

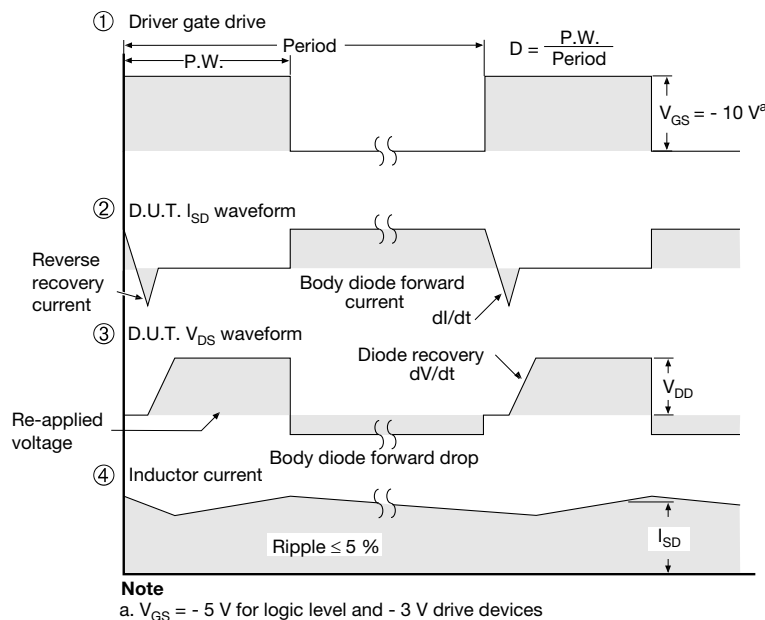
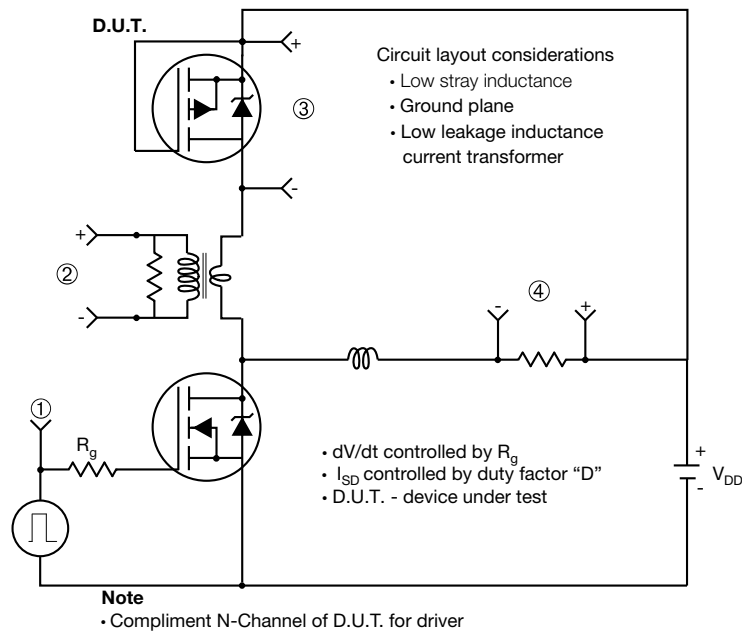


Fig. 14 - For P-Channel

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