Layout of a 4T (Four Transistor) CMOS Active Pixel Sensor

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***Abstract*—This paper is a continuation of our previous title "Design of a 4T (Four Transistor) CMOS Active Pixel Sensor ", which investigates the layout of the conventional 4T (four transistor) CMOS Active Pixel Sensor (APS). Cadence Virtuoso is used to design the schematics and layout utilizing silterraC13 PDK. Calibre allows for Design Rule Check (DRC) and Layout Versus Schematic (LVS) to benchmark and compare the schematics with the layout of the 4T CMOS APS. The single 4T CMOS APS is then arranged into array format for both schematic and layout, of which its dimensions are based on the QVGA format, 320 pixels x 240 pixels. Bus expansion techniques were employed to label all nets present on the 320x240 pixel array. The result of this study allows implementation of 4T CMOS APS in QVGA format, or other larger sizes for future works.**

Keywords—4T CMOS APS, QVGA, Cadence Virtuoso, Calibre, silterraC13 PDK, DRC, LVS, bus expansion.

I. Introduction

Following our previous discussion on the design and simulation of a 4T CMOS APS, this report presents the physical layout of a single 4T CMOS APS, and subsequently arranged into QVGA format of 320x240 pixel array.

Physical layout, or more commonly known as custom layout in the analog design flow is the process of placing individual components, such as instances (transistors, resistors, capacitors) and making connections using wires (nets) in a way that satisfies the design specifications whilst following manufacturing guidelines provided by the foundries. Since various types of materials are used in the fabrication process, of which the IC is produced layer by layer, custom layout allows the designer to interact with the placement and interconnection using different layers. The polysilicon layer is used for transistor gates, and metals of different layers (metal1, metal2, metal3 etc.) are used in routing and making connections between components.

DRC is a process that checks whether the custom layout of an integrated circuit adheres to the manufacturing design rules specified by the foundry or semiconductor fabrication process. These design rules define constraints and limitations related to dimensions, spacing, alignment, and other factors that ensure manufacturability and reliability of the final chip. DRC tools compare the layout against these rules and flag any violations, allowing designers to rectify them before fabrication [4].

LVS, on the other hand, is a process that verifies the consistency between the custom layout and its corresponding schematic representation. It ensures that the physical layout accurately reflects the intended circuit functionality as described in the schematic. LVS tools compare the connectivity and electrical properties of the layout against the schematic netlist, verifying that they match. Any discrepancies or inconsistencies between the two are reported for correction [5].

Both DRC and LVS are critical for ensuring the quality and reliability of integrated circuits. By performing DRC, designers can identify and rectify layout violations that may lead to manufacturing issues or functional problems. LVS helps verify the correctness of the layout with respect to the circuit design, preventing errors that could affect the circuit's performance or functionality. Together, these processes contribute to the successful layout design of reliable and functional integrated circuits.

II. Methodology

A 4T CMOS APS pixel structure was built in Cadence Virtuoso in schematic format. The circuit was constructed using the minimum length and width NMOS transistors, following the given lab sheet [1]. The pixel structure was stripped of any driving sources, namely the source follower biasing transistor (MSFB) and the current mirror transistor (MCM), which constitutes a four-transistor design of an active pixel sensor. Necessary ports such as VDD, VTX, VRST, VRSEL, VOUT and GND were created by pin placements. A cellview symbol of the corresponding circuit is then created and saved.

The Virtuoso Layout tool was used to create a physical layout for the 4T CMOS APS cell. From the toolbar, accessing Connectivity > Generate > All from source allowed for the existing layouts of NMOS transistors from the PDK (process design kit) to be extracted and placed onto the layout area. A floorplan of 10um x 10um was created as a constraint guide for the layout. The layout design will be following the lab sheet which prioritizes fill factor [1].

The layout was proceeded by running DRC (design rule check) using the Calibre tool to ensure that the layout conformed to the fabricators' manufacturing capabilities. If any DRC errors appeared, they were resolved and rerun until the DRC run was cleared successfully. Then, LVS (layout versus schematic) in which Calibre verified that the behaviour of both schematic and layout matched. The LVS

stage was passed when Calibre outputs “CORRECT” in its report.

Then, a new cell schematic is created to place the symbol of a single 4T CMOS APS into a QVGA format 320x240 array. The nets are connected as intended and bus expansion technique allows for all nets to be labelled correctly. The same step is employed in layout where the 320x240 pixel array is created by joining the previously designed single 4T CMOS APS. Finally, DRC and LVS checks are ran through the APS array to ensure that the design is behaving as intended.

III. NMOS Transistor Parameters

By accessing the technology files in the PDK, the electrical properties and physical dimensions of MOSFETs, in which NMOS parameters can be obtained. After locating the PDK directory, the spectre model directory within it is accessed. Since silterraC13 MOSFETs follows BSIM4 standard the threshold voltage (vth0), gate oxide thickness (toxe), channel length modulation coefficient (plcm), charge carrier mobility (u0), donor concentration (ndep), acceptor concentration (pdep), breakdown voltage (bvs/bvd), minimum length (lmin) and minimum width (wmin) are found and described below in Table 1. These parameters are utilized in the implementation of transistors for 4T CMOS APS schematic and layout design.

TABLE 1. PARAMETERS OF NMOS IN PROCESS DESIGN KITS (PDK)

PDK Name	silterraC13
Model Name	nm_hp: 1.2V NMOS Thin Oxide device
Threshold Voltage, vth0	0.229
Gate Oxide Thickness, toxe	2.4948e-009
Channel Length Modulation Coefficient, pclm	0.2996
Charge Carrier Mobility, u0	2.929000e-002
Donor Concentration, ndep	1e+017
Breakdown Voltage, bvs/bvd	10
Minimum Length, lmin	130e-009
Minimum Width, wmin	150e-009

IV. Results

A. Schematic Circuit of the 4T CMOS APS

The 4T CMOS APS circuit is shown in Fig. 1 below, constructed using four transistors namely the photodiode transistor (MPD), the reset transistor (MRST), the source follower transistor (MSF) and the row-select switch transistor (MRSEL). Necessary ports such as VDD, VTX, VRST, VRSEL, VOUT and GND were created by pin placements. The GND port connects all the bulk of the NMOS transistors.

The minimum dimensions of NMOS transistor of the silterraC13 pdk is used where lmin = 130nm and wmin = 150nm. Minimum dimensions allow for a smaller transistor area on the layout, where the photodiode area can occupy more space and a layout designed to prioritize fill factor is achieved.

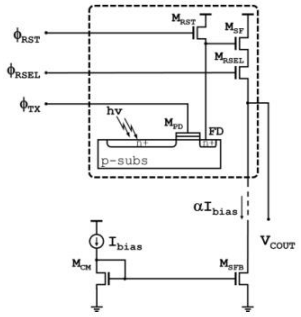

Fig. 1. Circuit design of 4T CMOS APS with external sources.

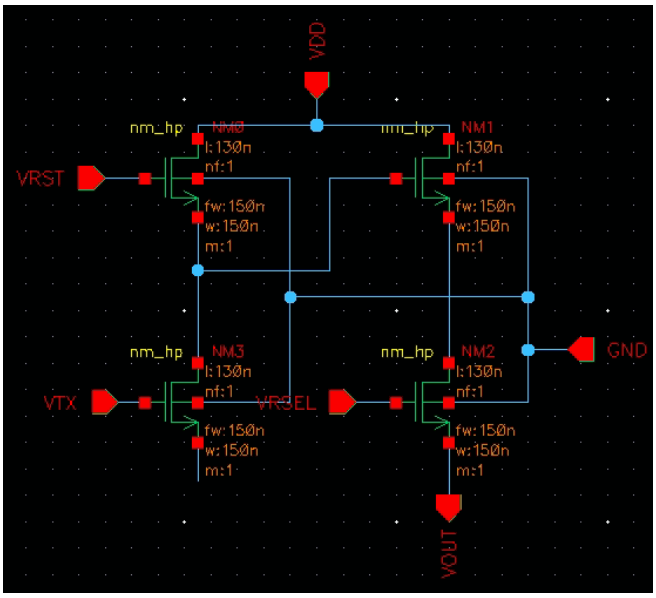

Fig. 2. Schematic of the 4T CMOS APS with ports.

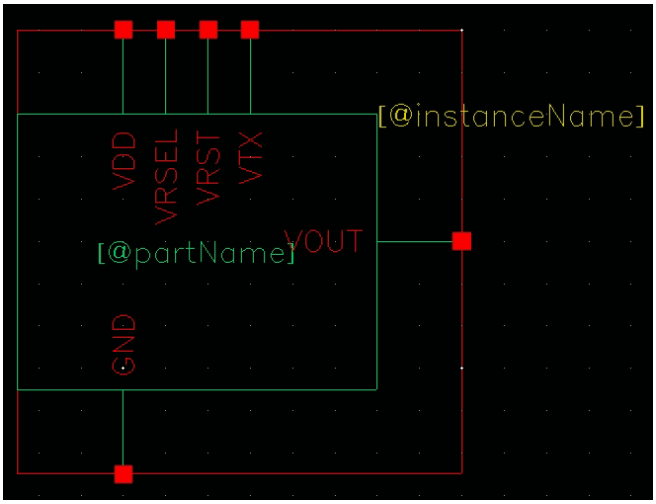

Fig. 3. Symbol of the 4T CMOS APS.

Fig. 2 follows Fig. 1’s circuit design to create a 4T CMOS APS pixel structure. The drain of the MPD is left empty to match for photodiode design in the layout process, of which the photodiode area will be as large as the design allows for. Fig. 3 shows the symbol cellview, where VDD, VRSEL, VTX and VRST are placed on top, VOUT is placed to the right, and GND is placed at the bottom to optimize for net routing for QVGA array arrangement at later stages.

B. Layout of the 4T CMOS APS

The layout is a cell view where the physical layer of the cell is constructed by drawing polygons using the Virtuoso tool. The goal is to produce a physical layout in which it does not challenge any DRC errors, which is a specification by the foundries to ensure there are no faults such as shorts or opens due to manufacturing defects. LVS errors should also be zero since it translates to a layout that matches the schematic in terms of number of instances, ports and nets.

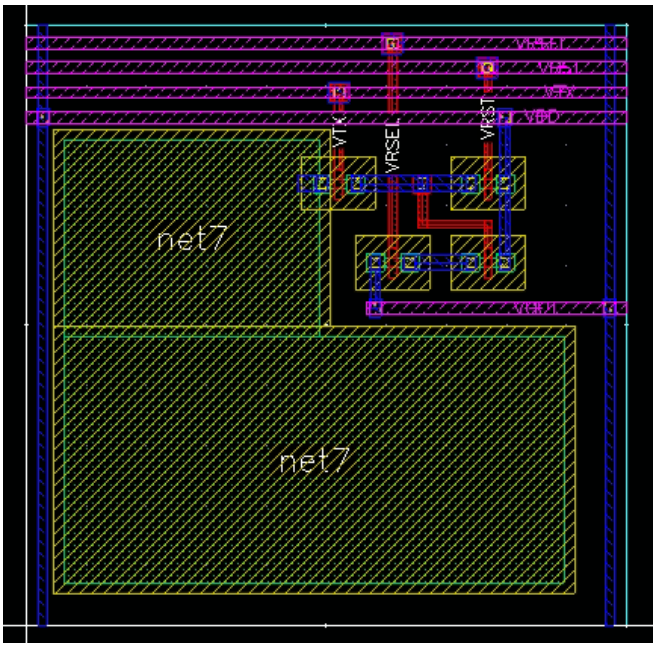

Fig. 4. Layout of the 4T_CMOS_APS cell [1] [2] [3].

Fig. 4 shows the layout of the 4T CMOS APS circuit, of which the green area (island layer) represents the photodiode area. The smaller island has dimensions of 4.255um x 3.275um whilst the larger island has dimensions of 8.31um x 4.1um. The total photodiode area comes up to 47.91 micrometres squared. Comparing to total APS area of 100 micrometres squared, the photodiode area represents a fill factor of 47.91%.

The blue strips signify nets in the metal1 layer. The left vertical strip signifies VDD, and the right vertical strip signifies VOUT, of which its height is 10um, fitting the entire height of the APS, and the width is 0.16um, the minimum requirement for clearing DRC in the later stages. There are also interconnections of metal1 layers between the NMOS transistors of which the widths of vertical connections are 0.16um and widths of horizontal connections are 0.26um to follow the width of the transistor nets.

The pink strips represent the metal2 layer, which also make up the nets of the 4T CMOS APS. The metal2 layer nets are kept horizontal with a width of 10um and a height of 0.2um which is the minimum specified by DRC rules. The metal2 layer houses the ports including VRST, VRSEL, VTX. VDD and VOUT. The GND port and net is not specified as it is recognized as a global power net. Metal1 and metal2 can be connected through vias, represented by 2 layers stacking on top of each other with a 0.16um x 0.16um contact layer.

The red strips represent the polysilicon layer of which functions as the gates of the NMOS transistors. They are connected to metal1 and metal2 layers through vias, to allow for electrical inputs to activate the NMOS transistors.

The following portion explains the DRC process [6].

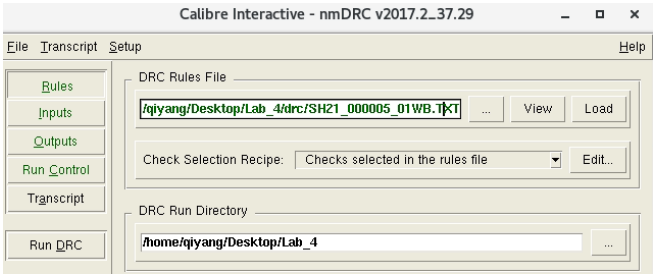

Fig. 5. Select DRC rules file in the Calibre tool.

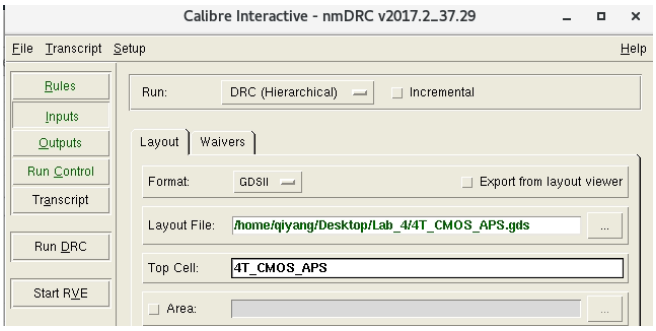

Fig. 6. Select GDSII file in the Calibre tool and "Run DRC".

```
----------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
----------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 1
TOTAL Original Layer Geometries: 65 (125)
TOTAL DRC RuleChecks Executed:   789
TOTAL DRC Results Generated:     0 (0)
```

Fig. 7. DRC is run successfully with zero errors found.

Fig. 5 shows the rules file which is sourced from the PDK. Fig. 6 shows the GDSII file which is a binary database file format and the industry standard for EDA data exchange of ICs. It can be generated through the Virtuoso Log of File > Export > Stream and outputting the GDSII file which is essential for DRC runs.

Fig. 7 shows that the layout of the 4T CMOS APS does not violate any DRC rules and is available to proceed with LVS. However, the DRC clearance does not occur on first try. Some memorable DRC errors include a) minimum metal1 area must be at least 0.122um – solved by stretching and area of metal1's which do not meet the requirement, b) metal2 side to side space to metal2 must be at least 0.18um – solved by having metal2 of different nets have a separation of 0.21um, c) metal1 end of line (at least 2 sides) to contacts must be at least 0.05um – solved by stretching the height of metal1 surrounding contacts with metal1 vias [7].

The following portion explains the LVS process [6].

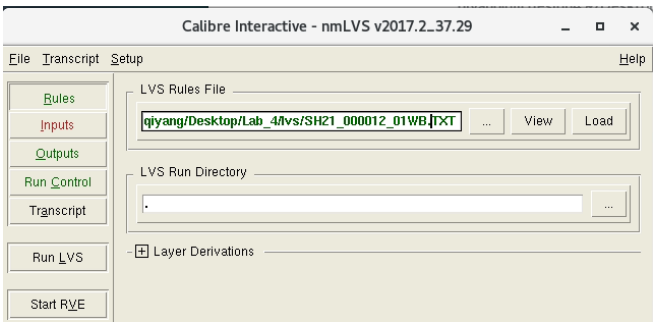

Fig. 8. Select LVS rules file in the Calibre tool.

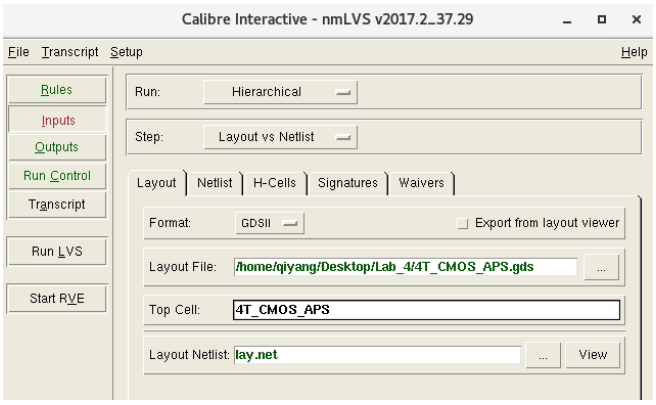

Fig. 9. Select GDSII file in the Calibre tool.

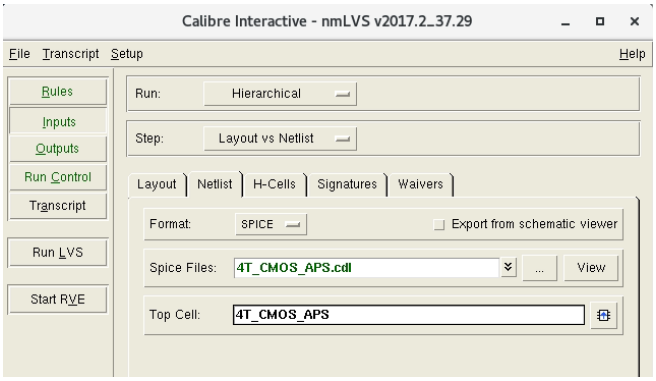

Fig. 10. Select CDL file in the Calibre tool and “Run LVS”.

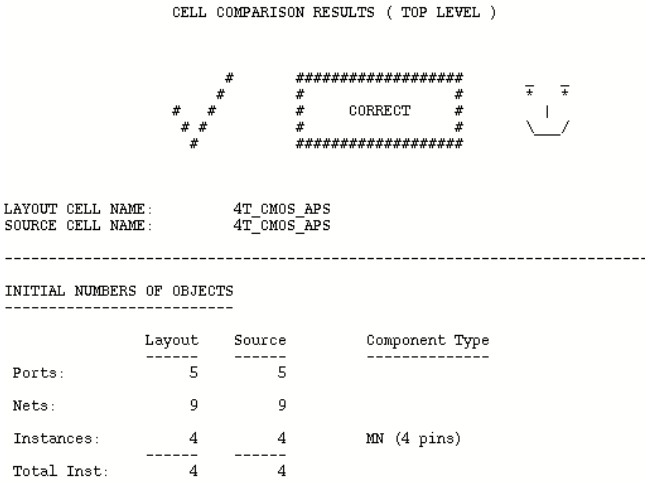

Fig. 11. LVS is run successfully with no errors found.

Fig. 8 shows the LVS rules file selected, while Fig. 9 and Fig. 10 takes in the GDSII and CDL files as input to compare the layout versus schematic. The CDL file can be generated through the Virtuoso Log of File > Export > CDL and selecting the schematic of the desired cell.

Fig. 11 shows that the LVS run is completed with zero errors, and thus the final step can be taken. Like prior DRC runs, is not a clean zero violation on first try. One of the most difficult violations to solve was having 0 ports on layout but 5 in source. The ports are VTX, VRSEL, VRST, VOUT and VDD. The violation is solved by labelling the respective nets using their respective metal text layers, not drawing layers. The GND port is ignored in the LVS as it is considered a global connection, and thus there is no need for a GND net or label in the layout as compared to the schematic.

C. APS Array Arrangement in QVGA Format

Since each individual pixels are modular, forming a QVGA format of 320 x 240 pixels just involves copy and pasting the pixels into that arrangement.

Firstly, a new cell schematic is created to produce the APS array. The 4T CMOS APS symbol is instantiated, copied, and arranged into an array of 320x240. Then all the ports are wired to relevant ports and interconnections between instantiations. The complete APS Array is shown in Fig.12 below.

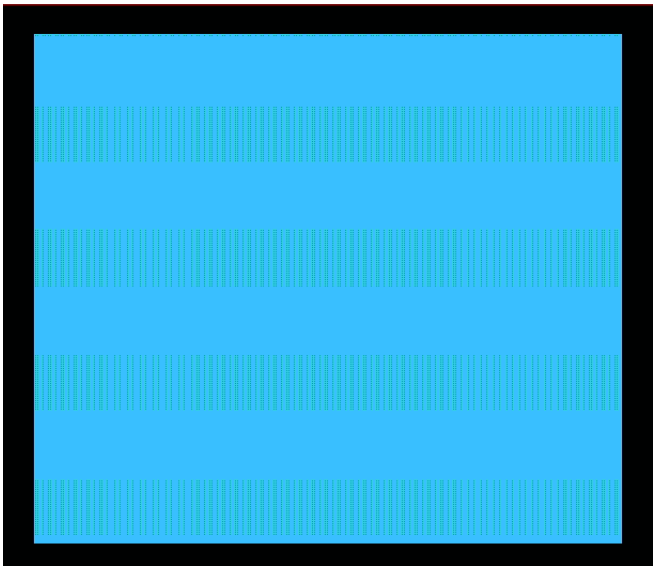

Fig. 12. Complete APS array in schematic cellview.

Zooming in close, referring to Fig. 13, allows us to observe the detailed interconnections to each port on each 4T CMOS APS. VTX, VRST, and VRSEL form horizontal nets extending the entire row allowing the entire row of APS to be activated by the same input pulses at once. VTX, VRST, and VRSEL are bus expanded downward for 240 rows with indices from 0 to 239. This allows each row to be controlled independently of one another. VOUT is routed similarly but it is extended through the entire column, allowing for VOUT of each column to be read independent of each other since it is bus expanded from 0 to 320. Since inputs are controlled by row and outputs are controlled by column, the APS can obtain

its exact pixel value independent of other APS. Hence, the operation of pixels in a row operating at the same time and outputting individual values, and then repeating down the rows to obtain the pixel values of an entire 320x240 frame is achieved. VDD and GND is routed both horizontally and vertically to all APS, meaning that all devices share the same VDD and GND. Hence VDD and GND does not require bus expansion.

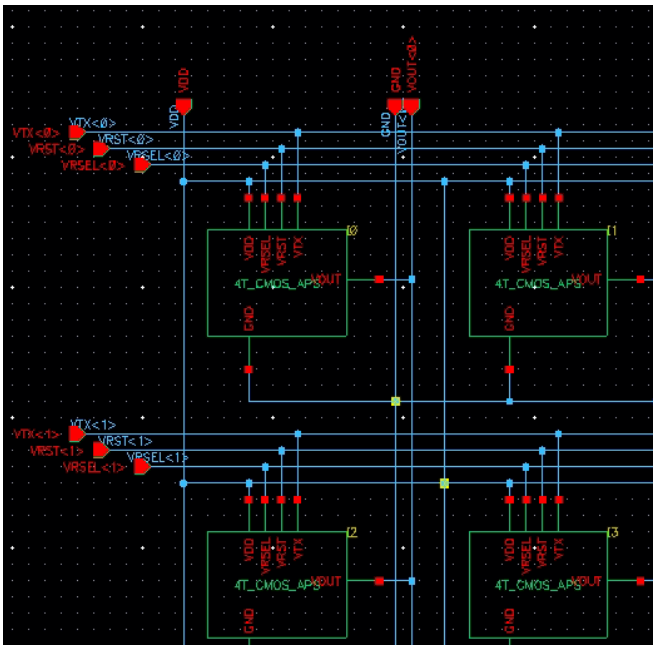

Fig. 13. Close up view of the APS array in schematic cellview.

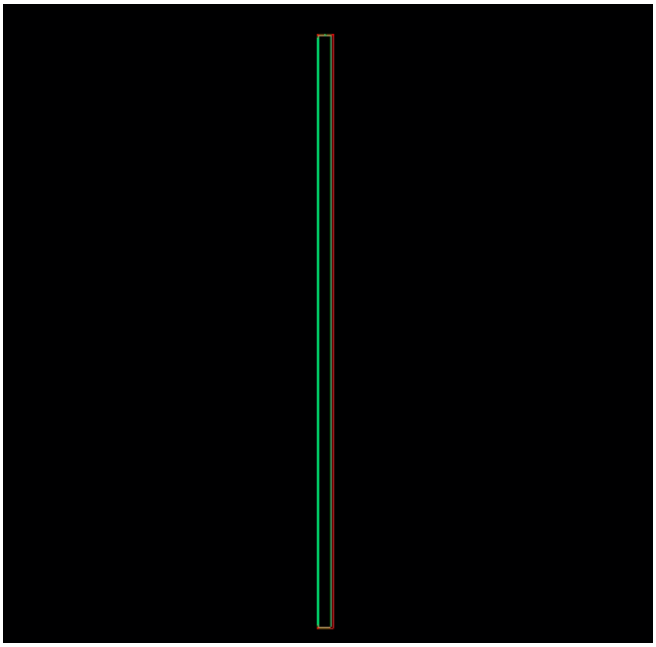

Fig. 14. Symbol of the APS array.

The symbol of the APS array is shown in Fig. 14 above where it is a long rectangular shape. It has a VDD port at the top, a GND port at the bottom, VOUT<0:319> ports on the right and VRSEL<0:239>, VRST<0:239> and VTX<0:239> ports on the left. Fig. 15 and Fig. 16 shows the close-up view of the symbol, where VTX, VRSEL and VRST ports are arranged according to index.

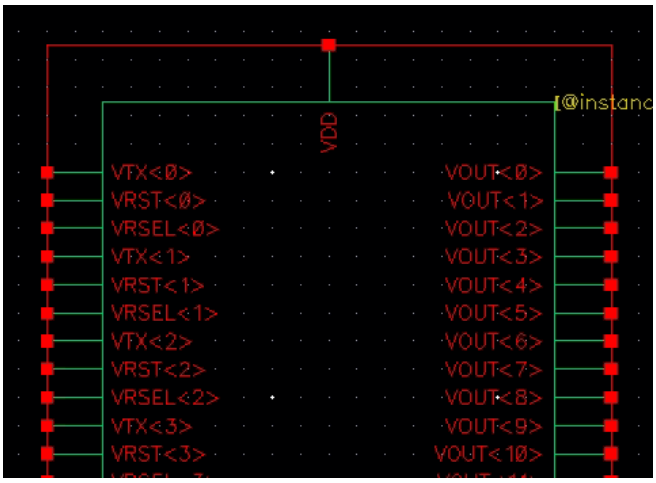

Fig. 15. Close up view of the symbol top of the APS array.

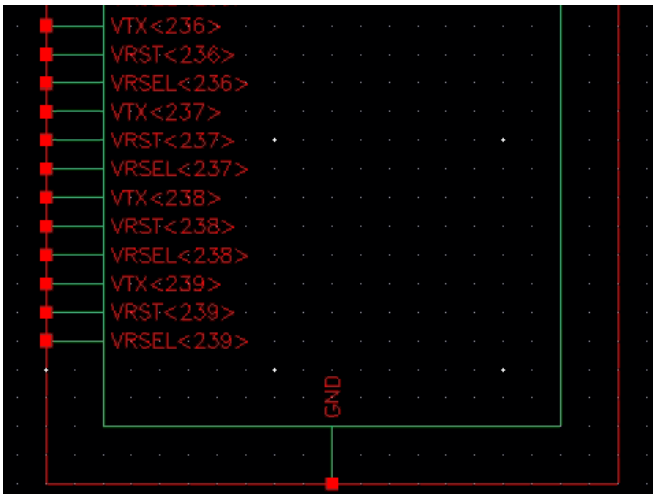

Fig. 16. Close up view of the symbol bottom of the APS array.

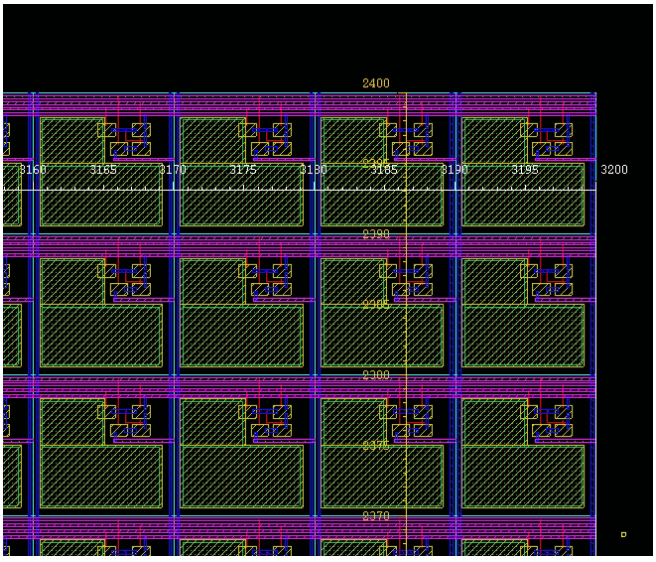

Fig. 17. Close up to the layout of the APS array.

The layout of the APS array can also be achieved by concatenating each 4T CMOS APS. The entire layout view of 320x240 array cannot be shown due to each individual tiny pixel. Hence, a ruler shown in Fig. 17 measuring from the bottom and leftmost shows that the size is indeed 3200um x 2400um, which verifies the QVGA 320x240 structure.

The following section repeats the DRC and LVS processes above and shows the respective results in Fig. 18 and Fig. 19 below.

```
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  1
TOTAL REAL Time:                 1
TOTAL Original Layer Geometries: 77 (10521600)
TOTAL DRC RuleChecks Executed:   789
TOTAL DRC Results Generated:     0 (0)
```

Fig. 18. Close up to show each pixel's interconnection.

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


              #        ###################
             #         #                 #       _   _
          #   #        #     CORRECT     #       *   *
           # #         #                 #         |
            #          ###################      \___/


  Warning:  Ambiguity points were found and resolved arbitrarily.
  Warning:  LVS property resolution maximum exceeded.

LAYOUT CELL NAME:        4T_CMOS_APS_array
SOURCE CELL NAME:        4T_CMOS_APS_array

--------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                  Layout     Source          Component Type
                  ------     ------          --------------
 Ports:                0          0

 Nets:            231442     231442

 Instances:       307200     307200          MN (4 pins)
                  ------     ------
 Total Inst:      307200     307200
```

Fig. 19. Close up to show each pixel's interconnection.

Fig. 18 shows that DRC run is cleared with zero violations, and vice versa Fig. 19 shows a clean LVS run. Instances values are correct as 320 times 240 times 4 transistors equals to 307200 instances.

V. Conclusion

The layout of the 4T CMOS APS is the continuation after verifying the circuit behaviour through simulation in the last paper. Thus, the current schematic does not require any external drivers and only declared ports to create a symbol to be instantiated in the subsequent array design.

The custom layout portion is done through Cadence Virtuoso which specifies the dimensions of all components excluding the predefined NMOS provided by silterraC13 PDK. The custom design is prioritized for fill factor, which achieves 47.91%, whilst metal1 layer have height of 10um and widths of 0.16um and 0.26um, and metal2 have height of 0.2um and width of 10um for all ports except VOUT which has a shorter width.

Different layers are routed and the interactions between each other are kept in check by following DRC run violations to ensure that manufacturing defects does not lead to chip faults yielding a bad chip. LVS run compares the layout and schematic to ensure number of nets, ports, and instances in both are equal. Although not comprehensive, executing both DRC and LVS checks can help avoid a huge part of errors in the custom layout design compared to the schematic design.

Since both layout and schematic of the 4T CMOS APS are designed to be modular, copy and pasting individual instances and routing them together into 320x240 structure creates a 4T CMOS APS array fit for capturing QVGA format frames, for both image and video, and the objective of the lab is achieved.

References

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[2] Paolo Minotti (2017). *Cadence Virtuoso – Simulation of a pixel*. Retrieved May 25, 2023, https://docplayer.net/41562688-Cadence-virtuoso-simulation-of-a-pixel.html

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