Design of a 4T (Four Transistor) CMOS Active Pixel Sensor

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***Abstract*—This paper investigates the design layout of the conventional 4T (four transistor) CMOS Active Pixel Sensor (APS), of which its dimensions are based on the QVGA format, 320 pixels x 240 pixels, with 60fps and 30% fill factor specifications. The Cadence Virtuoso tool is used to design and simulate the schematic circuit, utilizing the silterraC13 PDK. Transient analysis for multiple periods is conducted to ensure a single pixel's operation is as expected.**

Keywords—4T CMOS APS, QVGA, Cadence Virtuoso, silterraC13 PDK.

I. Introduction

A 4T (four transistor) CMOS Active Pixel Sensor (APS) is a type of image sensor commonly used in digital cameras and imaging devices. It is designed to convert light into electrical signals, enabling the capture of digital images or videos. The 4T APS utilizes complementary metal-oxide-semiconductor (CMOS) technology, which offers numerous advantages such as low power consumption, high integration density, and compatibility with standard CMOS fabrication processes.

The "4T" in 4T CMOS Active Pixel Sensor (APS) refers to the four transistors that are integrated within each pixel of the sensor [2]. These transistors play critical roles in the operation of the sensor, enabling the capture and processing of light signals.

The first transistor, known as the photodiode transistor, acts as the light-sensitive element. It absorbs photons from the incident light and converts them into an electrical charge proportional to the light intensity. This charge is stored temporarily within the pixel. The second transistor is the reset transistor, which ensures that the photodiode transistor starts each light measurement from a known state. It resets the voltage of the photodiode transistor, preparing it for accurate and consistent readings during subsequent light measurements. The third transistor, called the row-select switch transistor, acts as a switch. It allows the electrical charge stored in the photo-sensing transistor to be read out and transferred to the output circuitry for further processing. The select transistor controls the flow of charge and facilitates efficient signal transfer. Lastly, the source follower transistor plays a crucial role in regulating the charge transfer within the pixel. It allows the controlled flow of charges from the photo-sensing transistor to the output circuitry, ensuring efficient signal amplification and conversion. Together, these four transistors form the foundation of the 4T CMOS APS, providing pixel-level control and signal processing capabilities.

Overall, 4T CMOS APS can be found in of our daily routine life. Its CMOS incorporation allows for enhanced performance in terms of signal-to-noise ratio, dynamic range, and overall image quality compared to Charged-Coupled Devices implementation in modern imagery devices [3].

II. Simulation Methodology

A 4T CMOS APS pixel structure was first built in Cadence Virtuoso in schematic format. The circuit was constructed using the minimum length and width NMOS transistors, following the given lab sheet [1]. The pixel structure was then connected to two more individual NMOS transistors, namely the source follower biasing transistor (MSFB) and the current mirror transistor (MCM). Necessary inputs such as VDD, VTX, VRST, VRSEL and IBIAS were driven by external voltage and current sources through connecting pins.

A necessary step before simulation is to calculate the important parameter required for the simulation, which includes the period of a single pixel, the timings, delays, pulse widths and initial voltage of each voltage pulses, and the values of components such as the capacitance, CD. Parameters of IBIAS and IPH are varied to find an optimum value, of which the optimum value is then used as a constant during the simulation of the 4T CMOS APS.

A transient analysis was then performed to analyse the outputs in the time domain. The variables of the simulation were mapped from the schematic cell view, and the outputs were selected from the design to be plotted. Since the design variables were set in a way that they could be controlled in the ADEL simulator user interface, it was easier to test with various values to observe the subsequent changes. The simulation was run, and the output plots were observed and analysed.

III. NMOS Transistor Parameters

By accessing the technology files in the PDK, the electrical properties and physical dimensions of MOSFETs, in which NMOS parameters can be obtained. After locating the PDK directory, the spectre model directory within it is

accessed. Since silterraC13 MOSFETs follows BSIM4 standard the threshold voltage (vth0), gate oxide thickness (toxe), channel length modulation coefficient (plcm), charge carrier mobility (u0), donor concentration (ndep), acceptor concentration (pdep), breakdown voltage (bvs/bvd), minimum length (lmin) and minimum width (wmin) are found and described below in Table 1. These parameters are utilized in the implementation of transistors for 4T CMOS APS schematic and layout design.

TABLE 1. PARAMETERS OF NMOS IN PROCESS DESIGN KITS (PDK)

PDK Name	silterraC13
Model Name	nm_hp: 1.2V NMOS Thin Oxide device
Threshold Voltage, vth0	0.229
Gate Oxide Thickness, toxe	2.4948e-009
Channel Length Modulation Coefficient, pclm	0.2996
Charge Carrier Mobility, u0	2.929000e-002
Donor Concentration, ndep	1e+017
Breakdown Voltage, bvs/bvd	10
Minimum Length, lmin	130e-009
Minimum Width, wmin	150e-009

IV. RESULTS

A. *Schematic Circuit of the 4T CMOS APS*

The 4T CMOS APS circuit is shown in Fig. 1 below, constructed using four transistors namely the photodiode transistor (MPD), the reset transistor (MRST), the source follower transistor (MSF) and the row-select switch transistor (MRSEL). The pixel structure was then connected to two more individual NMOS transistors, namely the source follower biasing transistor (MSFB) and the current mirror transistor (MCM). Necessary inputs such as VDD, VTX, VRST, VRSEL and IBIAS were driven by external voltage and current sources through connecting pins.

The minimum dimensions of NMOS transistor of the silterraC13 pdk is used where lmin = 130nm and wmin = 150nm. Using the minimum dimensions allow for a smaller transistor area for the physical layout, in which the photodiode area can occupy more space and thus achieve the specification of at least 30% fill factor, which translates to 30% of the 10um x 10um area.

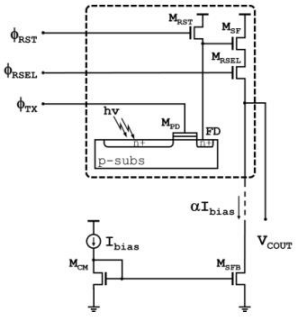

Fig. 1. Circuit design of 4T CMOS APS with external sources.

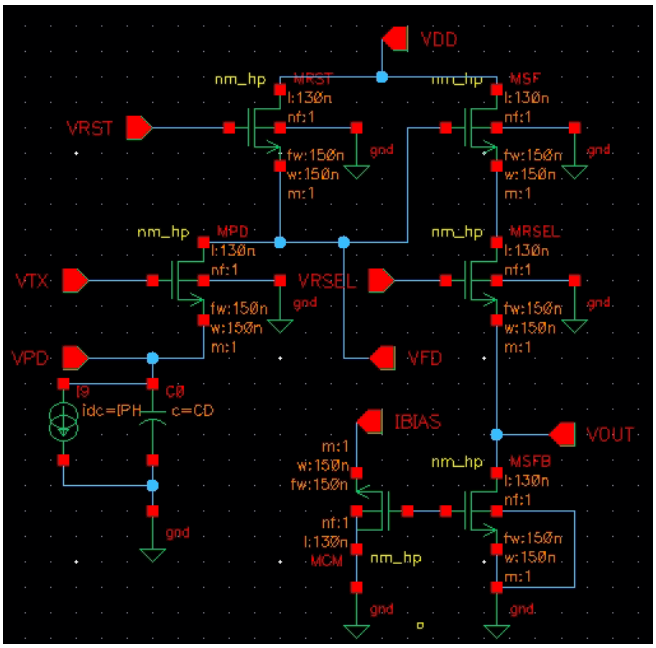

Fig. 2. Schematic of the 4T CMOS APS.

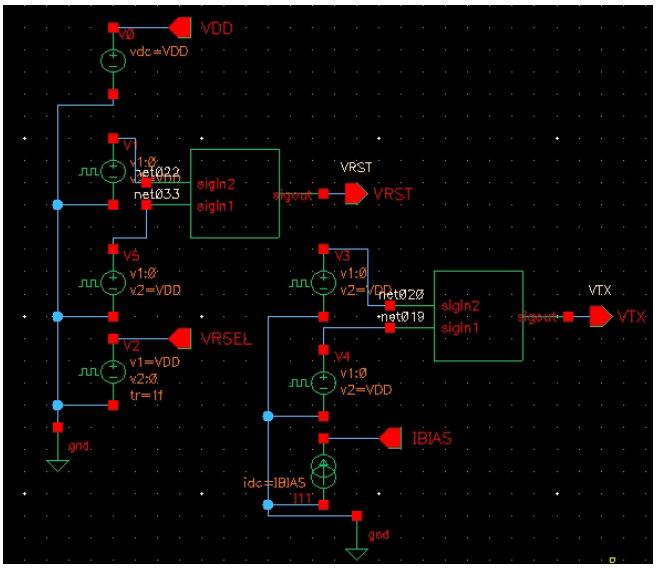

Fig. 3. Schematic of the external sources.

Fig. 2 and Fig. 3 shows the schematic circuit, which fulfils the requirements as shown in Fig. 1 to be considered a 4T CMOS APS circuit. Adder modules are included to allow multiple pulses in a single period cycle.

B. *Simulation of the 4T CMOS APS*

Simulation of the 4T CMOS APS requires transient analysis, where the time is long enough for several cycles of the charging and discharging of the APS to showcase that it functions optimally. Prior to the simulation, some calculations are performed to determine the values to be used in the variables.

Firstly, the QVGA format is 320 pixels wide and 240 pixels tall, translating to 240 rows and 320 columns of pixels. Since the specification requires 60 frames per second (fps):

$$60fps = \frac{60\ frames}{1\ second} = 16.67\ ms\ per\ frame$$

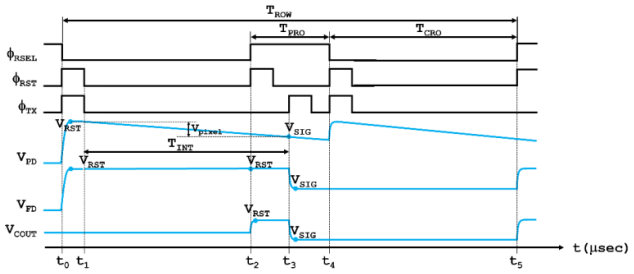

Fig. 4. Voltage signals with respect to time.

Following Fig. 4, T_{ROW} and T_{PIXEL} can be calculated by taking:

$$T_{ROW} = \frac{16.67\ ms}{240\ rows} = 69.44us\ per\ row$$

$$T_{PIXEL} = \frac{69.44\ ms}{320\ columns} = 217ns\ per\ pixel$$

Therefore, the maximum time for a pixel is 217ns, which indicates that period of voltage pulses (PER) is 217ns. DEL_VRST (150ns) and DEL_VTX (190ns) are the delays for the secondary pulses from the voltage sources such that the pixel can be stimulated twice within 1 period by referring to Fig. 5 which is a rough timing diagram produced to simulate the 4T CMOS APS cell.

The DEL_VRST and DEL_VTX timings are approximated based on the timing diagram in Fig. 4. The pulse width of VRST and VTX are set to 10ns, with initial voltage of VDD (5V) and drops to 0V whereas pulse width of VRSEL is set to 150ns with initial voltage of 0V and rises to 5V (VDD) when pulse width ends.

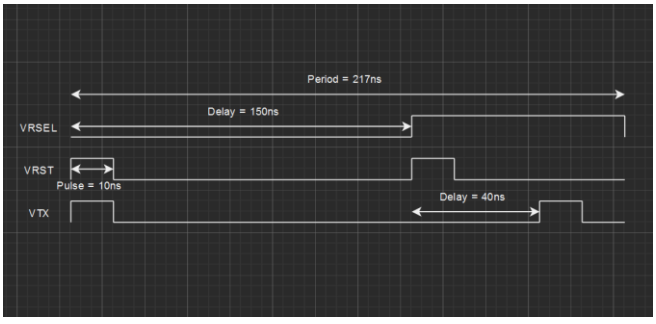

Fig. 5. Timing diagram of a single pixel.

CD indicates the photodiode capacitance, which can be calculated using the formula, where CD is represented by C_{diff}.

$$C_{diff} = C_j L_{source} W + C_{jsw}(W + L_{source})\ \text{--- (1)}$$

To calculate L_{source}, the area of the photodiode of which the specification requires a fill factor of at least 30%, indicating that the photodiode area must be at least 30% of the entire pixel sensor's area occupied. By taking photodiode dimensions of 5um x 7.05um, which has a total area of 3235 nanometres squared, the L_{source} can be calculated as shown below:

$$L_{source} = \frac{Photodiode\ area}{wmin} = \frac{5um\ x\ 7.05um}{150nm} = 235um$$

The parameters of C_j and C_{jsw} F can be found from the BSIM4 model file for NMOS of silterraC13 PDK through pattern matching "cjs" and "cjsws" in the model file. The values obtained are shown below. Skew of C_j is assumed to be 0 in our calculation, hence the parameters of C_j and C_{jsw} are obtained as 0.0013F and 0.1112nF respectively.

```
+cjs      = 0.0013*(1+(skew_hp_cjn/100))
cjsws     = 1.112e-010
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Thus, taking L_{source} = 235um, allows for the calculation of CD using equation (1) such that:

$$CD = (0.0013F)(235um)(150nm) + (0.1112nF)(150nm + 2(235um))$$

$$CD = 98.105fF$$

Therefore, using these values and plugging it into ADEL for simulation as shown in Fig. 5, the outputs of VRSEL, VRST, VTX, VPD, VFD and VOUT can be plotted as shown in Fig. 7, which shows four cycles of the charging and discharging of photodiode. The transient analysis, shown in Fig. 6, is set to be 900ns such that it allows for four whole periods (217ns) of the pixel cycle to be simulated, thus ensuring that the signals repeats which is an expected behaviour. IBIAS is set to 1uA and IPH is set to 500nA.

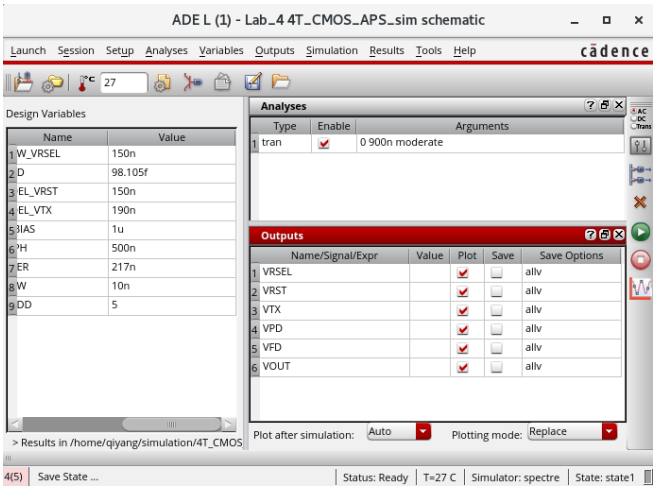

Fig. 6. Simulation menu of 4T CMOS APS [4].

Initially, when the simulation is first plotted, all plotted signals are a mesh of each other and not segregated as shown in Fig. 7. The signals must be separated to show uniformity and allow for easy observation with comparison to one another. The signal lines were also thickened for observation.

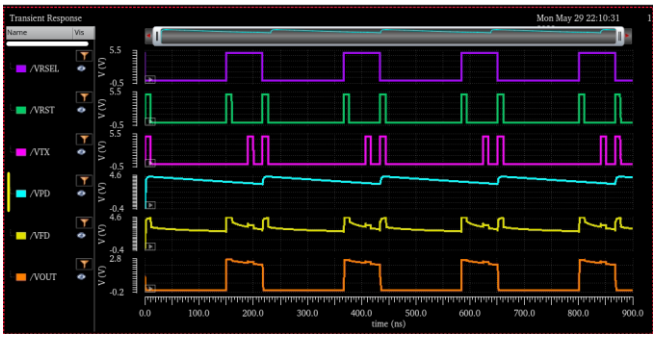

Fig. 7. Simulation plotted outputs for 4T CMOS APS.

Comparing Fig. 4 and Fig. 7 shows that most signals, including VRSEL, VRST, VTX, VPD and VOUT have similar waveforms. However, VFD in both figures have a stark difference whereby VFD in Fig. 4 rises, then stays at a constant plateau, and finally falls at the end of the cycle. VFD in Fig. 6 rises for a while and then falls to half its amplitude and stays flat until the end of the signal where it rises and falls sporadically causing a messy pattern. However, the cause of this difference in VFD signal is still unknown.

V. Conclusion

The 4T CMOS APS includes four CMOS transistors namely the photodiode transistor, the reset transistor, the row-select switch transistor, and the source follower transistor. These four transistors make up the modular structure of a pixel sensor. External transistors such as the source follower biasing transistor and the mirror current transistor is added to drive the APS for simulation purposes, the same goes for various voltage and current sources added to the schematic circuit.

The simulation of the 4T CMOS APS requires several parameters to be calculated, including the diffusion capacitance which correlates to the photodiode's ability to store charges, and also timings for gate voltage inputs from VTX, VRSEL and VRST. The timing calculation must be precise and modular such that when the APS is stacked together, they will behave the same as the simulation of a single pixel. The transient simulation allows for the plotted outputs to be analysed with respect to the time domain.

References

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