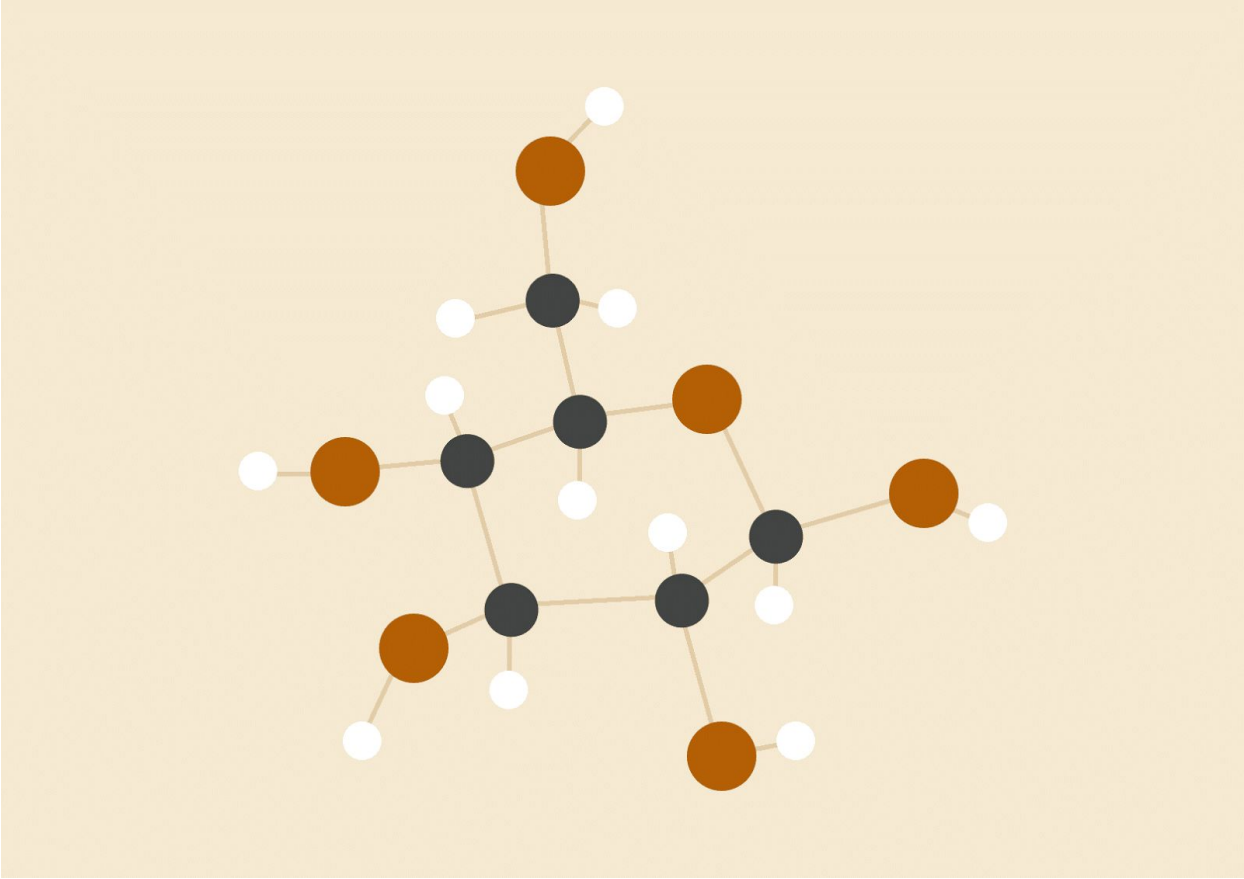
FINAL PROJECT REPORT

DDR3 DRAM Memory Controller Simulator



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PROJECT DESCRIPTION

Our task for this project was to create a DDR3 DRAM memory controller simulator capable of reading in memory requests and generating the required DDR3 memory commands.

PROJECT CONSTRAINTS

The project description gives the following constraints:

- Assume a single requestor (CPU) and a single memory channel.
- Up to 16 requests are placed into a queue. Additional requests cannot be added until a pending request has been serviced and is removed from the queue.
- Memory addresses are 32-bits.
- The DIMM has 32K rows, 8 banks, and 2K columns.
- The DRAM clock runs at ¼ the speed of the CPU clock.

DESIGN DECISIONS

- All code written in the C programming language
- Out-of-order, access scheduling policy
- Only PRE, ACT, RD, and WR commands are issued by the controller
- A memory request is considered starved if it is not completed within 250 CPU cycles

TIMING CONSTRAINTS

The following timing constraints were given in the project description:

AS	Value	Parameter	Value
tRC	50	tRCD	14
tRAS	36	tWR	16
tRRD	6	tRTP	8
tRP	14	tCCD	4
tRFC	172	tBURST	4
tCWL (tCWD)	10	tWTR	8
tCAS (CL)	14		

Our simulator uses these timings to determine whether or not the desired memory command can be issued. Each command has the following constraints:

- PRE
  - Must wait at least tRAS after same bank ACT command
  - Must wait at least tRTP after same bank RD command
  - Must wait at least tWR + tCWD + tBURST after same bank WR command
- ACT
  - Must wait at least tRRD after any bank ACT command
  - Must wait at least tRP after same bank PRE command
- RD
  - Must wait at least tRCD after same bank ACT command
  - Must wait at least tCCD after same bank RD command
  - Must wait at least tWTR after same bank WR command
- WR
  - Must wait at least tRCD after same bank ACT command
  - Must wait at least tCCD after same bank WR command
  - Must wait at least tCAS + tCCD + 2 - tCWL after same bank RD command

SCHEDULING POLICY

Our simulator implements an out-of-order, access scheduling policy. Before issuing a memory command, our simulator checks every pending memory request to determine which commands are possible and then prioritizes these possible commands. If two or more commands have the same priority level, the command corresponding to the oldest request in the queue is issued. The possible priority levels, in ascending level of importance, are:

Priority	**Name**	**Comments**
-1	WAIT	There is a starved request and issuing the command would further delay the starved request.
0	PRE1	A request wants to precharge a bank but there are pending requests to an open row in the same bank.
2	ACT	A request wants to activate a row in a precharged bank.
3	PRE2	A request wants to precharge a bank and there are no pending requests to an open row in the bank.
4	RD or WR	A request wants to read or write to an open row.
10	STARVED	A request is starved.