Chapter 4 problem 12: More Forwarding

1.

First out how many stallings there are.
When there is an EX to 1st only dependency, there are 2 stallings. This is because the stalled instruction must wait after the IF phase until the other instruction finishes with the EX, MEM, and the first half of the WB phases (in the second half of the ID phase there must already be the correct register values).
This also applies when we have an EX to 1st and MEM to 2nd dependency, or a MEM to 1st dependency.
When there is a MEM to 2nd dependency only, there is one stalling (we wait until the instruction finishes the MEM and the first half of WB phases).
This also applies when we have an EX to 2nd dependency.
If there are no hazards, the CPI is 1. These stallings increase the CPI by

(0.05+0.2+0.1)*2 + (0.1 + 0.05)*1 = 0.85

So, the new CPI is 1.85. The ratio of the stalled cycles is

0.85/1.85 0.46 = 46%

2.

Forwarding removes all "to 2nd" hazards. If we have an EX to 2nd hazard, an EX phase of the first instruction is executed, then the result is cached in the next cycle, and finally we can forward it after the other instruction completes its ID phase. If we have a MEM to 2nd hazard, notice that the MEM phase of the first instruction finishes in the same time as the ID phase of the other instruction - just in time for forwarding to occur!

Forwarding also removed an EX to 1st hazard; the result is forwarded as the EX phase of the first instruction, and the ID phase of the second instruction, are complete.

However, notice that forwarding does not solve a MEM to 1st hazard. We must wait until the MEM phase of the first instruction finishes before we can forward its result to the second instruction. Therefore, there will be a 1-cycle-stall happening.
As in 1., we can find that the increase of CPI is

0.2*1 = 0.2

So, the new CPI is 1.2, and the ratio is

0.2/1.2 = 0.17 = 17%

3.

Usage of the forwarding with EX/MEM register clearly cannot remove the "to 2nd" hazards. These hazards cause only 1 cycle stall. Similarly, to 2., this forwarding cannot solve the problem of MEM to 1st hazards. Also, notice that now we have a problem with the EX to 1st, MEM to 2nd dependency type, which causes 1 stall. So, the increase in CPI is

(0.2+ 0.05 + 0.1 +0.1) x 1 = 0.45

On the other hand, MEM/WB register removes MEM to 2nd hazards. The MEM to 1st hazards cause 1 stall (as in 2.). This also removes the EX to 2nd hazards (we execute the EX phase, and after the MEM phase, the result is written in the MEM/WB register).
Notice that the EX to 1st cause 1 stall: the result is present in the MEM/WB register

after the MEM phase. Similarly, EX to 1st, MEM to 2nd hazards cause 1 stall. Therefore, the increase in CPI is

(0.05 + 0.2 + 0.1) x 1 = 0.35

So, the second option is actually better.