Chapter 4 problem 8: single vs multi vs pipelining

1.

Non-pipelined version

Notice it needs 5 stages to execute a lw instruction. Therefore, the duration of the execution of the lw is

250 + 350 + 150 + 300 + 200 = 1250 ps

The clock cycle time must be long enough to handle the slowest instruction. This would be our answer of 1250 ps

pipelined version

The clock cycle time is equal to the duration of the slowest stage; therefore it is 350 ps

2.

The latency of lw instruction in the nonpipelined version is 1250ps rather than the pipelines latency is

5*350 = 1750 ps

3.

If we split a stage, the cycle time should remain the same as long as ID isn't touched. So, when we split ID the new stage takes 350/2 = 175ps. The new cycle time would be 300 ps or the duration of the MEM stage.

4.

The Data memory used only for sw and lw instructions. the utilization is

20% + 15% = 35%.

5.

The port is used only for alu and lw instructions. the utilization is

45% + 25% = 65%.

6.

The cycle time of the multi cycle version is equal to the slowest stage which is still 350 ps.

The execution of a pipelined version would be

exit time of pipe = number of instructions*cycle time

therefore 1250/350 or 3.57

lw takes 5 cycles while all other instructions take 4. So, the execution time is cycle time of multi + 3.2 cycle time multi/ cycle time pipe = 4.2