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-- Company:
-- Engineer:
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-- Create Date: 10/07/2020 07:17:15 PM
-- Design Name:
-- Module Name: mux2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mux2 is
    Port ( a : in std_logic_vector(15 downto 0);
           b : in STD_LOGIC_VECTOR(15 downto 0);
           sel : in STD_LOGIC;
           mux_out : out STD_LOGIC_VECTOR(15 downto 0));
end mux2;

architecture Behavioral of mux2 is

begin
      process(a, b)
        begin case sel is
          when '0' => mux_out <= a;
```

```
        when '1' => mux_out <= b;
        end case;
    end process;

end Behavioral;
```