Bachelor in Computer Vision

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Digital Electronics
Labs 4

Test board implementation

We propose in this labs to implement some basic operatior on the test board named Nexys 4.

*NB : all examples should be check using **test-benchs** and simulatuon tools before to use the board!!!*

Problem 1

Create a design which allows to display a value between 0 and F of one 7-segement Display.

Problem 2

Create a design which allows to display a value between 0 and F of one 7-segement Display which will select by using swichtes on the board.

Problem 3

Create a design which allows to display the value coming from a counter modulo F on a particular 7-segment display. Use the clock of the card as an input of your counter.

Problem 4

Create a design which allows to display the value coming from a counter modulo 9999 on a particular 7-segment display. Use the clock of the card as an input of your counter.

Notes

The datasheet of the Nexys 4 here : `https://reference.digilentinc.com/_media/nexys:nexys4:nexys4_rm.pdf`.

In order to connect real output of the FPGA to semantic name of the Buses of your own design, you need to use the **UCF** file given by the Diligent : `https://reference.digilentinc.com/_media/reference/programmable-logic/nexys-4/nexys4_master_ucf.zip`

The UCF file is an ASCII file specifying constraints and netlist on the logical design. You can create this file and enter your constraints with any text editor. You can also use the Constraints Editor to create constraints within a UCF file. These constraints affect how the logical design is implemented in the target device. You can use the file to override constraints specified during design entry