

FPGA STOCK TRADING PREDICTION

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ABSTRACT

The paper describes the implementation process for a FPGA hardware approach in computing daily highs and lows for ten different types of stocks and how compares to that of a computer software architecture approach in terms of speed.

1. INTRODUCTION

The type of data streams for stock values is of stochastic kind and so therefore, the complexity of an algorithm to predict such values will increase. As the complexity of such abstract machine representations of an algorithm increases, so does the actual architectural components of the computer system architecture required to perform such operations whether in sequence or in parallel in order to compute the resultant values accurately with a given set of input parameters. FPGA's inherent pipeline and parallel architecture rendered an hypothesis of their potential to compute huge amount of stochastic input data for daily highs and lows prediction in stock trading. This implementation process also takes advantage of the innate data flow system of the FPGA's construction during the implementation process of the algorithm.

2. HIGH LEVEL REQUIREMENTS

Note that there might be some changes during the implementation process.

- Predict the stock prices (*Day's High and Day's Low*).
- Use a web server to feed the stock details to the FPGA and display the prediction results.
- Create a software model of the prediction algorithm.
- Implement the prediction algorithm on the FPGA hardware.
- Compare the performance of software and hardware versions of algorithm implementations.

3. PROJECT DESIGN PHASES AND SPECIFICATIONS

3.1 Research Phase

3.1.1 Algorithm Analysis and Implementation Research

- The Daily high and low bid-ask spreads are calculated based on the assumptions that the buyers initiates the prices for highs and that of lows are initiated by the sellers (Corwin, Schultz,). Also the advantage of using this procedure has been proven by previous research (Corwin, Schultz,) in which they outperformed previous methods of estimating daily highs and lows.
- Coupled with the fitness computation of genetic algorithm, we try to first classify each input into a binary class such as that of genetic alleles using the sigmoid function:

$$P_t = \frac{1}{1 + e^{-t}} \quad (1)$$

- Genetic algorithm as implemented by evolutionary biology tries to find the best possible mutational selection and crossover of the best attributes of previous or parent results of a species unto the offspring's genetic structure. So in this case as implemented by (cite paper), the objective is to compute the best potential outcome in terms of combination of all genetic makeup in the child's copy of genotype.
- With a population size N, binary fitness of

$$f_j$$

and

$$f_i$$

$$P_i = \frac{f_i}{\sum_{j=1}^N f_j} \quad (2)$$

3.1.2 Data Gathering Research

The data collection phase uses the yahoo TQA data for the following stocks:

- 3.1.3 *FPGA Design Methodology Research*
- 3.1.4 *Front End Software Design Methodology Research GUI*
- 3.1.5 *Back End Software Design Methodology Research CRUD*
- 3.1.6 *Research on Best Testing methods on Software*
- 3.1.7 *Research on Software Maintenance Methodology*

3.2 Software Design Specification

- 3.2.1 *Stock Data Gathering Software Design Specification*
- 3.2.2 *Algorithm Design in C++ Specification*
- 3.2.3 *FPGA Design Specification*
- 3.2.4 *Back End Software Design Specification*
- 3.2.5 *Front End GUI Design Specification*
- 3.2.6 *Software Testing Specification*

3.3 Detailed Description Of Algorithm Design

3.4 Detailed Description Algorithm Implementation in C++

3.5 Detailed Description Hardware Design

3.6 Detailed Description Algorithm Implementation in Hardware Description Language

3.7 Detailed Description Components Definitions

4. REFERENCES