Pegasus DRC / LVS Walkthrough

Introduction

This guide will walk through the process of conducting both Design Rule Checks (DRC) and Layout vs. Schematic Checks (LVS) on a design in Virtuoso using Cadence's Pegasus software. As the GUI is not compatible with the current setup, the command-line interface will be used.

Design Rule Checks scan through a physical design to ensure that all of the fabrication rules provided by the fabrication process are met. This is to ensure that the chip can actually be made.

Layout vs. Schematic Checks compare the netlists generated from the schematic and physical layout to ensure that the two views represent the same design.

These checks take place after completing both the schematic and physical layout of a design.

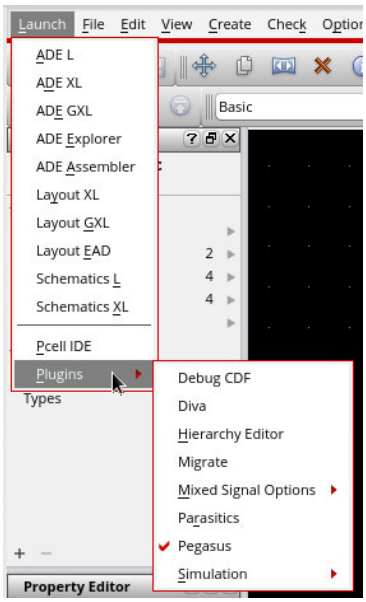
Loading Modules

First, use the following commands to load the modules for Virtuoso, Spectre, and Pegasus:

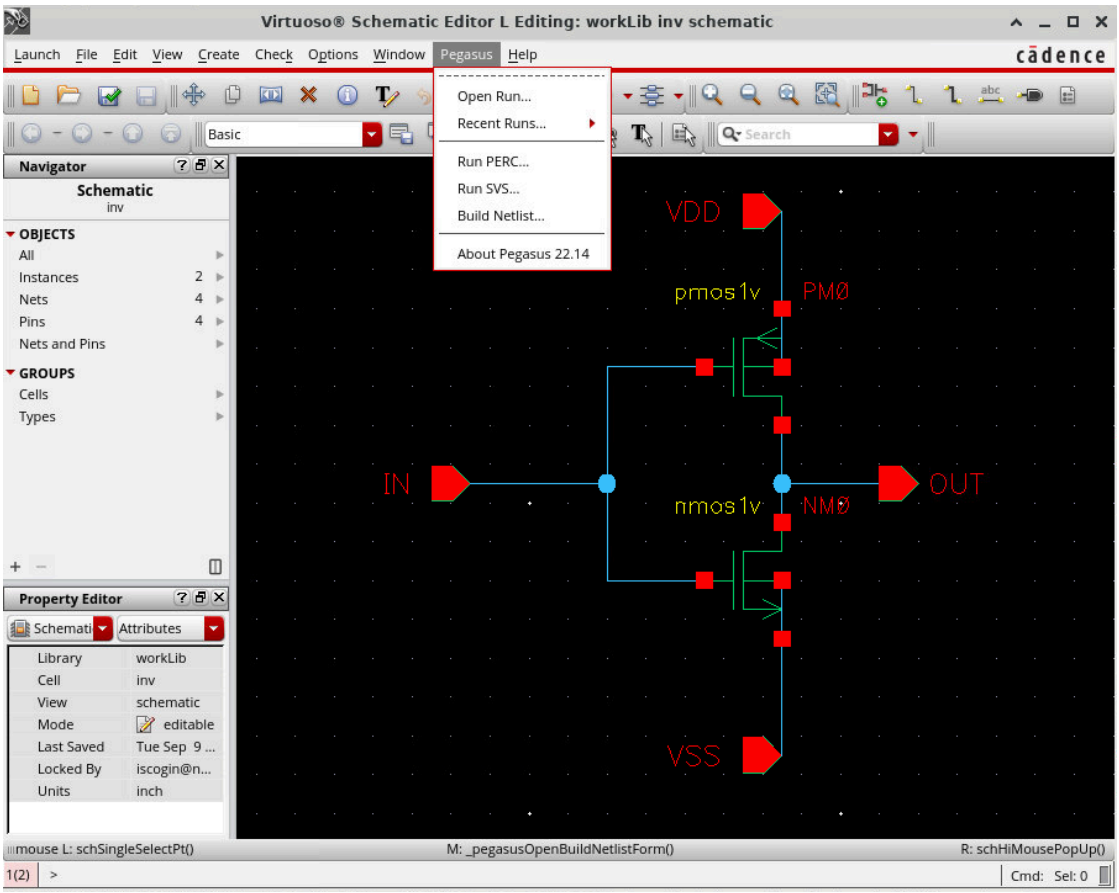
module load cadence/IC/618
module load cadence/SPECTRE/211
module load cadence/PEGASUS/221

Exporting the Schematic

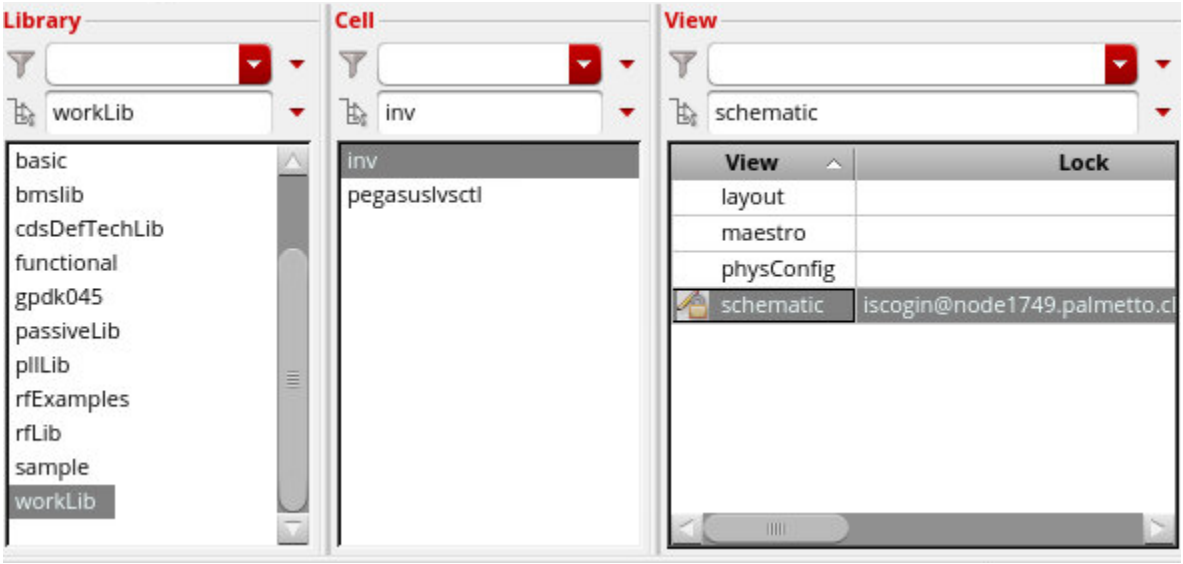
For this guide, a simple inverter design will be used. The first step in conducting the LVS check is exporting a netlist of the schematic design as a .cdl file. If the Pegasus tab is not available in the top of your design, enable it via Launch > Plugins > Pegasus. Note that this step is not required for DRC.



Once you have access to the Pegasus menu, choose Pegasus > Build Netlist… to begin exporting your netlist.



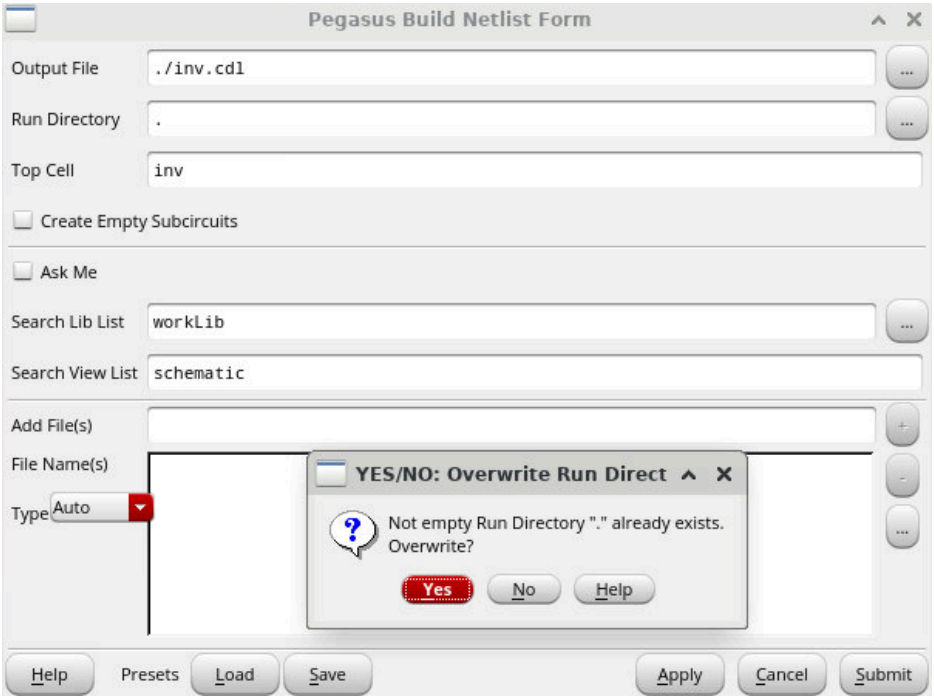
Each cell has a unique Library/Cell/View path. In this case, the cellview of the inverter schematic is located at workLib/inv/schematic. Take note of this path for your design, as you will need it.



In the Pegasus Build Netlist Form, enter your Run Directory and Top Cell. In this case, I am using my working directory (.) as the Run Directory (though you can make a subfolder if you want to keep your working directory clean), and the inverter's cell name (inv) as my Top Cell.

Make sure that your library is in the Search Lib List and that you include "schematic" in the Search View List .

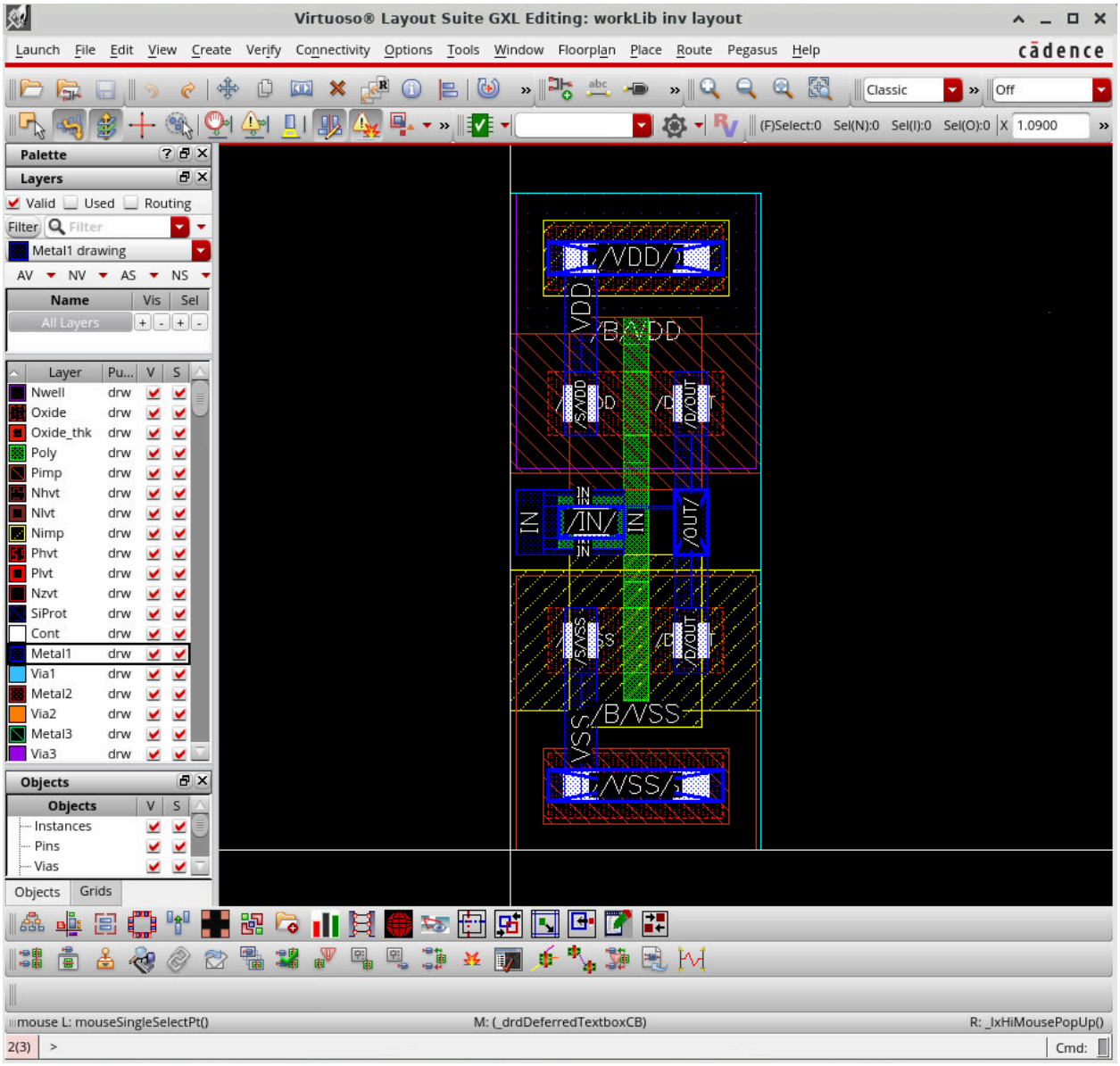
Confirm any overwrites and Pegasus should produce a .cdl netlist.




```
************************************************************
* CDL produced by pvsBuildNetlist on Oct 19 20:08:31 2025 *
************************************************************


*pvsViewList = auLvs schematic
*pvsStopList = ("auLvs")
*pvsSimName  = auLvs



*.EXPAND_ON_M_FACTOR
*.MEGA



.subckt inv IN OUT VDD VSS
*PVSCELL netlisted from workLib inv schematic
  MNM0 OUT IN VSS VSS g45n1svt m=1 l=45n w=120n
  MPM0 OUT IN VDD VDD g45p1svt m=1 l=45n w=120n
.ends inv


************************************************************
*             Completed at Oct 19 20:08:31 2025            *
************************************************************
```

Exporting the Layout

Open your layout view and ensure that you can open the Pegasus menu by checking the Launch > Plugins menu. Note that I have introduced a short between IN and OUT for the purpose of illustration.



To export the layout, choose the File > Export Stream from VM option. This should create a .gds layout file corresponding to the cell name. In my case, the output was inv.gds.

Running DRC

Before starting, I recommend using the command ‘pegasus -h’ to view the different input parameters for the Pegasus software.

To run DRC, you will need to use the following command with the correct inputs:

pegasus -drc -run_dir (run directory) -gds (input layout file) -top_cell (cell name) (path to rules)

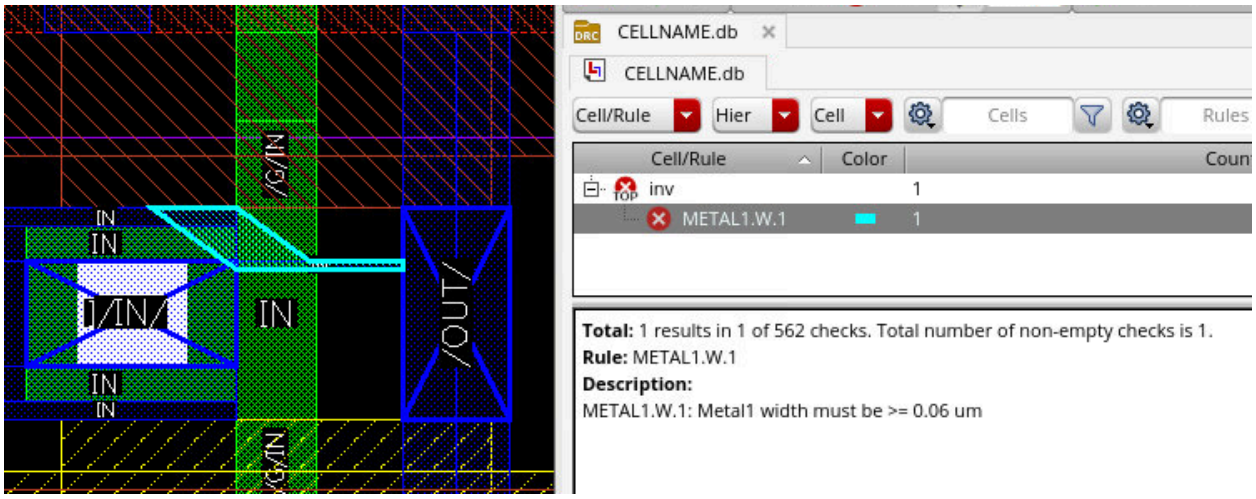
For my inverter design using the gpdk045 technology library, the input is as follows:

pegasus -drc -run_dir . -ui_data -gds inv.gds -top_cell inv /software/commercial/cadence/pdk/gpdk045_v_6_0/pvs/pvlDRC.rul

```
        Worker resource usage  summary: Total CPU[s]: 1  Run duration[s]: 3  Max peak memory[MB]: 19
        Worker CPU utilization summary: 1 of 3 available CPU seconds (33.33%) with 1 average available CPU(s)
INFO:   Generating summary in /home/iscogin/work/result.sum
INFO:   All selected rules completed
        Total CPU Time                  : 2(s)
        Total Real Time                 : 3(s)
        Total Original Geometry         : 57(57)
        Total DRC RuleChecks            : 562
        Total DRC Results               : 1 (1)
        ASCII report database is /home/iscogin/work/CELLNAME.db
INFO:   Checking in all SoftShare licenses.
[iscogin@node1749 work]$ pegasus -drc -run_dir . -gds inv.gds -top_cell inv /software/commercial/cadence/pdk/gpdk045_v_6_0/pvs/pvlDRC.rul
```

To view the results, go to Pegasus > Open Run… from within the layout editor and choose the output report database (CELLNAME.db). This will bring up a list of all design rule errors. Double clicking any given error will highlight it in the design.

In this case, the only error is that the short between IN and OUT is too thin to be manufactured. Note that this says nothing about the connectivity of the design, only the geometry.



Running LVS

For LVS, a similar process is used:

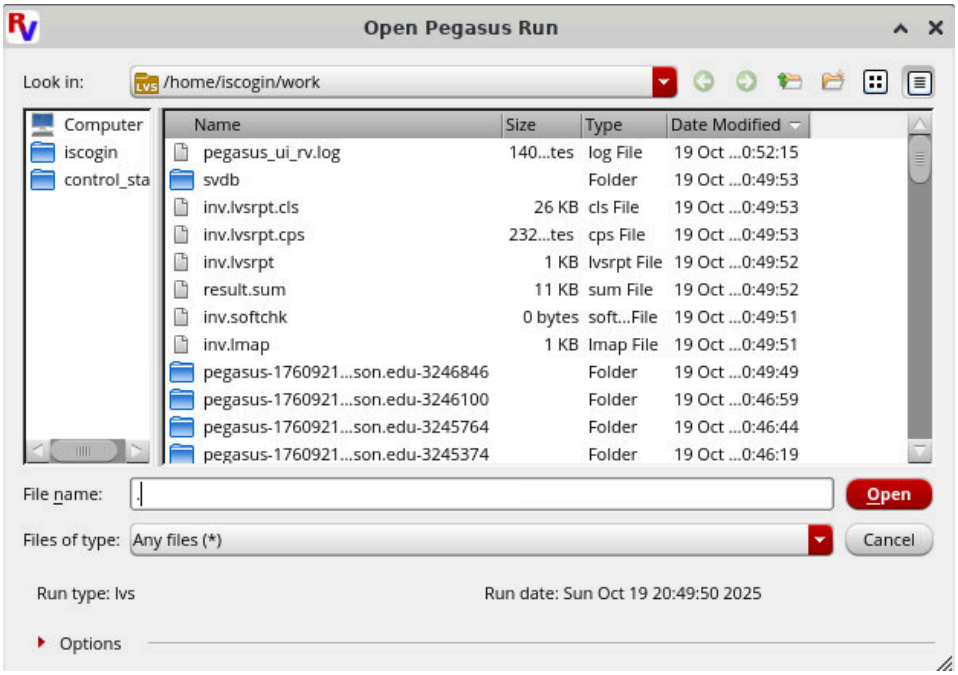
pegasus -lvs -run_dir (run directory) -ui_data -top_cell (cell name) -source_top_cell (cell name) -source_cdl (input schematic netlist) -gds (input layout file) (path to rules)

For this design, the input is:

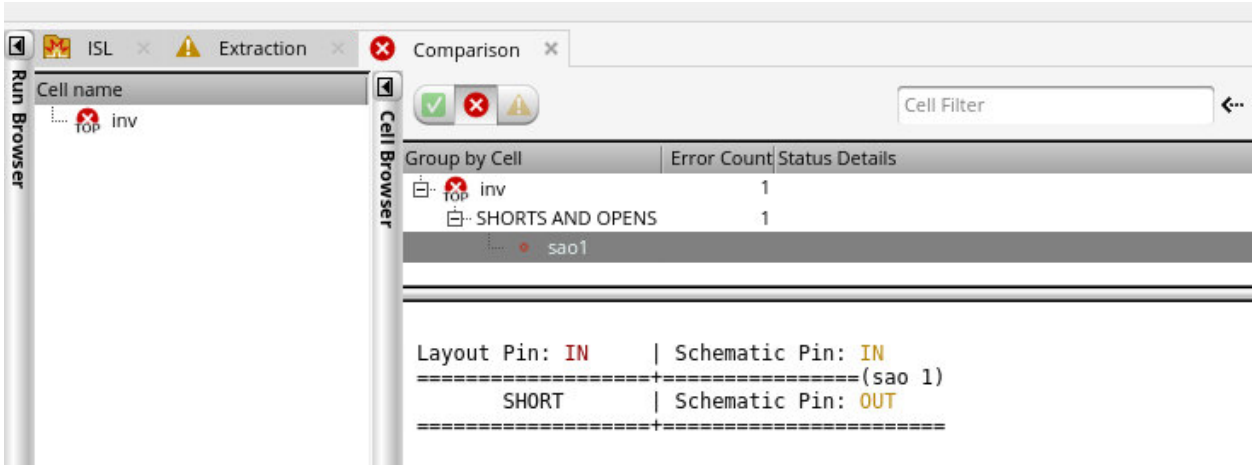
pegasus -lvs -run_dir . -ui_data -top_cell inv -source_top_cell inv -source_cdl inv.cdl -gds inv.gds /software/commercial/cadence/pdk/gpdk045_v_6_0/pvs/pvlLVS.rul

```
    ################################################################################
    #                                                                              #
    # Run Result             : MISMATCH                                            #
    #                                                                              #
    # Run Summary            : [ERROR] Connectivity Mismatches                     #
    #                        : [WARN]  Extraction Warnings (refer to Extraction Report File)  #
    #                        : [INFO]  ERC Results: Empty                          #
    #                                                                              #
    # ERC Summary File       : result.sum                                          #
    # Extraction Report File : inv.lvsrpt                                          #
    # Comparison Report File : inv.lvsrpt.cls                                      #
    #                                                                              #
    ################################################################################

INFO:    Checking in all SoftShare licenses.

[iscogin@node1749 work]$ pegasus -lvs -run_dir . -top_cell inv -source_top_cell inv -source_cdl inv.cdl -gds inv.gds /software/commercial/cadence/pdk/gpdk045_v_6_0/pvs/pvlLVS.rul
```

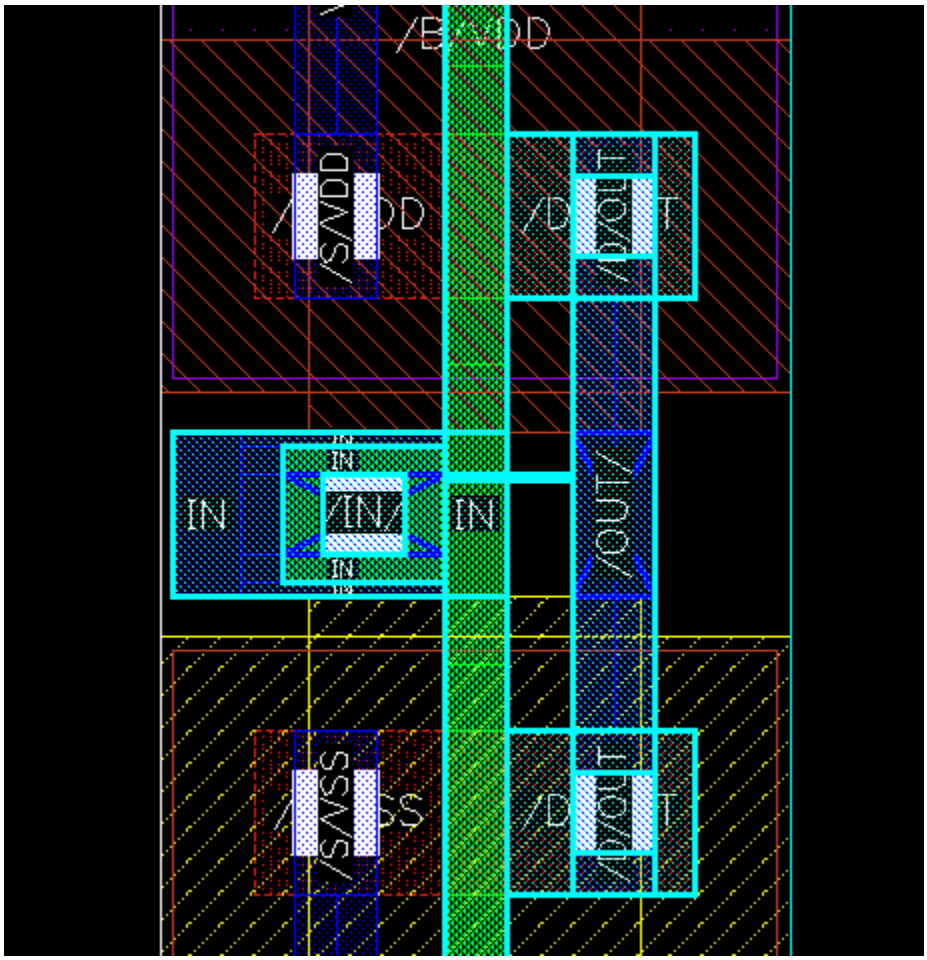
LVS outputs its data directly to the run directory, so to view the LVS results in more detail choose the Pegasus > Open Run… option and input the run directory (in this case .).



Opening the comparison tab reveals that there is a short between the IN and OUT nets. To fix the issue, remove the short.



Note that you can click the red net names in the comparison window to highlight the layout nets in question.



Removing the short, exporting a new gds, and rerunning DRC/LVS reveals zero errors.

```
INFO:    Generating summary in /home/iscogin/work/result.sum
INFO:    All selected rules completed
         Total CPU Time                    : 2(s)
         Total Real Time                   : 3(s)
         Total Original Geometry           : 56(56)
         Total DRC RuleChecks              : 562
         Total DRC Results                 : 0 (0)
         ASCII report database is /home/iscogin/work/CELLNAME.db
INFO:    Checking in all SoftShare licenses.
```

```
#############################################################
#                                                           #
# Run Result              : MATCH                           #
#                                                           #
# Run Summary             : [INFO]  ERC Results: Empty      #
#                         : [INFO]  Extraction Clean        #
#                                                           #
# ERC Summary File        : result.sum                      #
# Extraction Report File  : inv.lvsrpt                      #
# Comparison Report File  : inv.lvsrpt.cls                  #
#                                                           #
#############################################################
```