Virtuoso Layout Fundamentals

Introduction

This guide will walk the user through basic methods for translating a schematic design in Virtuoso into layout using the built-in layout editor. Before continuing, make sure that you have completed both the 'Virtuoso Palmetto Cluster Setup' guide and the 'Virtuoso Schematics & Simulation' guide, as this will draw upon prior knowledge. Additionally, this guide is followed by the physical verification tutorial 'DRC & LVS with Pegasus'.

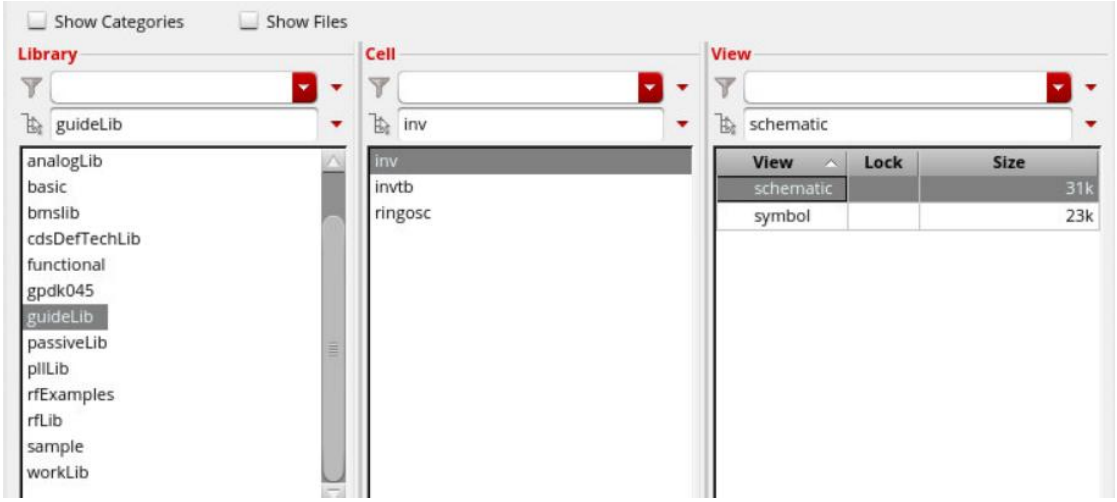
Creating the Layout View

In the previous tutorial, you created schematic views from scratch and populated them with components from various libraries to create an inverter and a ring oscillator. Creating a layout view is slightly different in that each layout instance corresponds to a distinct instance in the schematic. As you will see, this allows for layout views to pull instances directly from schematic views.

Load the general Palmetto Cluster modules using the following commands:

module load cadence/IC/618
module load cadence/SPECTRE/211

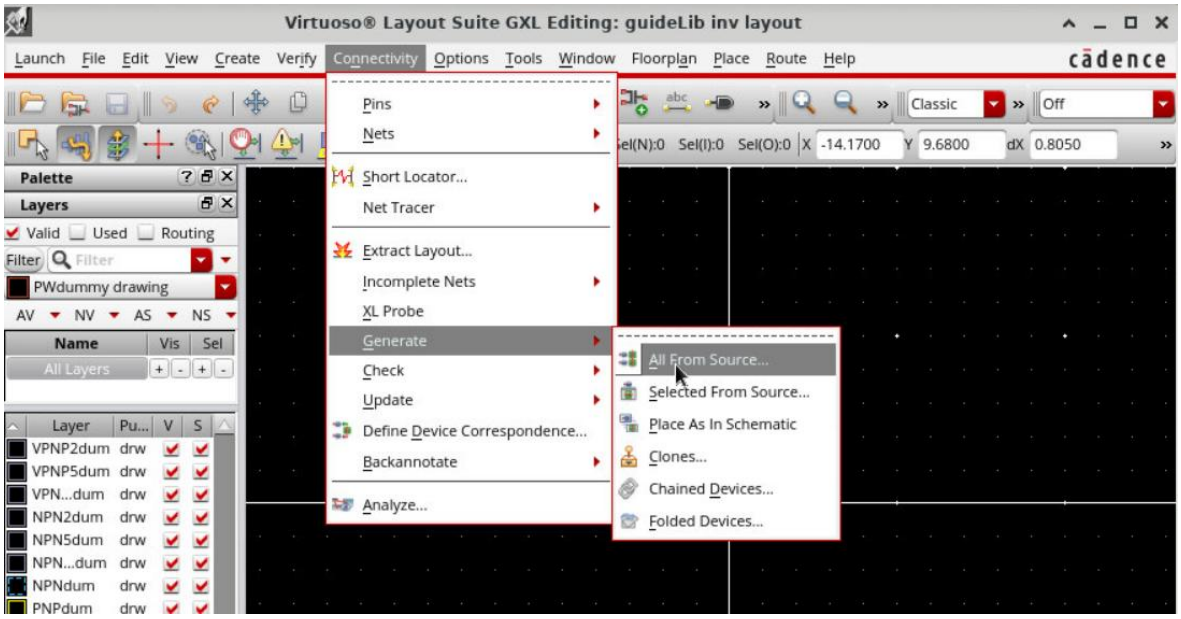
Open the Library Manager from the CIW (Tools > Library Manager) and then open the inverter schematic located in guideLib/inv/schematic (the same one used in the previous lab).



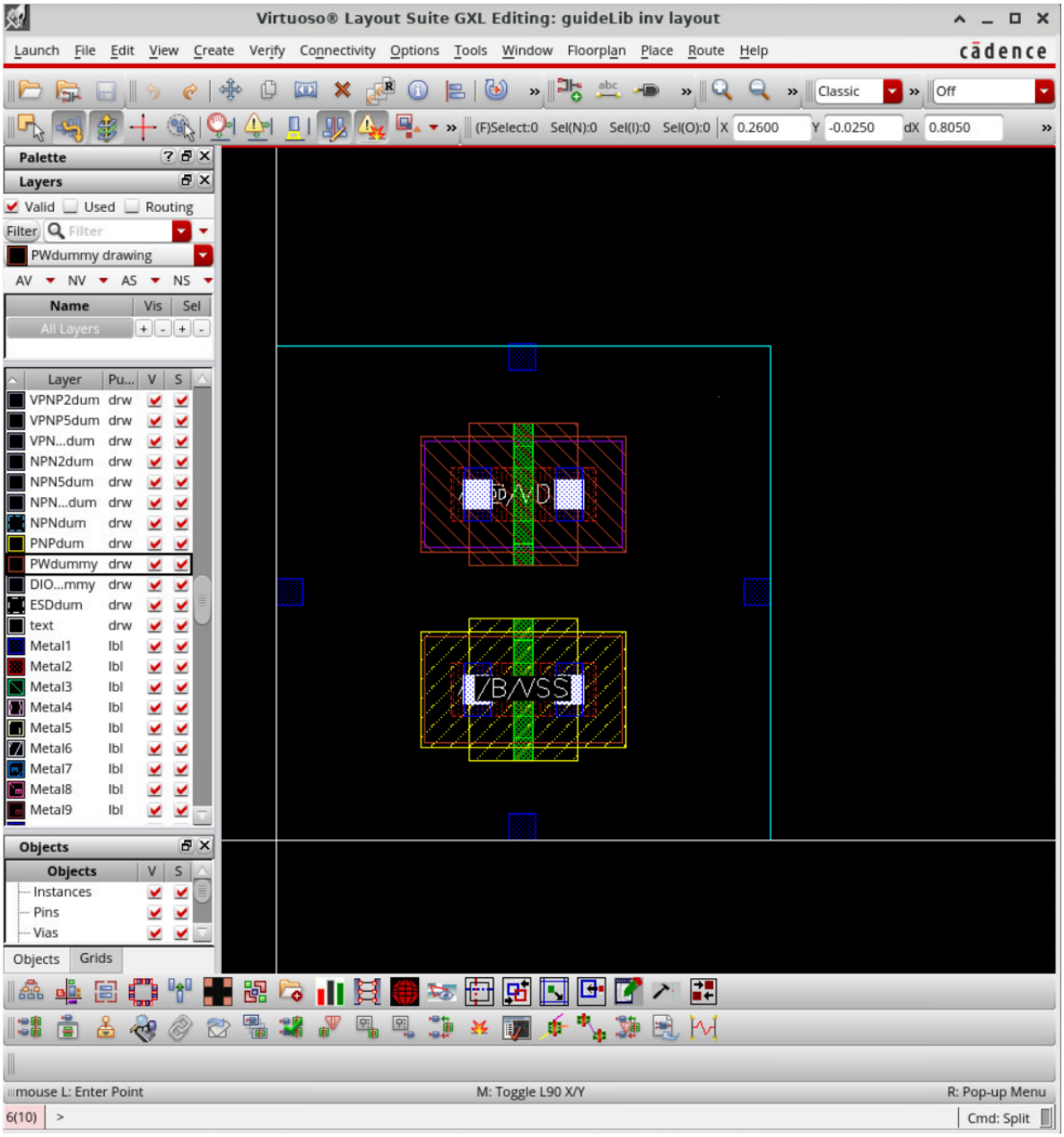
For the sake of this guide, both the NMOS and PMOS in the inverter schematic will have default dimensions L=45nm and W=120nm with 1 finger and a multiplier of 1.

To create the layout view, first launch the layout tool from Launch > Layout GXL. Ensure that the Layout field is set to 'Create New' and Configuration to 'Automatic'. When the New File menu appears, ensure that the settings are as follows:

If you get a licensing error, repeat the previous step selecting 'Layout XL' instead of GXL. Creating the view automatically opens the Virtuoso Layout Suite. Bring in instances by choosing Connectivity > Generate > All From Source...

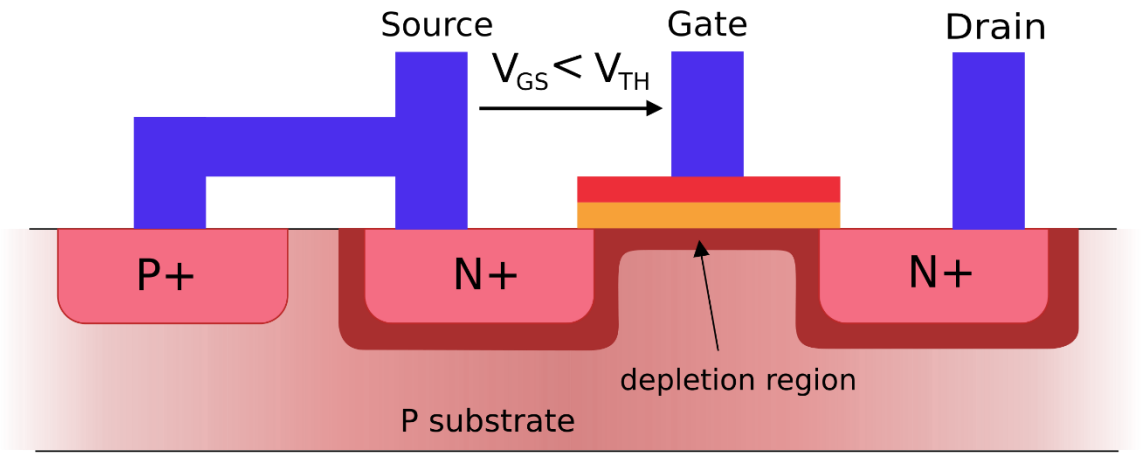


Leave the options in the ‘Generate Layout’ menu as their defaults and press OK to generate parameterized NMOS and PMOS cells from the inverter schematic. Note you can also create instances with the i hotkey, but you must manually define device correspondence between the layout and the schematic with this approach. Use the Shift+F and Ctrl+F hotkeys to toggle between layer and instance visibility.



FET Basics

The layout view represents a top-down picture of layers to be fabricated on a silicon substrate. Some helpful hotkeys off the bat are f (zoom fit), k (measurement tool), u (undo), shift+u (redo), and t (layer tap). Compare the cross-sectional NMOS view below to the top-down view shown previously.



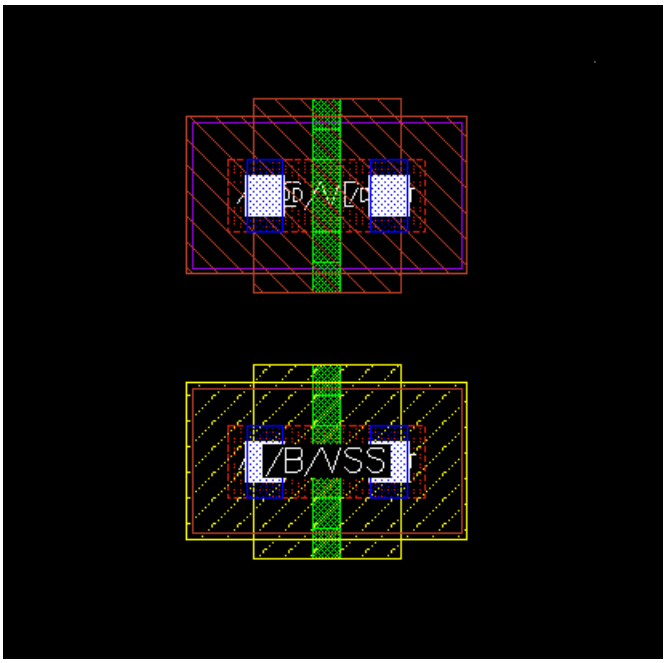
In the top-down view, device geometry is defined by stacked rectangles assigned to different layers. For the NMOS, the p-type substrate is represented by the yellow PWdummy layer. Note that substrate is always assumed to be p-type, so some technologies allow for this layer to be skipped (though n-wells must always be manually defined for PMOS transistors). Within this p-well, the general n-type doping region is defined by the red Nimp (n-type implant) layer. Additionally, the "active region" of the transistor where the source/channel/drain are located is defined by the dense red oxide (oxide diffusion) layer.

The gate, which determines the exact channel geometry based on its placement, is drawn in the green poly (polysilicon) layer. Source/drain contacts from the active region to the lowest metal layer (Metal1) are drawn with the Cont layer. PMOS transistors have a similar makeup, instead using n-wells and p-type implant.

Generating Well Taps

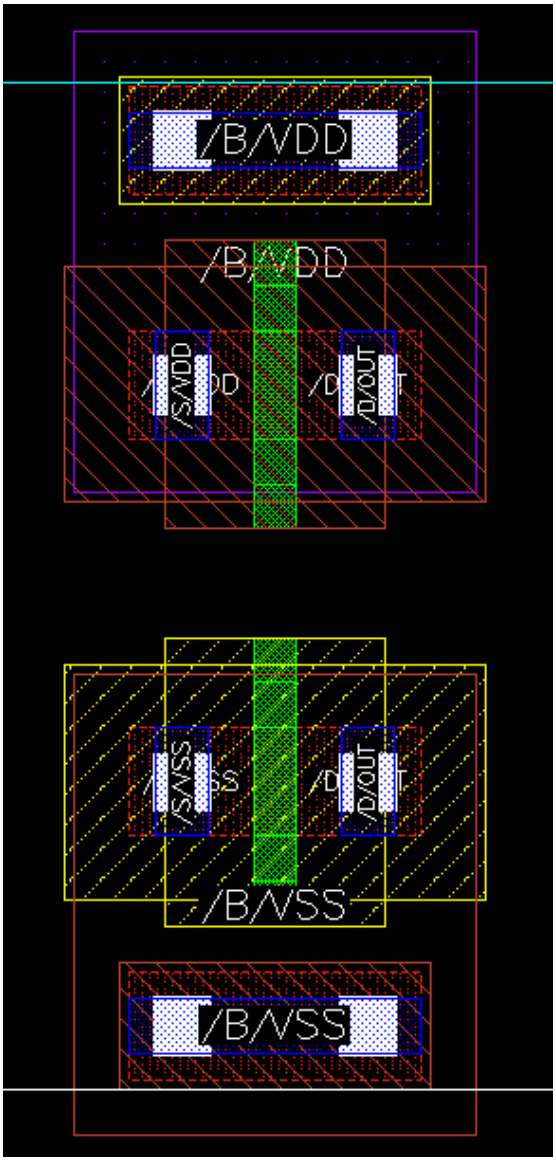
Transistors are generated with three contacts to allow for connection of the source, gate, and drain terminals. However, the previous cross-sectional figure shows that standard FET devices have an additional fourth terminal at the body. This extra terminal has the effect of biasing the substrate beneath the transistor, which directly impacts the threshold voltage. For instance, if an NMOS has a greater source voltage than body voltage, then the body-source pn junction becomes reverse-biased and a greater gate-source voltage must be applied to negate the depletion region and invert the channel.

To access this “hidden” terminal, we must place well taps for both the n-well and the p-well. If they were imported, delete the blue pins on the top/bottom and left/right of the two transistors to clear space.



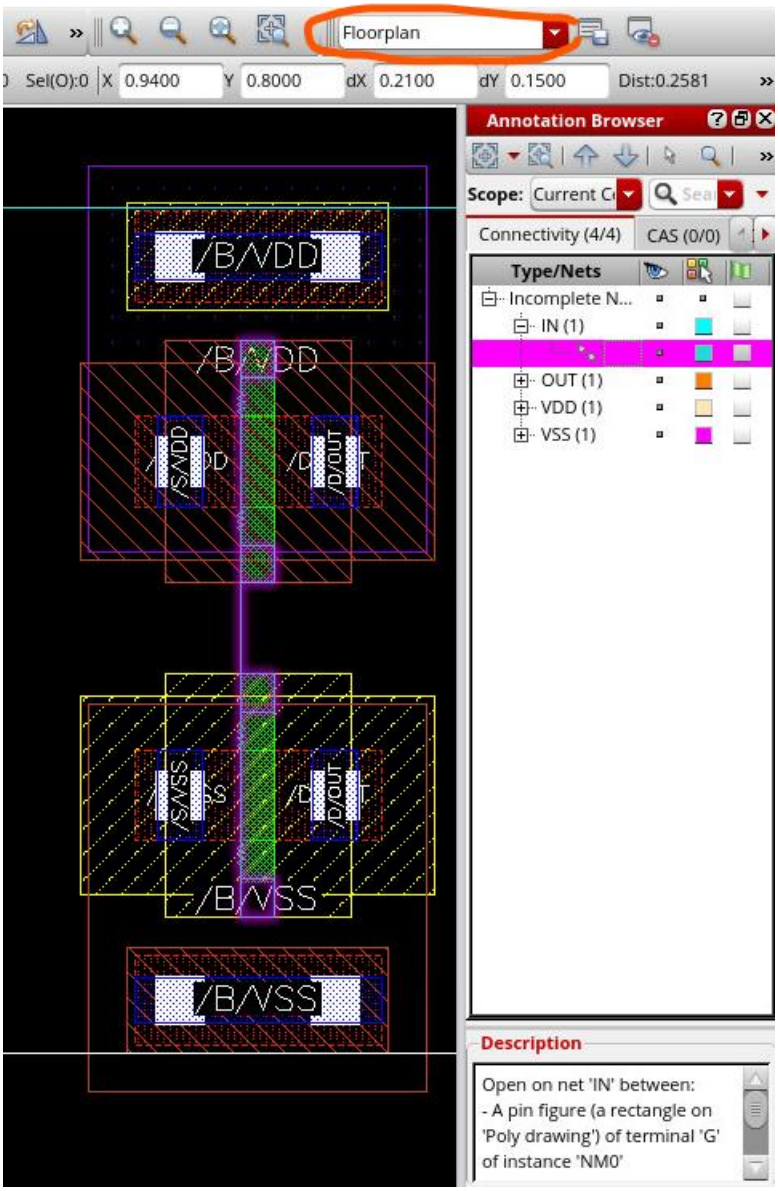
Select the NMOS transistor (the yellow one) and press the q hotkey to open the properties (“query”) menu. Swap to the “Parameter” menu and set the “Bodytie Type” property to “Detached”. Check “Bottom Tap” ONLY and press OK. Do the same for the PMOS (purple/pink one), but select the top tap instead of the bottom.

Bodytie Type	Detached
Left Tap	☐
Right Tap	☐
Bottom Tap	☑
Top Tap	☐



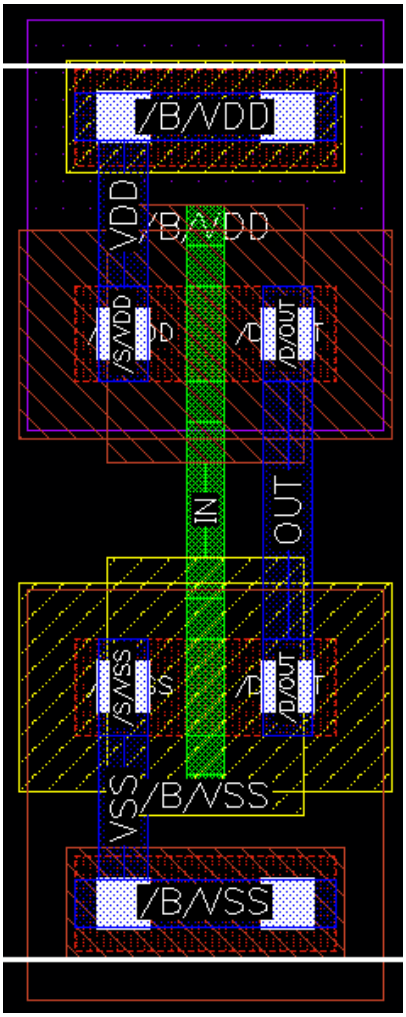
Routing Nets

As this is a relatively simple design, identifying disconnected nets is easy to do visually. However, for more complex designs it may be helpful to open the Annotation Browser assistant (right click top bar > Assistants > Annotation Browser OR switch the workspace to Floorplan) to browse design-wide connectivity notices. This step is not necessary for this guide, but may help in the future.



When routing nets, it is important to balance condensed layout with proper electromagnetic consideration. Stacked power or signal layers will introduce parasitic capacitance and crosstalk, while long traces can introduce unintended resistance and inductance.

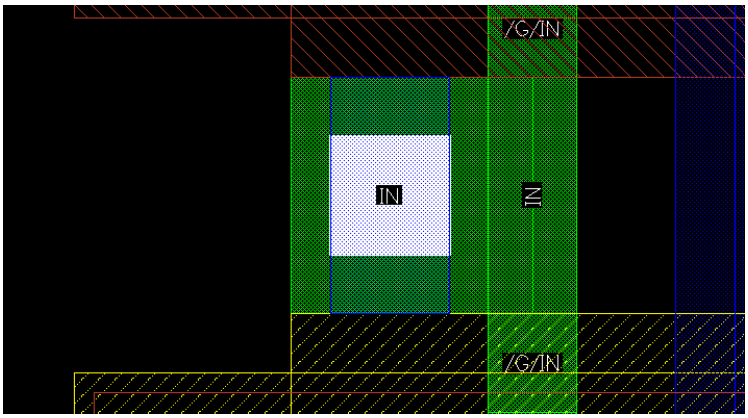
Switch back to the Classic workspace and zoom into the gates of the two transistors. Typically, it is best to avoid routing in Poly due to its high sheet resistance (measured in Ohms per square), but since the gates are already so close it ends up being better with the saved space from avoiding vias (which also have significant resistance). Select the Poly layer from the Layer Palette on the left edge of the window and use the “r” or “p” hotkeys to either manually draw a rectangle or continue the path to close the gap between the two gates. Switch to the Metal1 layer and use the same steps to connect the NMOS source to VSS, PMOS source to VDD, and the two drains together.

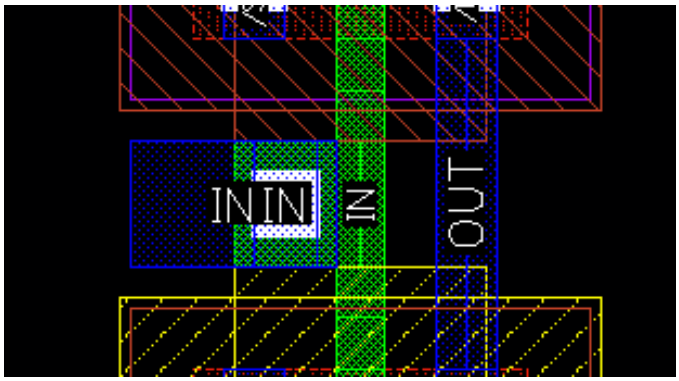


Creating Vias and Pins

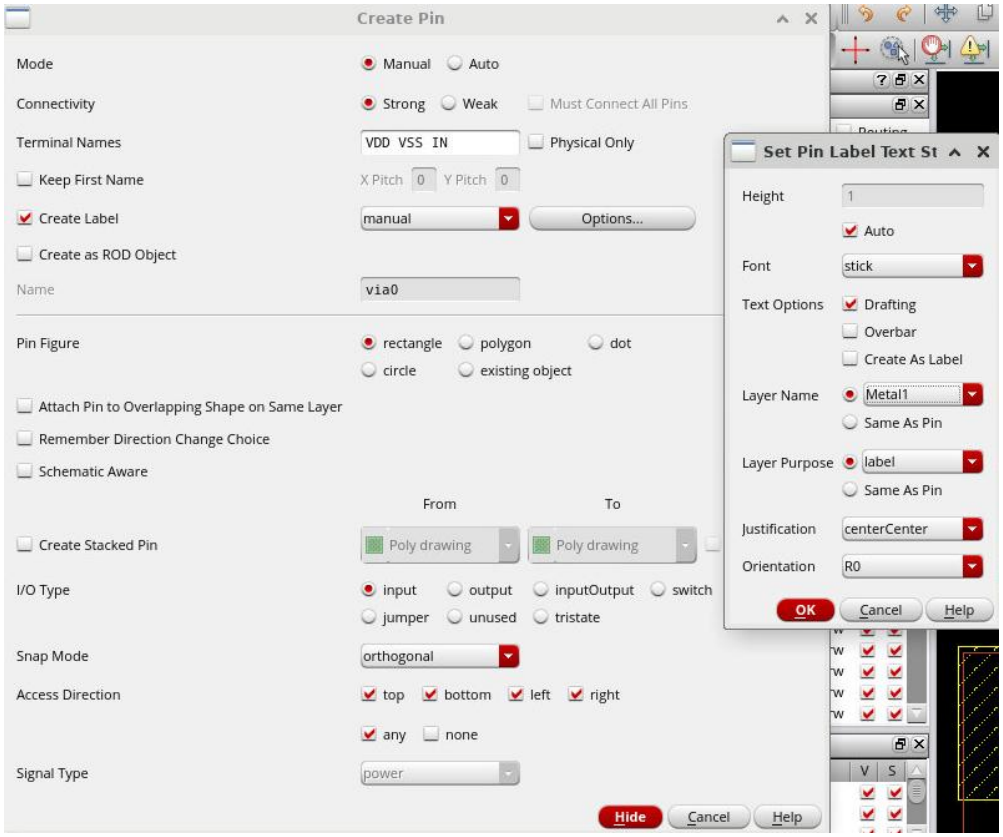
With all of the nets routed (check the Annotation Browser for confirmation), it is time to bring all I/O nets to routing layers. In this case, the only net we need to worry about is the IN net (currently on Poly). Press o to open the via menu, change the mode to “Stack”, and define your start / end layers (in this case Poly > Metal1).

Hide the menu and place the via in the middle of the gate line as shown below. Once placed, make sure to place a larger metal area to ensure that the pin meets the minimum layer area requirement for fabrication.

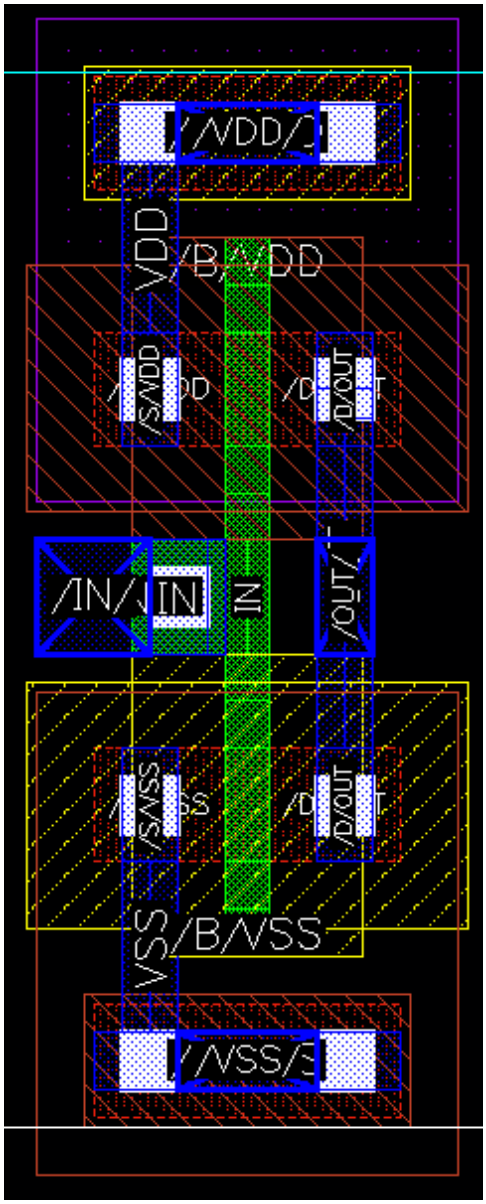




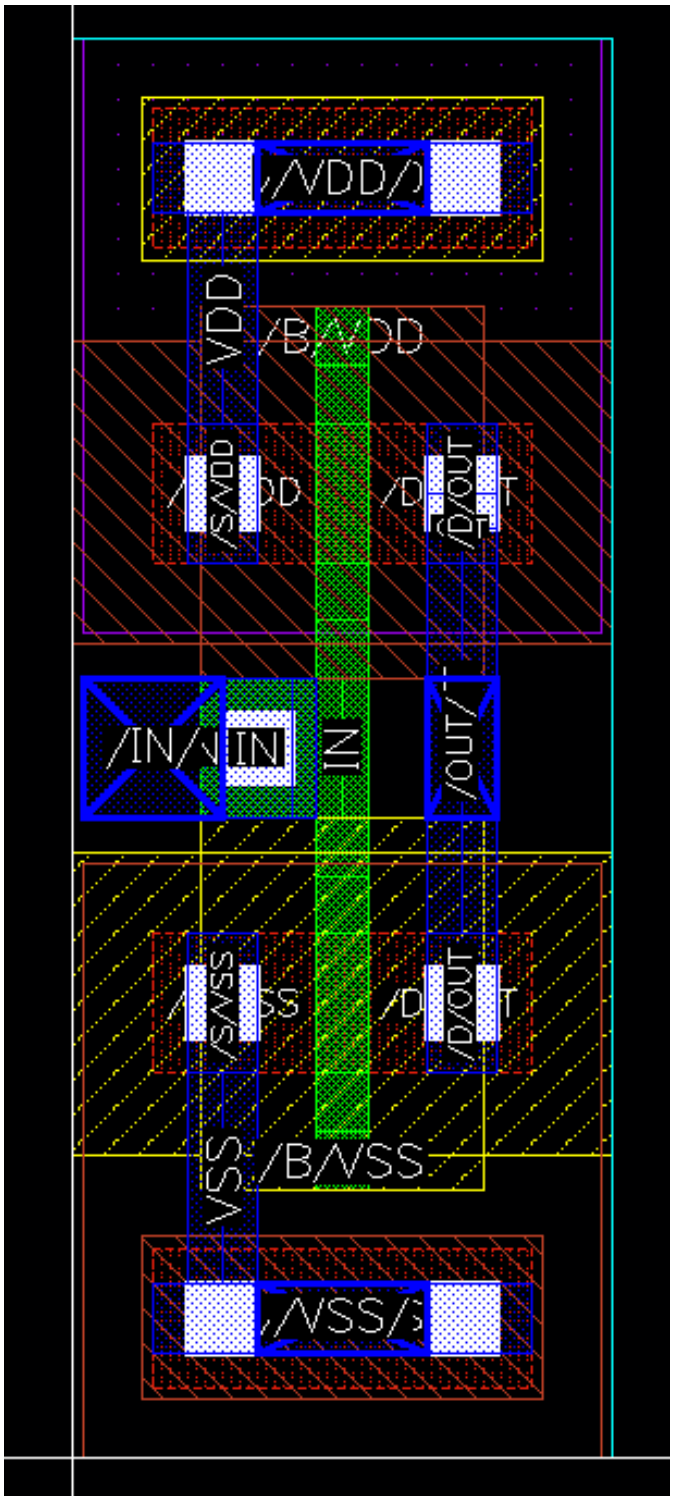
With this, the actual layout is now complete, and the only remaining step is to assign pins for connectivity. Press ctrl+p to open the pin creation menu and enter VDD VSS IN (separated by spaces) in the “Terminal Names” field so that they can be created one after another. Check the “Create Label” box, set the option to “manual”, and open the “Options…” button. In this form, check the “Auto” box under the height field (or set “Height” to 0.01 if this ends up being too big), set the “Layer Purpose” field to “label” and press OK. Set the I/O type to “input” and hide the form to begin creating pins.



For each input pin (VDD/VSS/IN), select the Metal1 pin layer (separate from the drw layer!) and use the pin tool to draw a rectangle on the appropriate net where the pin should be. Once each rectangle is drawn, click once more in the middle of it to assign the label.



Click & drag to select the entire inverter, then use the m hotkey to move (or a to align) the structure with the origin. Use the s hotkey to resize the bounding box to fit the cell, and the inverter layout is complete. Note that if you are having trouble seeing or moving certain layers, visibility and selection toggles are available in the Layer Palette.



Ian Scogin (iscogin@clemson.edu) – Spring 2026