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Abstract

The goal of this project is to create a simplified ISA and processor from scratch. Although simplistic, this processor will incorporate elements and optimizations present in modern processors. To simplify the design, the processor will only use the NAND instruction for data processing, use a very small number of logic registers, and operate on a small amount of data.

NAND CPU

[Document subtitle]

Instruction Formats

|  |  |  |  |
| --- | --- | --- | --- |
| Assembly | Format | Name | Description |
| CP | 0000-X4-P4-D4 | Copy | D = P |
| NND | 0001-S4-P4-D4 | NAND | D = NAND(P, S) |
| IL | 0010-I8-D4 | Load Immediate Low | D[7:0] = I |
| IH | 0011-I8-D4 | Load Immediate High | D[15:8] = I |
| EQ | 01000000-P4-S4 | Equals | PSR = P == S |
| NE | 01000001-P4-S4 | Not Equal | PSR = P != S |
| BR | 01000010-P4-X4 | Branch Register | PC = P |
| JLR | 01000011-P4-D4 | Jump Link Register | PC = P, D = PC |
| INT | 010001-I10 | Interrupt |  |
| HLT | 0100100000000000 | Halt |  |
| B | 010011-I10 | Branch | PC = P |
| JL | 0101-I8-D4 | Jump Link | PC = I, D = PC |
| SL | 0110-I4-P4-D4 | Shift left | D = P << I |
| RL | 0111-I4-P4-D4 | Rotate left | D = P << I |
| LD | 100-I5-A4-D4 | Load | D = MEM[A] |
| ST | 101-I5-A4-D4 | Store | MEM[A] = D |
| J | 11-I14 | Jump | PC = I |