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Abstract

The goal of this project is to create a simplified ISA and processor from scratch. Although simplistic, this processor will incorporate elements and optimizations present in modern processors. This processor is not designed to be efficient, but rather to demonstrate some performance enhancing implementations implemented in modern processors. To simplify the design, the processor will primarily use the NAND instruction for data manipulation, use a very small number of logic registers, and operate on only a small amount of data at a time.

NAND CPU

Description

8-bit instruction CPU with 16 16-bit registers. Works by accumulator architecture; R0 acts as the accumulator, an implied operand and destination in most instructions. R15 acts as the

Instruction Formats

|  |  |  |  |
| --- | --- | --- | --- |
| Assembly | Format | Name | Description |
| CL | 00000000 | Clear | A = 0 |
| CP | 0000-R4 | Copy | R = A |
| NND | 0001-R4 | NAND | A = NAND(A, R) |
| LS | 0010-R4 | Left Shift | A << R |
| RS | 0011-R4 | Right Shift | A >> R |
| EQ | 0100-R4 | Equal | PS = A == R |
| NE | 0101-R4 | Not Equal | PS = A != R |
| BR | 0110-R4 | Branch Register | PS == 1 -> PC = R |
| JRL | 0111-R4 | Jump Register Link | PC = R, R = PC |
| LI | 10-I2-I4 | Load Immediate |  |
| LD | 1100-R4 | Load | A = MEM[R] |
| ST | 1101-R4 | Store | MEM[R] = A |
| INT | 1110-I4 | Interrupt | (Not fully supported) |
| HLT | 1111-I4 | Halt |  |