Tips for Low Level Electrical Measurements by SEM Equipped with Micromanipulators

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Abstract

In this paper, an extensive experimental analysis was conducted to identify the main sources of measurement errors, when low-level electrical measurements are performed on micro- to nano-scaled devices as carbon nanotubes in a scanning electron microscope, equipped with in-chamber micromanipulators. We applied our expertise on wafer-level microelectronic-device characterization to reduce noise and leakage problems that can affect the electrical characterization, when the proper cabling and guarding techniques are not used. In conclusion, guidelines are given to obtain an accurate and reliable measurement setup.

1. Introduction

Low-level electrical characterization of micro- and nano-scaled electronic devices is not an easy, well-established issue [1], [2]. In our research activity, we have the necessity to characterize a small number of Carbon NanoTubes (CNTs), at best one single CNT, grown on silicon (Si) substrate between two contact pads. The Devices-Under-Test (DUTs) were put in a Scanning Electron Microscope (SEM) and contacted by means of remote-controlled MicroManipulators (MMs).

The tentative request for the electrical characterization was to measure at least 1 pA of DC current through the DUT, but even this not-so-stringent limit can be difficult to achieve without taking the necessary care to minimize leakage current and parasitic capacitance, which are inherent to test structure design and measurement configuration.

Moreover, in our experience, the SEM chamber cannot be considered a noise-free environment. Different noise sources can be found, such as the electron beam and the electrical noise due to external equipments (vacuum pumps, ground loops). We found that also MMs, whose motors are driven by high frequency power signals, are a potential cause of noise, if cabling is not accurate.

In this paper, after a brief description of our measurement system and of the test structure (Section 2), we will review different possible configurations connecting instruments to the DUT (Section 3). In these configurations, we have applied our expertise on wafer-level microelectronic-device characterization to reduce noise and leakage problems, as well as measurement errors, due to a wrong setup. In Section 4, the result of different tests will be examined and discussed. Finally, in Section 5, we will summarize the guidelines to obtain the most reliable measurement setup. At the end, in Appendix A the effects of the MOS capacitor, intrinsic to the adopted test structure, will be discussed in detail, while additional results will be presented in Appendix B.

Notice that in this paper we will not present actual results on CNTs, but only measurements on the test structures. As a consequence, in our tests we have not used four-wire (Kelvin) connections, which are the required configuration when performing current-voltage (*I-V*) characterization on CNTs [3]. However, all the suggestions given in this paper depend only on the test-structure design versus cable and instrument setup, so they should be plainly extended to four-wire measurements.

We would like to demonstrate that our analysis is a necessary preliminary step to the actual measurements on devices, to understand the results and to avoid possible errors.

2. Experimental

We have performed our tests inside a Zeiss SEM, model Gemini Leo 1530 (Figure 1).

Figure 1: SEM system at CNR-IMM Bologna.

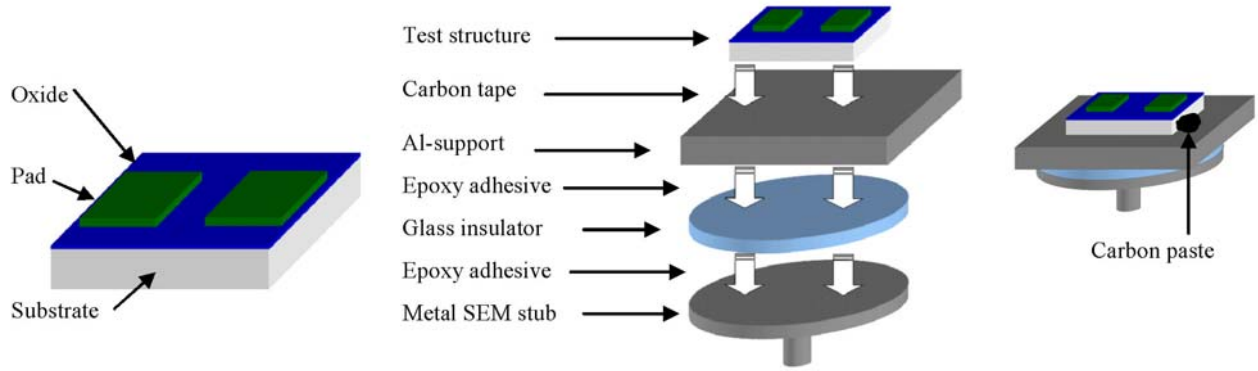


Figure 2: Test structure sketch (left), assembly (centre) and final mount (right).

The SEM is equipped with two Kleindiek MM3A-EM micromanipulators with both standard and custom Low Current Measurement Kit (LCMK-EM), as described in Section 3.1, and tungsten Picoprobe T-4 tips (point radius < 0.1µm).

The electrical measurements were taken by a Semiconductor Parameter Analyzer Hewlett-Packard (now Agilent) HP4145B, which is equipped with four Source-Measure Units (SMUs), each unit capable of sourcing and/or measuring 1pA to 100mA and 1mV to 100V (current measurement resolution 50fA).

The test structures, sketched in Figure 2 (left), are square chips, with area of ~1cm^2, consisting of:

- A n-type Si substrate (light grey), ~500µm thick, doped with a donor atom concentration N_D ~3×10^{15}at/cm^3;
- An insulating SiO_2 layer (blue), 100nm thick, thermally grown;
- Two insulated pads (green), realized from a poly-Si layer, 300nm thick, which has been deposited by LPCVD and n-doped heavily by phosphorus to be conductor-like (sheet resistance $R_{\square}$ = 20Ω/□). The pads have been defined by photolithography with an area of ~2.5×10^{-3}cm^2 each and with a spacing of 2µm.

CNTs are intended to be grown or deposited between the two poly-Si pads, so that an *I-V* measurement could be performed easily by contacting the pads with two (or four) MMs, assuming a good ohmic contact between the CNTs and the pads.

To mount and manage easily the test structures over the SEM stage, samples have been glued on an aluminium support (dark grey square item in Figure 2, centre) by a conducting carbon-based tape. In turn, this support was glued on a glass insulator layer (cyan round object), consisting of a microscope slide, by a moisture insulating adhesive (Torseal epoxy). Finally, the sample was glued on the metal SEM stub (dark grey round object), to be fixed to the SEM stage by the same epoxy adhesive.

Al-support holds a pin connector to provide an electrical connection to the substrate. To optimize the contact resistance between substrate and Al-support, conducting carbon-based paste was deposited on one substrate side (black spot in, right) in addition to the carbon tape, thus obtaining a typical value < 80Ω. On the contrary, the insulation of the substrate versus the SEM stub was successfully verified.

3. Measurement configurations

Low level measurements impose a lot of precautions to minimize errors, including proper grounding, screening and guarding of the measurement system, which should be intended as a whole, including the test structure, the instruments and the cabling.

3.1. Cable guarding and screening issues

Figure 3 shows (left schematics) two possible sources of error when making current measurement on a CNT, represented as a resistor (red). Here the measured current is the sum of: (*i*) the real current flowing through the CNT, I_C, plus (*ii*) the electromagnetic-induced noise current, I_N, and (*iii*) the leakage current, I_L, related to the cables and the test structure design. Note that also the capacitive paths in the circuit could influence quasi-static measurements, because of the non-zero RMS value of I_N and the possible long transient displacement components in I_L.

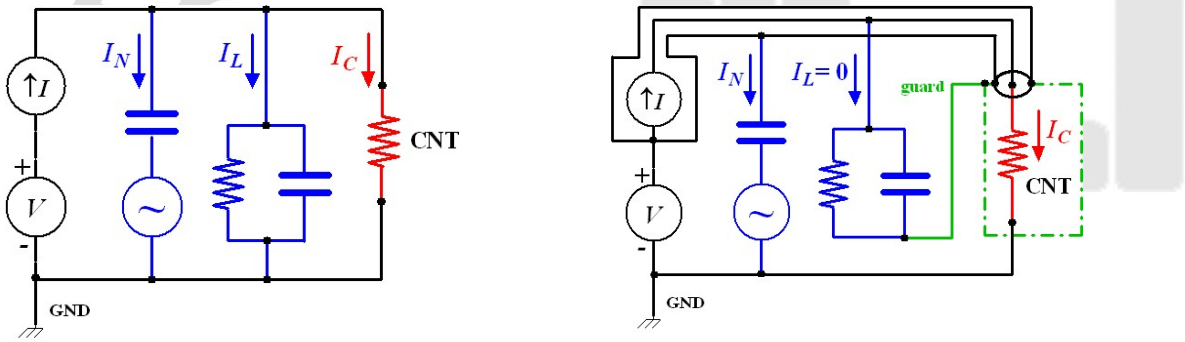


Figure 3: Unguarded (left) and guarded (right) measurement configurations.

To minimize these problems, a guard technique is usually suggested (Figure 3, right schematic), where a coaxial guard screen surrounds the measurement cable from the current meter to a point very close to the DUT. Because of the low internal impedance of the current meter, the guard is driven to the same measure potential, thus effectively shorting ($I_L = 0$) the leakage path due to the cable. Also the electromagnetic noise is reduced ($I_N \sim 0$), because it is induced mainly in the guard loop, thus not affecting the measured current. Note the opportunity of extending the guard screen ("full-guarded" configuration) to comprise the test structure (green hatched rectangle in right schematics), thus shorting even the admittance paths to ground localized in the DUT.

To make feasible these connections, Kleindiek Nanotechnik provided a couple of custom triaxial LCMK-EM cables, shown in Figure 4. The differences versus the standard LCMK-EM are outlined:

- The outer screen of the triaxial cable at COM reference potential (see next Section 3.2) is isolated from ground (insulating cable cover, isolated MM3A-EM feedthrough connector, isolated cable clip);
- A pin connector is provided at the end of the outer screen for the SMU COM reference point (at ground potential), suitable for a connection to the test structure and/or to the SEM stage;
- A pin connector is provided at the end of the inner screen for a full-guarded connection to the test structure.

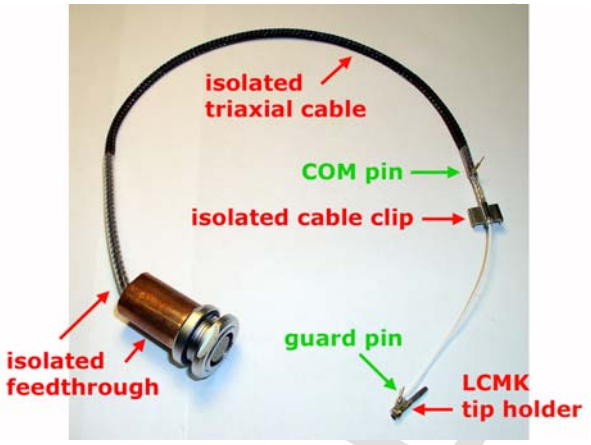


Figure 4: Custom LCMK-EM provided by Kleindiek.

3.2. Test configurations

Figure 5 shows how the full-guarded technique has been implemented in our tests with the custom cables.

SMU-1 of the HP4145B is connected to our test structure by the triaxial cable and LCMK-EM, which extends as close as possible to the DUT. The inner conductor (Hi) is connected to the left pad via the probe tip. The inner shield of this cable is the guard, driven to the same potential and electrically connected to the substrate, with a wire (green) as short as possible. Of course, the substrate is isolated from the SEM stage.

SMU-3 is the ground unit, which imposes a zero reference potential (COM) to the right pad (Lo) through another triaxial cable and LCMK-EM, but without guard connected to the test structure.

The SEM stage was held to ground potential. In this way, all interferences in the measurement results, due to a floating electrode, should be avoided. For this purpose, SMU-2 was used as ground unit (COM reference point) during our tests, so giving the possibility also to measure the current through the SEM stage to ground.

It should be recommended, in order to avoid ground loops, to keep separated the overall ground (GND) from the SMU COM point (virtual ground, i.e. the zero-voltage node where all currents converge), which corresponds also to the triaxial outer screen. The joining should be done only in one point: a jumper is provided in the back panel of HP4145B for this purpose.

Notice that, once verified the correct setup for electrical measurements, both SMU-2 and SMU-3 could be eliminated, connecting directly SEM stage and right pad to COM by the wire tied to the outer screen of the left LCMK-EM (SMU-1). In this way, only one SMU is really necessary.

To remark the benefits of the guard technique permitted by the custom cables, notice that, if the oxide is leaking, the current value through the CNT, measured by SMU-1, is wrong, i.e. $I_1 = I_C + I_{L1}$, without using the guard wire (green in Figure 5). However, the correct reading is obtained connecting guard to substrate. In fact, $I_{L1} = 0$, because there is no voltage difference between the left pad and the substrate. As a consequence, SMU-1 measures the true current through the CNT, i.e. $I_1 = I_C$. Also the capacitive effects, due to the oxide, are cancelled. Note that, in this configuration, the ground unit SMU-3 measures a wrong current through the CNT, i.e. $I_3 = -(I_C + I_{L3})$.

Conversely, the substrate could be connected to the SMU-3 guard (COM ground potential): in this case SMU-3 should measure $I_3 = -I_C$ correctly, while SMU-1 measures a wrong current. Incidentally, this is also the only measurement possible with the standard LCMK-EM cables, connecting the substrate to COM via Al-support and SEM stub.

To point out the enhancements using the custom LCMK-EM cables, we have compared four different configurations ("*Setup*") of cables/connections to the test structure, without any CNT grown between the pads. The distinctive features of all configurations are summarized in Figure 6.

Effectively, we have compared the configuration feasible by the custom LCMK-EM cables (*Setup #1*, as in Figure 5) with the configuration done by the standard LCMK-EM (*Setup #2*). In addition, *Setup #3* differs from *#1* for the substrate connection (ground vs. guard), while *Setup #4* is equivalent to *#2*, but using the custom cables. No setup was defined leaving the substrate floating, i.e. Al-support not connected, to avoid unpredictable and not-measurable capacitive effects.

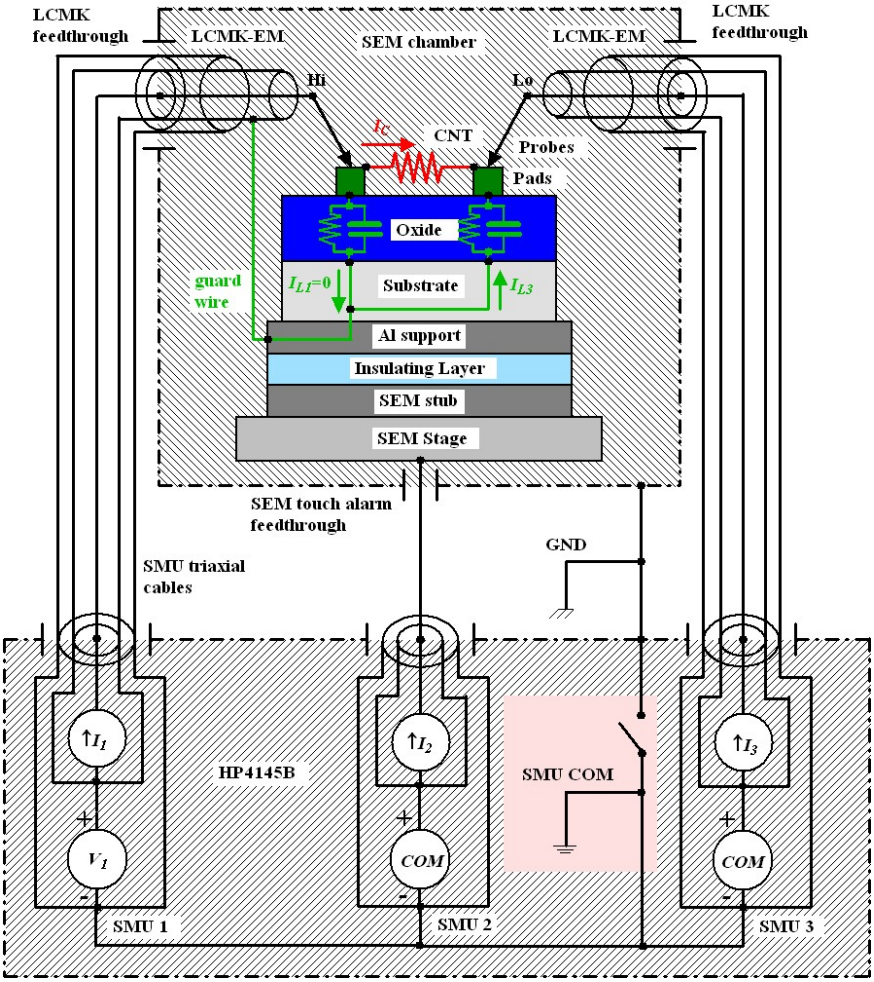


Figure 5: Guarded measurement configuration with test structure (*Setup #1*).

3.3. Test conditions

We have chosen to perform all tests without any CNT grown between the pads, thus effectively evaluating only the noise sources in the measurement system and the leakage paths in the test structure. In fact, these interferences could seriously affect the accuracy of the electrical measurements on the DUT.

The various tests were performed by HP4145B on three channels (SMU-1, SMU-2, SMU-3, see Figure 5) by forcing voltage and acquiring current. Digital averaging was not used, i.e. only one current measurement was taken for each measurement step (time or voltage), choosing a SHORT integration time. Two kinds of measurements were performed:

a. Time-Domain Measurements

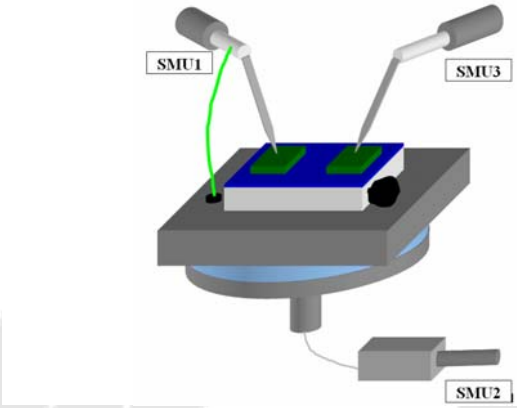
In this case, the voltage, forced by SMU-1, was held at a constant value V_1, chosen between the three values 0V and ±30V, while the other two SMUs were programmed as ground units (COM ground potential). The current values for all three channels were measured at an Interval Time ranging from 0.5s to 5s. The total measurement time was fixed to 300s (reduced when the Interval Time was 0.5s, because of acquisition buffer limits), thus the total number of acquired points depends on the Interval Time.

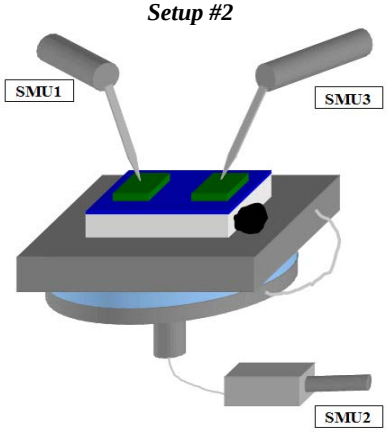
b. Sweep Measurements

In this case, an *I-V* characterization was performed sweeping the voltage forced by SMU-1, V_1, in a staircase manner from 0V to $V_{1,max}$, with the other two SMUs set to COM. Note the two separate sweeps, for negative and positive voltages. The maximum voltage $V_{1,max}$ was chosen between the two values ±70V, while the voltage step was defined as $V_{1,max}/100$. The step duration was the sum of the programmed step Delay Time, ranging from 0.1s to 2s, plus the analogue integration time, needed to sample and measure the current.

Moreover, all measurements have been performed in two different conditions (see Figure 7), i.e.:

1. Lifting up the two probe tips, well-separated each other, so effectively avoiding any current path through the test structure ("*tips up*"). In this way, it is possible to establish a reference condition with the minimum noise and leakage levels attainable, due only to the measurement setup without any interference from the test structure;
2. Keeping the two probe tips in electrical contact with the respective poly-Si pads on the test structure ("*tips down*"), thus pointing out the leakage and the capacitive effects due to the test structure.

<table>
<tr>
<td>Setup #1
 

Custom LCMK-EM triaxial cables (Figure 4).
Substrate connected to SMU-1 guard (inner triaxial screen) by a wire, via the Al-support.
</td>
<td>Setup #2
 

Standard LCMK-EM triaxial cables.
Substrate biased to COM (ground) level by SMU-2, via the Al-support connected to the SEM stub.
</td>
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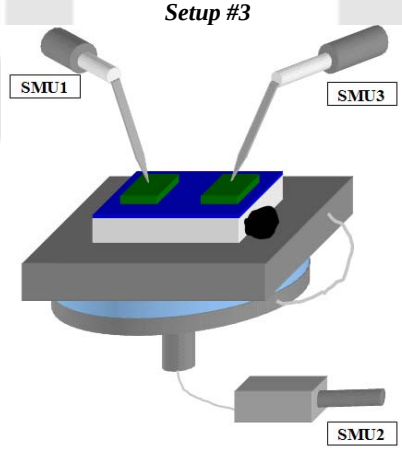
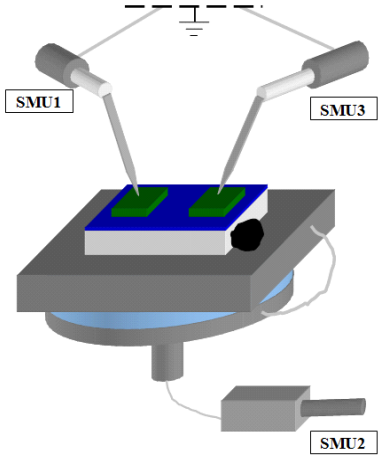
<tr>
<td>Setup #3
 

Custom LCMK-EM triaxial cables (Figure 4).
Substrate biased to COM (ground) level by SMU-2, via the Al-support connected to the SEM stub.
</td>
<td>Setup #4
 

Custom LCMK-EM triaxial cables (Figure 4).
Substrate biased to COM (ground) level by SMU-2, via the Al-support connected to the SEM stub.
</td>
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<tr>
<td>Setups #1 and #3:

Outer triaxial screens of all SMU tied at HP4145B COM, isolated from GND inside the SEM chamber.
COM terminal should be connected to GND by a jumper in HP4145B back panel (Figure 5).
</td>
<td>Setups #2 and #4 (electrically equivalent):

SMU-1 and SMU-3 outer triaxial screens connected to GND inside the SEM chamber.
It is recommended not to connect COM to GND at HP4145B back panel, to avoid possible ground loops.
</td>
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</table>

Figure 6: Different measurement configurations under test.

Tips up ***Tips down***

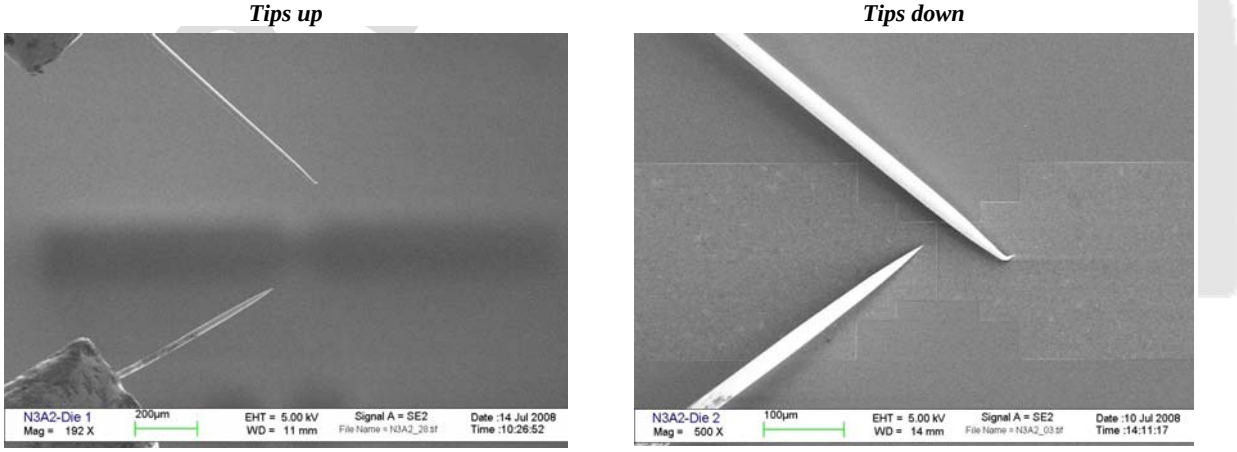

Figure 7: Test conditions for the probe tips.

4. Results and discussion

In this Section, we will firstly discuss on the main sources of noise we have identified during our tests (Section 4.1), giving also some hints on how to minimize these problems. Notice that noise is independent of the different configurations. Secondly (Sections 4.2 and 4.3), we will compare the results obtained with different measurement configurations.

4.1. Noise sources

Different noise sources can be identified in the measure system itself, in particular the electron beam current and the electrical noise from the MM control boxes. In the following tests, remarking that noise is independent of the different configurations, we used *Setup #1* with *tips down*.

a. Noise from the SEM beam

To examine the noise induced by SEM beam, whose energy was set at 5keV, the scanning area was reduced (see Figure 8) to cover (*i*) only some portion of the right poly-Si pad, where SMU-3 was connected (green square), or (*ii*) a smaller portion of the right pad and some area of the surrounding oxide, in addition to part of the right probe tip (red square). Note that the left probe and pad, which are connected to SMU-1, are never directly exposed to the e-beam. To avoid noise from MMs (see next Section 4.1b), their cables were disconnected from the control boxes.

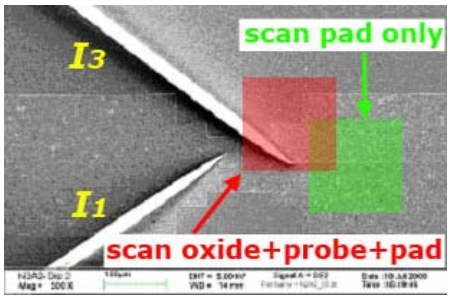

Figure 8: Test setup for e-beam noise.

Time-domain measurements of I_1 and I_3 (Figure 9), without any voltage applied, show the result of these tests: the measure of I_1 (left plot) is not influenced by the SEM beam in both conditions, because the probe is electrically isolated from the beam-induced current by the oxide. On the contrary (right plot), I_3 is strongly affected by the e-beam. When the beam is all the time on the right pad (right plot, green curve), it generates free charge carriers in the exposed portion of the pad, which are partially collected by SMU-3 as a constant current of ~50pA. In the second condition (right plot, red curve), at some time there is a reduced or null current collected by SMU-3 when the beam is outside the pad, over the insulating oxide.

Luckily, the noise due to the SEM beam can be simply cured, in our system, by switching off the beam during the effective low-level measurement, after the operator has placed the MM probes on the pads and is certain of a good electrical contact. Note that, when observing with SEM the MM movements to place probes, before actually taking electrical measurements, it is suggested to keep the substrate at ground potential to avoid DUT charging as much as possible. In *Setup #1* this can be obtained simply programming SMU-1 as ground unit for the needed time, while no problems arise in the other configurations.

In all following issues, we will assume that the SEM beam has been switched off during the electrical measurements.

b. Noise from MM control boxes

When not adequately connected as suggested below, the Kleindiek NanoControl (NC) boxes, which drive the MM3A-EM piezo motors, can be source of electrical noise.

Figure 10 shows time-domain measurements of I_1, with *tips down* and without any voltage applied, when the NC boxes, properly grounded by the *Shield* port on the rear panel (see Figure 11 and related text below), are powered. An undesired signal in the ±100pA range is introduced on I_1 (red curve). Similar results are found measuring I_3.

This signal could be due to electromagnetic noise generated by NC boxes and picked up by the LCMK-EM tip. This is not surprising, since Kleindiek uses a digitized sawtooth signal, with amplitude ±80V and frequency ~2.7kHz to drive the MM piezo actuators. However, the strange shape of the red curve is probably only an artefact, depending on HP4145B sampling the RMS value of the noise. The signal is strongly reduced to ±4pA when the NC boxes are switched off (black curves), and it is present (±3pA) even if the boxes are unplugged from the AC power line. The signal disappears (blue curves) only unplugging the MM air-side cable, which links the NC

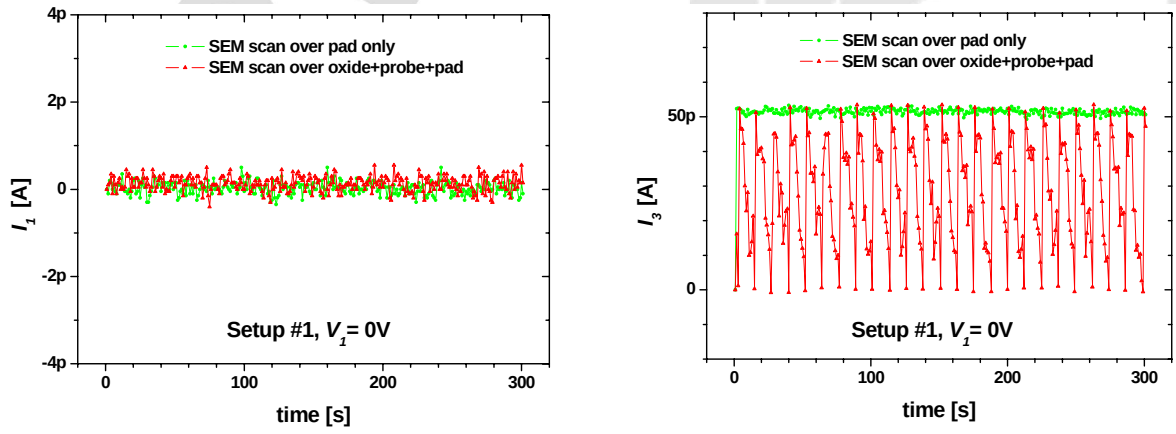

Figure 9: Test results on e-beam noise (*Setup #1*).

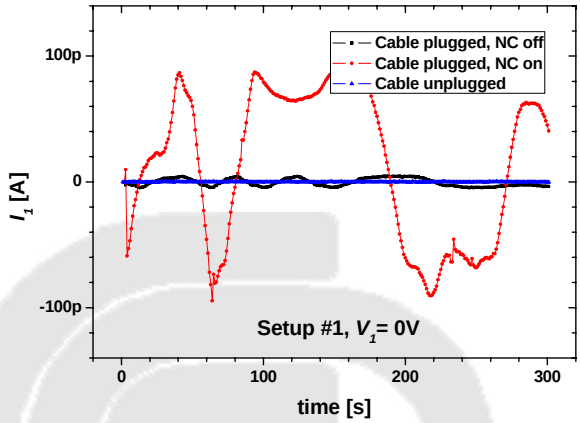

Figure 10: Test results on noise due to micromanipulator control box (*Setup #1*).

boxes to the SEM feedthrough via the air-side splitter box, suggesting that NC boxes are picking up also environmental noise.

If disconnecting the control cable is obviously an impracticable solution to reduce noise, also switching off/on the NC boxes must be avoided, because this operation makes the probe tips visibly move! This undesired movement could negatively affect the electromechanical contact with the pads, but also it could damage the test structure and/or the tip, at the worst.

Luckily, also this noise source can be cured as shown in the following paragraphs, i.e. connecting to ground the *Tip* port on the rear panel of the NC box. ‡

‡ **Note:** Kleindiek system manuals do not provide clear and extensive information about this issue:

- At page 7 of the MM3A-EM System Setup and Quick Reference Guide it is written, for systems containing only one manipulator: "*Ground the tip of the manipulator by connecting the Tip port to the Shield port using the grounding cable provided. In order to measure electrical current with the tip of the manipulator, connect your measurement device to the Tip port at the back of the NanoControl*". For systems containing multiple manipulators, the manual suggests the use of the BNC connectors, provided on the air splitter box, to achieve the same purpose.
- At page 4 of the MM3A-EM Micromanipulator System manual it is written: *"Shield port is intended for grounding the manipulator. For Life Science applications, this should be connected to common ground. For Material Research applications with systems that contain only one manipulator this port should be connected to the Tip port using the grounding cable provided"*, as well as "*Tip port is connected to the tip of the manipulator and allows current measurements (probing) to be performed*".
- At page 2 of the LCMK-EM Low Current Measurement Kit for the MM3A-EM manual it is written *"Ground the tip holder in order to keep magnetic pickup as low as possible: for systems with one manipulator connect the Tip and Shield ports at the back of the NanoControl using the grounding cable provided. For systems with multiple manipulators, use a BNC terminator on the respective BNC output of the air-side splitter box"*.

To the MM user, it is clear the purpose of the *Shield* port on the rear panel (Figure 11): it should be connected to ground (GND), following all the well-known recommendations, i.e. adopting a star-type distribution of the GND lines from a single point to all instruments, thus avoiding ground loops.

Figure 11: Rear panel of NanoControl box.

Conversely, the usefulness of the *Tip* port, which provides a direct connection to the probe tip when using the standard (not triaxial) tip holder, is much less intuitive when LCMK-EM is used. In fact, all the signals carried by the triaxial LCMK-EM, i.e. inner conductor to the probe tip, inner shield or guard, outer shield or COM/GND, are isolated from the *Tip* port. As a consequence, the MM user could leave disconnected the *Tip* port, as in the noise tests of Figure 10.

However, Figure 12 shows time-domain measurements of I_1 and I_3 in the same conditions previously used, i.e. with *tips down*, without any voltage applied and with the NC boxes properly grounded by *Shield* port, but, in addition, connecting the *Tip* port on the rear of the boxes to GND just by a jumper between *Shield* and *Tip* ports. In this way, the noise signals related to NC boxes are totally suppressed, thus having the same noise level (±0.5pA on I_1 and ±1.2pA on I_3) which were found disconnecting the controller cables (blue curve in Figure 10), regardless of the NC box status (switched on/off, cables plugged/unplugged).

The greater noise found on I_3 with respect to I_1 could be due to the lower efficacy of the SMU-3 guard screen, which does not include the substrate.

In all following issues, we will assume that the *Tip* port has been grounded during the measurements.

4.2. Time-domain measurement results

Once applied all the suggestions given in Section 4.1, time-domain measurements (see Section 3.3) have been carried out on the test structures forcing by SMU-1 two voltage values, $V_1 = \pm 30$V, and measuring current. In this way, we are able to compare the performance of the different configurations proposed in Section 3.2.

Firstly, we have found with *tips up* the same reference noise levels as in Figure 12, for both currents, I_1 and I_3.

With *tips down*, Figure 13 shows the results obtained using *Setup #1*, i.e. using the custom LCMK-EM cables with guard connection to the substrate. The different curves in each plot are related to three choices of the

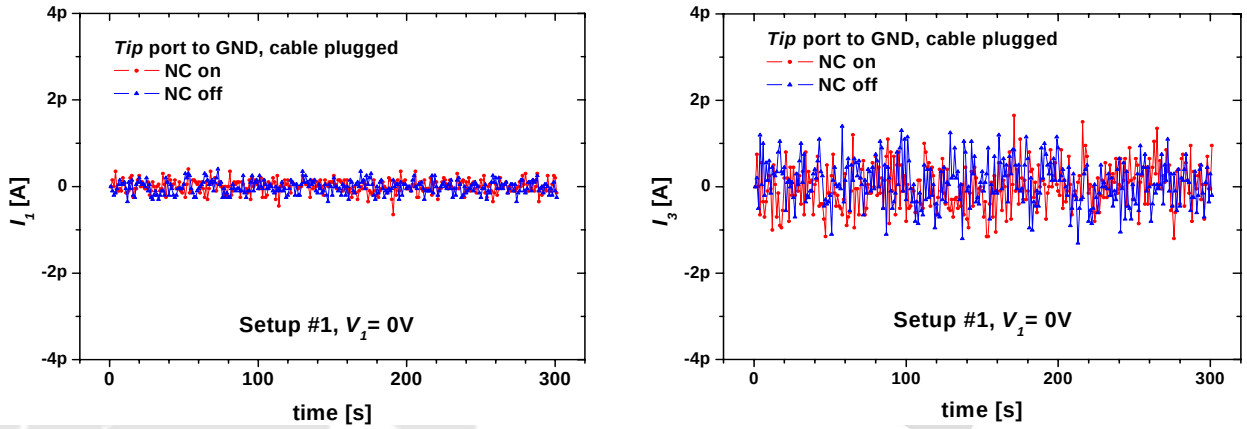

Figure 12: Test results on noise when *Tip* port on NanoControl box is connected to ground (*Setup #1*).

Interval Time (0.5, 1 and 5s) for the HP4145B acquisition. No worsening, with respect to the reference noise levels, is found in I_1 measurement for both V_1 values (left plots), excluding a very low, negligible capacitive effect at the beginning of data acquisition. Conversely, the I_3 measurement, which is only slightly noisier for negative V_1 value (right bottom plot), shows for positive V_1 value a huge capacitive-like effect, i.e. a peak displacement current of ~100pA (right up plot).

This result proves the efficacy of the full-guarded technique on the parasitic admittance effects, due to both measure system and test structure. In our test (see Figure 5), I_1 is the sum of both the leakage and displacement current flowing through the right pad and the oxide to the substrate. But no current is present because pad and substrate are at the same potential, thanks to the guard wire. Thus, the oxide capacitance and conductance are effectively shortened.

Conversely, I_3 is the displacement charging current of a MOS capacitor, consisting of the gate (right poly-Si pad at COM ground potential), the underlying oxide, and the substrate (at V_1 potential through the SMU-1 guard wire). The asymmetry of I_3, with respect to the V_1 sign, can be justified (see Appendix A for more details) considering that:

- The n-type substrate is driven in accumulation of charge at the surface with oxide, when its potential is negative (V_1 = -30V in our test) with respect to the gate at COM potential. In this case, the majority charge movement is very fast and it is not revealed by our measurements;

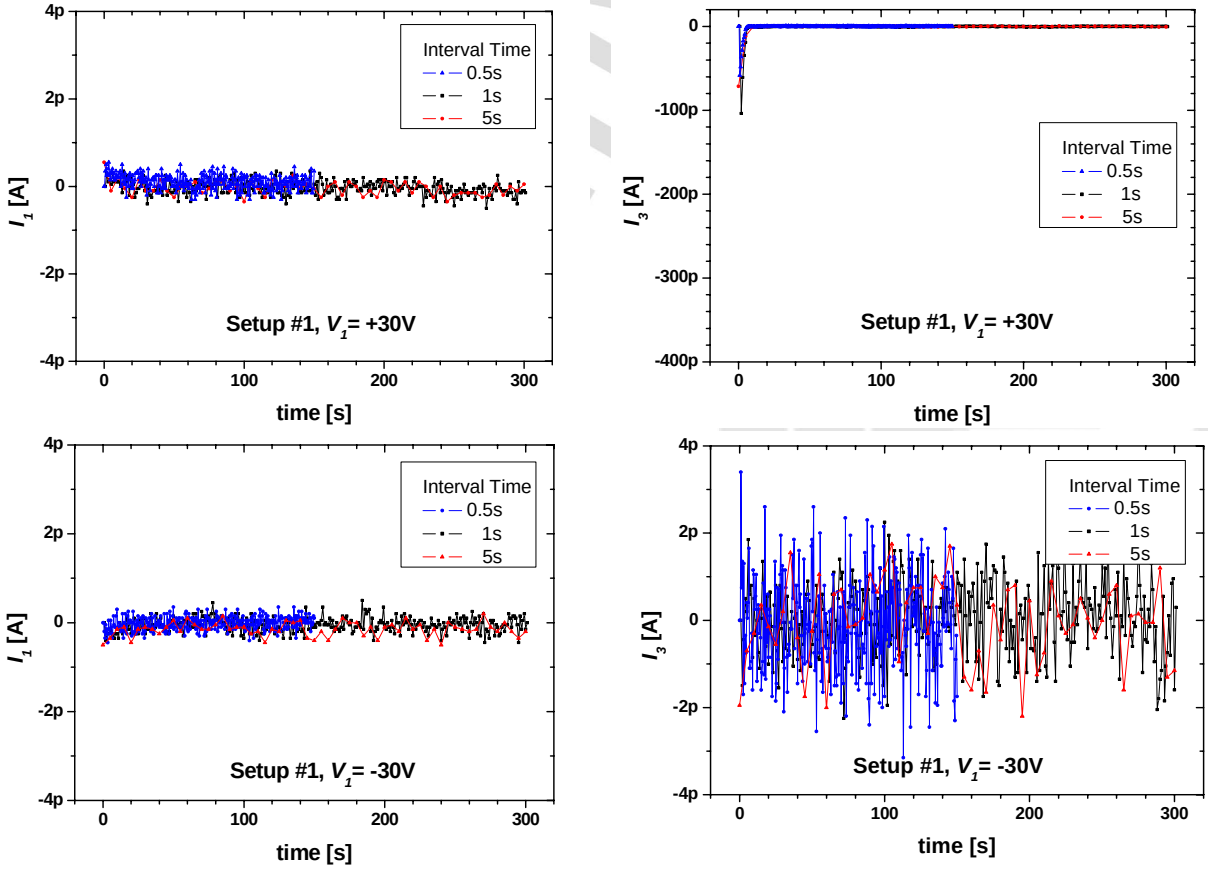

Figure 13: Time-domain current measurement results, obtained with *Setup #1* and V_1 = ±30V.

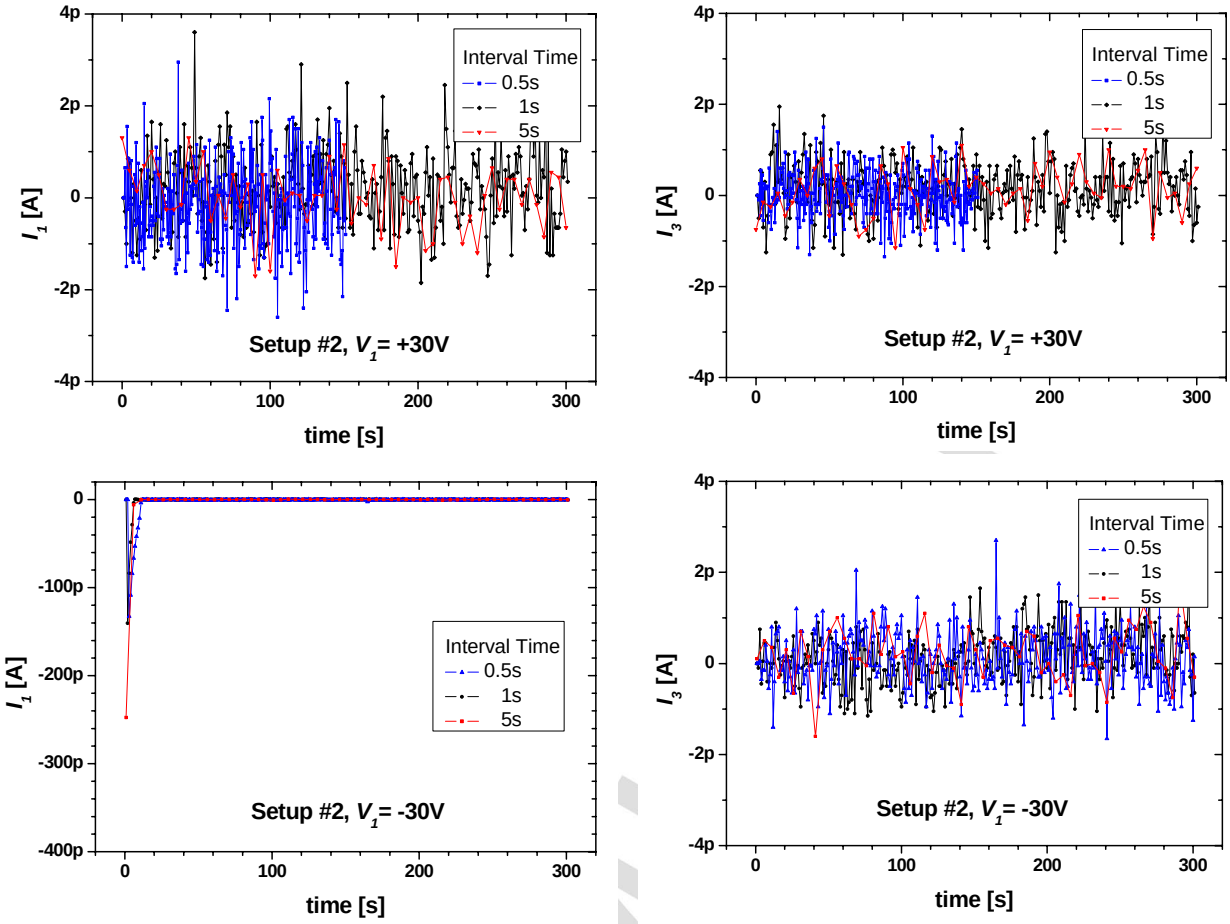

Figure 14: Time-domain current measurement results, obtained with *Setup #2* and V_1 = ±30V.

- The n-type substrate is driven in charge inversion at the surface with oxide when its potential is positive (V_1 = +30V in our test) with respect to the gate. In this case, the minority charge build-up is slow, so a displacement current is detected after applying V_1.

For comparison, Figure 14 shows the results obtained using *Setup #2*, i.e. using the standard LCMK-EM cables without guard wire. The different curves in each plot are related to the same three choices of the Interval Time (0.5, 1 and 2s) for the HP4145B acquisition.

In this configuration, I_1 measure is fairly good only for positive V_1 (left up plot in Figure 14), while for negative V_1 value (left bottom plot), I_1 shows a huge capacitive-like effect, i.e. a peak displacement current of more than 200pA. Conversely, in this configuration no effects are present in I_3 measure, which preserves its usual noise levels, i.e. higher than those measured on I_1 using *Setup #1*, probably for the absence of guard line to the substrate.

In fact, the situation is reversed with respect to *Setup #1* (see Appendix A for more details):

- The MOS capacitor under the right pad is not biased (both gate and substrate are at COM ground potential), so I_3 is always null;
- The MOS capacitor under the left pad now has the gate at V_1 potential and the n-type substrate at ground potential. It is driven in inversion only when the gate is negative (V_1 = -30V in this test), thus showing the peak displacement current of left bottom plot in Figure 14.

The measurements relative to *Setup #3* and *Setup #4* are completely equivalent to those obtained for *Setup #2*, so they are not discussed here, but reported in Appendix B, Figure 20 and Figure 21 respectively. §

From all preceding considerations, the usefulness of using *Setup #1* has been demonstrated to reduce leakage and capacitive-like current components when measuring I_1, which represents the real current forced in the DUT, when it is present. For other *Setups*, the real DUT current could be evaluated only from the return-to-ground current I_3, but at the expense of more noise. On the contrary, measuring the reciprocal currents, i.e. I_3 for *Setup #1* or I_1 for *Setup #2*, will produce tricky measurement errors, because of these undesired current components.

§ **Note:** As additional information, we have acquired the data (not shown) related to I_2, i.e. the current through the SEM stage to ground (COM), measured by SMU-2 (see Figure 5). For *Setup #1*, we found a huge (peak value of ~300pA) and long (~200s) transient, which can be attributed to dielectric absorption in the glass layer, which is biased between V_1 by SMU-1 guard, connected to the Al-support, and COM by SMU-2, connected to SEM stage. In this case, the return currents, corresponding to $-I_3$ and $-I_2$, cannot be measured on the SMU-1 guard line. For *Setups #2*, *#3* and *#4*, we measured a current $I_2 = -I_1$, because in these configurations the substrate is directly connected to the ground, so SMU-2 is just the return-to-ground path of the current imposed by SMU-1 on the left MOS capacitor. Corresponding results were obtained for sweep measurements.

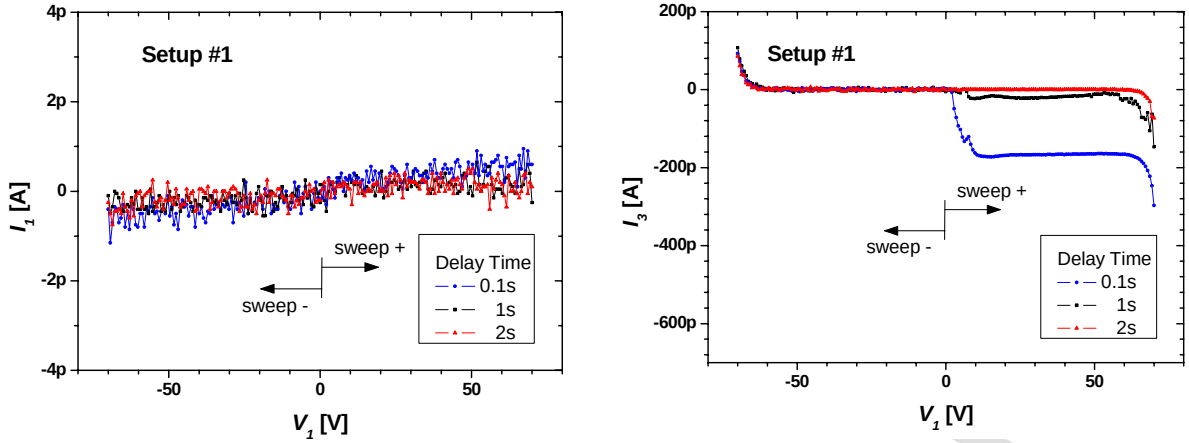

Figure 15: Sweep current measurement results, obtained with *Setup #1* and $V_{1,max}$ = ±70V.

4.3. Sweep measurement results

I-V sweep measurements confirm the time-domain results, presented in Section 4.2.

Two different sweeps, positive and negative, have been performed varying V_1 from 0V to $V_{1,max}$, with $V_{1,max}$ = ±70V (see Section 3.3).

For both currents I_1 and I_3, we found with *tips up* the same reference noise levels shown in Figure 12, there without any voltage applied.

With *tips down*, Figure 15 shows the results obtained with *Setup #1*, varying the Delay Time (0.1, 1 and 2s) for the HP4145B staircase generation and data acquisition. The I_1 measurement (left plot) is quite good, the noise is low and a negligible effect of the Delay Time was found. Conversely, huge capacitive-like effects are visible in I_3 measurements (right plot), for positive sweeps and when a relatively short Delay Time is chosen.

In addition, the leakage current in the oxide is quite evident in I_3 sweeps when the applied voltage is over ±60V, while I_1 measurements are unaffected, again for the reason that no voltage is applied to the MOS capacitor under the left pad (SMU-1).

The asymmetry of I_3, with respect to the V_1 sign, can be explained as for time-domain measurements in Section 4.2 (see Appendix A for more details). In particular, for positive V_1 sweeps, the I_3 shape can be justified by the displacement current needed to grow the inversion layer in the MOS capacitor under the right pad: when successive staircase voltage steps are applied, after each step the displacement current shows a fast rising peak, which decays more slowly in the step duration. The actual current measurement is taken by HP4145B in each step after a fixed Delay Time: the longer is this, the smaller is the measured displacement current (no current at all after a Delay Time of 2s in our tests). Conversely, for negative V_1 sweeps, the n-substrate is driven in accumulation, so the very-fast-decaying displacement current pulses are not revealed by the "slow" HP4145B.

For comparison, Figure 16 shows the results relative to *Setup #2*, using the standard LCMK-EM cables. As discussed in Section 4.2 (see Appendix A for more details), now capacitive-like effects, related to the inversion charge, clearly affect the measurements of I_1 current (left plot), but only for negative sweeps. Also, leakage in the oxide, when V_1 exceeds ±60V, is quite evident. Both interferences seem higher than in *Setup #1*. The I_3 current does not show wrong behaviour (right plot), but the noise level is higher than I_1 in *Setup #1*, because of the minor screening effect permitted by *Setup #2*.

The sweep measurements, made with *Setups #3* and *#4*, are completely equivalent to those obtained with *Setup #2*, as expected from time-domain results (Section 4.2). For this reason, the results are not discussed here, but reported in Appendix B, Figure 22 and Figure 23 respectively.

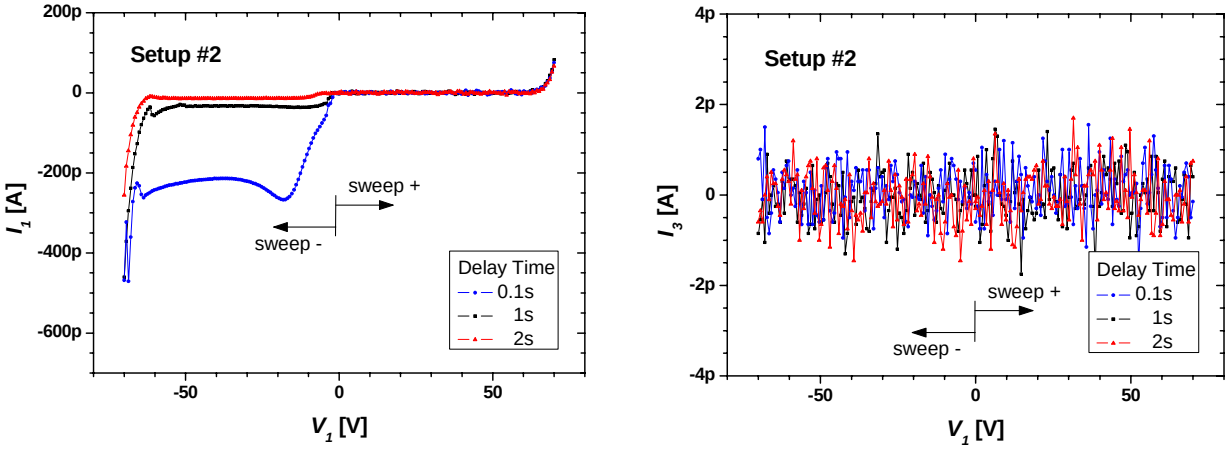

Figure 16: Sweep current measurement results, obtained with *Setup #2* and $V_{1,max}$ = ±70V.

5. Conclusions and guidelines

An accurate analysis has suggested the usefulness of the guard technique for low-level electrical measurements, especially to avoid measurements errors on nanoscaled devices, such as CNTs, due to undesired displacement and leakage currents, which are intrinsic to the test-structure design.

Custom triaxial cables were prepared to achieve a full-guarded configuration for low-level electrical measurements, to be performed in a SEM equipped with Kleindiek micromanipulators. From our tests, this configuration shows reduced noise and lower capacitive-like effects, with respect to the configuration using standard cables, thus allowing noise lowering below 1pA. Moreover, only the full-guarded configuration permits the direct measurement of the current forced through the DUT.

Finally, some guidelines can be given to reduce noise problems and measurement errors:

- The test structure, holding the DUT, should be carefully designed to minimize leakage paths and parasitic capacitances. When possible, electrodes and conductive layers, able to act as electrical screen, should be provided, as well as electrical connections to them (Section 2);
- Guarded measurements are recommended to minimize possible measurements errors, due to leakage paths in the test structure and displacement current effects (Sections 3.1 and 3.2). To realize full-guarded configurations, special LCMK-EM triaxial cables are needed, which can be provided by Kleindiek Nanotechnik (Section 3.1).
- During low-level electrical measurements, the SEM e-beam should be switched off, to reduce the noise due to charge collection from the DUT. The probes should be placed before the actual measurement, keeping the test structure to a ground potential, in order to avoid charging the DUT (Section 4.1a);
- Using Kleindiek MM3A-EM micromanipulators with LCMK-EM triaxial cables, the connection of the NanoControl *Tip* port to ground (*Shield* port) is of fundamental relevance to suppress the noise contribution from the control boxes (Section 4.1b). **

Applying the above guidelines, a noise-current level under 1pA can be easily reached (Sections 4.2 and 4.3), but these could be further and easily reduced employing digital averaging techniques, i.e. using a LONG integration time with HP4145B.

** **Note**: It is desirable a modification of the MM3A-EM power supply design by Kleindiek Nanotechnik, to give also the possibility to switch on/off all electrical signals from the piezo actuators in the MMs, but, of course, avoiding any unexpected movement of the tip. In this way, an enhanced protection could be achieved against both physical damage of the DUT and low-level electrical noise.

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Appendix A. Effects of the MOS test structure

1. *Outline of the MOS dynamic regime*

Capacitance vs. voltage (*C-V* plot) and capacitance vs. time (*C-t* plot) measurements are well suited to explain [4] the frequency dependence of the parasitic MOS capacitor in the test structure, which is responsible for the effects we noticed in our tests (Sections 4.2 and 4.3).

Figure 17 shows *C-V* plots, measured on the parasitic MOS capacitor, consisting of the metal-like poly-Si pad, the underlying oxide and the n-substrate (see Section 2). The measurements were performed on a probe station, outside the SEM chamber, by a Keithley System 82, comprising *C-V* Meters Model 590 and 595. Non-ideality of the MOS capacitor is taken into account through the plot abscissa $V_{gate} - V_{FB}$, being V_{gate} the voltage applied to the poly-Si gate with respect to the substrate, and V_{FB} the measured flat-band voltage, which is the voltage shift due to the charge distribution in the actual structure. In this way, the *C-V* plot resembles that of an ideal MOS capacitor, to which the following outline will be referred.

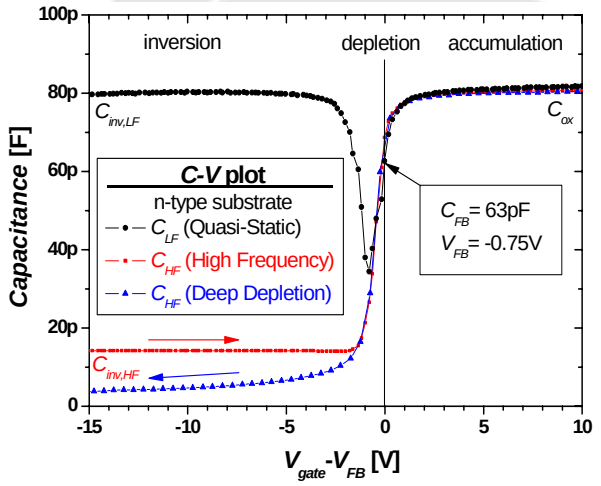

Figure 17: Capacitance-voltage measurements on MOS capacitor between pad and substrate of the test structure.

For an ideal MOS capacitor with n-type substrate, the *accumulation* state is obtained applying a positive gate voltage: the charge on the gate must be balanced by an equal negative charge in the substrate, given by an enhanced concentration of majority carriers (electrons), which diffuse from the bulk to a very thin layer at the substrate-oxide interface. Any variation of the positive gate voltage is followed almost instantaneously by the variation of the negative charge in the accumulation layer, i.e. the response time of the majority carriers is very fast (picoseconds). As a consequence, the MOS capacitance in accumulation is equal to the oxide capacitance, C_{ox}, being the opposite charge layers localized at the oxide surfaces. In accumulation, no dependence of the capacitance on the frequency is observed, as shown in Figure 17, right side.

Conversely, a negative voltage applied to the gate should be counterbalanced by a positive charge increase in the n-type substrate. Depending on the gate voltage value, firstly a reduction on the concentration of the majority carriers (electrons) is observed, i.e. a *depletion* state, when an extended space-charge region is created in the substrate at the oxide interface. In this region the mobile-carrier concentration is negligible and only the positive charge exists, due to the donor-dopant fixed ions. The capacitance of the MOS structure decreases in depletion, being the series of C_{ox} and C_d, which is the capacitance of the depletion region (central zone in Figure 17).

Further increasing the negative gate voltage, an enhanced concentration of positive minority carriers (holes) is reached in a thin layer of the substrate at the oxide interface. This is called *inversion* state, because effectively the n-substrate becomes p-type in this layer. Notice that the response time of the minority carriers is quite slow (from hundredth to tenth of seconds at ambient temperature in a dark environment), because the minority carriers can be provided only by thermal generation of electron-hole couples in the depletion region or by diffusion from the substrate bulk.

In inversion, a strong dependence of the MOS capacitance on the measurement frequency can be observed, as shown in Figure 17, left side:

a. *Low Frequency* or *Quasi-Static*. In this case, the negative gate voltage is swept very, very slowly, thus its charge can be completely counterbalanced by a charge change in the inversion layer, while the amplitude of the depletion region remains constant. Thus, the measured capacitance is $C_{inv,LF} = C_{ox}$, as in accumulation (black curve, measured by Keithley 595 with voltage step 100mV and step time 70ms);

b. *High Frequency*. Here, a small sinusoidal signal with relatively high frequency is superimposed to a slow-variable gate bias. Only the majority carriers at the border of the space-charge region can follow the fast sinusoidal signal, while the bias is completely counterbalanced by the charge change in the inversion layer. As a consequence, amplitude and capacitance, C_d, of the depletion region remain both constant, and the overall MOS capacitance, series of C_{ox} and C_d, is $C_{inv,HF} < C_{ox}$ (red curve measured by Keithley 590 at 100kHz with voltage step 100mV and step time 70ms);

c. *Deep Depletion*. The third measurement is similar to the previous (HF), but adopting a fast-variable negative gate bias. Now, the gate charge change can be balanced only by a fast and large change of the amplitude of the depletion region, because the inversion charge cannot change so rapidly. As a consequence, also the MOS capacitance, series of C_{ox} and C_d where the latter is no more constant, changes rapidly (blue curve measured at 100kHz by Keithley 590, sweeping rapidly V_{gate} from accumulation toward depletion, with voltage step 0.5V and step time 1ms).

All the previous considerations can be applied to p-type substrates, only changing the sign of the gate voltage.

2. Time-domain measurement discussion

In these tests (see Section 4.2), a huge voltage step (±30V) is applied to the MOS structure, starting from the equilibrium state (0V). This type of stimulus, but at a lower voltage (±20V), is replicated in Figure 18, where *C-t* plots are reported, measured by a Keithley 590 with time step 1ms and rate 75readings/s.

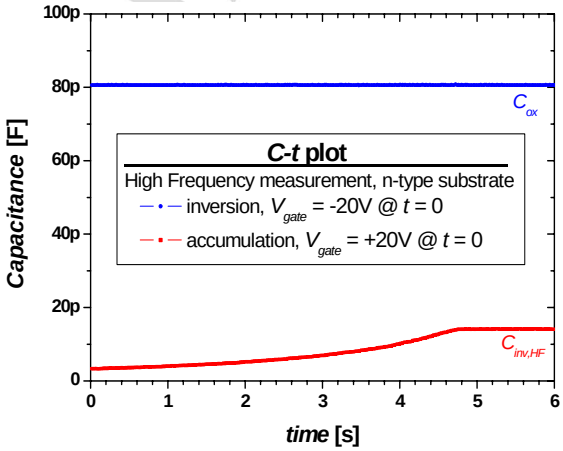

Figure 18: Capacitance-time measurements on MOS capacitor between pad and substrate of the test structure.

Driving the structure in accumulation (positive V_{gate}), the charge balance is quite instantaneous, so:

- The MOS capacitance remains at the constant value C_{ox} (blue curve in Figure 18);
- The very fast displacement-current transient is exhausted before the first current measurement by the "slow" HP4145B (*Setup #1* in Figure 13, right-bottom plot, and *Setup #2* in Figure 14, left-up plot).

Conversely, when the structure is driven in inversion (negative V_{gate}):

- The (red curve in Figure 18) shows a slow capacitance transient, corresponding to the inversion layer build-up. In fact, the Zerbst method [4], using the *C-t* plot, is currently adopted to estimate the free carrier lifetime;
- The slow transient of the corresponding displacement current is sampled by the HP4145B (*Setup #1* in Figure 13, right-up plot, and *Setup #2* in Figure 14, left-bottom plot). Of course, this transient is independent of the different Interval Time values chosen. Notice also that for both *Setups*, the displacement current is a current of holes from the substrate, having the same sign, i.e. negative entering the SMU.

3. Sweep measurement discussion

In this case (see Section 4.3), quite large consecutive voltage steps (0.7V) are applied to the MOS structure, starting from the equilibrium state (0V). At each step, a slow displacement current transient should be measured. This transient is exactly the same as above, only with reduced amplitude.

As above, when the structure is driven in deeper accumulation (*Setup #1* in Figure 15 right plot, sweep- and *Setup #2* in Figure 16 left plot, sweep+), the charge balance is quite instantaneous and no displacement current is measured by the "slow" HP4145B after any possible value of the Delay Time.

Conversely, when the structure is driven towards deeper inversion, the slow transient of the displacement current, needed to build the inversion layer, is sampled by the HP4145B (*Setup #1* in Figure 15, right plot, sweep+ and *Setup #2* in Figure 16, left plot, sweep-).

In this case, the shape of the *I-V* curve depends on the value chosen for the Delay Time: the shorter is the Delay Time, the larger is the measured current. If the Delay Time is long enough that the transient is exhausted, no current is measured. Notice that, for very short Delay Time, the next voltage step leads to a further increase of the amplitude of the next displacement current transient.

These "capacitive-like" transients are not necessarily exponential, but, for our purpose, could be simulated by a *RC* circuit, subjected to the same staircase voltage as in our sweeps. *I-V* simulations are reported in Figure 19 using different values of the Delay Time, expressed in fractions of τ, where $\tau = 1$ is the *RC* nominal time constant. As expected, the curves show a similar shape that in Figure 15 and Figure 16.

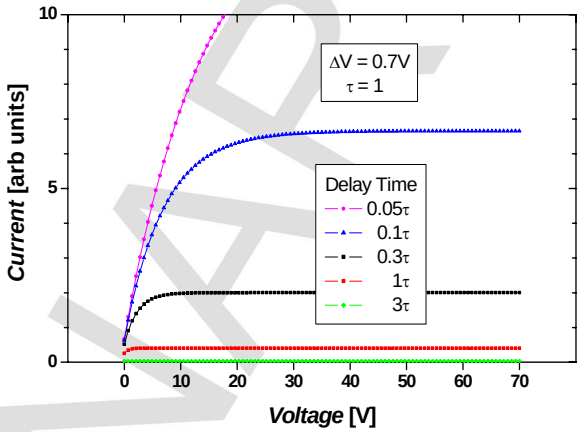

Figure 19: Current-voltage relationship of a *RC* circuit subjected to an increasing staircase voltage.

Appendix B. Additional test results

In this Appendix, the additional results for time-domain and sweep measurements, relative to the *Setups #3* and *#4*, will be presented. As anticipated in Sections 4.2 and 4.3, the results will not be discussed, because they are completely equivalent to those obtained with *Setup #2*.

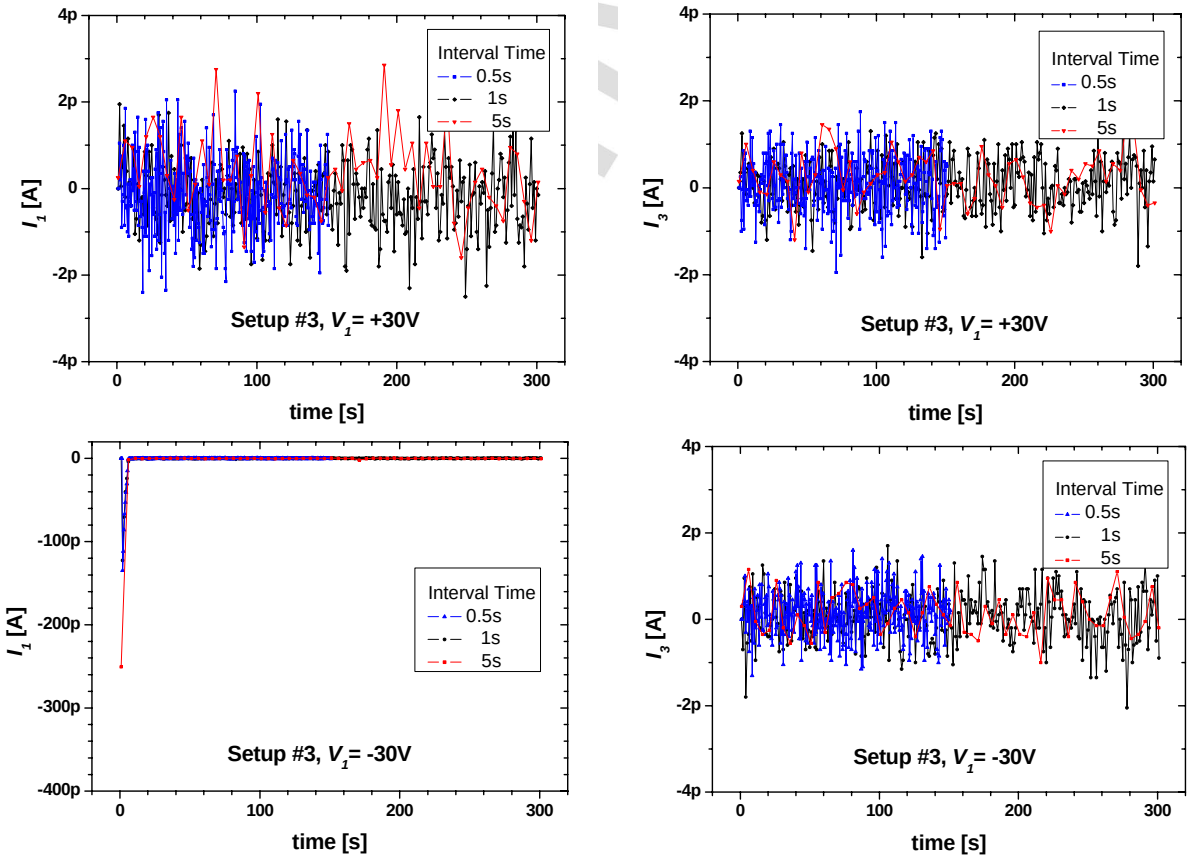

Figure 20: Time-domain current measurement results, obtained with *Setup #3* and $V_1 = \pm 30$V.

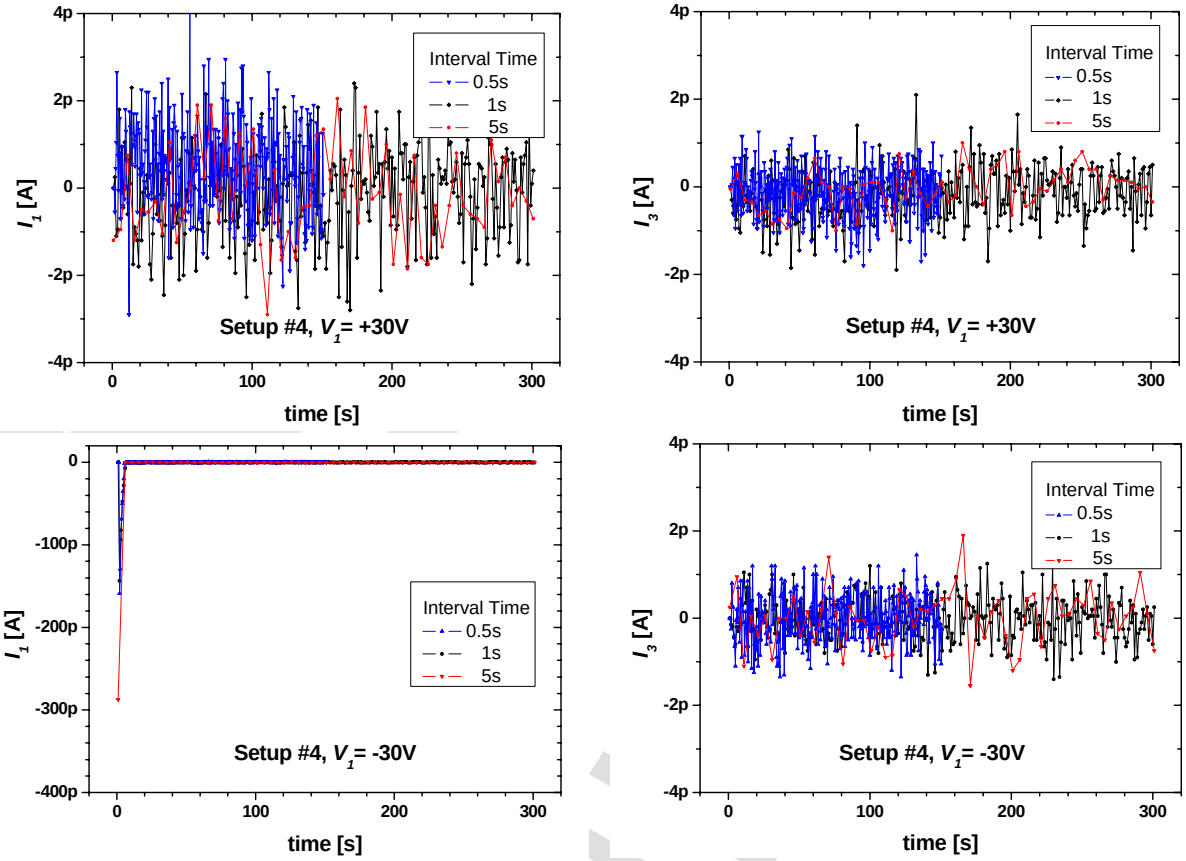

Figure 21: Time-domain current measurement results, obtained with *Setup #4* and V_1 = ±30V.

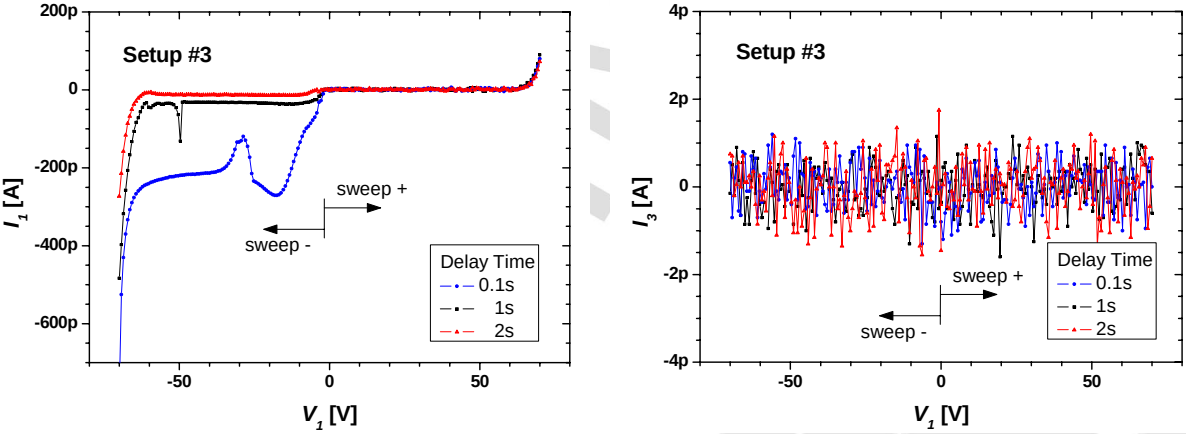

Figure 22: Sweep current measurement results, obtained with *Setup #3* and $V_{1,max}$ = ±70V.

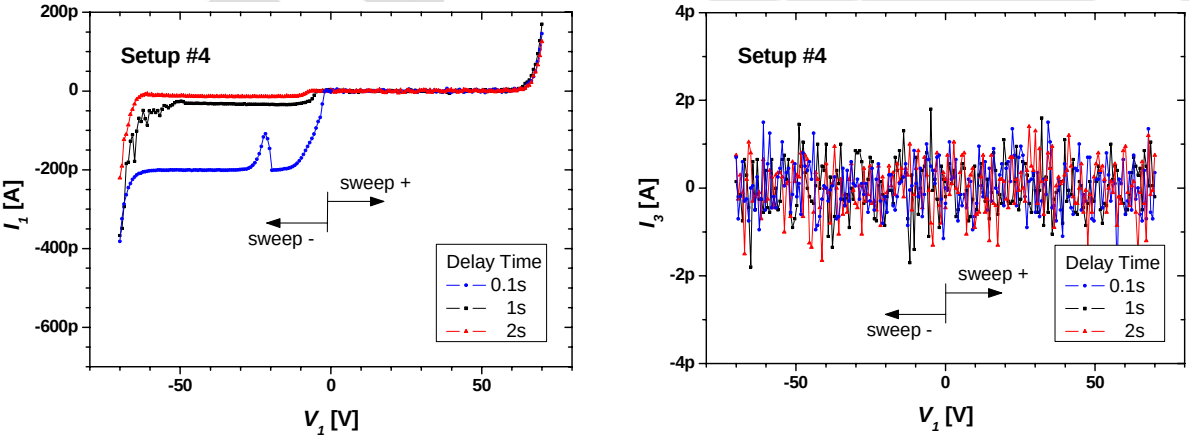

Figure 23: Sweep current measurement results, obtained with *Setup #4* and $V_{1,max}$ = ±70V.