uPI SEMI

uP8308

Li-Ion/Polymer 2/3/4-Cell Secondary Protection IC with Voltage Regulator

General Description

The uP8308 series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short circuits between cells accommodate series connection of two to four cells. In order to drive an external RTC. A voltage regulator of 3.3V or 3.0V is incorporated in uP8308. uP8308 is available in the WDFN2x2-8L package.

Applications

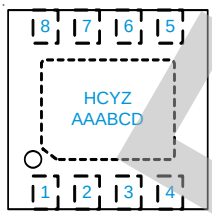
- **Lithium-Ion Rechargeable Battery Packs (for Secondary Protection)**
- **Notebook Computers**
- **Portable Instrumentation**
- **Portable Equipment**

Ordering Information

Order Number	Package	Remark
uP8308PDN8-YZ	WDFN2x2-8L	YZ is the version code. Please refer to Page 2 for detail definition.

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Marking Information

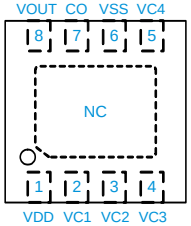


HC : Product Code
YZ : Version Code
AAABCD: Date Code

Features

- **High Accuracy Voltage Detection Circuit for Each Cell**
  - **Overcharge Detection Voltage n (n = 1 to 4)**
    4.3V to 5.0V (in 50mV steps)
    Accuracy: 20mV (+25°C)
    Accuracy: 25mV (0°C to +60°C)
  - **Overcharge Hysteresis Voltage n (n = 1 to 4)**
    -0.38V±150mV
- **Delay Time for Overcharge Detection Can Be Set by An Internal Circuit (No External Capacitor Required)**
  - **Optional Overcharge Detection Delay Time: 2s, 4s, 6s, and 8s**
  - **Optional Output Delay of Shutdown: 2s, 4s, 6s, and 8s**
- **High Withstand Voltage Devices:**
  - **Absolute Maximum Rating: 32V**
  - **Wide Operating Voltage Range: 4V to 24V**
- **Wide Operating Temperature Range: -40°C to +85°C**
- **Low Current Consumption**
  - **At 3.1V for Each Cell: 4.0uA max.(+25°C)**
  - **At 2V for Each Cell: 0.4uA max. (+25°C)**
- **CO Pull Up Voltage: 4.7V**
- **Support Test Mode to Shorten Mass Production Time**
- **Voltage Regulator:**
  - **V_{OUT}: 3.0V/3.3V (±2%)**
  - **V_{OUT} Off Voltage: 2.5V/2.8V/3.0V**
  - **Output Current: 2mA (max.)**
  - **VR Short Circuit Protection**
- **RoHS Compliant and Halogen Free**

Pin Configuration

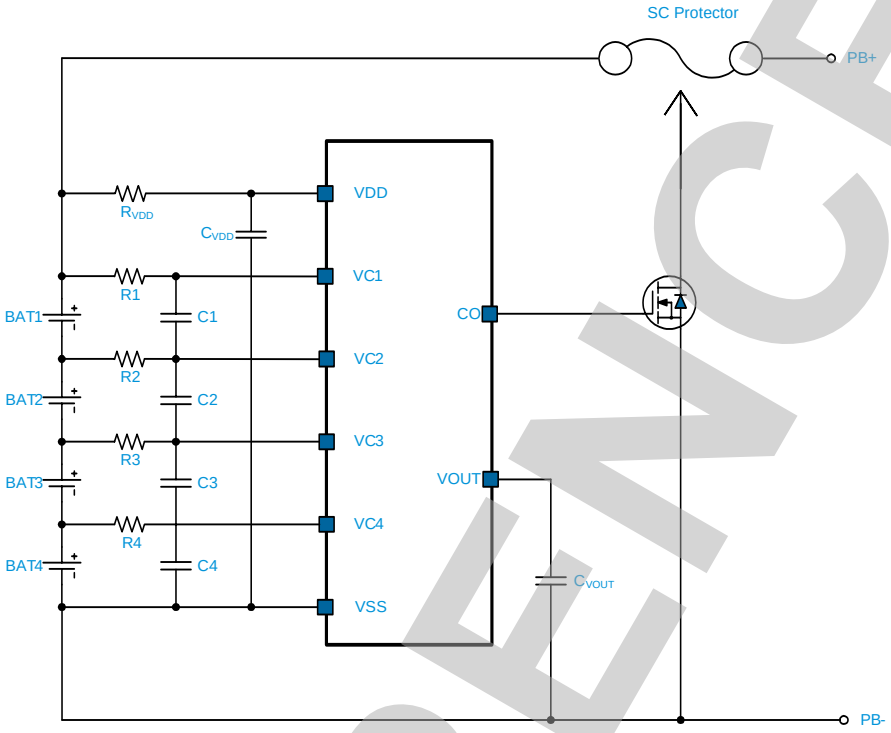


WDFN2x2-8L

Ordering Information

Order Number	Overcharge Protection Voltage (VCUn)	Shutdown Threshold Voltage (VSDn)	Overcharge Detection Delay Time (tCU)	Shutdown Delay Time (tSD)	VR Output Voltage (VOUT)	Top Marking (YZ)
uP8308PDN8-EK	4.35	2.5	6.0	6.0	3.0	HCEK
uP8308PDN8-NK	4.50	2.5	6.0	6.0	3.0	HCNK
uP8308PDN8-QK	4.55	2.5	6.0	6.0	3.0	HCQK
uP8308PDN8-TK	4.60	2.5	6.0	6.0	3.0	HCTK
uP8308PDN8-XK	4.65	2.5	6.0	6.0	3.0	HCXK
uP8308PDN8-YK	4.70	2.5	6.0	6.0	3.0	HCYK
uP8308PDN8-FK	4.75	2.5	6.0	6.0	3.0	HCFK
uP8308PDN8-HK	4.80	2.5	6.0	6.0	3.0	HCHK
uP8308PDN8-WK	4.35	3.0	6.0	6.0	3.0	HCWK
uP8308PDN8-ZK	4.50	3.0	6.0	6.0	3.0	HCZK
uP8308PDN8-1K	4.55	3.0	6.0	6.0	3.0	HC1K
uP8308PDN8-2K	4.60	3.0	6.0	6.0	3.0	HC2K
uP8308PDN8-3K	4.65	3.0	6.0	6.0	3.0	HC3K
uP8308PDN8-0K	4.70	3.0	6.0	6.0	3.0	HC0K
uP8308PDN8-JK	4.75	3.0	6.0	6.0	3.0	HCJK
uP8308PDN8-KK	4.80	3.0	6.0	6.0	3.0	HCKK
uP8308PDN8-4K	4.60	2.5	6.0	6.0	3.3	HC4K
uP8308PDN8-5K	4.50	2.5	6.0	6.0	3.3	HC5K
uP8308PDN8-6K	4.55	2.5	6.0	6.0	3.3	HC6K
uP8308PDN8-9K	4.65	2.5	6.0	6.0	3.3	HC9K
uP8308PDN8-AK	4.70	2.5	6.0	6.0	3.3	HCAK
uP8308PDN8-BK	4.75	2.5	6.0	6.0	3.3	HCBK
uP8308PDN8-CK	4.80	2.5	6.0	6.0	3.3	HCCK

Typical Application Circuit



Cautions:

1. The above connection example does not guarantee operation. Perform thorough evaluation using the actual application.

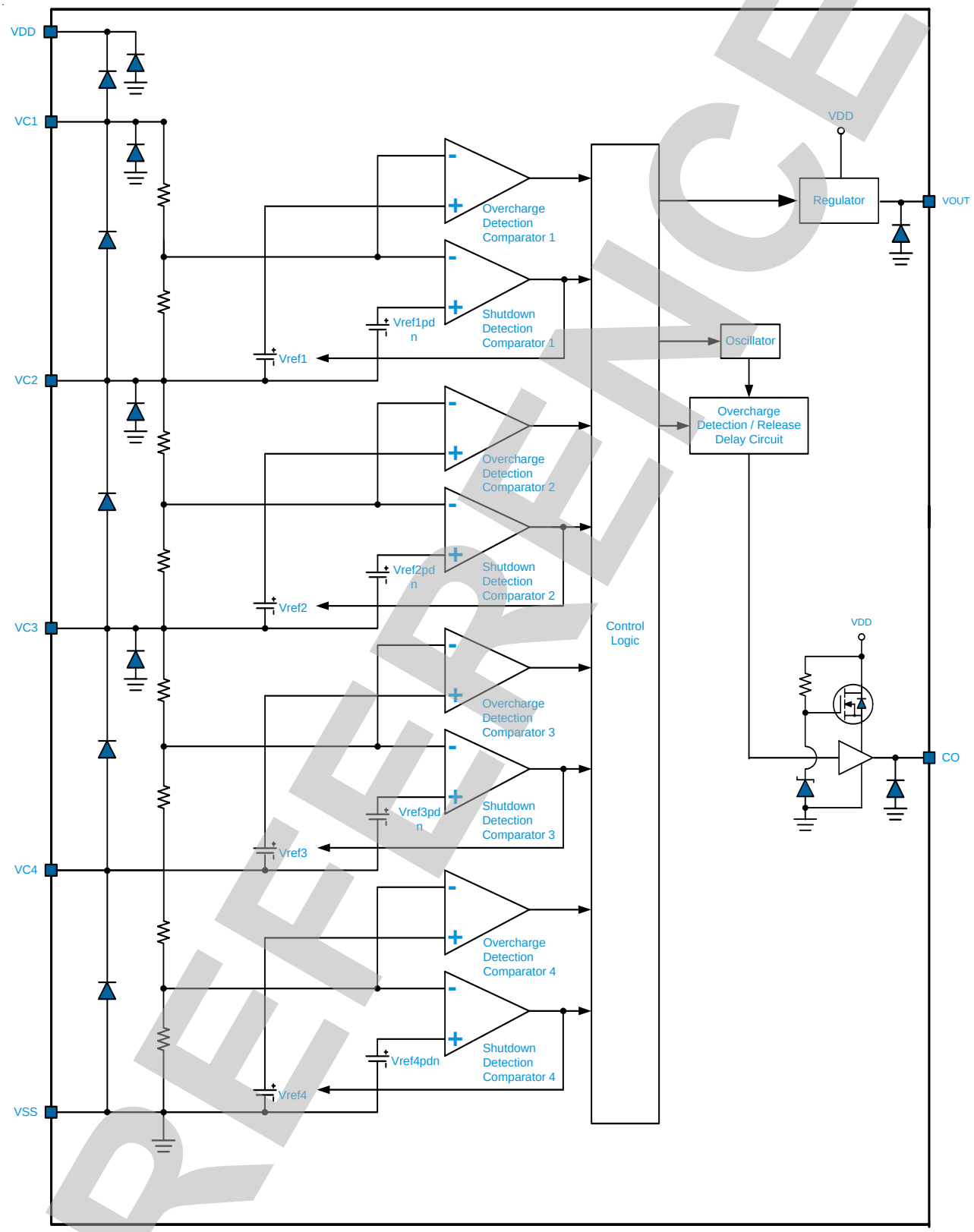
2. Cell connection: To prevent incorrect output activation, the VSS pin must be connected first. Follow the connecting sequence below:

Configuration of 4 serial cell : BAT4 -> BAT3 -> BAT2 -> BAT1

Configuration of 3 serial cell : BAT3 -> BAT2 -> BAT1

Configuration of 2 serial cell : BAT2 -> BAT1

Functional Block Diagram



Functional Pin Description

NO.	Name	Pin Function
1	VDD	PositivePower Input Pin.
2	VC1	Positive Voltage Connection Pin of Battery 1.
3	VC2	Negative Voltage Connection Pin of Battery 1. Positive Voltage Connection Pin of Battery 2.
4	VC3	Negative Voltage Connection Pin of Battery 2. Positive Voltage Connection Pin of Battery 3.
5	VC4	Negative Voltage Connection Pin of Battery 3 Positive Voltage Connection Pin of Battery 4.
6	VSS	Negative Voltage Connection Pin of Battery 4. Negative Power Input Pin.
7	CO	FET Gate Connection Pin for Charge.
8	VOUT	Voltage Regulator Output Pin.
Exposed Pad	NC	Not Conncted.

Functional Description

The uP8308 series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high accuracy voltage detection circuit and a delay circuit. Short circuits between cells accommodate series connection of two to four cells. In order to drive an external RTC. A voltage regulator of 3.3V or 3.0V is incorporated in uP8308.

Overcharge Detection

The uP8308 monitors VC1 to VC2, VC2 to VC3, VC3 to VC4, and VC4 to VSS voltage for over voltage protection. When the voltage of any cell exceeds V_{CU} during charging and lasts for equal to or longer than Overcharge Detection Delay Time (t_{CU}), CO pin turns to H. This is called overcharge protection mode. CO pin drives the connecting FET to provide charge control and a second protection.

Once the voltage of each cell is lower than $V_{CUn} + V_{HCn}$ and lasts for 16ms(Typ.) or longer, uP8308 enters normal mode.

Test Mode

Overchage Detection Delay Time (t_{CU}) can be shortened by entering the test mode. The test mode can be triggered by forcing a voltage equal to or higher than 4.0V between VDD pin and VC1 for 40ms or longer. The test mode is retained by internal latch even if the voltage of VDD pin drops to the same level as the voltage of VC1. After overcharge event occurs, uP8308 resets the latch for retaining the test mode and exits test mode under the overcharge state.

Overcharge Timer Reset

When an overcharge release noise that forces the voltage of the battery temporarily below the overcharge detection voltage (V_{CU}) is input during the overcharge detection delay time (t_{CU}) counting period. The overcharge detection delay time will be continuously counted if the period of overcharge release noise is shorter than the overcharge timer reset delay time (t_{TR}). Otherwise, counting of t_{CU} will be reset if the period of overcharge release noise is equal to t_{TR} or longer. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

Shutdown Detection

The uP8308 monitors VC1 to VC2, VC2 to VC3, VC3 to VC4, and VC4 to VSS voltage for shutdown protection. When the voltage of any cell is less than the V_{SD} during discharge and lasts for equal to or longer than shutdown delay time (t_{SD}), VOUT pin turns to L. Once the voltage of each cell exceeds V_{SDn} + 0.3V(typ.) , uP8308 enters normal mode and VOUT pin turns to H.

Functional Description

Battery Protection IC connection Examples

(1) 4-serial cell

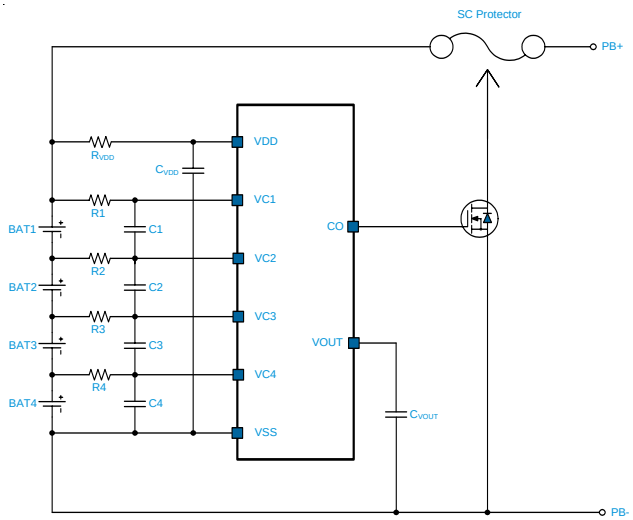


Table 1. Constants for 4-Serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.1	1	10	kΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	1000	Ω
4	C_{VOUT}	--	0.1	--	uF

Caution

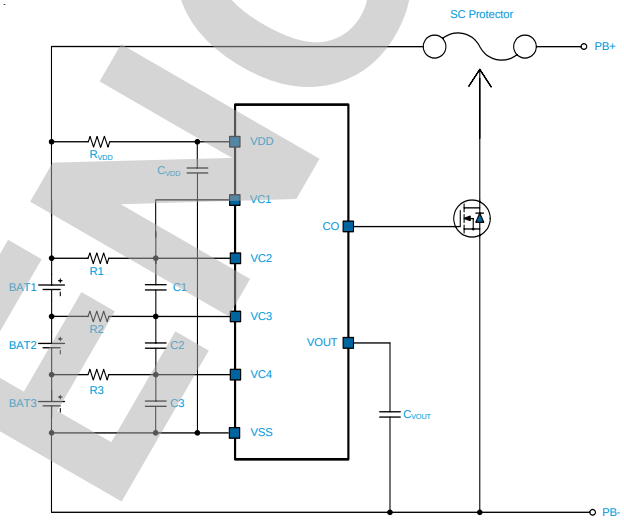
1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.
4. Set R_{VDD}, C1 to C4, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C4, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.
5. Set R1 to R4, C1 to C4, and C_{VDD} so that the condition (R1 to R4) . (C1 to C4, C_{VDD}) ≥ $1x10^{-4}$is satisfied.
6. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

   4-series cell configuration

   BAT4 → BAT3 → BAT2 → BAT1

7. Under operating at room temperature, the drop voltage limitation of VDD is as formula: RVDD*IOUT< 0.3V. The application of VOUT regulator should not exceed 0.3V drop voltage between VDD and VC1 to prevent from abnormal operation. For example: if IOUT=2mA, the RVDD should be less than 0.3V/0.002A=150Ω.

(2) 3-serial cell



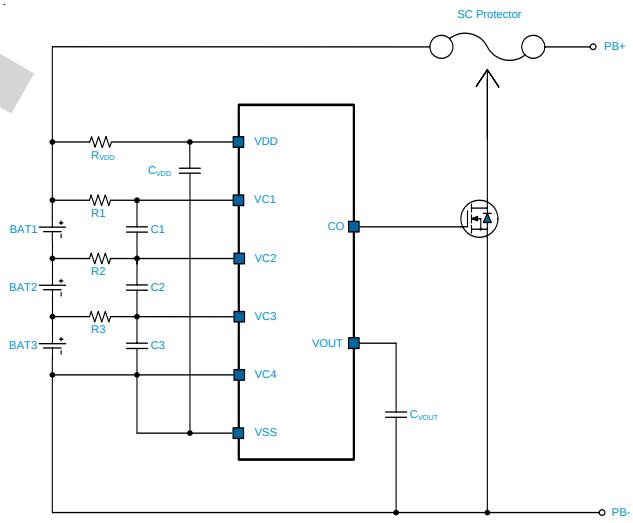


Table 2. Constants for 3-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.1	1	10	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	1000	Ω
4	C_{VOUT}	--	0.1	--	uF

Functional Description

Caution

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.

4. Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C3, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) . (C1 to C3, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

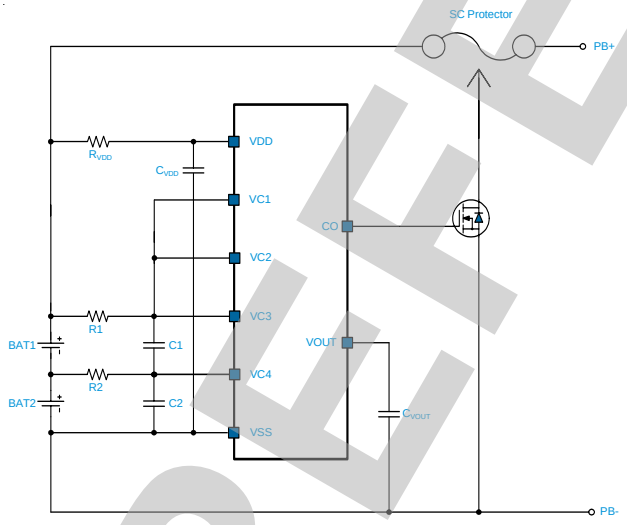
6. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

3-series cell configuration

BAT3 → BAT2 → BAT1

7. Under operating at room temperature, the drop voltage limitation of VDD is as formula: RVDD*IOUT< 0.3V. The application of VOUT regulator should not exceed 0.3V drop voltage between VDD and VC1 to prevent from abnormal operation. For example: if IOUT=2mA, the RVDD should be less than 0.3V/0.002A=150Ω.

(3) 2-serial cell



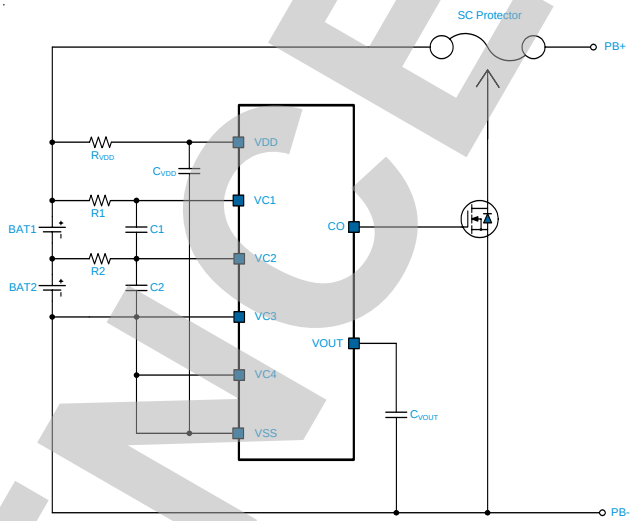


Table 3. Constants for 2-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R2	0.1	1	10	kΩ
2	C1 to C2, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	500*	Ω
4	C_{VOUT}	--	0.1	--	uF

*For 2-serial application, if choosing Rvdd over 500Ω, VOUT voltage will not reach 3.3V and 3V in operation, depends on voltage drop on VDD pin.

Caution

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R2 and to C1 to C2 and C_{VDD}.

4. Set R_{VDD}, C1 to C2, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C2, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R2, C1 to C2, and C_{VDD} so that the condition (R1 to R2) . (C1 to C2, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

6. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

2-series cell configuration

BAT2 → BAT1

Functional Description

7. Under operating at room temperature, the drop voltage limitation of VDD is as formula: RVDD*IOUT< 0.3V. The application of VOUT regulator should not exceed 0.3V drop voltage between VDD and VC1 to prevent from abnormal operation. For example: if IOUT=2mA, the RVDD should be less than 0.3V/0.002A=150Ω.

Precautions

Do not connect batteries charged with V_{CU} + V_{HC} or more. If the connected batteries include a battery charged with V_{CU} + V_{HC} or more, *H* may be output at CO after all pins are connected.

In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.

Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figures in *Battery Protection IC Connection Example.*

The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.

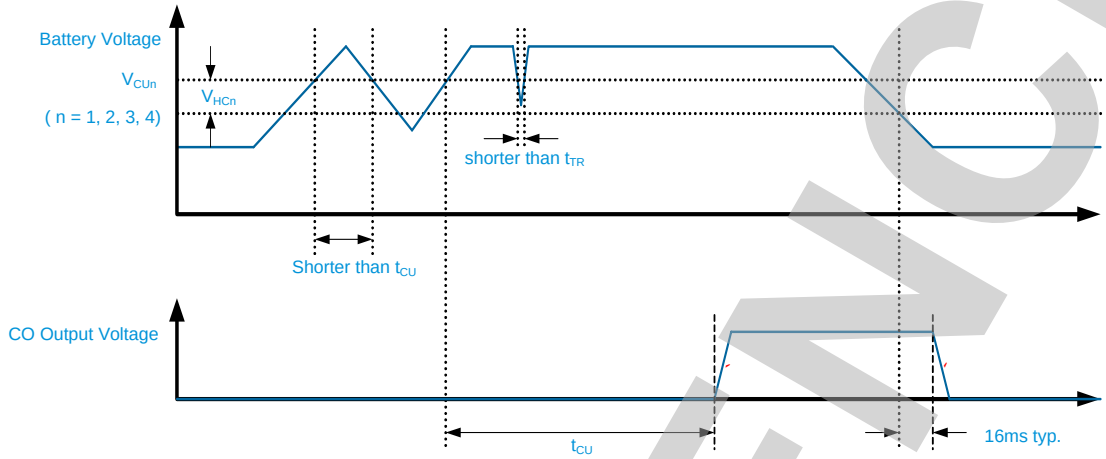
Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.

uPI claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

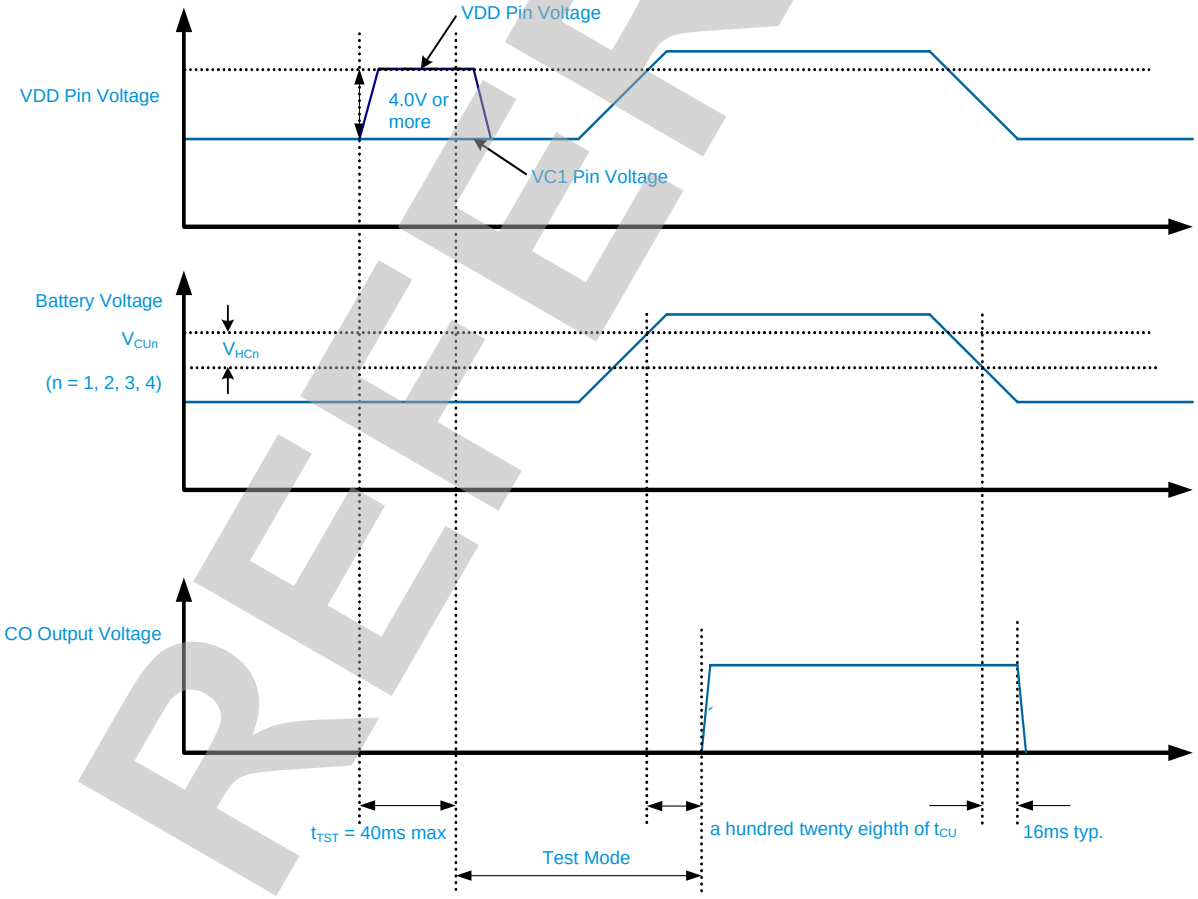
Functional Description

Timing Chart

Overcharge Protection

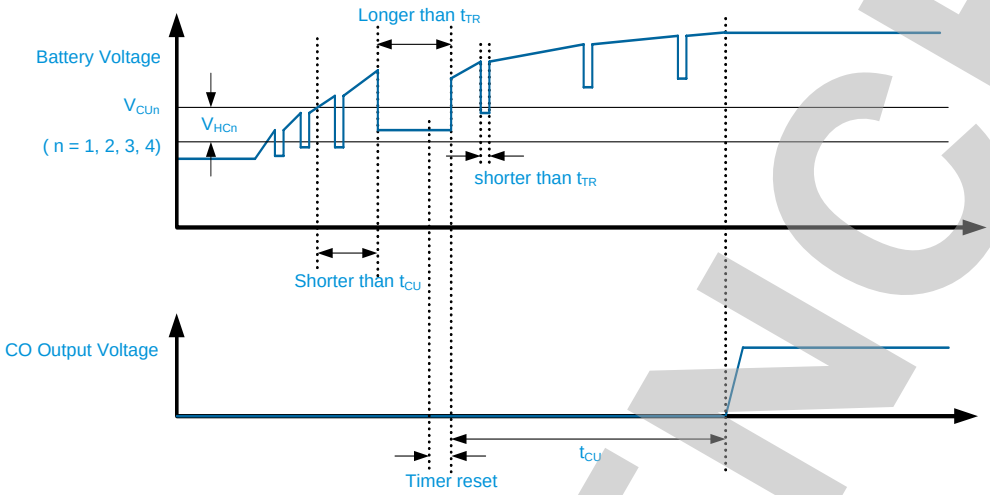


Test Mode

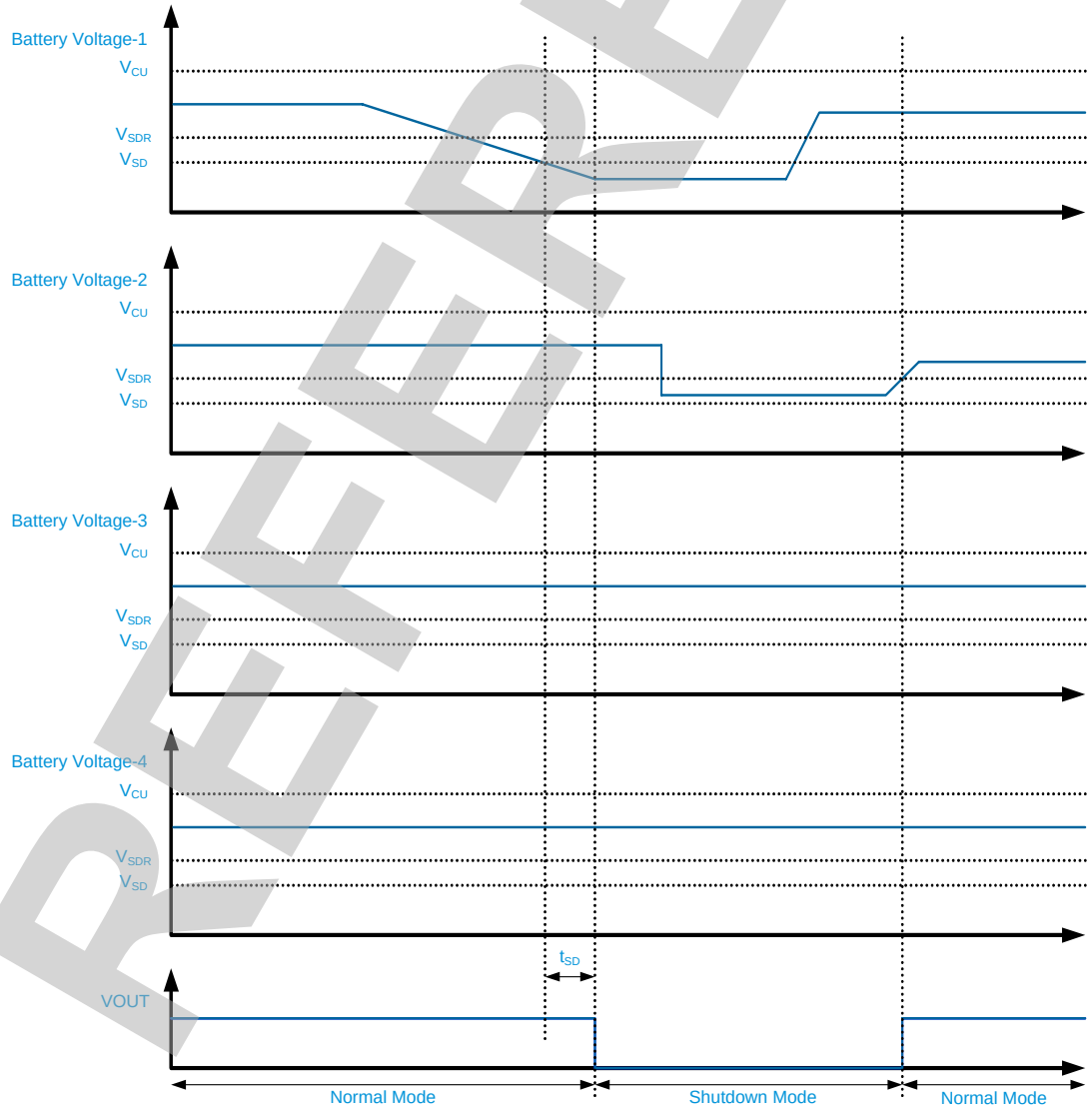


Functional Description

Overcharge Timer Reset



Voltage Regulator Operation



Absolute Maximum Rating

(Note 1)

Supply Voltage Range between VDD and VSS ---------- VSS-0.3V to VSS+32V
Pulse < 1ms, < 5mA, > VSS-1.5V
Supply Input Voltage Range between VDD and VC1 ---------- VC1-0.3V to VC1+6.5V
Supply Input Voltage Range, VCn,n=1,2,3 ---------- VC(n+1)-0.3V to VC(n+1)+6.5V
Supply Input Voltage Range, VC4 ---------- -0.3V to +6.5V
Pulse < 1ms, < 5mA, > VSS-1.5V
CO Output Pin Voltage Range, CO ---------- -0.3V to +5.7V
Pulse < 1ms, < 5mA, > VSS-1.5V
VOUT Output Pin Voltage Range, VOUT---------- -0.3V to +6.5V
Pulse < 1ms, < 5mA, > VSS-1.5V
Storage Temperature Range ---------- -45°C to +125°C
Junction Temperature ---------- 125°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
WDFN2x2 - 8L θ_{JA} ---------- 155°C/W
WDFN2x2 - 8L θ_{JC} ---------- 20°C/W
Power Dissipation, P_D @ T_A = 25°C
WDFN2x2 - 8L P_D ---------- 0.65*1W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range (Note 4) ---------- -40°C to +100°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Voltage, VDD, VSS ---------- +4V to +24V
Input Voltage, VC1-VC2, VC2-VC3, VC3-VC4, VC4-VSS ---------- 0V to +5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Circuit
Detection Voltage							
Overcharge Detection Voltage n (n = 1, 2, 3, 4)	V_{CUn}		V_{CUn}-0.020	V_{CUn}	V_{CUn}+0.020	V	1
		T_A = 0°C to + 60°C(*1)	V_{CUn}-0.025	V_{CUn}	V_{CUn}+0.025		
uP8308PDN8-EK, uP8308PDN8-WK	V_{CUn}	T_A = 25°C	4.33	4.35	4.37	V	
uP8308PDN8-NK, uP8308PDN8-ZK, uP8308PDN8-5K			4.48	4.5	4.52		
uP8308PDN8-QK, uP8308PDN8-1K, uP8308PDN8-6K			4.53	4.55	4.57		
uP8308PDN8-TK, uP8308PDN8-2K, uP8308PDN8-4K			4.58	4.6	4.62		
uP8308PDN8-XK, uP8308PDN8-3K, uP8308PDN8-9K			4.63	4.65	4.67		
uP8308PDN8-YK, uP8308PDN8-0K, uP8308PDN8-AK			4.68	4.70	4.72		
uP8308PDN8-FK, uP8308PDN8-JK, uP8308PDN8-BK			4.73	4.75	4.77		
uP8308PDN8-HK, uP8308PDN8-KK, uP8308PDN8-CK			4.78	4.80	4.82		
uP8308PDN8-EK, uP8308PDN8-WK	V_{CUn}	T_A = 0°C to + 60°C(*1)	4.325	4.35	4.375	V	
uP8308PDN8-NK, uP8308PDN8-ZK, uP8308PDN8-5K			4.475	4.5	4.525		
uP8308PDN8-QK, uP8308PDN8-1K, uP8308PDN8-6K			4.525	4.55	4.575		
uP8308PDN8-TK, uP8308PDN8-2K, uP8308PDN8-4K			4.575	4.6	4.625		
uP8308PDN8-XK, uP8308PDN8-3K, uP8308PDN8-9K			4.625	4.65	4.675		
uP8308PDN8-YK, uP8308PDN8-0K, uP8308PDN8-AK			4.675	4.70	4.725		
uP8308PDN8-FK, uP8308PDN8-JK, uP8308PDN8-BK			4.725	4.75	4.775		
uP8308PDN8-HK, uP8308PDN8-KK, uP8308PDN8-CK			4.775	4.80	4.825		
Overcharge Hysteresis Voltage n (n = 1, 2, 3, 4)	V_{HCn}		-0.53	-0.38	-0.23	V	1
Shutdown Threshold Voltage n (n = 1, 2, 3, 4)	V_{SDn}	Detect falling edge of supply voltage	V_{SDn}-0.05	V_{SDn}	V_{SDn}+0.05	V	9
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{SDn}	T_A = 25°C	2.45	2.5	2.55	V	
uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK			2.95	3	3.05		

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Circuit
Detection Voltage (cont)							
Shutdown Release Voltage n (n = 1, 2, 3, 4)	V_{SDRn}	Detect rising edge of supply voltage	V_{SDRn}-0.1	V_{SDn}+0.3	V_{SDRn}+0.1	V	9
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{SDRn}	T_A = 25°C	2.7	2.8	2.9	V	
uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK			3.2	3.3	3.4		
Test Mode Transition Threshold	V_{TST}		4	--	6.5	V	2
Input Voltage							
Supply Voltage between VDD and VSS	V_{DSOP}		4	--	24	V	--
Input Current							
Current Consumption During Operation	I_{OPE}	V1=V2=V3=V4=3.1V	--	2	4	uA	3
	I_{OPE1}	V1=V2=V3=V4=4.15V	--	3	5	uA	3
Current Consumption During Overdischarge	I_{PDN}	V1=V2=V3=V4=2.0V	--	--	0.4	uA	3
VC1 Pin Current	I_{VC1}	V1=V2=V3=V4=3.1V	--	--	0.88	uA	4
VC2 Pin Current	I_{VC2}	V1=V2=V3=V4=3.1V	-0.3	0	0.3	uA	4
VC3 Pin Current	I_{VC3}	V1=V2=V3=V4=3.1V	-0.3	0	0.3	uA	4
VC4 Pin Current	I_{VC4}	V1=V2=V3=V4=3.1V	-0.3	0	0.3	uA	4
Delay Time							
Overcharge Detection Delay Time	t_{CU}	VCn=3.1V, VC1=3.1V→V_{CU}+0.1V (n=2,3,4)	t_{CU}x0.8	t_{CU}	t_{CU}x1.2	s	2
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K ,uP8308PDN8-5K, uP8308PDN8-6K ,uP8308PDN8-9K, uP8308PDN8-AK ,uP8308PDN8-BK, uP8308PDN8-CK	t_{CU}	T_A=25°C	4.8	6	7.2	s	
Overcharge Release Delay Time	t_{CL}	VCn=3.1V, VC1=V_{CU}+0.1V→3.1V (n=2,3,4)	12.8	16	19.2	ms	2

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Circuit
Delay Time (cont)							
Shutdown Delay Time	t_{SD}	VCn=3.2V, VC1=3.2V→V_{SD1}-0.2V (n=2,3,4)	t_{SD}x0.8	t_{SD}	t_{SD}x1.2	s	10
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	t_{SD}	T_A=25°C	4.8	6	7.2	s	
Overcharge Timer Reset Delay Time	t_{TR}		--	--	0.48	ms	2
Overcharge Detection Delay Time in Delay Shorten Mode	t_{CUT}		t_{CU}x1/128 X0.8	t_{CU}x1/128	t_{CU}x1/128 X1.2	s	2
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	t_{CUT}	T_A=25°C	0.038	0.047	0.056	s	
Transition Time to Test Mode	t_{TST}		--	--	40	ms	--
CO Output Voltage							
CO Pin Drive Voltage	V_{OH1}	VC1-VC2 or VC2-VC3 or VC3-VC4 or VC4-VSS =V_{CU}, I_O=0mA	4	4.7	5.4	V	5
	V_{OH2}	VC1-VC2 or VC2-VC3 or VC3-VC4 or VC4-VSS=V_{CU}, I_O=-1mA	V_{OH1}-0.5	V_{OH1}-0.1	--		6
	V_{OL}	VC1=VC2=VC3=VC4=4.15V, I_O=50uA	--	0.1	0.5		7
Voltage Regulator							
VR Output Voltage	V_{OUT}	VDD=5.1 to 25V, I_{OUT}=10uA	2.94	3.0	3.06	V	8
			3.234	3.3	3.366		
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK	V_{OUT}	T_A=25°C	2.94	3.0	3.06	V	

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Circuit
Voltage Regulator(cont.)							
uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{OUT}	T_A=25°C	3.234	3.3	3.366	V	
VR Output Current	I_{OUT}	VDD=5.1 to 25V	--	--	2	mA	8

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Electrical Characteristics

(T_A=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Detection Voltage						
Overcharge Detection Voltage n (n = 1, 2, 3, 4)	V_{CUn}		V_{CUn}-0.041	V_{CUn}	V_{CUn}+0.033	V
uP8308PDN8-EK, uP8308PDN8-WK	V_{CUn}	T_A = -40°C to 85°C	4.309	4.35	4.383	V
uP8308PDN8-NK, uP8308PDN8-ZK, uP8308PDN8-5K			4.459	4.5	4.533	
uP8308PDN8-QK, uP8308PDN8-1K, uP8308PDN8-6K			4.509	4.55	4.583	
uP8308PDN8-TK, uP8308PDN8-2K, uP8308PDN8-4K			4.559	4.6	4.633	
uP8308PDN8-XK, uP8308PDN8-3K, uP8308PDN8-9K			4.609	4.65	4.683	
uP8308PDN8-YK, uP8308PDN8-0K, uP8308PDN8-AK			4.659	4.70	4.733	
uP8308PDN8-FK, uP8308PDN8-JK, uP8308PDN8-BK			4.709	4.75	4.783	
uP8308PDN8-HK, uP8308PDN8-KK, uP8308PDN8-CK			4.759	4.80	4.833	
Overcharge Hysteresis Voltage n (n = 1, 2, 3, 4)	VHCn		-0.57	-0.38	-0.19	V
Shutdown Threshold Voltage n (n = 1, 2, 3, 4)	V_{SDn}	Detect falling edge of supply voltage	V_{SDn}-0.093	V_{SDn}	V_{SDn}+0.061	V
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{SDn}	T_A = -40°C to 85°C	2.407	2.5	2.561	V
uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK			2.907	3	3.061	
Shutdown Release Voltage n (n = 1, 2, 3, 4)	V_{SDRn}	Detect rising edge of supply voltage	V_{SDRn}-0.10	V_{SDn}+0.3	V_{SDRn}+0.10	V
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{SDRn}	T_A = -40°C to 85°C	2.656	2.8	2.933	V
uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK			3.156	3.3	3.433	
Test Mode Transition Threshold	V_{TST}		4	--	6.5	V

Electrical Characteristics

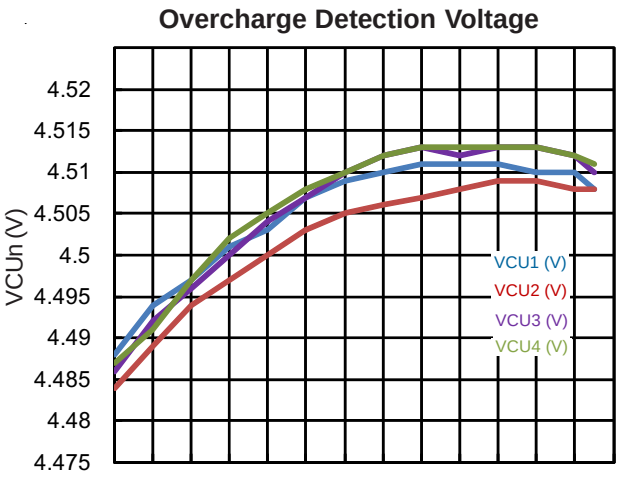
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage						
Supply Voltage between VDD and VSS	V_{DSOP}		4	--	24	V
Input Current						
Current Consumption During Operation	I_{OPE}	V1=V2=V3=V4=3.1V	--	2	5.5	uA
	I_{OPE1}	V1=V2=V3=V4=4.15V	--	3	8.25	uA
Current Consumption During Overdischarge	I_{PDN}	V1=V2=V3=V4=2.0V	--	--	0.47	uA
VC1 Pin Current	I_{VC1}	V1=V2=V3=V4=3.1V	--	--	1.42	uA
VC2 Pin Current	I_{VC2}	V1=V2=V3=V4=3.1V	-0.42	0	0.42	uA
VC3 Pin Current	I_{VC3}	V1=V2=V3=V4=3.1V	-0.42	0	0.42	uA
VC4 Pin Current	I_{VC4}	V1=V2=V3=V4=3.1V	-0.42	0	0.42	uA
Delay Time						
Overcharge Detection Delay Time	t_{CU}	VCn=3.1V, VC1=3.1V→V_{CU}+0.1V (n=2,3,4)	t_{CU}x0.55	t_{CU}	t_{CU}x1.5	s
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	t_{CU}	T_A=-40°C to 85°C	3.3	6	9	s
Overcharge Release Delay Time	t_{CL}	VCn=3.1V, VC1=V_{CU}+0.1V→3.1V (n=2,3,4)	9	16	23.6	ms
Shutdown Delay Time	t_{SD}	VCn=3.2V, VC1=3.2V→V_{SD1}-0.2V (n=2,3,4)	t_{SD}x0.55	t_{SD}	t_{SD}x1.5	s
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	t_{SD}	T_A=-40°C to 85°C	3.3	6	9	s

Electrical Characteristics

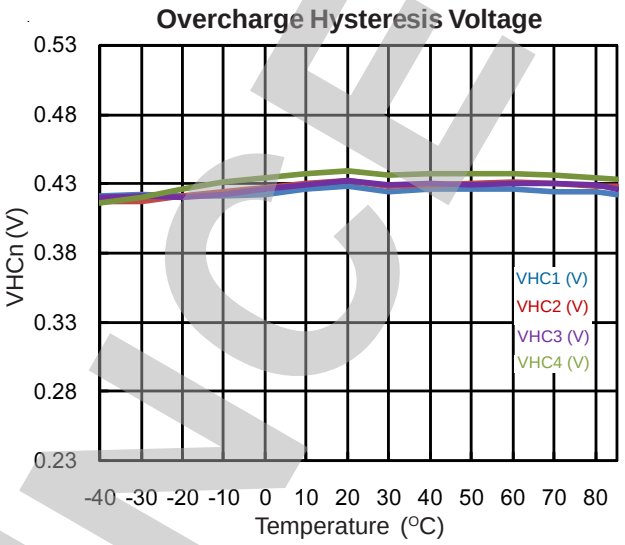
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Delay Time (cont.)						
Overcharge Timer Reset Delay Time	t_{TR}		--	--	0.48	ms
Overcharge Detection Delay Time in Delay Shorten Mode	t_{CUT}		t_{CU}x1/128 X0.8	t_{CU}x1/128	t_{CU}x1/128 X1.5	s
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK, uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	t_{CUT}	T_A=-40°C to 85°C	0.026	0.047	0.070	s
Transition Time to Test Mode	t_{TST}		--	--	80	ms
CO Output Voltage						
CO Pin Drive Voltage	V_{OH1}	VC1-VC2 or VC2-VC3 or VC3-VC4 or VC4-VSS =V_{CU}, I_O=0mA	3.94	4.7	5.44	V
	V_{OH2}	VC1-VC2 or VC2-VC3 or VC3-VC4 or VC4-VSS=V_{CU}, I_O=-1mA	V_{OH1}-0.5	V_{OH1}-0.1	--	
	V_{OL}	VC1=VC2=VC3=VC4=4.15V, I_O=50uA	--	0.1	0.512	
Voltage Regulator						
VR Output Voltage	V_{OUT}	VDD=5.1 to 25V, I_{OUT}=10uA	2.89	3.0	3.10	V
			3.19	3.3	3.4	
uP8308PDN8-EK, uP8308PDN8-NK, uP8308PDN8-QK, uP8308PDN8-TK, uP8308PDN8-XK, uP8308PDN8-YK, uP8308PDN8-FK, uP8308PDN8-HK, uP8308PDN8-WK, uP8308PDN8-ZK, uP8308PDN8-1K, uP8308PDN8-2K, uP8308PDN8-3K, uP8308PDN8-0K, uP8308PDN8-JK, uP8308PDN8-KK,	V_{OUT}	T_A= -40°C to 85°C	2.89	3.0	3.10	V
uP8308PDN8-4K, uP8308PDN8-5K, uP8308PDN8-6K, uP8308PDN8-9K, uP8308PDN8-AK, uP8308PDN8-BK, uP8308PDN8-CK	V_{OUT}	T_A= -40°C to 85°C	3.19	3.3	3.4	V
VR Output Current	I_{OUT}	VDD=5.1 to 25V	--	--	2	mA

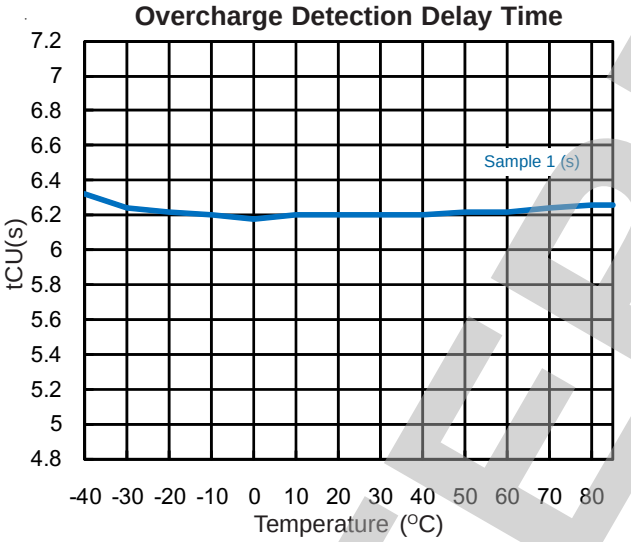
*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Typical Operation Characteristics

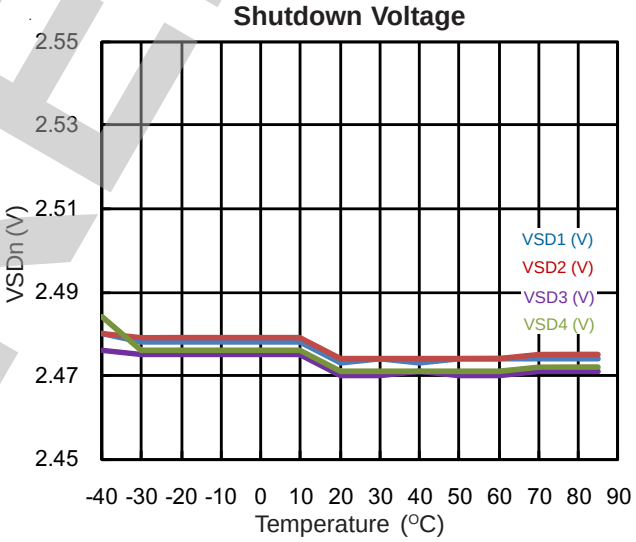


The curve of the product with VCUn=4.5V

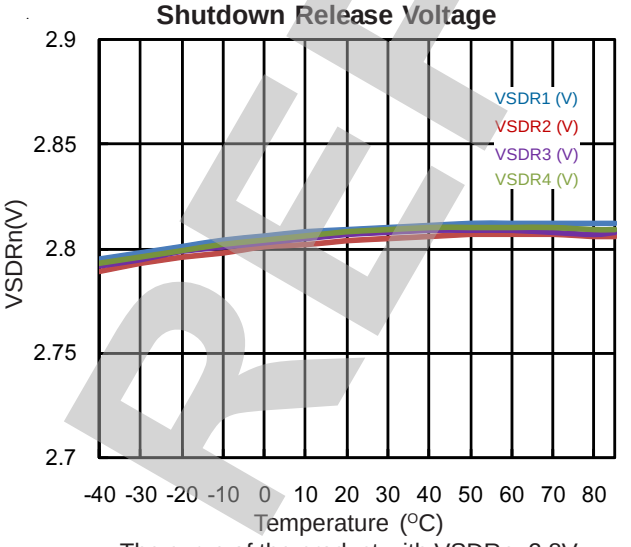




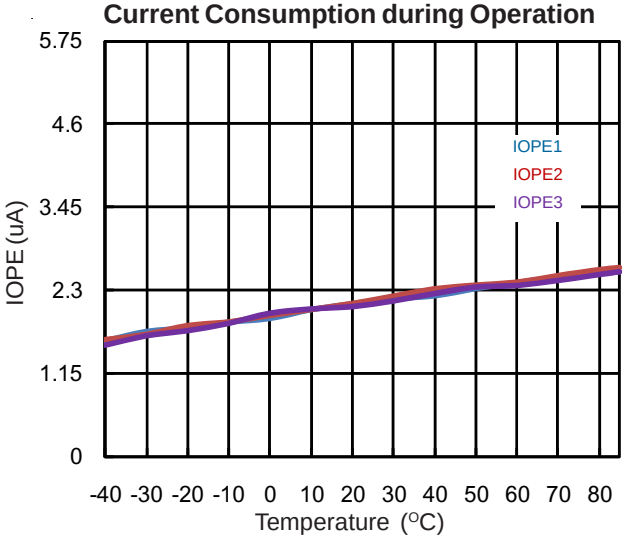
The curve of the product with t_{CU}=6s



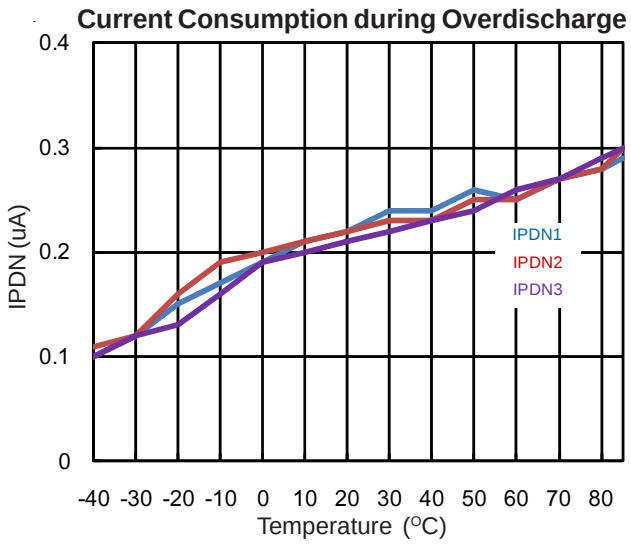
The curve of the product with VSDn=2.5V

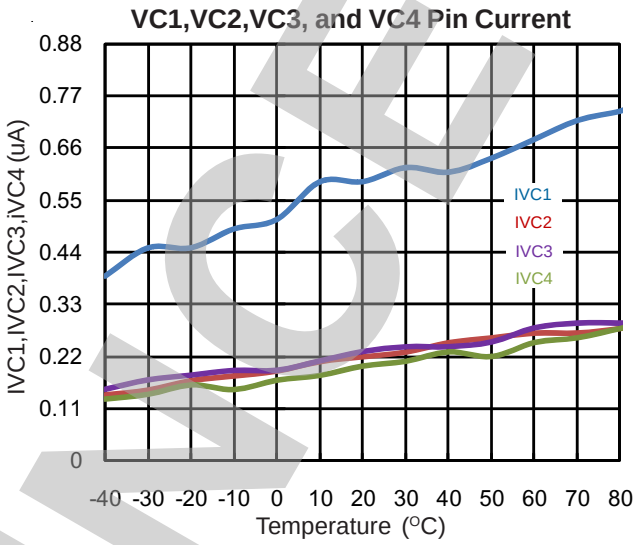


The curve of the product with VSDRn=2.8V



Typical Operation Characteristics





Test Circuit

1. Overcharge Detection Voltage and Overcharge Hysteresis Voltage

(Test Circuit 1)

Set V1, V2, V3, and V4 to 3.5V. Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO turns to H after the voltage of V1 gradually increases. The overcharge hysteresis voltage (V_{HC1}) is the difference between V1 and V_{CU1} when CO turns to L after the voltage of V1 gradually decreases. Overcharge detection voltage V_{CUn} (n = 2, 3, 4) and overcharge hysteresis V_{HCn} (n = 2, 3, 4) can be determined in the same way as when n = 1.

2. Overcharge Detection Delay Time and Overcharge Release Delay Time

(Test Circuit 1)

Set V1, V2, V3, and V4 to 3.5V, and within 10us, V1 is increased up to 5.0V. The overcharge detection delay time (t_{CU}) is the duration from when V1 reaches 5.0V until when CO turns to H. After that, V1 is lowered down to 3.5V within 10 us. The overcharge release delay time (t_{CL}) is the duration from when V1 reaches 3.5V until when CO turns to L.

3. Overcharge Timer Reset Delay Time (t_{TR})

(Test Circuit 1)

Set V1, V2, V3, and V4 to 3.5V. V1 is driven up to 5.0V and this is defined as the first rise. Then V1 is lowered down to 3.5V again and instantly resumes to 5.0V. This rise is defined as the second rise. When the duration between the V1 fall and the second rise is short enough, CO turns to H after the t_{CU} following the first rise; when the duration between the V1 fall and the second rise is long enough, CO turns to H after the t_{CU} following the second rise. The overcharge timer reset delay time (t_{TR}) is the duration from V1 fall to the second rise. For detailed illustration, please refer to the Timing Chart of Overcharge Timer Reset on page 10.

4. Transition Time to Test Mode

(Test Circuit 2)

Setting V1, V2, V3 and V4 to 3.5V and V5 to 0V. Bring V5 up to 4V(max) and halt for a quick pause and then drop back to 0V again. The transition time t_{TST} (40ms max.) is defined as the duration between the rise and fall of V5. When the duration between the rise and fall of V5 is shorter than t_{TST}. it will result in overcharge detection protection after going through t_{CU}; however, when the overcharge detection time is made longer than t_{TST}, overcharge detection protection will occur within duration much shorter than t_{CU} which is typically one sixty-fourth of t_{CU}. For more detailed illustration, please refer to the Timing Chart of Test Mode on page 9.

5. Operation Current Consumption and Overdischarge Current Consumption

(Test Circuit 3)

The current consumption during operation (I_{OPE}) is the total of the currents that flow in the VDD pin and VC1 pin when V1, V2, V3, and V4 are set to 3.1V. The current consumption during over discharge (I_{PDN}) is the total of the currents that flow in the VDD pin and VC1 pin when V1, V2, V3, and V4 are set to 2.0V.

6. VC1, VC2, VC3, VC4 Current Consumption

(Test Circuit 4)

When V1, V2, V3, and V4 are set to 3.1V, the current of VC1 pin is I_{VC1}; the current of VC2 pin is I_{VC2}; the current of the VC3 pin is I_{VC3}; and the current of the VC4 pin current is I_{VC4}.

7. CO Function Test

(Test Circuit 5, Test Circuit 6, Test Circuit 7)

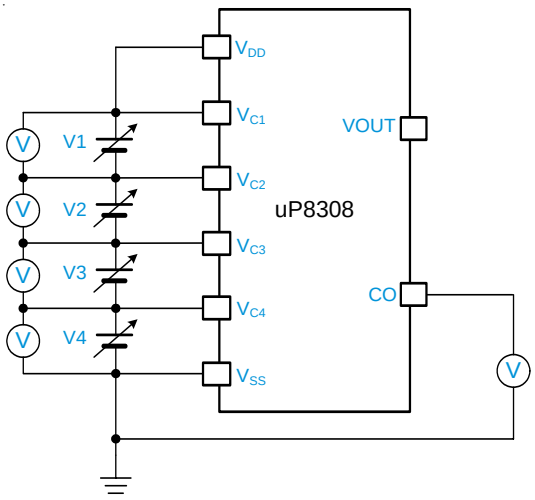
Setting V1 or V2 or V3 or V4=V_{CU}, the voltage of the rest of the cells is 3.5V. After t_{CU} the CO will become High, the voltage of V_{OH1} is 4.7V (Typ). When CO is High, add 1mA load between CO and GND. The voltage of V_{OH2} is V_{OH1}-0.1V (Typ). Setting V1=V2=V3=V4=4.15V, add 50uA current source between CO and GND. The voltage of V_{OL} is 0.1V (Typ).

8. Voltage Regulation

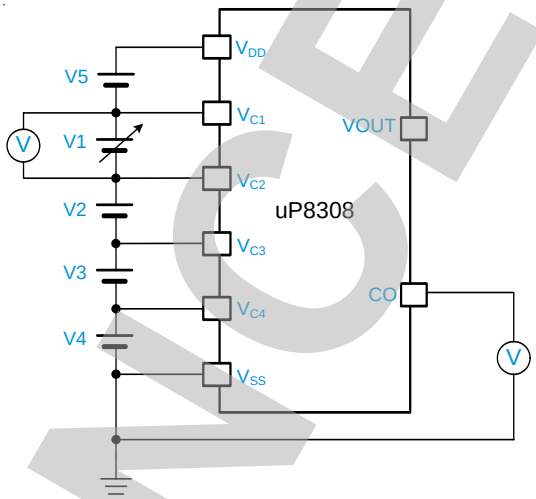
(Test Circuit 8, Test Circuit 9, Test Circuit 10)

When V1+V2+V3+V4 voltage is 5.1V to 25V and each cell voltage is above V_{SD}+0.3V(Typ.), the voltage of VOUT is 3V or 3.3V. The maximum capability of VOUT is 2mA.

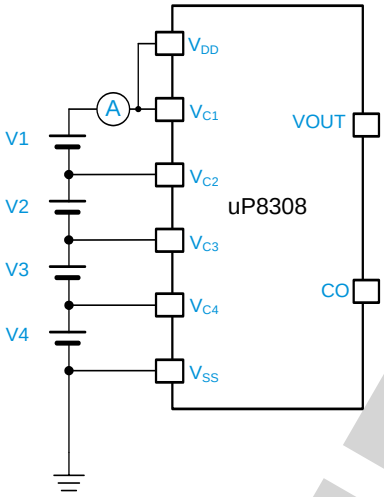
When V1 and V2 and V3 and V4 are supplied, any cell voltage drops below V_{SD}, after t_{SD} the VOUT will be turned off. At shutdown mode, when all cell voltage reaches V_{SD}+0.3V (Typ), the Voltage Regulation will be turned on immediately.



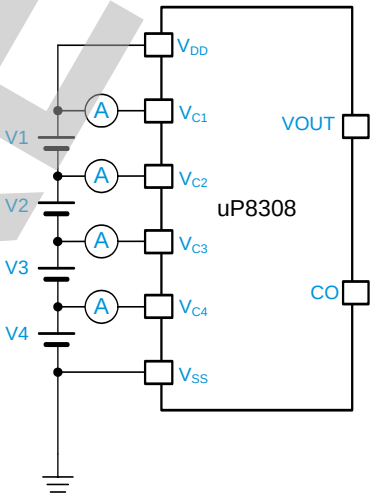
Test Circuit 1



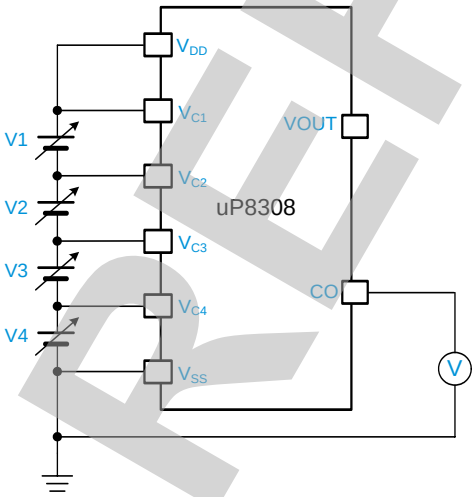
Test Circuit 2



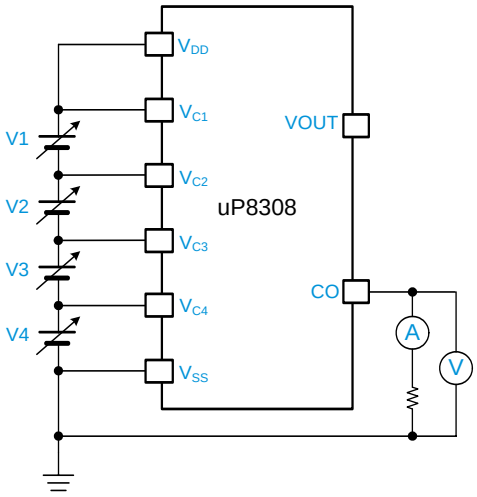
Test Circuit 3



Test Circuit 4

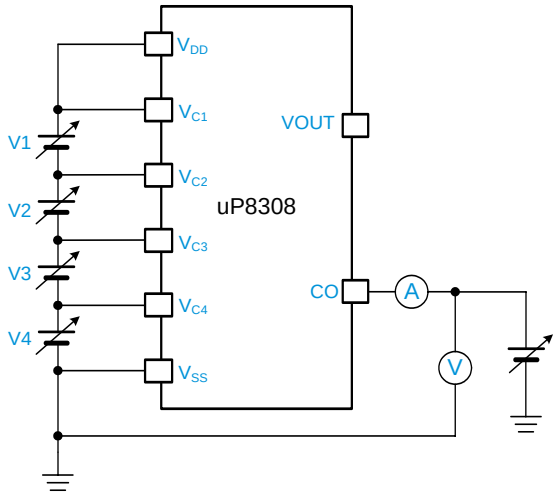


Test Circuit 5

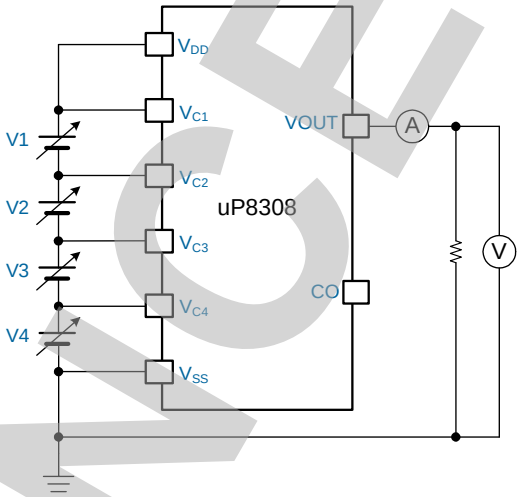


Test Circuit 6

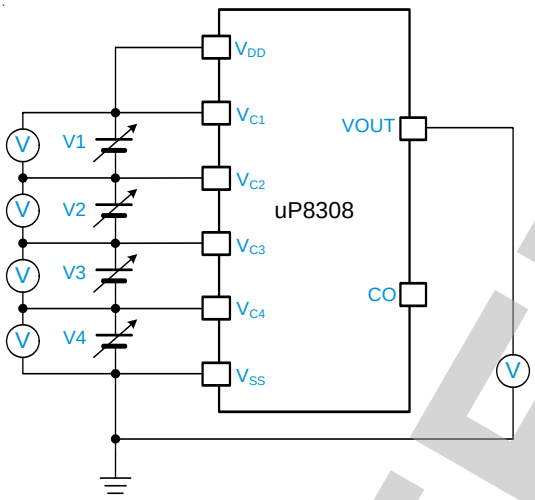
Test Circuit



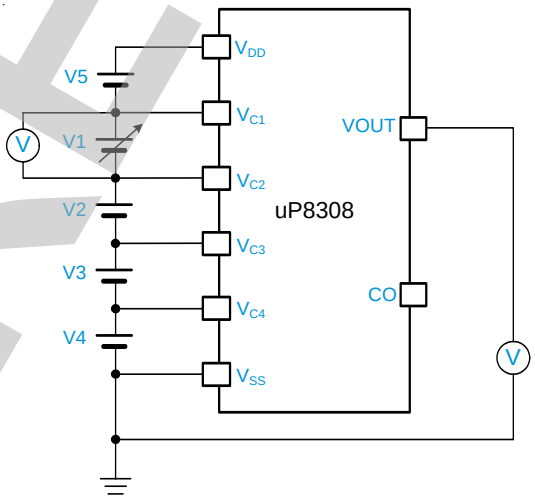
Test Circuit 7



Test Circuit 8



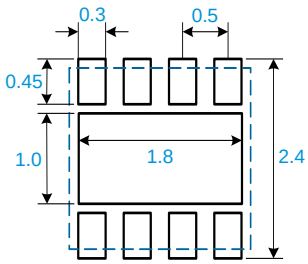
Test Circuit 9



Test Circuit 10

Application Information

Recommended Footprint:

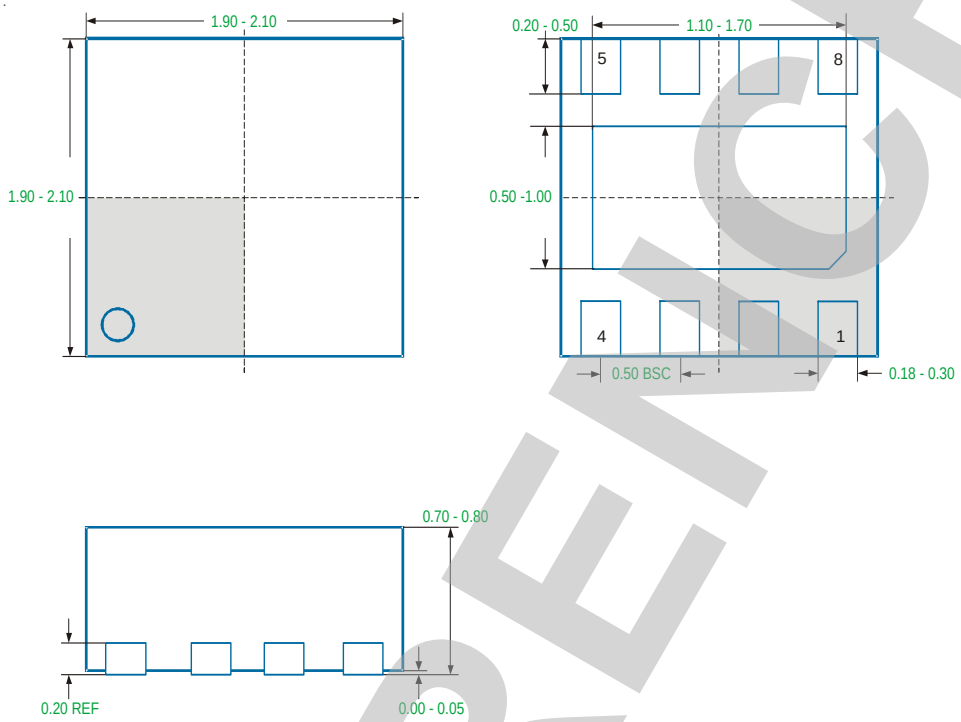


Package Type: WDFN2x2-8L
Tolerance: ±0.03
Unit: mm

CAUTION: The above information is for reference only. It may be adjusted based on the manufacturing parameters provided by PCB and assembly venders.

Packaging Information

WDFN2x2 - 8L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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