BQ2969 Overvoltage Protection for 2-Series, 3-Series, and 4-Series Cell Li-Ion Batteries with Regulated Output Supply

1 Features

- 2-series, 3-series, and 4-series cell overvoltage protection (OVP)
- Factory programmed OVP threshold (3.6V to 5.2V) with ±12mV accuracy
- Fixed delay timer to trigger FET drive output (0.25s to 6.5s options)
- Output pin options:
  - Active high
  - Open-drain - active pulldown
  - Open-drain - inactive pulldown
- Integrated 3mA regulated output programmable to 3.8V, 3.3V, 3.15V, 3.0V, 2.5V, 1.8V, or 1.5V
- Factory programmed undervoltage (UV) detection threshold (1V to 4.15V) to disable regulator
  - OVP remains operational even in undervoltage condition
- Multiple power modes:
  - NORMAL mode - no OV or UV: $I_{CC} \cong 1.23\mu A$
  - Undervoltage mode - UV detected: $I_{CC} \cong 0.25\mu A$
  - Overvoltage mode - OV detected: $I_{CC} \cong 19\mu A$
- Low leakage current per cell input < 100nA
- Small package footprint
  - 8-Pin WSON (2mm × 2mm)

2 Applications

- Notebook PC
- Ultrabooks
- Portable medical electronics
- UPS battery backup systems

3 Description

The BQ2969 family is a high-accuracy, low-power overvoltage protector with a 3mA regulated output supply for Li-ion and $LiFePO_4$ (LFP) battery pack applications.

Each cell in a 2-series to 4-series cell stack is individually monitored for an overvoltage condition. An internally fixed-delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output pin is triggered into an active state to indicate that an overvoltage condition has occurred.

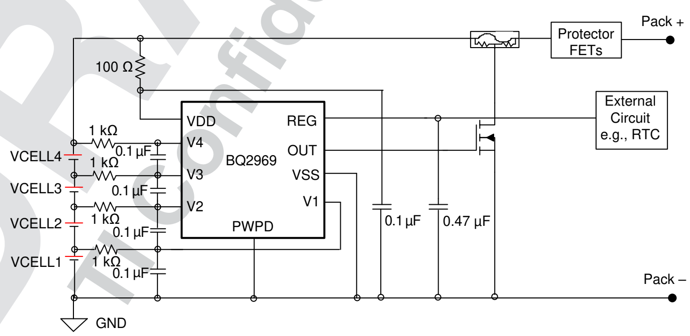
The regulated output supply delivers up to 3mA output current to drive always-on circuits, such as a real-time clock (RTC) oscillator. The BQ2969 family has a self-disable function to turn off the regulated output if any cell voltage falls below a programmable undervoltage threshold, thereby preventing drain on the battery.

The BQ2969 family provides exceptionally low power operation, drawing only 1.23µA during normal operation (excluding regulator load current), and dropping to 0.25uA when in an undervoltage condition. Even when in the undervoltage state, the device can still detect an overvoltage condition on any other cell (which can occur in an imbalanced pack) and can assert the output pin.

Package Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
BQ2969xy	DSG (8-WSON)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

ADVANCE INFORMATION

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4 Device Comparison Table

Table 4-1. BQ2969 Device Options

BQ2969 Device	OVP (V)	OVP DELAY (s)	OVP HYSTERESIS (mV)	UV (V)	LDO (V)	OUT PIN MODE	LATCH OUT
BQ296900	4.65	6.5	300	2.5	3.3	active high	No
BQ296901[(1)]	4.65	6.5	300	2.5	3	active high	No
BQ296902[(1)]	4.65	6.5	300	3	3	active high	No
BQ296907	4.65	6.5	300	2.5	1.5	active high	No
BQ296909[(1)]	4.65	6.5	300	2.7	3.3	active high	No
BQ296910[(1)]	4.35	6.5	300	1.8	3.0	active high	No
BQ2969xy[(1)]	3.6 – 5.2	0.25, 0.5, 1, 2, 3, 4, 5.5, 6.5	150, 300	1 – 4.15	1.5, 1.8, 2.5, 3.0, 3.15, 3.3, 3.8	active high, open-drain active pulldown, open-drain inactive pulldown	Yes, No

(1) PRODUCT PREVIEW. Contact TI for more information.

5 Pin Configuration and Functions

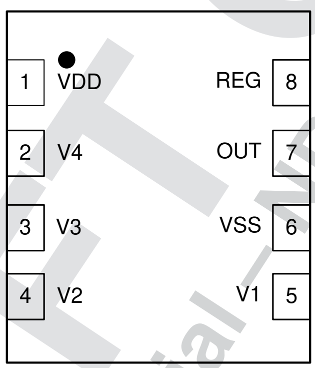

Figure 5-1. 2-Series to 4-Series BQ2969 (Top View)

Table 5-1. Pin Functions

PIN NAME	PIN BQ2962	TYPE[(1)]	DESCRIPTION
VDD	1	P	Power supply input
V4	2	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack
V3	3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
V2	4	IA	Sense input for positive voltage of the second cell from the bottom of the stack
V1	5	IA	Sense input for positive voltage of the lowest cell from the bottom of the stack
VSS	6	P	Electrically connected to integrated circuit ground and negative terminal of the lowest cell in the stack
OUT	7	OA	Analog output drive for an overvoltage fault signal; CMOS output high or open-drain active pulldown or open-drain inactive pulldown
REG	8	OA	Regulated supply output. Requires an external ceramic capacitor for stability
PWPD	-	P	TI recommends connecting the exposed pad to VSS on PCB.

(1) IA = Analog input, OA = Analog Output, P = Power connection

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range of –40°C to 110°C (unless otherwise noted)[(1)]

PARAMETER		MIN	MAX	UNIT
Supply voltage range	VDD – VSS	–0.3	30	V
	VDD – V4	–0.3	30	V
Input voltage range	V1 – VSS, V2 – VSS, V3 – VSS, V4 – VSS	–0.3	30	V
Output voltage range	REG – VSS	–0.3	5.0	V
Output voltage range	OUT – VSS	–0.3	30	V
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

PARAMETER			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VDD = 15.2V, MIN/MAX values stated where T_A = –40°C to 110°C, and V_{DD} = 3V to 22V (unless otherwise noted).

PARAMETER		MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	Supply voltage, V_{DD} (REG ≤ 2.5V)	3		22	V
	Supply voltage, V_{DD} (REG ≤ 3.3V)	4		22	V
	Supply voltage, V_{DD} (REG ≥ 3.8V)	7.5		22	V
	Normal operation, V_{DD} – V4[(1)]	–0.2		0.2	V
	Customer test mode, V_{DD} – V4		10		V
Input voltage range	V4 – V3, V3 – V2, V2 – V1, V1 – VSS	0		5.5	V
Operating ambient temperature range, T_A	Operating ambient temperature range, T_A	–40		110	°C

(1) Specified by design

6.4 Thermal Information

THERMAL INFORMATION [(1)]		BQ2969	UNIT
		SON	UNIT
		(8 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 15.2V, MIN/MAX values stated where T_A = –40°C to 110°C, and V_{DD} = 3V to 22V (unless otherwise noted).

PARAMETER	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Protection Thresholds						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	R_{IN} = 1kΩ		Applicable Voltage: 3.6V to 5.2V		V
V_{OVHYST}	OV Detection Hysteresis	Nominal setting of 150mV	100	150	200	mV
		Nominal setting of 300mV	250	300	350	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–12		12	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature[1]	T_A = –40°C	–40		40	mV
		T_A = -10°C	–22		22	mV
		T_A = 55°C	–24		24	mV
		T_A = 85°C	–37		37	mV
		T_A = 110°C	–50		50	mV
Supply and Leakage Current						
I_{DD}	Supply Current in NORMAL mode	$(V_n – V_{n-1})$ = $(V1 – V_{SS})$ = 3.8V, n = 2, 3, 4, VDD = 15.2V, I_{REG} = 0mA, T_A = –10°C to 60°C		1.23	2	µA
		$(V_n – V_{n-1})$ = $(V1 – V_{SS})$ = 3.8V, n = 2, 3, 4, VDD = 15.2V, I_{REG} = 0mA, T_A = –40°C to 110°C			2.5	µA
	Supply Current in UV	$(V_n - V_{n-1})$ = 3.8V, n = 2, 3, 4, and V_{UVQUAL} < $(V1 - V_{SS})$ < V_{UVREG}, VDD = 11.4V, T_A = –10°C to 60°C		0.25	0.5	µA
		$(V_n - V_{n-1})$ = 3.8V, n = 2, 3, 4, and V_{UVQUAL} < $(V1 - V_{SS})$ < V_{UVREG}, VDD = 11.4V, T_A = -40°C to 110°C			0.7	µA
	Supply Current in OV	$(V_n - V_{n-1})$ = 3.8V, n = 2, 3, 4, and V_{OV} < $(V1 - V_{SS})$, VDD = 15.2V, T_A = -40°C to 110°C		19	30	µA
I_{IN}	Input Current at V_n Pins	$(V_n – V_{n-1})$ = $(V1 – V_{SS})$ = 3.8V, n = 2, 3, 4, VDD = 15.2V, T_A = 25°C	–0.1		0.1	µA
Input Voltage						
OUT Pin Driver						
V_{OUT}	Output Drive Voltage	OUT pin configured in active high mode, $(V_n – V_{n-1})$ or $(V1 – V_{SS})$ > V_{OV}, n = 2, 3, 4, I_{OH} = 100µA, VDD ≥ 7.5V	5.5		8	V
		OUT pin configured in active high mode, $(V_n – V_{n-1})$ or $(V1 – V_{SS})$ > V_{OV}, n = 2, 3, 4, I_{OH} = 100µA, 3V < VDD < 7.5V	VDD – 1.5	VDD – 1.1	VDD	V
		OUT pin configured in active high mode, $(V_n – V_{n-1})$ and $(V1 – V_{SS})$ < V_{OV}, n = 2, 3, 4, I_{OL} = 100µA flowing into OUT pin.		190	400	mV
I_{OUTH}	OUT Source Current (during OV)	OUT pin configured in active high mode, $(V_n – V_{n-1})$ or $(V1 – V_{SS})$ > V_{OV}, n = 2, 3, 4, OUT = 0V, current measured sourced from OUT pin.	0.6		5.2	mA
I_{OUTL}	OUT Sink Current	OUT pin configured in active high, open-drain active pulldown, or open-drain inactive pulldown. Device output in pulldown state, OUT driven to 0.5V, current measured into OUT pin.	0.2		4	mA
OV Delay Timer						
t_{DELAY}	OV Delay Time[2]	Internal fixed delay, 0.25 second delay option[3]	0.14	0.25	0.38	s
		Internal fixed delay, 0.5 second delay option[3]	0.34	0.5	0.68	s
		Internal fixed delay, 1 second delay option[3]	0.74	1	1.28	s
		Internal fixed delay, 2 second delay option[3]	1.54	2	2.48	s
		Internal fixed delay, 3 second delay option[3]	2.4	3	3.6	s
		Internal fixed delay, 4 second delay option[3]	3.2	4	4.8	s
		Internal fixed delay, 5.5 second delay option[3]	4.4	5.5	6.6	s
		Internal fixed delay, 6.5 second delay option[3]	5.2	6.5	7.8	s

Typical values stated where T_A = 25°C and VDD = 15.2V, MIN/MAX values stated where T_A = –40°C to 110°C, and V_{DD} = 3V to 22V (unless otherwise noted).

PARAMETER	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY_CTM}	OV Delay Time in Test Mode	Internal fixed delay		15		ms
t_{DELAY_RESET}	OV Delay Reset Time	With one cell voltage above V_{OV}, others cells below V_{OV}, minimum time the high cell voltage must fall below V_{OV} to reset OV Delay Timer(3)	0.1			ms
Regulated Supply Output, REG						
V_{REG}	REG Supply	VDD ≥ 7.5V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 3.8V, T_A = 25°C	3.724	3.8	3.876	V
		VDD ≥ 4V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 3.3V, T_A = 25°C	3.234	3.3	3.366	V
		VDD ≥ 4V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 3.15V, T_A = 25°C	3.087	3.15	3.213	V
		VDD ≥ 4V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 3.0V, T_A = 25°C	2.94	3.0	3.06	V
		VDD ≥ 3V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 2.5V, T_A = 25°C	2.45	2.5	2.55	V
		VDD ≥ 3V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 1.8V, T_A = 25°C	1.764	1.8	1.836	V
		VDD ≥ 3V, I_{REG} = 10μA, C_{REG} = 0.47μF, V_{REG} = 1.5V, T_A = 25°C	1.470	1.5	1.530	V
V_{REG}	REG Supply	VDD ≥ 7.5V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 3.8V	3.58	3.8	3.88	V
		VDD ≥ 4V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 3.3V	3.12	3.3	3.39	V
		VDD ≥ 4V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 3.15V	2.98	3.15	3.23	V
		VDD ≥ 4V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 3.0V	2.84	3.0	3.08	V
		VDD ≥ 3V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 2.5V	2.35	2.5	2.57	V
		VDD ≥ 3V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 1.8V	1.70	1.8	1.85	V
		VDD ≥ 3V, I_{REG} = 3mA, C_{REG} = 0.47μF, V_{REG} = 1.5V	1.42	1.5	1.56	V
$I_{REG\_SC\_Limit}$	REG Output Short Circuit Current Limit	REG = V_{SS}, C_{REG} = 0.47μF	3.2		25	mA
R_{REG_PD}	REG pull-down resistor	Activated when REG is disabled	20	30	40	kΩ
Regulated Supply Undervoltage Self-disable						
V_{UVREG}	Undervoltage detection accuracy	Factory Configuration: 1.0V to 4.15V in 50mV steps, T_A = 25 °C	–50		50	mV
V_{UVHYS}	Undervoltage detection hysteresis		250	300	350	mV
$t_{UVDELAY}$	Undervoltage detection delay(3)		5.2	6.5	7.8	s
V_{UVQUAL}	Cell voltage to qualify for UV detection		0.45	0.5	0.55	V

(1) Specified by a combination of characterization and production test
(2) Delay values specified when transitioning from NORMAL mode to OVERVOLTAGE mode. While device is in UNDERVOLTAGE mode, the delay can increase by a value between 0 and 1.2 seconds.
(3) Specified by a combination of design and production test

6.6 Typical Characteristics

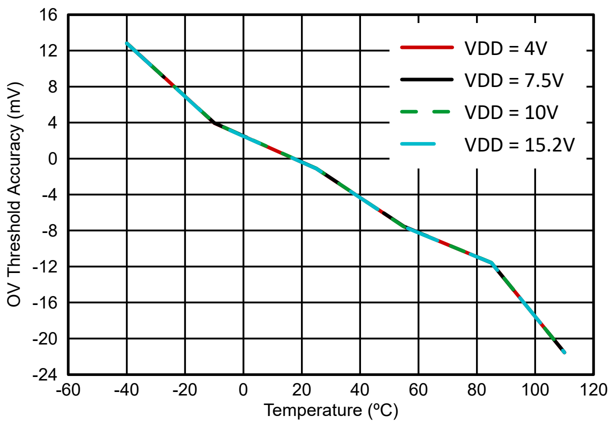

Figure 6-1. Overvoltage Threshold Accuracy vs. Temperature

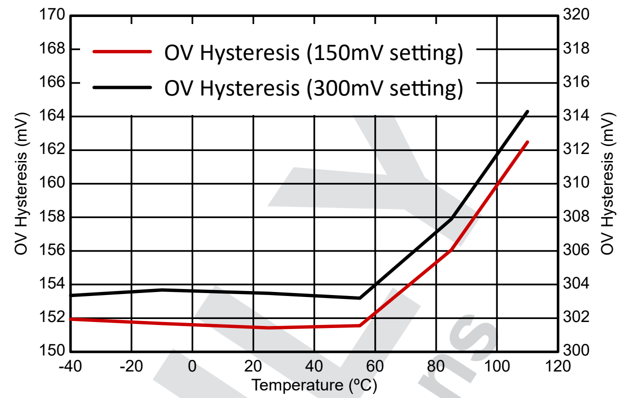

Figure 6-2. Overvoltage Hysteresis vs. Temperature

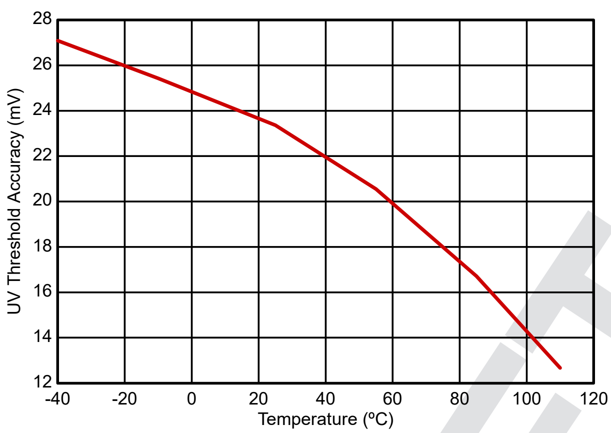

Figure 6-3. Undervoltage Threshold Accuracy vs. Temperature

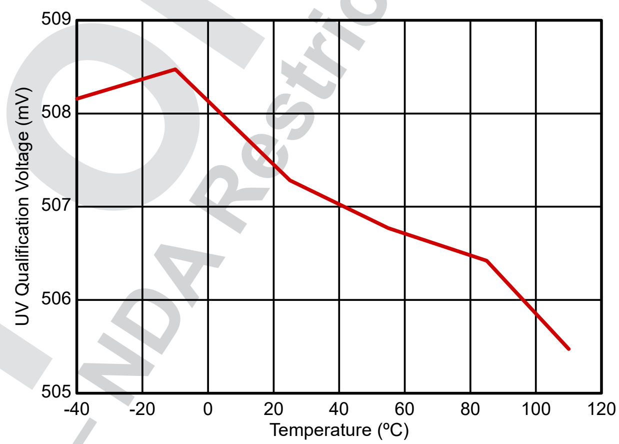

Figure 6-4. Undervoltage Qualification Voltage vs. Temperature

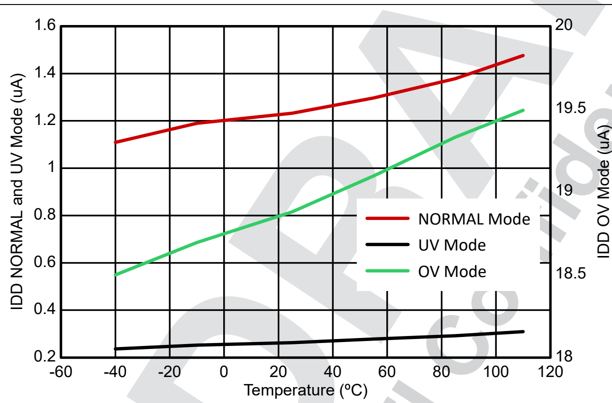

Figure 6-5. I_{DD} vs. Temperature

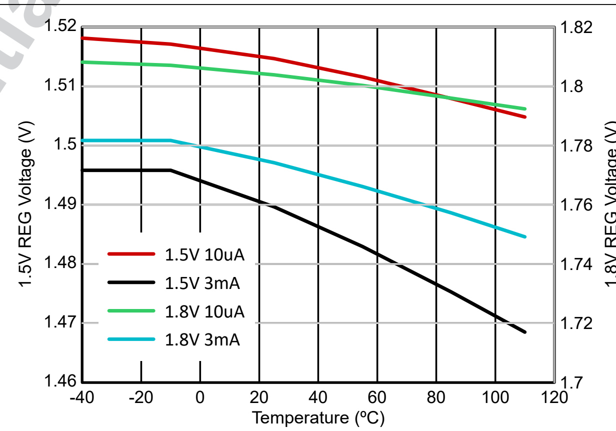

Figure 6-6. Regulator Output vs. Temperature, 1.5V and 1.8V Settings

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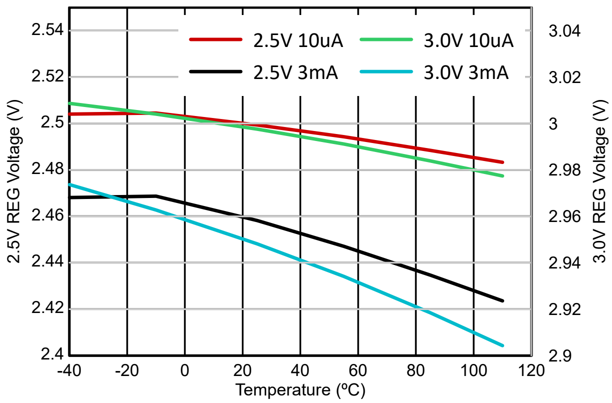

Figure 6-7. Regulator Output vs. Temperature, 2.5V and 3.0V Settings

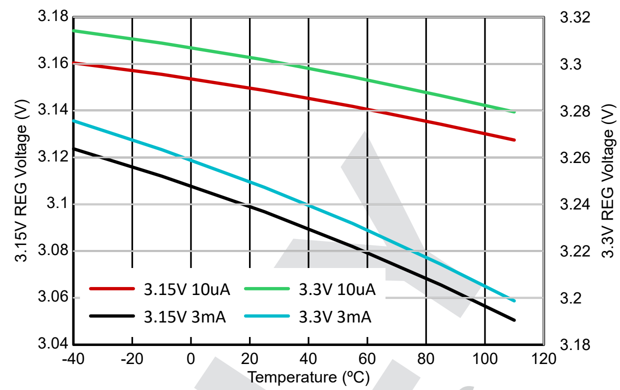

Figure 6-8. Regulator Output vs. Temperature, 3.15V and 3.3V Settings

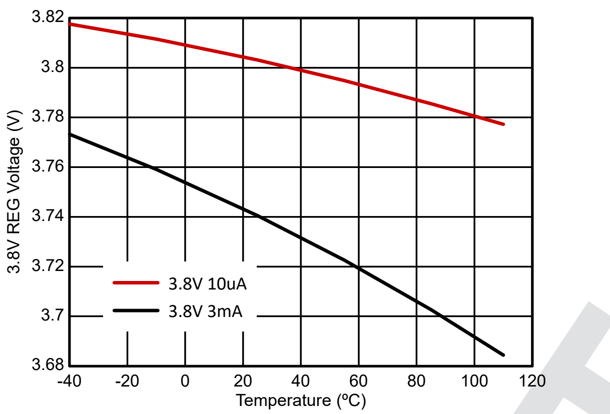

Figure 6-9. Regulator Output vs. Temperature, 3.8V Setting

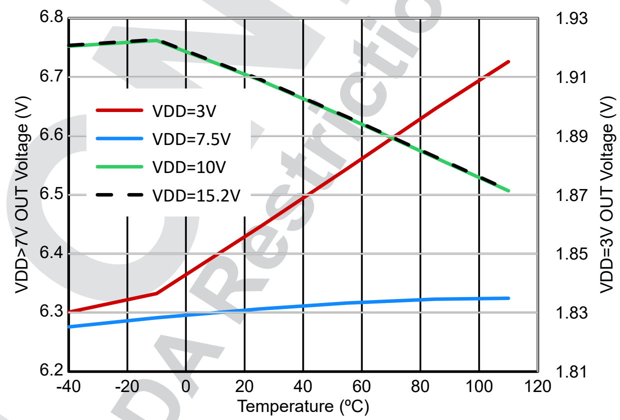

Figure 6-10. V_{OUT} vs Temperature, with 100µA Load Current on OUT

7 Detailed Description

7.1 Overview

The BQ2969 family is a high-accuracy, low-power second-level overvoltage protector with a 3mA regulated output supply for Li-ion and $LiFePO_4$ (LFP) battery pack applications.

Each cell in a 2-series to 4-series cell stack is individually monitored for an overvoltage condition by comparing the actual cell voltage to an overvoltage threshold V_{OV}. The overvoltage threshold is preprogrammed at the factory with a range between 3.6V to 5.2V. The device initiates an internal fixed-delay timer when an overvoltage condition is detected on any cell. Upon expiration of the delay timer, the output pin is triggered into an active state to indicate that an overvoltage condition has occurred. The output pin can be configured to be active-high, open-drain active pulldown, or open-drain inactive pulldown. The device recovers from the overvoltage condition when all cell voltages are detected below the overvoltage threshold by a hysteresis level, which can be programmed to 150mV or 300mV. Alternatively, the output pin can be programmed to latch and not recover whenever it is activated.

The regulated output supply is programmable from 1.5V to 3.8V and delivers up to 3mA output current to drive always-on circuits, such as a real-time clock (RTC) oscillator. The BQ2969 family has a self-disable function to turn off the regulated output if any cell voltage falls below a programmable undervoltage threshold, thereby preventing drain on the battery. This undervoltage threshold can be programmed over a range from 1V to 4.15V.

The BQ2969 family provides extremely low power operation, drawing only 1.23µA during normal operation (excluding regulator load current), and dropping to 0.25uA when in an undervoltage condition. Even when in the undervoltage state, the device still monitors cell voltages and can detect an overvoltage condition on any other cell (which can occur in an imbalanced pack) and assert the output pin.

Table 7-1. Programmable Parameters

OVERVOLTAGE RANGE (V)	OVERVOLTAGE DELAY (s)	OVERVOLTAGE HYSTERESIS (mV)	UNDERVOLTAGE RANGE (V)	OUT PIN MODE	LATCHED OUT	REGULATOR (V)
3.6 to 5.2 in 1mV steps	0.25, 0.5, 1, 2, 3, 4, 5.5, 6.5	150, 300	1.0 to 4.15 in 50mV steps	active high, open-drain active pulldown, open-drain inactive pulldown	yes, no	1.5, 1.8, 2.5, 3.0, 3.15, 3.3, 3.8

7.2 Functional Block Diagram

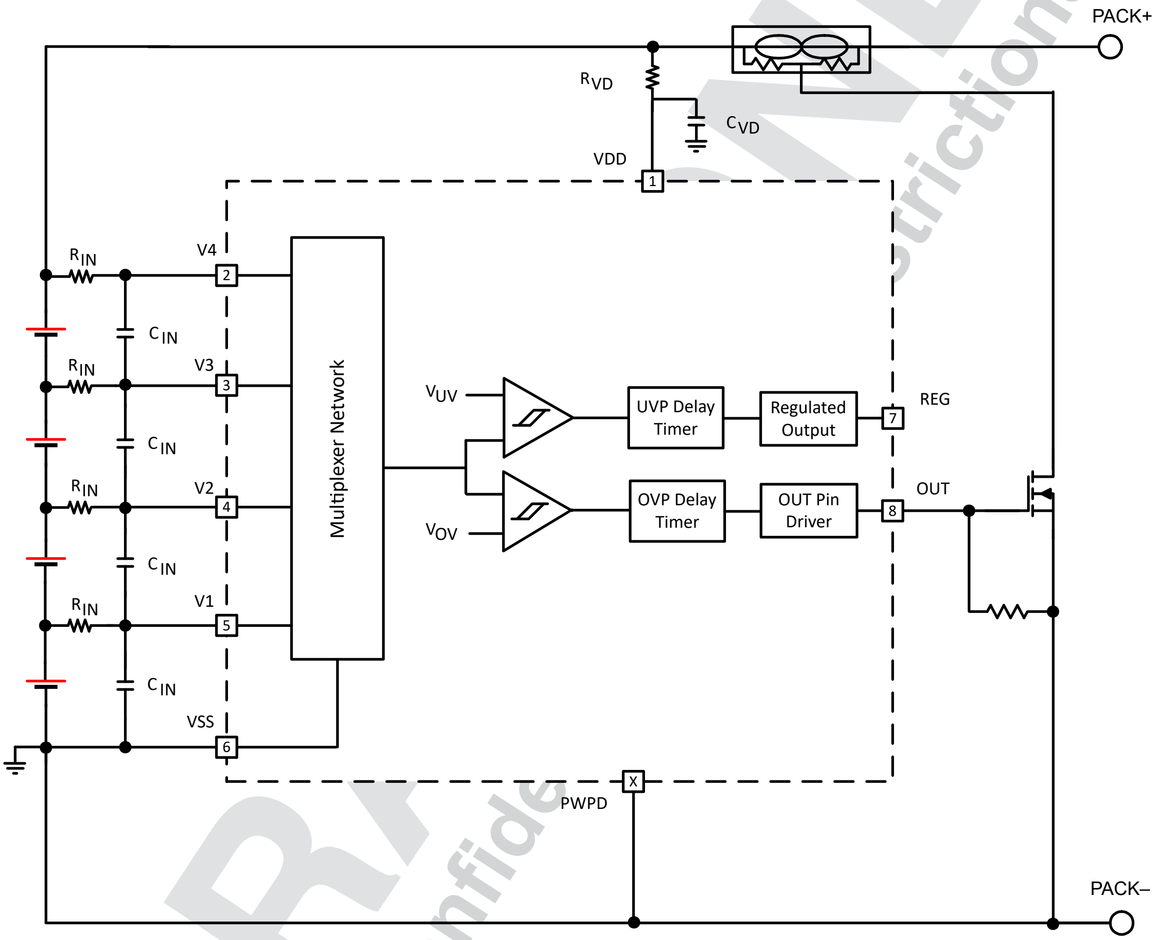

Figure 7-1. BQ2969 Block Diagram

7.3 Feature Description

7.3.1 Pin Details

7.3.1.1 Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

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7.3.1.2 Output Drive, OUT

This terminal serves as the fault signal output whenever an overvoltage condition on any cell is detected. The pin can be configured as active high, open-drain active pulldown, or open-drain inactive pulldown. The pin can also be programmed to latch asserted when an overvoltage condition occurs, or to recover after the maximum cell voltage drops 150mV or 300mV below the overvoltage threshold.

7.3.1.3 Supply Input, VDD

This terminal is the unregulated input power source for the device. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

7.3.1.4 Regulated Supply Output, REG

The BQ2969 provides a regulated supply on the REG pin, which can be used to power external circuitry such as a real-time clock or other function. The REG output includes current limit protection circuit and also detects and protects for excessive power dissipation due to short circuit of the external load. This pin requires a ceramic 0.47μF capacitor connection to VSS for stability, noise immunity, and ESD performance of the supply output. This capacitor must be placed close to the REG and VSS pins for connection.

7.3.2 Overvoltage Sensing for OUT

Each cell in the BQ2969 device is monitored independently for an overvoltage condition. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed V_{OV} value, an internal timer circuit is activated. After the timer completes a fixed, pre-programmed delay, the OUT pin transitions from an inactive state to the active state.

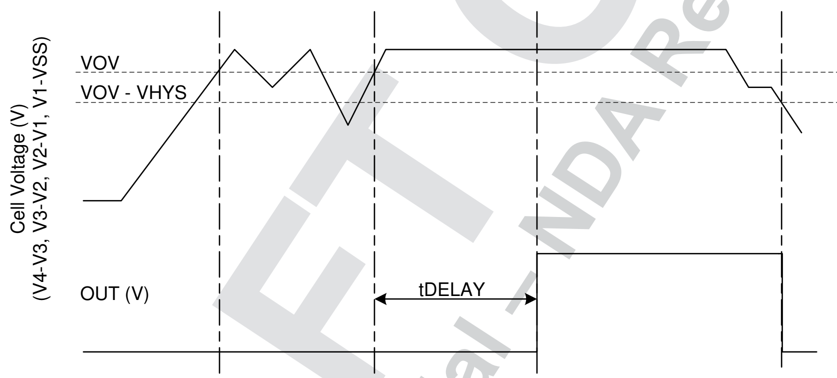

Figure 7-2. Timing for Overvoltage Sensing for OUT

7.3.3 Regulator Output Voltage

At power up, the regulator output in the BQ2969 is on by default. If any cell voltage is below V_{UVREG} at device power up, the regulator output remains on until the $t_{UVDELAY}$ time has passed, then the device disables the regulator output.

During discharge, if any cell voltage falls below the V_{UVREG} threshold for $t_{UVDELAY}$ time, the regulator output is self-disabled. The regulator output turns on again when all the cell voltages are above V_{UVREG} + V_{UVHYS}.

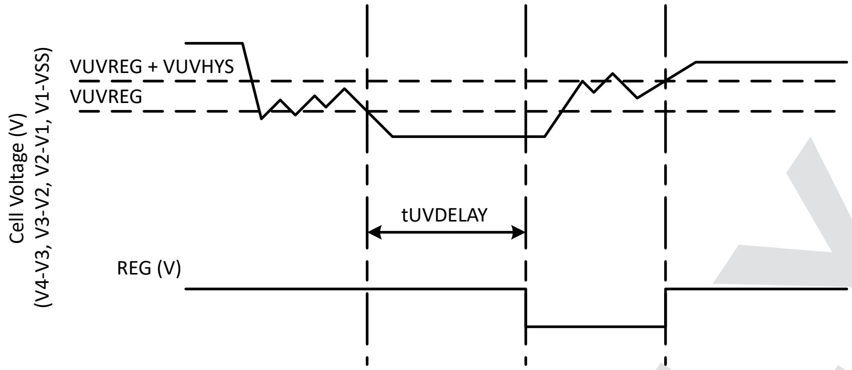

Figure 7-3. REG Output Timing

7.4 Device Functional Modes

7.4.1 NORMAL Mode

When all of the cell voltages are below the V_{OV} threshold AND above the V_{UVREG} threshold, the device operates in NORMAL mode. The device regularly monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive in this mode, and the regulated output is enabled.

7.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceed the overvoltage threshold, V_{OV}, for a configured OV delay time. The OUT pin is activated after a delay time pre-programmed at the factory. This pin is typically used to then enable an external FET and blow a fuse to disable the pack. When all of the cell voltages fall below (V_{OV} – V_{HYS}) and remain above the V_{UVREG} threshold, the device returns to NORMAL mode if the output is not configured to latch when asserted. The regulated output remains enabled in this mode if all cell voltages are above V_{UVREG}.

7.4.3 UNDERVOLTAGE Mode

The UNDERVOLTAGE mode is detected if any of the cell voltage across (V1–VSS), (V2–V1), (V3–V2), or (V4–V3) is below the V_{UVREG} threshold for $t_{UVDELAY}$ time. In this mode, the regulated output is disabled. To return to NORMAL mode, all the cell voltages must be above (V_{UVREG} + V_{UVHYS}) and below V_{OV}.

If the device is used in a system with fewer than 4 cells, V_n pin can be shorted to the (V_{n-1}) pin. The device ignores any differential cell voltage below the V_{UVQUAL} threshold for undervoltage detection.

Even when in the UNDERVOLTAGE mode, the device continues to regularly monitor each cell voltage, checking if any cell voltage exceeds the V_{OV} threshold. If a condition occurs whereby a cell voltage is above V_{OV} and another cell voltage is below V_{UVREG}, such as can happen in a heavily imbalanced pack, then the OUT pin is activated and the regulator is disabled.

7.4.4 CUSTOMER TEST MODE

The Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay-timer parameter once the circuit is implemented into the battery pack. To enter CTM, the VDD pin must be set at approximately 10V higher than V4 (see Figure 7-4). In this mode, the overvoltage delay timer is reduced to approximately 20ms, considerably shorter than the timer delay in normal operation. To exit CTM, reduce the VDD voltage back to the voltage of V4, which causes the device to exit this mode.

CAUTION
Avoid exceeding any Absolute Maximum Voltages on any pins when placing the device into CTM. Stressing the pins beyond the rated limits can cause permanent damage to the device.

Figure 7-4 shows the timing for the Customer Test Mode.

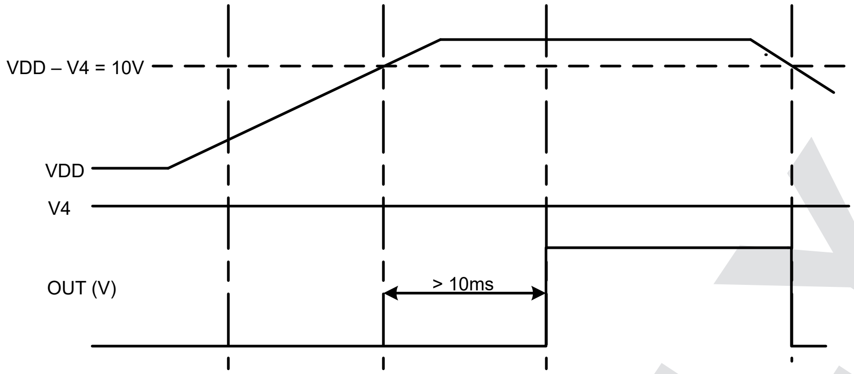

Figure 7-4. Timing for Customer Test Mode

Figure 7-5 shows the measurement for current consumption of the product for VDD and the cell input pins.

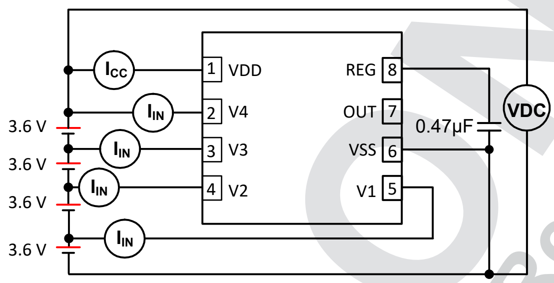

Figure 7-5. Configuration for Integrated Circuit Current Consumption Test

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The BQ2969 family of second-level protectors is used for overvoltage protection of the battery pack in the application. A regulated output is available to drive local external circuitry. The device OUT pin can be configured in one of 3 drive types and is asserted whenever the device enters the overvoltage mode. The pin is typically used to drive an NMOS FET that blows a fuse in the event of a fault condition, thereby disconnecting the pack power path.

8.2 Typical Application

Figure 8-1 shows a simplified application schematic using the BQ2969 together with the associated passive components and external NFET to flow a high-side fuse.

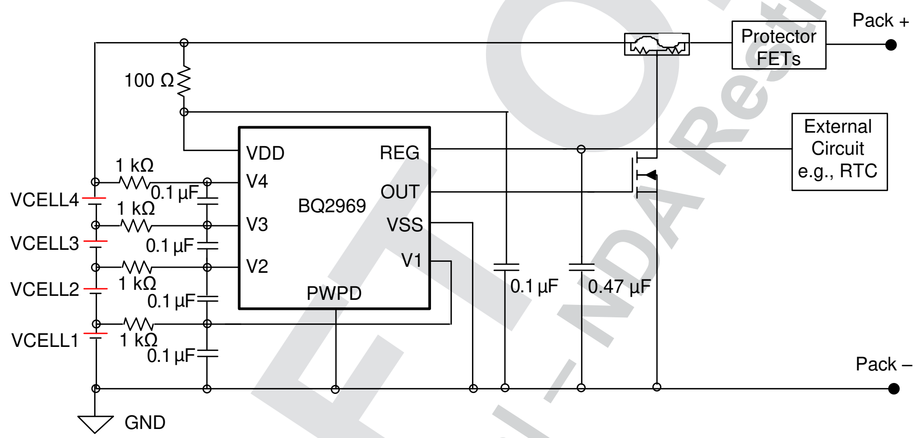

Figure 8-1. BQ2969 4-Series Cell Typical Implementation (Simplified Schematic)

A full schematic of a basic circuit based on the BQ2969 for a 4-series battery pack evaluation module is shown below. Figure 10-1 and Figure 10-2 show the board layout for this design.

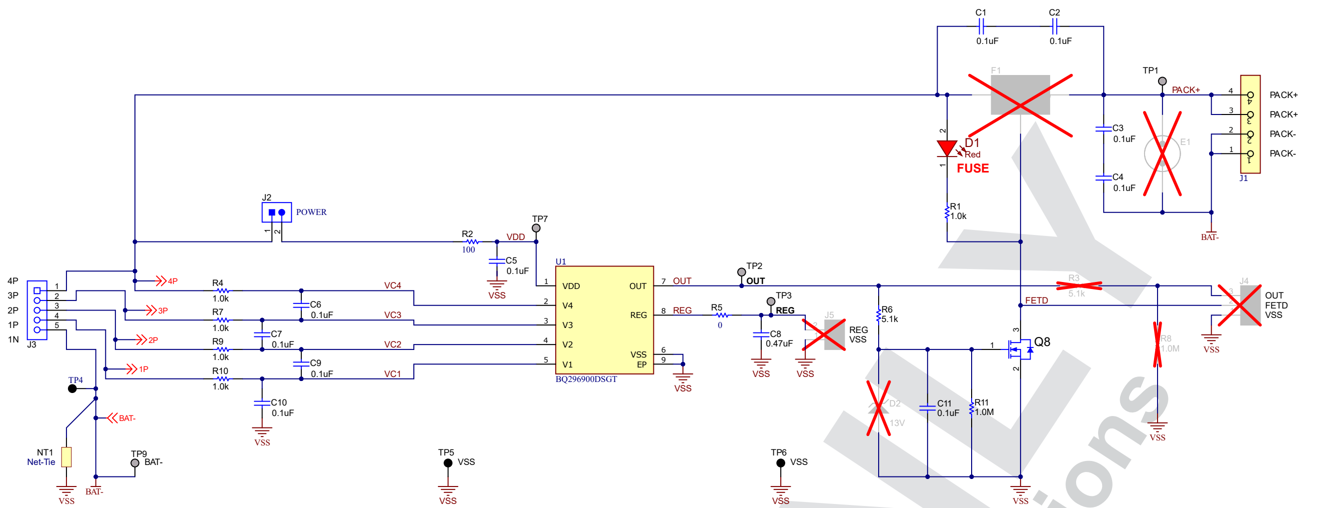

Figure 8-2. BQ2969 4-Series Cell Schematic Diagram - Protector and Fuse Blow Circuitry

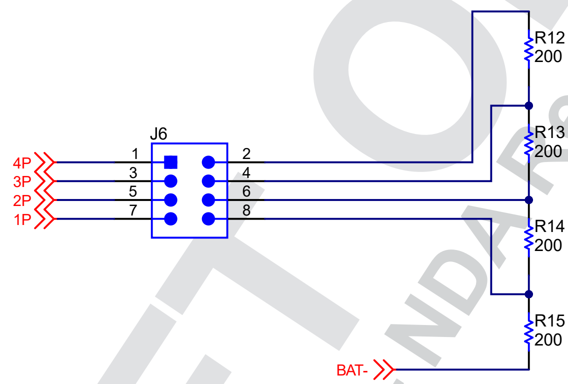

Figure 8-3. BQ2969 4-Series Cell Schematic Diagram - Cell Simulator Circuitry

8.2.1 Design Requirements

Note

Changes to the ranges shown in Table 8-1 can impact the accuracy of the cell measurements.

Table 8-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	µF
Supply voltage filter resistance	R_{VD}	100	—	1000	Ω
Supply voltage filter capacitance	C_{VD}	—	0.1	1.0	µF
REG output capacitance	C_{REG}	0.47	1	—	µF

Note

The device is calibrated using an R_{IN} value = 1000Ω. Using a value other than the recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

8.2.2 Detailed Design Procedure

1. The device allows a random cell connection to the VSS, V1, V2, V3, and V4 pins. The device does not require VSS to be connected first and does not require cells to be connected in a particular order. However, it is possible for the OUT pin to be temporarily asserted during cell attach, depending on the timing of the attachment and the external circuitry connected to the device. The user may want to take measures to ensure this does not cause issues on the production line.
2. If fewer than 4 cells are used, then an unused cell input pin V_n must be shorted to the next lower cell input pin (V_{n-1}).
3. The cell input capacitors, the supply pin capacitor, and the REG output capacitor are recommended to be placed close to the device, minimizing trace length on the PCB.

8.2.3 Application Curves

The scope plots below show the response of the device transitioning among the different states. Figure 8-4 shows the device detecting an overvoltage event and asserting the OUT pin to blow an external fuse after the overvoltage delay period. Figure 8-5 displays the device recovering from the overvoltage event when all cell voltages have fallen below the overvoltage threshold by the required hysteresis level, and the OUT pin deasserting. Figure 8-6 shows the device detecting an undervoltage condition and disabling the REG LDO output after the undervoltage delay period. Figure 8-7 then depicts the device recovering from the undervoltage condition and re-enabling the REG LDO when all cell voltages have risen above the undervoltage threshold by the required hysteresis level.

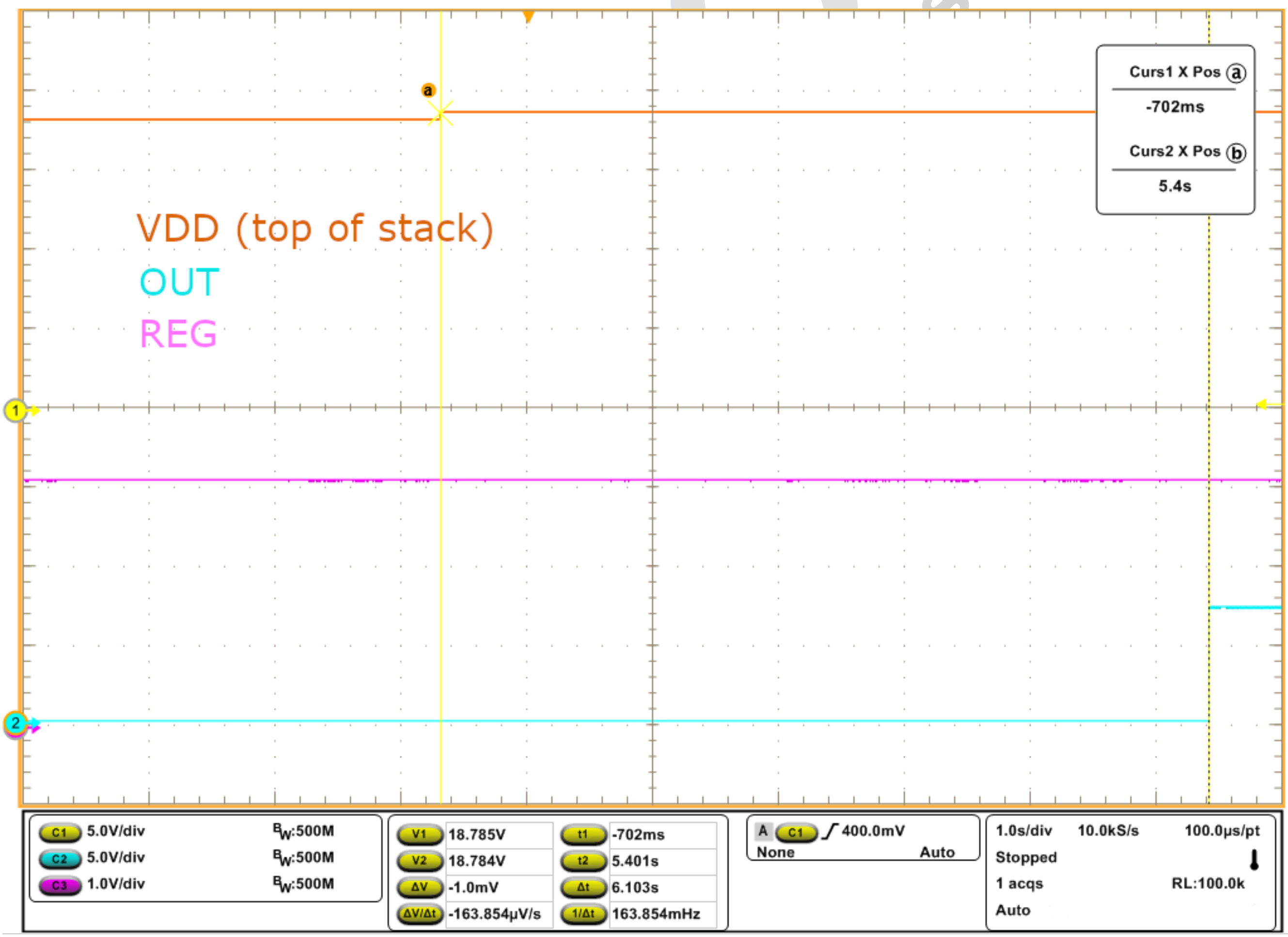

Figure 8-4. Overvoltage Protection Triggering

ADVANCE INFORMATION

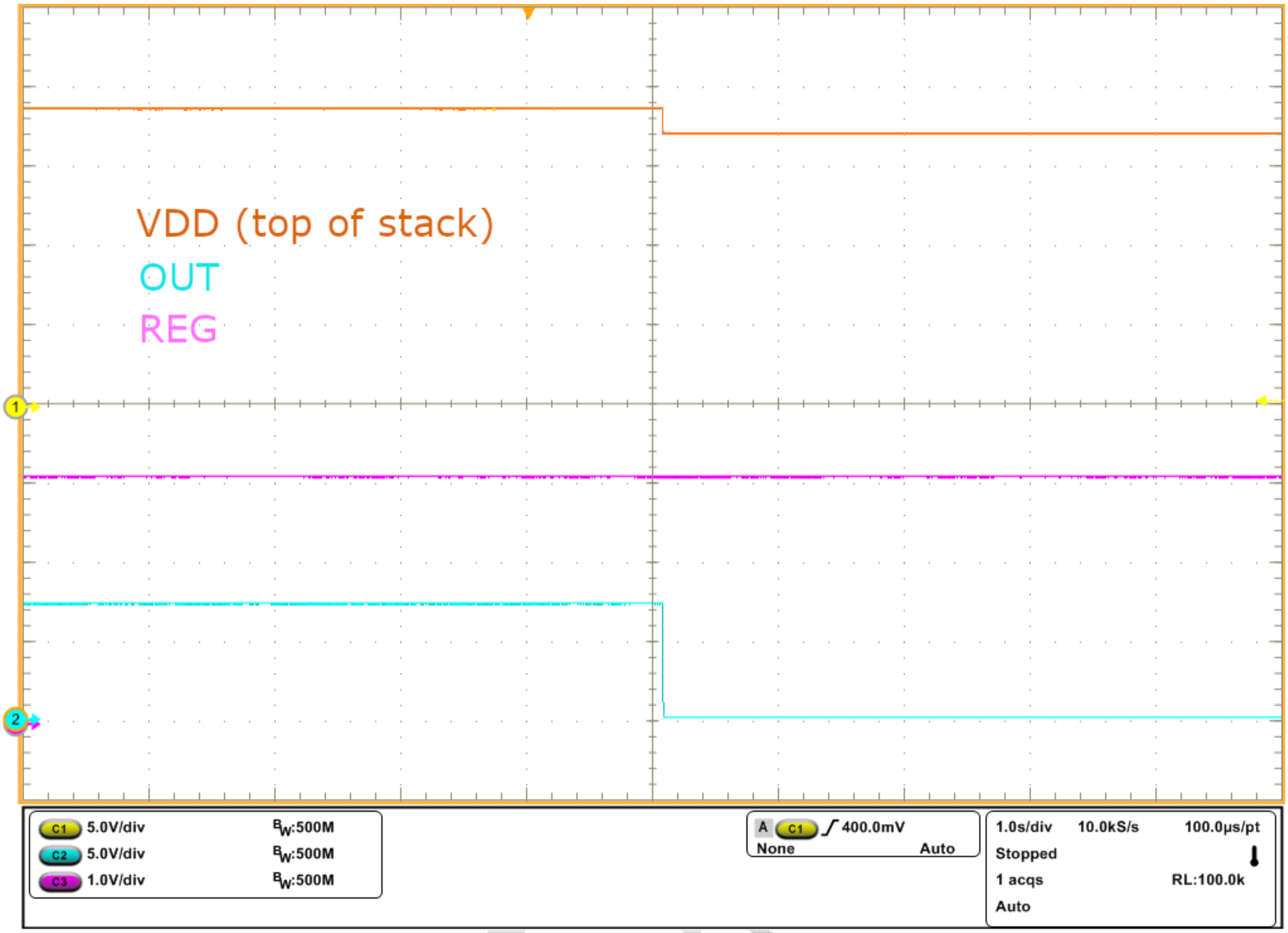

Figure 8-5. Overvoltage Protection Recovery

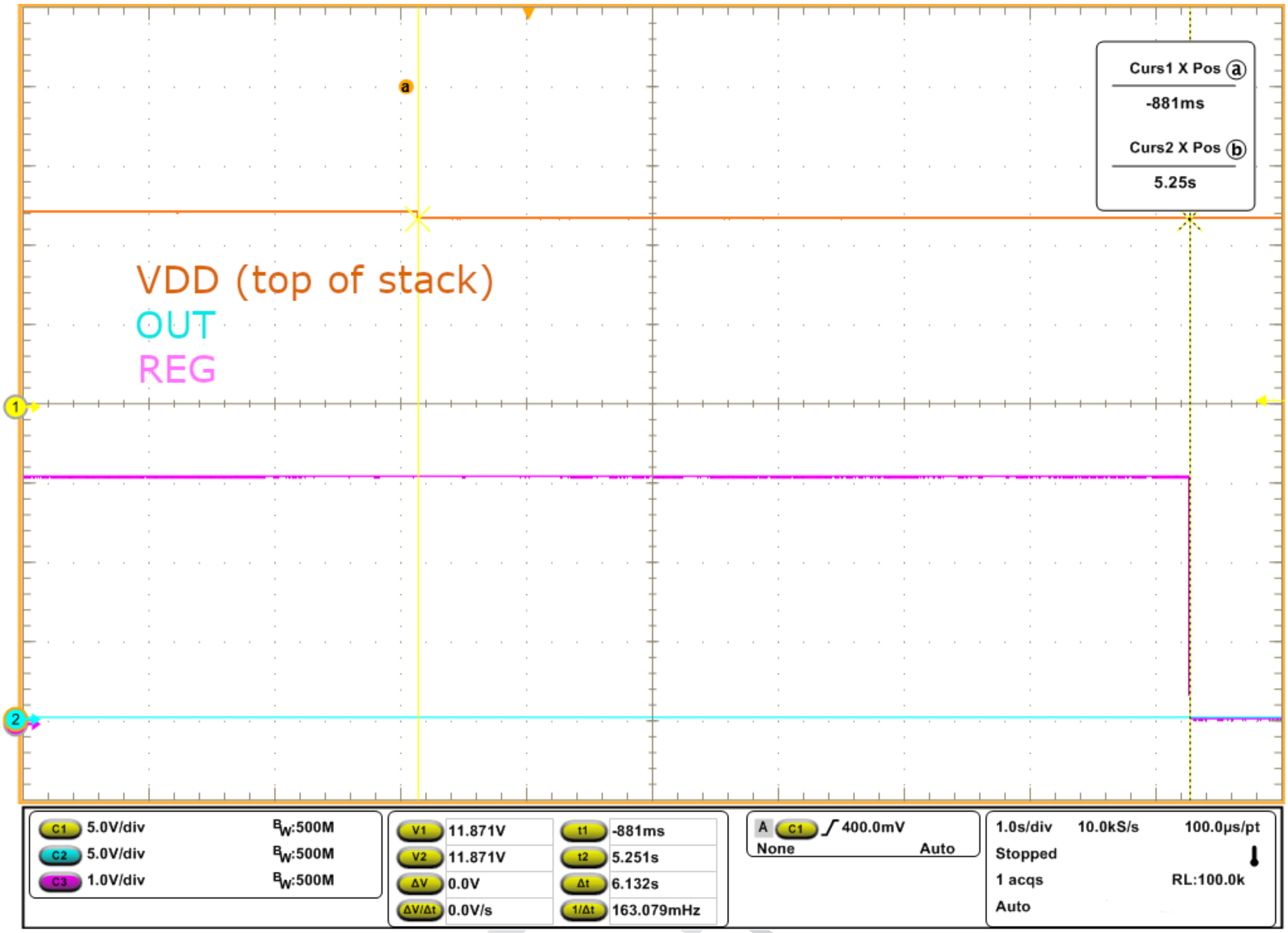

Figure 8-6. Undervoltage Detection to Disable the Regulator

ADVANCE INFORMATION

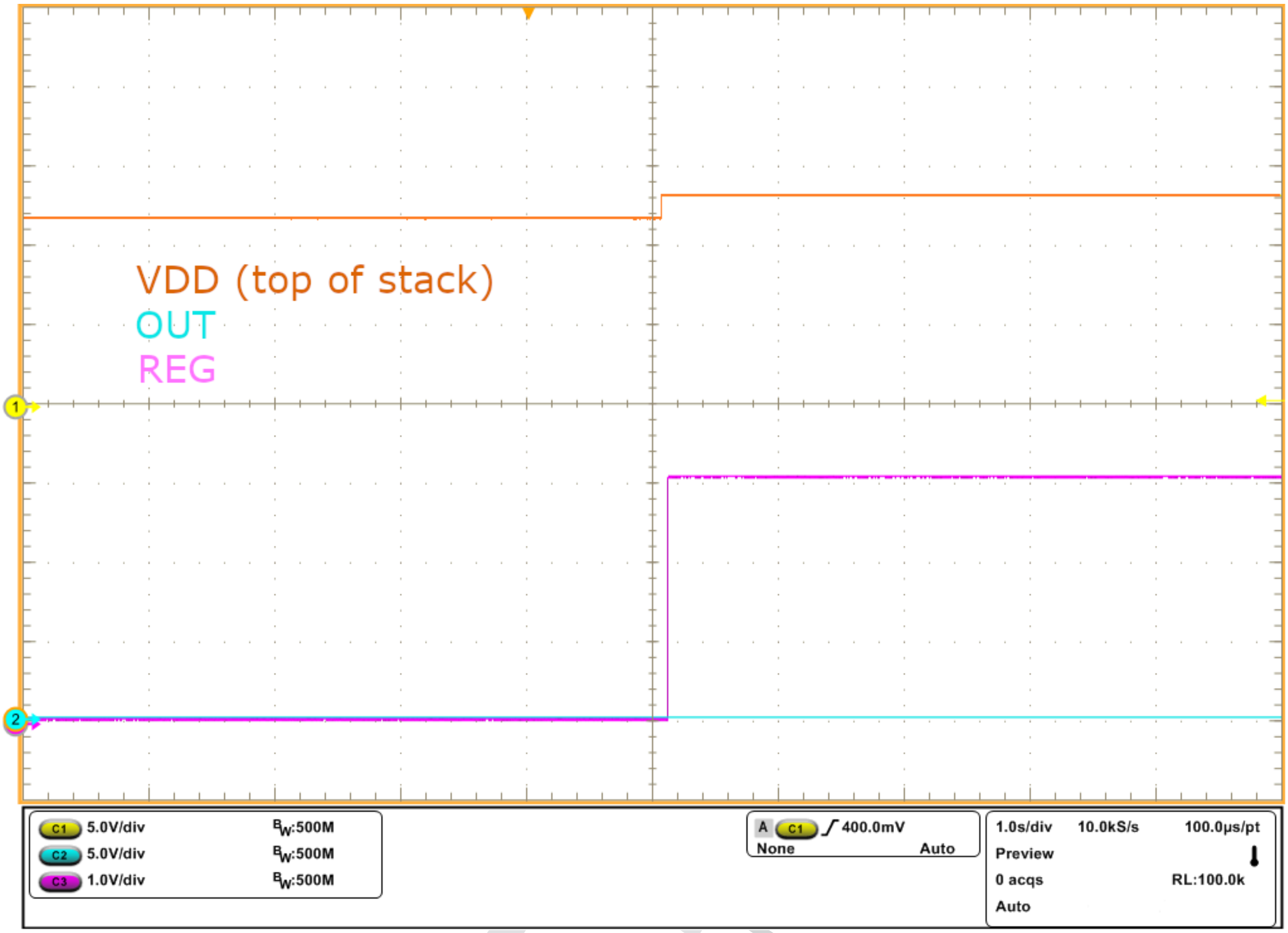

Figure 8-7. Undervoltage Recovery to Re-enable the Regulator

9 Power Supply Recommendations

Connect a series resistor between the top of the cell stack and the VDD pin on the BQ2969. Connect a capacitor between the VDD and VSS pins on the device, positioned close to the pins on the PCB. Connect the VSS pin to the bottom of the cell stack.

10 Layout

10.1 Layout Guidelines

Use the following layout guidelines:

1. Ensure the RC filters for the cell input pins (V4, V3, V2, V1, VSS) and VDD pin are placed as close as possible to the target pin, reducing the tracing loop area.
2. Place the regulator output capacitor between REG and VSS, keeping the capacitor close to the device pins.
3. Ensure the trace connecting the fuse through the NFET to the Pack– is sufficient to withstand the expected current during a fuse blow event.

10.2 Layout Example

An example circuit layout using the BQ2969 device in a 4-series cell design is described below in Figure 10-1 and Figure 10-2. The design implements the schematic shown in Figure 8-2 and Figure 8-3, and uses a 2-layer circuit card assembly with cell connections on the left edge and pack connections on the right edge of the board.

Care must be taken to place the RC filter components close to the VC pins of the device. Be sure to use a sufficiently wide trace for the NFET source and drain connections to support the maximum current that flows during a fuse blow event.

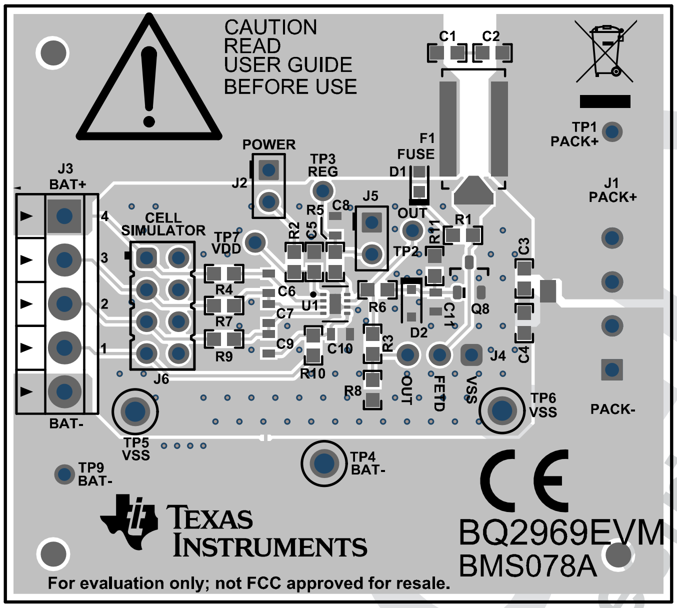

Figure 10-1. BQ2969 Two-Layer Board Layout - Top Layer

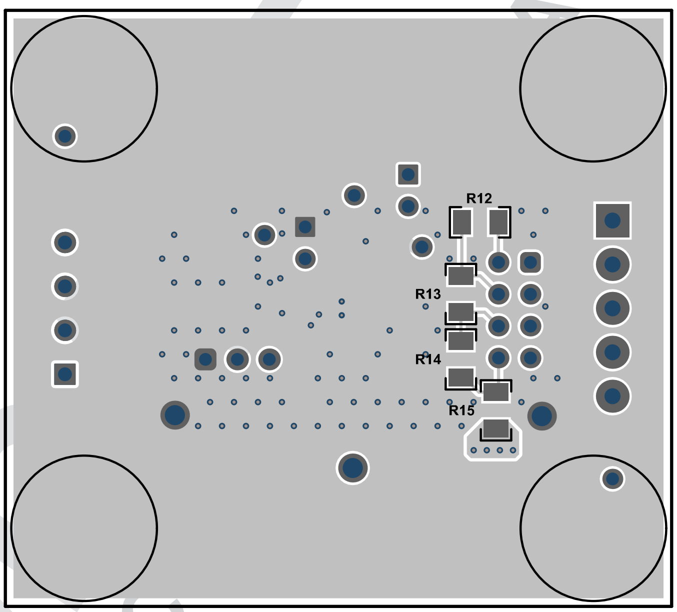

Figure 10-2. BQ2969 Two-Layer Board Layout - Bottom Layer

11 Device and Documentation Support

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (May 2025) **Page**

- Added BQ296910 and BQ296909 to Device Comparison Table 3
- Modified t_{DELAY_RESET} description in Electrical Characteristics 4
- Added clarification information in Detailed Design Procedure 15
- Modified Pin1 quadrant for all versions in Mechanical, Packaging, and Orderable Information 20

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.