# A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking

Sachin Jain and Vivek Agarwal, *Senior Member, IEEE*

***Abstract*—This paper proposes a high performance, single-stage inverter topology for grid connected PV systems. The proposed configuration can not only boost the usually low photovoltaic (PV) array voltage, but can also convert the solar dc power into high quality ac power for feeding into the grid, while tracking the maximum power from the PV array. Total harmonic distortion of the current, fed into the grid, is restricted as per the IEEE-519 standard. The proposed topology has several desirable features such as better utilization of the PV array, higher efficiency, low cost and compact size. Further, due to the very nature of the proposed topology, the PV array appears as a floating source to the grid, thereby enhancing the overall safety of the system. A survey of the existing topologies, suitable for single-stage, grid connected PV applications, is carried out and a detailed comparison with the proposed topology is presented. A complete steady-state analysis, including the design procedure and expressions for peak device stresses, is included. Necessary condition on the modulation index "$M$" for sinusoidal pulsewidth modulated control of the proposed inverter topology has also been derived for discontinuous conduction mode operation. All the analytical, simulation and experimental results are presented.**

***Index Terms*—Efficiency, grid-connected, inverter, photovoltaic (PV), single-stage.**

## I. Introduction

HIGH initial investment and limited life span of a photovoltaic (PV) array makes it necessary for the user to extract maximum power from the PV system. The nonlinear $i$–$v$ characteristics of the PV array [1] and the rotation and revolution of the earth around the sun, further necessitate the application of maximum power point tracking (MPPT) [2] to the system. In this context, grid connected PV systems have become very popular because they do not need battery back-ups to ensure MPPT. Stand alone systems can also achieve MPPT, but they would need suitable battery back-ups for this purpose.

Though, multistage systems [1] have been reported for certain applications, grid connected PV systems usually employ two stages [Fig. 1(a)] [3]–[7] to appropriately condition the available solar power for feeding into the grid. While the first stage is used to boost the PV array voltage and track the maximum solar power, the second stage inverts this dc power into high quality ac power. Typically, the first stage comprises of a boost or buck-boost type dc–dc converter topology. Such two-stage configurations are time tested and work well, but have drawbacks such as higher part count, lower efficiency, lower reliability, higher cost and larger size. The question is whether it is possible to reduce the number of power processing stages in such systems or, in short, is it possible to realize the situation depicted in Fig. 1(b)? Two simple and straightforward solutions to this requirement could be as follows.

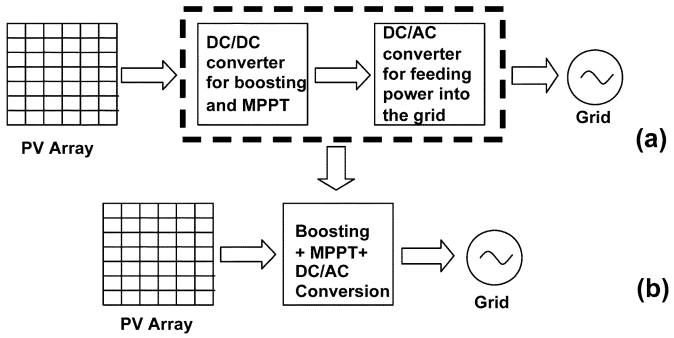


Fig. 1. Grid connected PV system topologies: (a) conventional two-stage and (b) single-stage configuration.

1) Using the conventional H-bridge inverter followed by a step-up transformer [8].
2) Using an array with sufficiently large PV voltage, which may be realized using a string of series connected modules followed by an H-bridge inverter [9], [10].

While these options are feasible, they suffer from the following drawbacks. Adding a transformer (corresponding to the grid frequency) will add to the bulk and cost of the system, besides adding losses. On the other hand, a PV array with large dc voltage suffers from drawbacks such as hot-spots during partial shading of the array, reduced safety and increased probability of leakage current through the parasitic capacitance between the panel and the system ground [11], [12]. Further, in both the options, the inverter must take care of the MPPT.

In view of the ongoing discussion, it is reasonable to conclude that the best option is to have only a single power electronic stage between the PV array and the grid to achieve all the functions—namely the electrical MPPT, boosting and inversion [Fig. 1(b)] leading to a compact system. Such compact systems are also in line with the modern day need to have highly integrated systems built into modules having high reliability, high performance (e.g., intelligence, protection, low electromagnetic interference (EMI), etc.), reduced weight and low cost [11]–[14]. Lesser is the number of (power) stages, easier is the module integration. Also, the number of devices in a power stage should also be minimized. In other words, a complete circuit optimization is required [13].

Manuscript received August 24, 2006; revised January 14, 2007. Recommended for publication by Associate Editor R. Teodorescu.

The authors are with the Applied Power Electronics Laboratory, Department of Electrical Engineering, Indian Institute of Technology-Bombay, Mumbai 400 076, India (e-mail: agarwal@ee.iitb.ac.in).

Digital Object Identifier 10.1109/TPEL.2007.904202

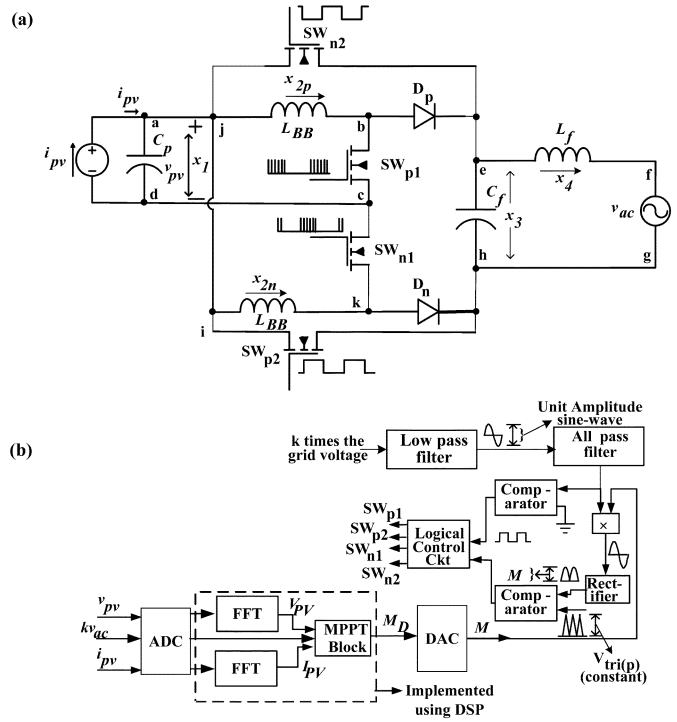


Fig. 2. Complete schematic diagram of the proposed single-stage grid connected PV system along with the control strategy. $x_1, x_2, x_3$, and $x_4$ are the state parameters. $M_D$ and $M$ denote the digital and analog equivalents respectively of the modulation index "$M$": (a) topology and (b) control scheme.

A survey conducted by the authors revealed that limited literature [15]–[19] is available related to single-stage, grid connected PV systems. There are some other configurations [20]–[22] which are not originally intended for PV applications, but can be considered for grid connected PV applications. Some of these topologies are briefly discussed in Section II of this paper.

This paper proposes a new single-stage configuration, suitable for grid connected PV or stand alone applications. The schematic diagram of the proposed topology, is shown in Fig. 2(a). Salient features of the proposed configuration are summarized as follows.

1) Better utilization of the available PV source compared to the topology proposed by Kasa *et al.* [16].
2) Proposed topology is simple, symmetrical and requires a simple sine triangle PWM control for its operation and maximum power point tracking of the PV source.
3) As the number of power devices is optimal, the system is reliable, efficient and economical.
4) Due to the very nature of the proposed topology, the PV source appears floating to the grid. This eliminates the requirement of a transformer for safety and grounding. A local earth, created for the grounding of the PV array, will suffice [12].
5) Optimal switching and conduction losses, in addition to the optimal utilization of switching devices, result in low losses and hence low cooling requirements. Only one device at a time is switched at high frequency, reducing the EMI concerns. Also number of devices conducting during any mode is optimum, resulting in minimum conduction losses apart from lowering the cost.
6) Power handling capacity of the proposed configuration is higher because for each half cycle of the grid voltage, there is a separate, dedicated inductor and switch to handle the power. Also, there are no coupled inductors or flyback transformer in the circuit for intermediate power transfer [23], [24].

## II. Survey of Single-Stage Topologies Suitable for Grid Connected PV Systems

Caceres and Barbi [20] have proposed an elegant single-stage boost cum inverter topology [Fig. 3(a)] having two boost converters operating in a complementary manner. Though, not specifically intended for PV applications, this circuit is a good candidate for a single-stage, compact grid connected PV application. However, the topology suffers from the following drawbacks. All the devices are simultaneously hard switched at high frequency, rendering the system prone to EMI problems and causing more switching losses.

Another topology, derived from the basic Zeta and Cuk configuration, has been proposed by Schekulin [15] and is shown in Fig. 3(b). This is an improved configuration as it uses minimal number of devices and does not have the drawbacks of simultaneous, high frequency operation of all the switching devices. In the positive half cycle of the grid voltage, S1 operates at high frequency while S2 and S4 are kept ON. Power transfer during this period is based on the buck-boost principle. Similarly, during the negative half cycle, S2 is operated at high frequency while S1 and S3 are kept continuously ON. Power transfer during this period follows the boost principle as source is active during both the ON and OFF intervals. This leads to asymmetrical operation of the converter in the two halves of the grid cycle, which is a major drawback of this system because it necessitates an appropriate (and probably complex) control strategy to prevent dc current injection into the grid. The main advantage of this configuration is that it has low switching losses.

Another topology proposed by Kasa *et al.*, [16], is based on a half-bridge buck-boost inverter configuration, as shown in Fig. 3(c). This configuration eliminates the drawback of asymmetrical operation during the two half cycles of a grid voltage. Again, it is a good configuration as it has minimum switching and conduction losses because only two devices are used during any half cycle of the grid voltage. Since a minimum number of switches are operated at high frequency so it has less EMI concerns and high reliability. The drawbacks with this configuration, however, are that it uses a pair of PV sources only one of which is utilized in a given half cycle of the grid voltage. High value of filter capacitor across each of these PV sources is required.

Kasa *et al.* [17] have also proposed an isolated, flyback configuration [Fig. 3(d)] which is a modification of the half bridge buck- boost topology shown in Fig. 3(c). This topology uses only three power devices and an isolation transformer. It also uses the buck-boost principle [16]. This is a good scheme, but is applicable to low power systems only, typically less than 500 W, due to the limitation on the value of primary inductance of the flyback transformer [24]. Also, there are additional losses due to the transformer, though it provides isolation between the PV and grid sides.

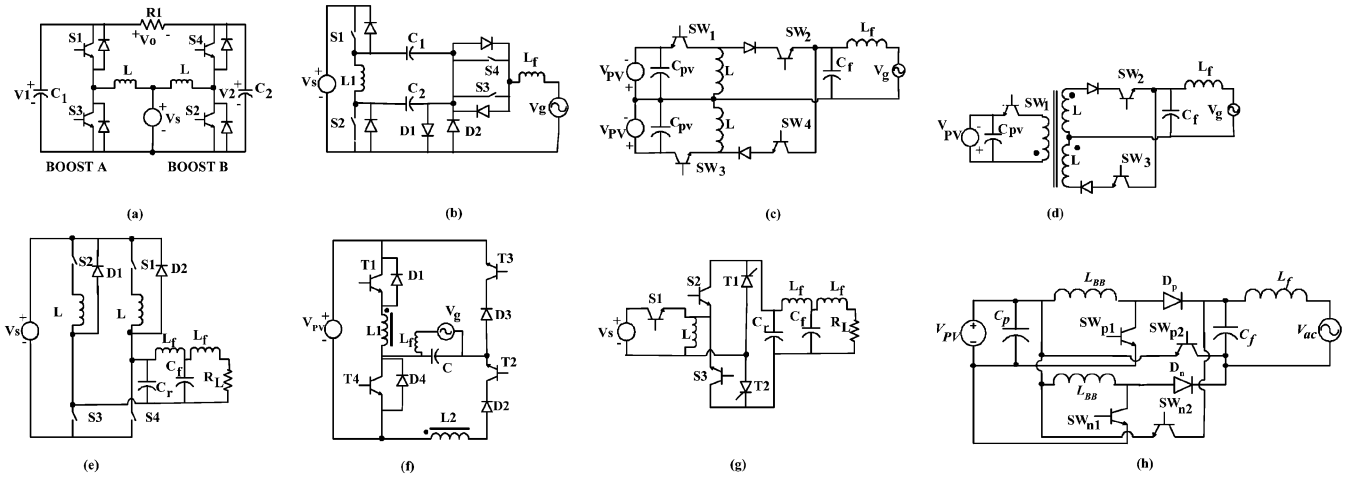


Fig. 3. (a)–(g): Schematic circuit diagrams of the various existing single-stage topologies [15]–[18], [20]–[22], [25] and (h) proposed scheme.

Wang [21] has proposed a single-stage, full bridge configuration based on the buck-boost principle as shown in Fig. 3(e). During the positive half cycle of the grid voltage, S4 operates at high frequency and S1 is kept continuously ON. The path during turn OFF is completed through S1 and D2. During the negative half cycle of the grid voltage, S3 operates at high frequency and S2 is kept continuously ON. During turn OFF, the path is completed through S2 and D1. This configuration has a large number of devices conducting at a given instant resulting in higher conduction losses.

Based on the buck-boost principle, Xue *et al.* [18] have proposed yet another single-stage grid connected PV system, as shown in Fig. 3(f). Proposed configuration uses flyback principle with mutually coupled coils during the negative half cycle of the grid voltage. The limitation of this system is that it can be used only for low power applications due to the limitation of the mutually coupled coils or flyback transformer to handle high power [24]. In addition to this, the switching and conduction losses are higher and the operation is asymmetrical in the two halves of the grid voltage cycle.

Wang [22] has proposed another single-stage configuration based on buck-boost principle as shown in Fig. 3(g). Though this configuration is not specifically intended for grid connected PV systems, it may be considered for this application. But the drawback with this configuration is that it uses five switches, with three switches operating at high frequency, leading to EMI concerns and higher switching losses.

Huang *et al.* [19] have proposed a single stage configuration for a split–phase system for PV applications, which uses a $Z$-source inverter. This configuration, which requires six switches, operating at high frequency, is recommended for high power applications.

This paper proposes a single stage topology based on buck-boost principle as shown in Fig. 3(h). During the positive half cycle of the grid voltage, $SW_{p1}$ operates at high frequency while $SW_{p2}$ is kept continuously ON. During the negative half cycle, $SW_{n1}$ is operated at high frequency while $SW_{n2}$ is kept continuously ON. As an optimum number of switches are operated at any given time, the proposed topology has the advantage of low switching and conduction losses, low EMI and low cooling requirements. The proposed topology overcomes several drawbacks of the topologies surveyed and described in this section. Working principle and all other details of this topology are presented in the following section.

## III. Proposed Topology

The proposed topology consists of two dc-to-dc, buck-boost converters connected as shown in Fig. 2. Each of these converters operates in DCM for one half cycle of the fundamental grid voltage. The resulting circuit acts as a current source inverter which feeds sinusoidal current into a low value capacitor across the grid. DCM operation helps in feeding sinusoidal current with near unity power factor (UPF) into the grid because the energy can be drawn in the form of "energy packets," whose magnitudes vary in a sinusoidal manner.

The power device $SW_{p1}$ (or $SW_{n1}$) is switched at high frequency while $SW_{p2}$ (or $SW_{n2}$) is kept continuously ON during the positive half cycle (or negative half cycle). $SW_{p1}$ (or $SW_{n1}$) is switched as per sine triangle pulse width modulation (SPWM) method. When $SW_{p1}$ is ON, energy is stored in the buck-boost inductor "$L_{\rm BB}$" by the PV source. When $SW_{p1}$ is OFF, $D_p$ (or $D_n$) gets forward biased, discharging the stored inductor energy into capacitor $C_f$ which feeds sinusoidal current into the grid. The state equations governing the operation of the proposed configuration during the positive half cycle of the grid voltage are given below. The switching control strategy implemented is also shown in Fig. 2(b). During the positive cycle the various state equations are as follows.

When power device $SW_{p1}$ is ON. Applying KCL to the nodes "a" and "e" and KVL to the loops a-b-c-d-a and e-f-g-h-e, the following state equations are obtained:

$$\begin{aligned} i_{pv} &= C_p x_1' + x_{2p}; \quad C_f x_3' + x_4 = 0; \\ x_1 &= L_{\rm BB} x_{2p}'; \quad x_3 = L_f x_4' + v_{\rm ac}. \end{aligned} \tag{1}$$

When power device $SW_{p1}$ is OFF, and diode is conducting. Applying KCL to the nodes "a" and "e" and KVL to the loops j-b-e-h-i-j and e-f-g-h-e, yields the following state equations:

$$\begin{aligned} i_{pv} &= C_p x_1'; \quad C_f x_3' + x_4 = x_{2p}; \\ -x_3 &= L_{\rm BB} x_{2p}'; \quad x_3 = L_f x_4' + v_{\rm ac}. \end{aligned} \tag{2}$$

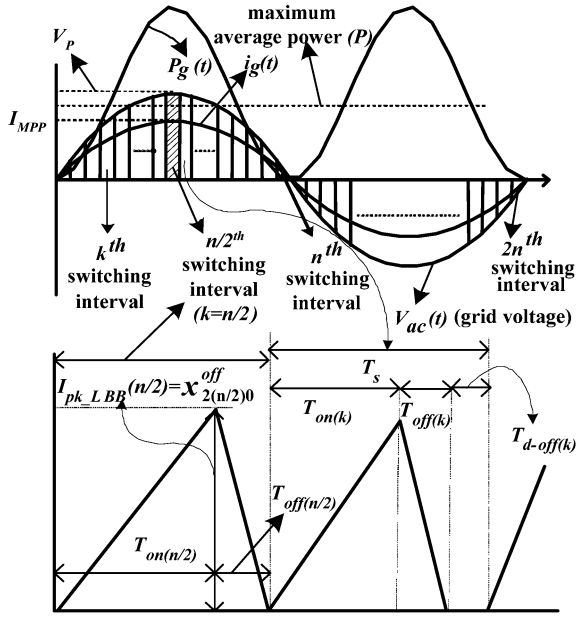


Fig. 4. Grid current and voltage waveforms considered for the analysis in discrete time domain. $k = n/2$ is the peak interval showing "Critical Conduction Mode" operation.

When power device $SW_{p1}$ is OFF, and diode is not conducting. Applying KCL to the nodes "a" and "e" and KVL to the loop e-f-g-h-e, results in the following state equations:

$$\begin{aligned} i_{pv} &= C_p x_1'; \quad C_f x_3' + x_4 = 0; \\ 0 &= L_{\rm BB} x_{2p}'; \quad x_3 = (L_f) x_4' + v_{\rm ac}. \end{aligned} \tag{3}$$

In a similar manner, state space equations can be written for negative cycle when other half of the inverter is operated. Using these state space equations, the complete PV system is simulated in MATLAB/SIMULINK software [26], [27].

## IV. Analysis of the Proposed Configuration

For analysis of the proposed configuration, the following assumptions are made.

1) Switching frequency is $2n$ times the fundamental frequency of the grid voltage.
2) Grid voltage is constant over a high frequency switching time period.
3) Value of duty cycle is constant over a high frequency switching time period.
4) DCM operation during the entire cycle of the grid voltage.
5) The PV array followed by '$C_P$' provides a dc voltage $V_{\rm PV}$ which is constant over the entire grid cycle.

In view of assumption (1), one complete cycle of grid voltage can be divided into $2n$ high switching periods [Fig. 4(a)]. For the $k$th division of the grid voltage the following expression may be written:

$$v_{ac(k)} = V_p \times \sin((\pi/n) \times k) \quad \text{[Fig. 4]}. \tag{4}$$

To feed UPF sinusoidal power into the grid, the energy, $E_{g(k)}$ that should be transferred during the $k$th switching interval is

$$E_{g(k)} = I_{MPP} \times V_p \times \sin^2((\pi/n) \times k) \times T_s \tag{5}$$

where $I_{MPP}$ is the amplitude of the current fed into the grid and is governed by the MPPT algorithm. '$T_s$' is the switching time period. Due to DCM operation, a definite amount of energy can be transferred during each switching cycle. Thus, for injecting sinusoidal current into the grid, the expression for duty ratio $D_k$, required in the $k$th switching cycle is derived as follows.

Energy drawn from the source during $k$th switching cycle

$$(E_{ik}) = \frac{V_{\rm PV}^2}{2L_{\rm BB}} D_k^2 T_s^2 \tag{6}$$

where $D_k$ is the duty ratio during the $k$th switching cycle. Equating (5) and (6) and solving for $D_k$ yields

$$D_k = \sqrt{(2V_p I_{MPP} L_{\rm BB} \sin^2(\pi k/n))/(V_{\rm PV}^2 T_s)}. \tag{7}$$

Writing (7) in continuous time domain yields an expression for the reference waveform r(t) given by

$$r(t) = \sqrt{\frac{(2V_p I_{MPP} L_{\rm BB} \sin^2(\omega t))}{(V_{\rm PV}^2 T_s)}} = M \sin(\omega t); \quad \text{where } M = \sqrt{\frac{2V_p I_{MPP} L_{\rm BB}}{(V_{\rm PV}^2 T_s)}} \tag{8}$$

where "$M$" is the modulation index determined by the MPPT algorithm. Thus, SPWM technique can be used to feed sinusoidal current into the grid with no voltage distortion. Using assumption (3), the duty ratio for the $k$th switching interval is given by

$$T_{{\rm on}(k)} = T_s \times M \times \sin((\pi/n) \times k). \tag{9}$$

The following notations are followed in the subsequent analysis.

$x_i(t_k^j)$ denotes the $i$th state variable as a function of time $t_k^j$ where "$j$" denotes the subinterval "on," "off" or "$d$-off" of the $k$th interval as shown in Fig. 4.

$x_{i(k)0}^j$ denotes the initial value of the $i$th state variable at the start of the subinterval "$j$" of the $k$th interval.

The following approximations regarding the initial values of state parameters $x_4$ and $x_3$ at the start of the ON period of the $k$th switching interval, represented by $x_{4(k)0}^{\rm on}$ and $x_{3(k)0}^{\rm on}$, respectively, can be made

$$\begin{aligned} x_{4(k)0}^{\rm on} &= I_{MPP} \sin((\pi/n)k); \\ x_{3(k)0}^{\rm on} &= V_p \sin((\pi/n)k). \end{aligned} \tag{10}$$

When switch $SW_{p1}$ is turned ON, the state equations governing the circuits in Fig. 2 are

$$\begin{aligned} V_{\rm PV} &= L_{\rm BB} x_2'; \quad C_f x_3' + x_4 = 0; \\ x_3 &= L_f x_4' + v_{ac(k)} \quad 0 \le t_k^{\rm on} \le T_{{\rm on}(k)}. \end{aligned} \tag{11}$$

Solving the differential (11) during the ON period ($0 \le t_k^{\rm on} \le T_{{\rm on}(k)}$) of the $k$th switching interval using the initial condition (10), yields (12), shown at the bottom of the next page, where $\omega_{\rm on} = 1/\sqrt{L_f C_f}$. Initial value of the state parameters for the OFF interval are the final value of the parameters during ON interval are obtained by substituting $t_k^{\rm on} = T_{{\rm on}(k)}$ [Fig. 4] in (12). When switch $SW_{p1}$ is turned OFF, and the diode is conducting, the governing state equations are

$$\begin{aligned} -x_3 &= L_{\rm BB} x_2'; \quad C_f x_3' + x_4 = x_2; \\ x_3 &= L_f x_4' + v_{ac(k)} \quad 0 < t_k^{\rm off} \le T_{{\rm off}(k)}. \end{aligned} \tag{13}$$

The differential (13) lead to the following solutions during the OFF period ($(0 < t_k^{\text{off}} \le T_{\text{off}(k)})$) of the $k$th switching interval

$$\begin{aligned} x_2\left(t_k^{\text{off}}\right) &= \frac{x_{4(k)0}^{\text{off}}}{\omega_{\text{off}}^2 L_{\text{BB}} C_f}\left(1-\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad - \frac{x_{3(k)0}^{\text{off}}}{\omega_{\text{off}} L_{\text{BB}}}\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right) \\ &\quad - \frac{v_{ac(k)}}{L_{\text{BB}}+L_f}\left(t_k^{\text{off}} - \frac{\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right)}{\omega_{\text{off}}}\right) \\ &\quad + \frac{x_{2(k)0}^{\text{off}}}{\omega_{\text{off}}^2 L_f C_f}\left(1-\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad + x_{2(k)0}^{\text{off}}\left(\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \end{aligned} \tag{14}$$

$$\begin{aligned} x_3\left(t_k^{\text{off}}\right) &= \frac{x_{2(k)0}^{\text{off}}}{\omega_{\text{off}} C_f}\left(\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad - \frac{x_{4(k)0}^{\text{off}}}{\omega_{\text{off}} C_f}\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right) \\ &\quad + \frac{v_{ac(k)}}{\omega_{\text{off}}^2 L_f C_f}\left(1-\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad + x_{3(k)0}^{\text{off}}\left(\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \end{aligned} \tag{15}$$

$$\begin{aligned} x_4\left(t_k^{\text{off}}\right) &= \frac{L_f x_{4(k)0}^{\text{off}} + L_{\text{BB}} x_{2(k)0}^{\text{off}}}{l_{\text{BB}}+L_f}\left(1-\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad - \frac{v_{ac(k)}}{L_{\text{BB}}+L_f}\left(t_k^{\text{off}} - \frac{\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right)}{\omega_{\text{off}}}\right) \\ &\quad + \frac{x_{3(k)0}^{\text{off}}}{\omega_{\text{off}} L_f}\left(\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \\ &\quad + x_{4(k)0}^{\text{off}}\cos\left(\omega_{\text{off}} t_k^{\text{off}}\right) \\ &\quad - \frac{v_{ac(k)}}{\omega_{\text{off}} L_f}\left(\sin\left(\omega_{\text{off}} t_k^{\text{off}}\right)\right) \end{aligned} \tag{16}$$

where $\omega_{\text{off}} = \sqrt{(L_{\text{BB}}+L_f)/(L_{\text{BB}} L_f C_f)}$. The OFF interval $(0 < t_k^{\text{off}} \le T_{\text{off}(k)})$ [Fig. 4] can be determined using the fact that the average voltage across $L_{\text{BB}}$ over a switching period is zero. Noting that the average voltage across $C_f$ during $T_{\text{off}(k)}$ is equal to the grid voltage during $k$th switching interval, yields the following:

$$\begin{aligned} &V_{\text{PV}} T_{\text{on}(k)} - v_{ac(k)} T_{\text{off}(k)} = 0 \\ &\qquad \Rightarrow T_{\text{off}(k)} = (V_{\text{PV}} T_{\text{on}(k)})/(v_{ac(k)}). \end{aligned} \tag{17}$$

Substituting the value of $T_{\text{off}(k)}$ from (17) in (14)–(16), yields the initial values of the state variables for the subsequent freewheeling state. When the switch $SW_{p1}$ is turned OFF, and the diode $D_p$ is not conducting ($t_k^{d-\text{off}}$), the governing state equations are

$$\begin{aligned} &0 = L_{\text{BB}} x_2'; \quad C_f x_3' + x_4 = 0; \\ &x_3 = L_f x_4' + v_{ac(k)} \quad 0 \le t_k^{d-\text{off}} \le T_{d-\text{off}(k)}. \end{aligned} \tag{18}$$

Solution of (18) is similar to the one obtained for turn ON condition of $SW_{p1}$ except for $x_2$ which is zero during the freewheeling interval ($T_{d-\text{off}(k)}$)

$$T_{d-\text{off}(k)} = T_s - \left(T_{\text{on}(k)} + T_{\text{off}(k)}\right). \tag{19}$$

Substituting the value of $T_{d-\text{off}(k)}$ in the solution of (19) gives the value of state variables at the end of the $k$th switching cycle which are also the initial values of the subsequent switching cycle.

### A. Peak Values of State Parameters

As maximum device stress and losses occur near $V_p$, the high frequency switching interval closest to $V_p$ (peak interval, $k = (n/2)$, Fig. 4) is considered for analysis i.e., $k \approx n/2$, (where $n$ is an odd integer). Substituting $k = n/2$ in (4), (9) and (10), we have

$$\begin{aligned} &V_{ac(n/2)} = V_p; \quad T_{\text{on}(n/2)} = MT_s; \\ &x_{4(n/2)0}^{\text{on}} = I_{MPP}; \quad x_{3(n/2)0}^{\text{on}} = V_p. \end{aligned} \tag{20}$$

Peak values of the various state variables in this switching interval are

$$\begin{aligned} &I_{pk\_L_{\text{BB}}}(n/2) \\ &\quad = x_{2(n/2)0}^{\text{off}} = \left(\frac{V_{\text{PV}}}{L_{\text{BB}}}\right) MT_s \end{aligned} \tag{21}$$

$$\begin{aligned} &V_{pk\_c_f}(n/2) \\ &\quad = x_3\left(T_{\text{off}(n/2)}\right) \\ &\quad = \frac{V_{\text{PV}} MT_s}{L_{\text{BB}}\omega_{\text{off}} C_f}\left(\sin\left(\omega_{\text{off}} T_{\text{off}(n/2)}\right)\right) \\ &\qquad + \frac{V_p}{(L_{\text{BB}}+L_f)}\left(L_{\text{BB}} + \left(\cos\left(\omega_{\text{off}} T_{\text{off}(n/2)}\right)\right) L_f\right) \ldots \\ &\qquad - \frac{I_{MPP}}{(2C_f)}\left(\sin\left(\omega_{\text{off}} T_{\text{off}(n/2)} + \omega_{\text{on}} MT_s\right)\right. \\ &\qquad \times \left(\frac{1}{\omega_{\text{on}}} + \frac{1}{\omega_{\text{off}}}\right) + \sin\left(\omega_{\text{off}} T_{\text{off}(n/2)}\right. \\ &\qquad \left.\left. -\omega_{\text{on}} MT_s\right)\left(\frac{1}{\omega_{\text{on}}} - \frac{1}{\omega_{\text{off}}}\right)\right) \end{aligned} \tag{22}$$

$$\left.\begin{aligned} x_2\left(t_k^{\text{on}}\right) &= \frac{V_{\text{PV}}}{L_{\text{BB}}} t_k^{\text{on}} \\ x_3\left(t_k^{\text{on}}\right) &= \frac{-x_{4(k)0}^{\text{on}}}{\omega_{\text{on}} C_f}\sin\left(\omega_{\text{on}} t_k^{\text{on}}\right) + x_{3(k)0}^{\text{on}}\cos\left(\omega_{\text{on}} t_k^{\text{on}}\right) + v_{ac(k)}\left(1-\cos\left(\omega_{\text{on}} t_k^{\text{on}}\right)\right) \\ x_4\left(t_k^{\text{on}}\right) &= \frac{x_{3(k)0}^{\text{on}}}{\omega_{\text{on}} L_f}\sin\left(\omega_{\text{on}} t_k^{\text{on}}\right) + x_{4(k)0}^{\text{on}}\cos\left(\omega_{\text{on}} t_k^{\text{on}}\right) - \frac{v_{ac(k)}}{\omega_{\text{on}} L_f}\left(\sin\left(\omega_{\text{on}} t_k^{\text{on}}\right)\right) \end{aligned}\right\} \tag{12}$$

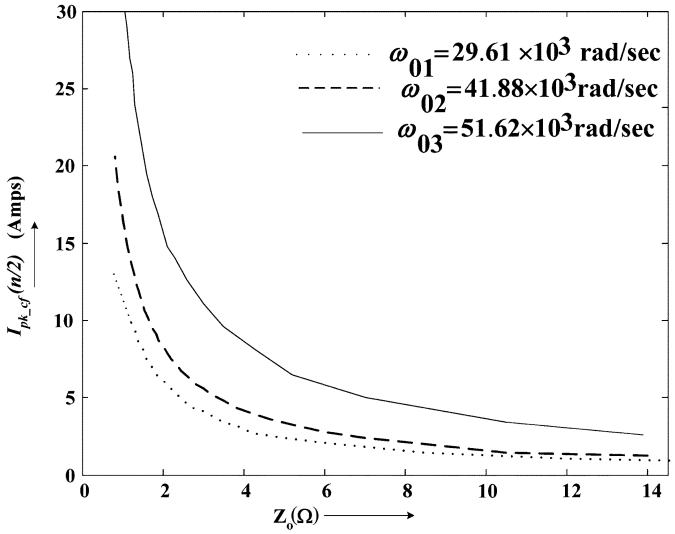


Fig. 5. Plot of $I_{pk\_g}(n/2)$ versus $z_o$ with $\omega_o$ as the parameter.

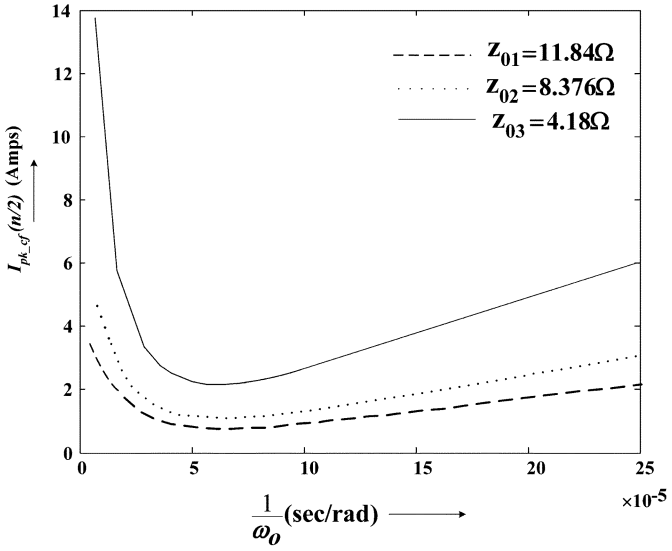


Fig. 6. Plots of $I_{pk\_g}(n/2)$ versus $(1/\omega_o)$ with $z_o$ as the parameter.

$$
\begin{aligned}
&I_{pk\_g}(n/2)\\
&\quad = x_4(T_{\text{off}(n/2)})\\
&\quad = \frac{V_{\text{PV}}MT_s}{L_{\text{BB}}+L_f}\left(1-\cos\left(\omega_{\text{off}}T_{\text{off}(n/2)}\right)\right)\\
&\qquad - \frac{V_p}{(L_{\text{BB}}+L_f)}\left(T_{\text{off}(n/2)}\right.\\
&\qquad - \left.\left(\left(\sin\left(\omega_{\text{off}}T_{\text{off}(n/2)}\right)\right)/\left(\omega_{\text{off}}\right)\right)\right)\\
&\qquad + I_{MPP}\left(\cos\left(\omega_{\text{on}}MT_s\right)\right.\\
&\qquad \times \left.\cos\left(\omega_{\text{off}}T_{\text{off}(n/2)}\right)\right)\left(L_{\text{BB}}/(L_{\text{BB}}+L_f)\right)\\
&\qquad - \sqrt{\frac{L_{\text{BB}}}{(L_{\text{BB}}+L_f)}}\sin(\omega_{\text{on}}MT_s)\sin\left(\omega_{\text{off}}T_{\text{off}(n/2)}\right)\\
&\qquad + \left(\cos(\omega_{\text{on}}MT_s)\left(\frac{L_{\text{BB}}}{(L_{\text{BB}}+L_f)}\right)\right) \qquad (23)
\end{aligned}
$$

where $I_{pk\_LBB}(n/2), V_{pk\_c_f}(n/2)$ and $I_{pk\_g}(n/2)$ are the peak values of the current in $L_{\text{BB}}$, voltage across $C_f$ and the current in $L_f$ respectively during $n/2$th interval. Value of $T_{\text{off}(n/2)}$ can be obtained by substituting (20) in (17), which yields

$$T_{\text{off}(n/2)} = ((V_{\text{PV}}MTs)/(V_p)). \qquad (24)$$

It is observed that $V_{pk\_c_f}(n/2)$ and $I_{pk\_g}(n/2)$ depend on the characteristic impedance $(z_o = \sqrt{(L_{\text{BB}})/(C_f)})$ and the resonant angular frequency $(\omega_o = \sqrt{(1)/(L_{\text{BB}} \times C_f)})$ of the circuit. Plots showing the variation of $V_{pk\_c_f}(n/2)$ and $I_{pk\_g}(n/2)$ with respect to $z_o$ and $\omega_o$ are shown in Figs. 5–8. These plots are useful for optimizing the design of the proposed converter.

### *B. Condition for DCM*

The proposed topology operates in DCM through out the grid cycle if it sustains DCM operation during the peak interval. Applying the condition for Critical Conduction Mode or DCM during interval $k = (n/2)$ yields

$$
\begin{aligned}
&T_{\text{off}(n/2)} + T_{\text{on}(n/2)} \le T_s \Rightarrow MT_s\\
&\qquad + ((V_{\text{PV}}MT_s)/(V_p)) \le T_s. \qquad (25)
\end{aligned}
$$

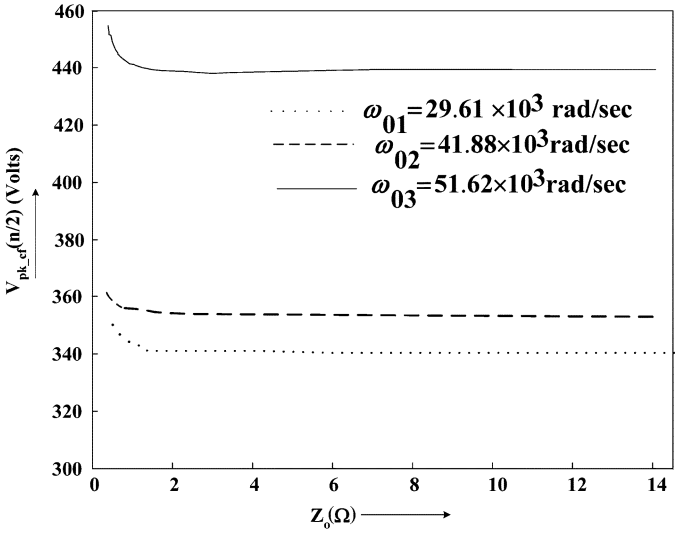


Fig. 7. Plot of $V_{pk\_c_f}(n/2)$ versus $z_o$ with $\omega_o$ as the parameter.

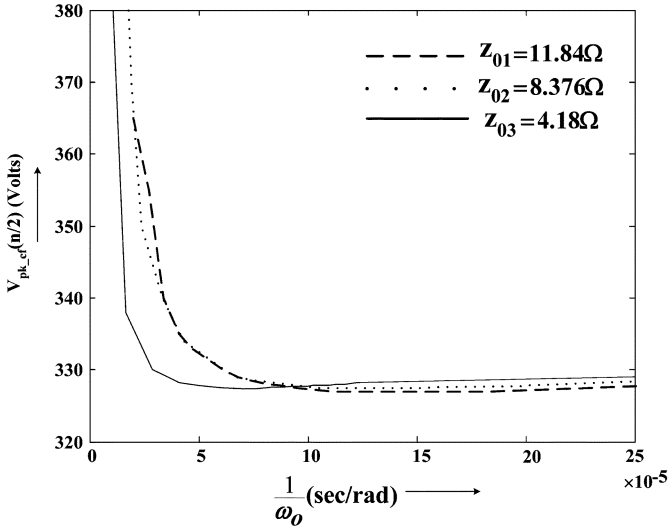


Fig. 8. Plot of $V_{pk\_c_f}(n/2)$ versus $(1/\omega_o)$ with $z_o$ as the parameter.

This leads to the condition for DCM operation of the system

$$M \leq \frac{1}{(1+V_{\rm PV}/V_p)}. \tag{26}$$

### C. Rating of Power Devices and Losses

Maximum instantaneous current rating of any power device in the circuit is determined by peak inductor current

$$I_{\rm rated} = I_{pk\_L_{\rm BB}}(n/2). \tag{27}$$

Also, root mean square value of the current through switch $SW_{p1}$ (or $SW_{n1}$) over half cycle of the grid voltage is given by

$$\begin{aligned} I_{\rm rms(SW_{p1})} &= \sqrt{\frac{1}{2\times n}\times\sum_{k=0}^{n}\frac{1}{T_s}\times\int_0^{T_{{\rm on}(k)}}\left(\frac{V_{\rm PV}\times t_k^{\rm on}}{L_{\rm BB}}\right)^2 dt_k^{\rm on}} \\ &= \frac{(2)^{1/2}\times V_{\rm PV}\times T_s\times(M)^{3/2}}{3\times L_{\rm BB}\times(\pi)^{1/2}}. \end{aligned} \tag{28}$$

Similarly, the root mean square current through switch $SW_{p2}$ (or $SW_{n2}$) over half cycle of the grid voltage is seen in (29), shown at the bottom of the page. The maximum voltage stress or the required forward blocking voltage $(V_{\rm FBV})$ of $SW_{p1}$ (or $SW_{n1}$) is given by

$$V_{\rm FBV} = V_{\rm PV} + V_d + V_{pk\_c_f}(n/2) \tag{30}$$

where $V_d$ is the voltage drop across the diode $D_p$ (or $D_n$). Similarly, the maximum voltage stress or the required reverse blocking voltage $(V_{\rm RBV})$ of $D_p$ (or $D_n$) is given by

$$V_{\rm RBV} = V_{pk\_c_f}(n/2). \tag{31}$$

### D. Design of Inductor $L_{\rm BB}$ and Capacitor $C_f$ [Figs. 2 and 4]

The buck-boost inductor, '$L_{\rm BB}$' acts as an energy storage element, which stores energy from the PV source and transfers it to the grid through capacitor $C_f$. The maximum energy is transferred during the peak interval, $k_{(n/2)}$ [Fig. 4] when PV is delivering rated power "$P$" W. If "Critical Conduction Mode" or DCM operation is ensured during this interval, DCM operation is guaranteed throughout the grid cycle and for all environmental conditions. Thus, design of $L_{\rm BB}$ is critical for proper operation of the converter. If the PV system can deliver a maximum dc power of "$P$" W, inductor $L_{\rm BB}$ should have a power handling capacity of "$2P$" W. This will ensure transfer of average power "$P$" W, into the grid. As the proposed SSGC configuration operates in DCM, it transfers energy in the form of packets during each switching interval to feed high quality sinusoidal power into the grid. Also, during each switching interval, the energy stored in the inductor is completely transferred to capacitor '$C_f$' connected across the grid. Thus, near the peak of the fundamental cycle of the grid voltage, energy transferred into the grid during $(n/2)$ switching interval is given by

$$E_{g\left(\frac{n}{2}\right)} = V_p \times I_{MPP} \times T_s. \tag{32}$$

This is two times the average energy $(=(V_p\times I_{MPP}\times T_s)/(2))$ transferred into the grid. Thus, inductor must be capable of handling twice the average energy fed into the grid. The maximum energy is transferred during the peak interval (when $k=(n/2)$) [Fig. 4]. Due to the "Critical Conduction Mode" operation during the peak interval, the following equations holds:

$$\frac{1}{2}\times L_{\rm BB}\times I^2_{pk\_L_{\rm BB}}(n/2) = 2\times P\times T_s. \tag{33}$$

Also from Fig. 4 considering $n/2$th interval yields

$$I_{pk\_L_{\rm BB}}(n/2)\times L_{\rm BB} = V_{\rm PV}\times T_{{\rm on}(n/2)} = V_p \times T_{{\rm off}(n/2)}. \tag{34}$$

Using (34) in (33), with $T_s = T_{{\rm off}(n/2)} + T_{{\rm on}(n/2)}$ and noting that $V_{\rm PV}/V_p$ <1 but positive, (33) can be simplified to give

$$L_{\rm BB} < \left(V^2_{\rm PV}\times T_s\right)/(4\times P). \tag{35}$$

Also, using (33) in (26) yields

$$L_{\rm BB} \leq \left(V^2_{\rm PV}\times M^2\times T_s\right)/(4\times P). \tag{36}$$

Combining (35) and (36)

$$L_{\rm BB} \leq \frac{(V^2_{\rm PV}\times M^2\times T_s)}{(4\times P)}. \tag{37}$$

The design value $L_{\rm BB}$ is chosen in such a way that the maximum value of '$M$' satisfies conditions (26) and (37) when the PV source is delivering rated power. This condition helps in ensuring DCM operation of the proposed configuration at any operating point under all environmental conditions.

To determine the value of $C_f$, the energy stored in the inductor $L_{\rm BB}$ during the ON interval can be equated to the change in capacitor energy during the OFF interval, resulting in the following expression:

$$C_f = \frac{\left(L_{\rm BB}\times I^2_{pk\_L_{\rm BB}}\right)}{4\times V_p\times\Delta V} \tag{38}$$

where $\Delta V$ is the ripple in the capacitor voltage.

$$\begin{aligned} I_{\rm rms(SW_{p2})} &= \sqrt{\frac{1}{2\times n}\times\sum_{k=0}^{n}\frac{1}{T_s}\times\int_0^{T_{{\rm off}(k)}}\left(\frac{-v_{ac(k)}\times t_k^{\rm off}+V_{\rm PV}\times T_{{\rm on}(k)}}{L_{\rm BB}}\right)^2 dt_k^{\rm off}} \\ &= \frac{(V_{\rm PV})^{3/2}\times T_s\times(M)^{3/2}}{L_{\rm BB}\times(12\times V_p)^{1/2}} \end{aligned} \tag{29}$$

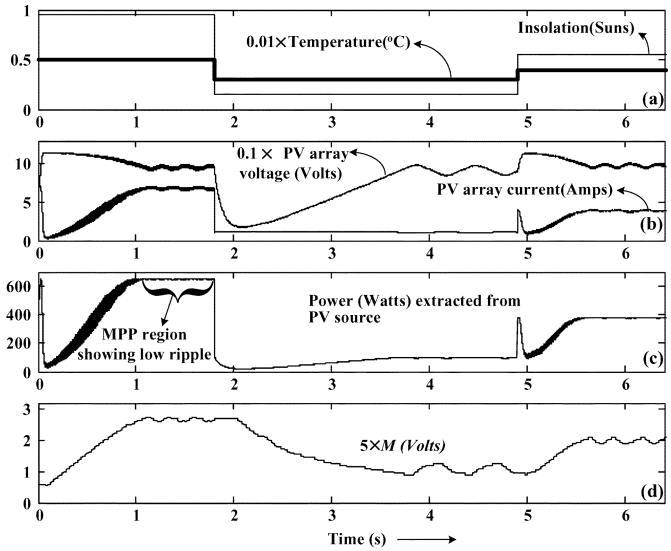


Fig. 9. MATLAB/SIMULINK simulation results of the proposed topology on the PV side. Subplot (d) shows the variation in the modulation index of the SPWM. The carrier (triangular) waveform has amplitude of 5 V.

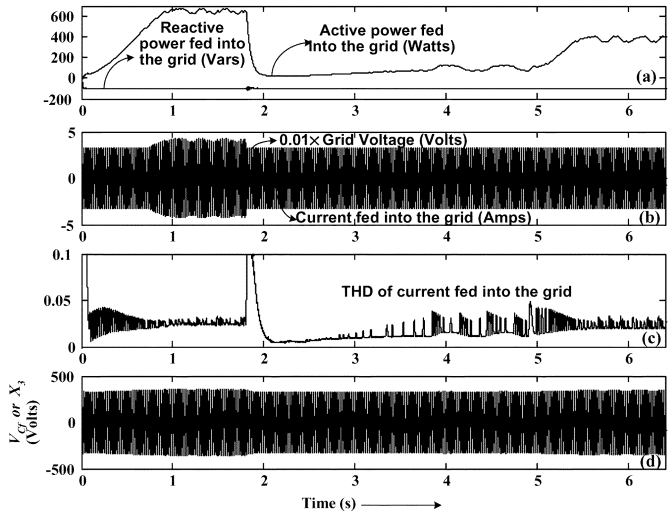


Fig. 10. MATLAB/SIMULINK simulation results of the proposed topology on the grid side.

*Design of $L_f$:* $L_f$ is the filter inductor which filters the high switching frequency component present in the current waveform fed into the grid. For design, it requires the cut off frequency $(f_c)$ to be lesser than the switching frequency $(f_s)$. Thus, the design value of $L_f$ *is* given by

$$L_f = \frac{1}{(2 \times \pi \times f_c)^2 \times C_f}. \tag{39}$$

*Design value of $C_p$:* $C_p$ acts as a buffer between the PV source and the proposed SSGC PV configuration. Value of $C_p$ decides the maximum amplitude of ripple in the voltage of the PV array. Let $\Delta v_{\rm PV}$ be the maximum value of the allowed ripple in the PV voltage and $f_g$ be the frequency of the fundamental cycle of the grid voltage, then the design value of $C_p$ is given by [7]

$$C_p = \frac{2 \times P}{4 \times (2 \times \pi \times f_g) \times V_{\rm PV} \times \Delta v_{\rm PV}}. \tag{40}$$

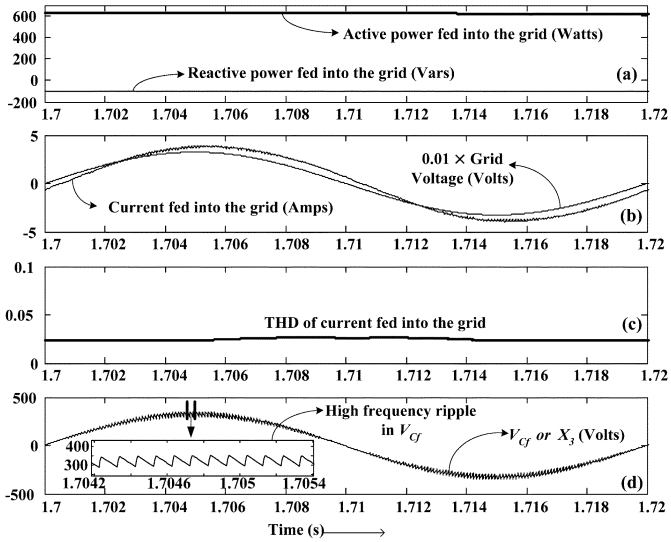


Fig. 11. Magnified view of Fig. 10. The subplot inset plot (d) shows the high frequency switching ripple in $V_{\rm Cf}$.

TABLE I
PARAMETERS USED IN THE SIMULATION OF THE PROPOSED CONFIGURATION

| Circuit Parameter | $C_p$ | $L_{BB}$ | $C_f$ | $L_f$ | $T_s$ | $V_p$ |
|---|---|---|---|---|---|---|
| Value | ≈3000μF | 150μH | 4.3μF | 3.6mH | 100μs | 325V |

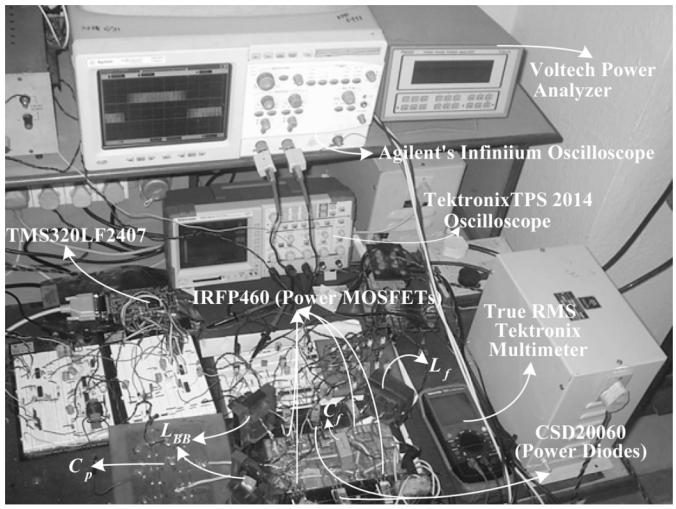


Fig. 12. Photograph of the experimental setup used for testing the proposed configuration.

## V. MAXIMUM POWER POINT TRACKING

"Hill climbing" or the "perturb and observe method" [1] has been used to track the maximum power point (MPP) of the PV source. This algorithm has been appropriately implemented in conjunction with the grid connected dc/ac configuration proposed in the paper.

Sine-triangle comparison technique is used to ensure that near-sinusoidal currents are fed into the grid. As inverter is feeding sinusoidal power into the grid, the second harmonic power is reflected on the PV source side. This appears in the current and voltage waveforms of the PV source. Therefore, to avoid wrong decisions, the MPPT algorithm uses average

TABLE II
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

| Circuit Parameter | $C_p$ | $L_{BB}$ | $C_f$ | $L_f$ | $T_s$ | $V_p$ | $V_{PV(MPP)}$* |
|---|---|---|---|---|---|---|---|
| Value | 2000μF | ≈ 220μH | 4.4μF | 3.25mH | 100μs | ≈ 150V | ≈ 85V |

TABLE III
RMS AND PEAK VALUES OF THE CURRENT AND VOLTAGES HANDLED BY THE VARIOUS COMPONENTS AND DEVICES

| Components | RMS current | RMS value of forward (F)or reverse ( R ) blocking voltage | Peak current | Peak value of forward (F)or reverse (R ) blocking voltage |
|---|---|---|---|---|
| $SW_{p1}$ and $SW_{n1}$ | ≈ 4.8A | ≈ 340V (F) | ≈ 23A | ≈ 440 (F) |
| $SW_{p2}$ and $SW_{n2}$ | ≈2.7A | - | ≈ 23A | - |
| $D_p$ and $D_n$ | ≈2.7A | ≈230.3V (R ) | ≈ 23A | ≈ 340V(R ) |

values of the PV array current $(I_{\rm pv})$ and voltage $(V_{\rm pv})$. These average values are obtained by using FFT block set in the SIMULINK software. In hardware, this is implemented using the DSP. Fig. 2(b) shows the complete control scheme implemented in software and hardware. The amplitude $(I_{MPP})$ of the sinusoidal reference signal, is governed by the MPPT algorithm and is updated (only) at the beginning of every fundamental cycle of grid voltage to avoid dc current injection into the grid. As $I_{MPP}$ varies, the magnitude of "$M$" varies and hence, the widths of the SPWM pulses vary. The string of pulses, whose widths vary in a sinusoidal manner, gets uniformly scaled upwards or downwards depending upon whether $M$ is increasing or decreasing. The maximum value of "$M$" is set by (26) and the minimum value is decided by the minimum amount of power to be transferred.

## VI. SIMULATION AND EXPERIMENTAL RESULTS OF THE PROPOSED INVERTER TOPOLOGY

The proposed inverter topology was simulated in MATLAB/SIMULINK software [26], using the PV model proposed by Walker [27]. The important waveforms corresponding to the PV and grid sides, obtained with computer simulations, are shown in Figs. 9 and 10, respectively. MPPT, as discussed in the previous section, was also incorporated in computer simulations. Tracking of maximum power for different environmental conditions is confirmed by the low ripple content in the PV power output around MPP as shown in Fig. 9. In Fig. 9, when there is a step change in insolation from 0.9 to 0.1 Suns, the operating voltage shifts to the current source region. The MPP algorithm then, decreases the value of "$M$" which increases the operating voltage of the array, approaching MPP. The variation of modulation index "$M$," as the MPP is tracked, is also shown in plot (d). Fig. 10 shows the plots of capacitor voltage ($x_3$ or $V_{\rm Cf}$) and total harmonic distortion (THD) of the current fed into the grid. In general, the grid current THD under different environmental conditions, remains with in 5%. Fig. 11 shows the magnified view of Fig. 10 for one fundamental cycle of the grid voltage. It also shows the high frequency switching ripple present in the capacitor voltage.

Calculations of the design parameters for a PV array voltage $(V_{\rm PV}) = 90$ V and peak grid voltage $(V_p) = 325$ V are shown in the following.

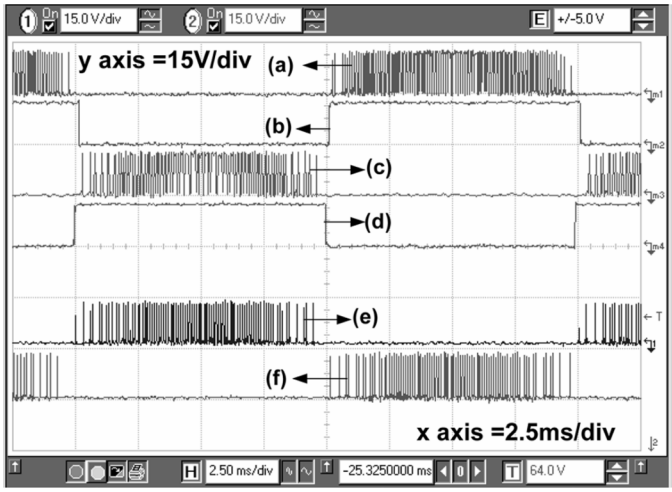


Fig. 13. Experimental waveforms of the switching pulses at the gates of controllable switches: Plot (a): $SW_{p1}$ for $M = 76.5\%$; Plot (b): $SW_{p2}$; Plot (c): $SW_{n1}$ for $M = 76.5\%$; Plot (d) $SW_{n2}$; Plot (e): $SW_{p1}$ for $M = 20\%$; Plot (f) $SW_{n1}$ for $M = 20\%$ [Plots (b) and (d) are independent of $M$].

Using (26), the value of "$M$" is given by

$$M \le \frac{1}{(1 + V_{\rm PV}/V_p)} \Rightarrow M \le 78.3. \tag{41}$$

Using (37), the value of buck-boost inductor for 700 W PV power is given by

$$L_{\rm BB} \le \frac{\left(V_{\rm PV}^2 \times M^2 \times T_s\right)}{(4 \times P)} \Rightarrow L_{\rm BB} \le 176\mu H \quad \text{where } T_s \text{ is } 100\ \mu\text{s}\ (f_s = 10\ \text{kHz}). \tag{42}$$

Thus, 176 $\mu$H is the critical value. In simulations, a lower value of $L_{\rm BB}$ was used to avoid CCM operation for power greater than the rated power. At the same time, precaution was taken not to use too low a value of $L_{\rm BB}$ (i.e., much lower than its critical value) to avoid high current stress and losses. With all these considerations, $L_{\rm BB} = 150\ \mu$H was chosen as an overall good compromise value. Taking capacitor voltage ripple, $\Delta V =$ 50 V, the value of $C_f$ is given by

$$C_f = \frac{\left(L_{\rm BB} \times I_{pk\_L_{\rm BB}}^2\right)}{4 \times V_p \times \Delta V} \Rightarrow C_f = 4.3\ \mu F. \tag{43}$$

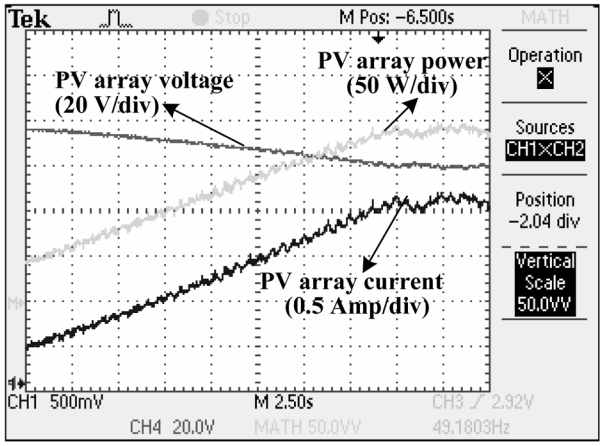


Fig. 14. Experimental results showing MPP tracking using the conventional hill climbing method. Horizontal x axis has a time scale of 2.5 s/div.

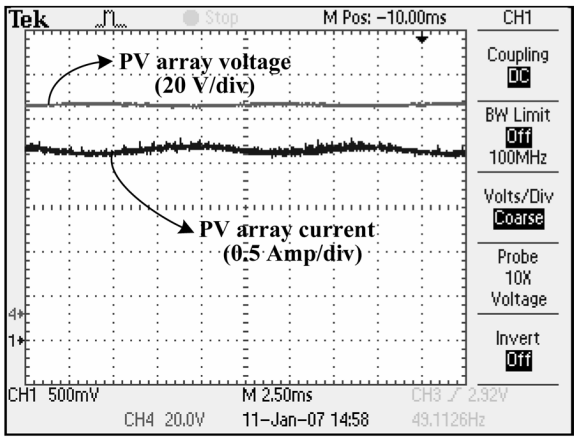


Fig. 15. Experimental waveforms of the input current and voltage (on the PV side). Horizontal $x$ axis has a time scale of 2.5 ms/div.

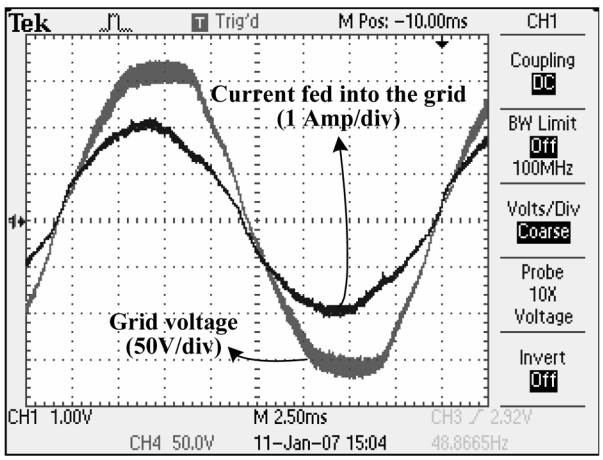


Fig. 16. Experimental waveforms of the current fed into the grid and the grid voltage. Horizontal $x$ axis has a time scale of 2.5 ms/div.

Similarly, other parameters can be calculated using (39) and (40). Table I shows the values of the parameters used in the simulation of the proposed single stage configuration.

A 300-W experimental prototype was built in the laboratory to verify the working of the proposed configuration. As SPWM is used, the control circuit requires grid voltage template. However, the grid voltage was found to have some distortion. Hence,

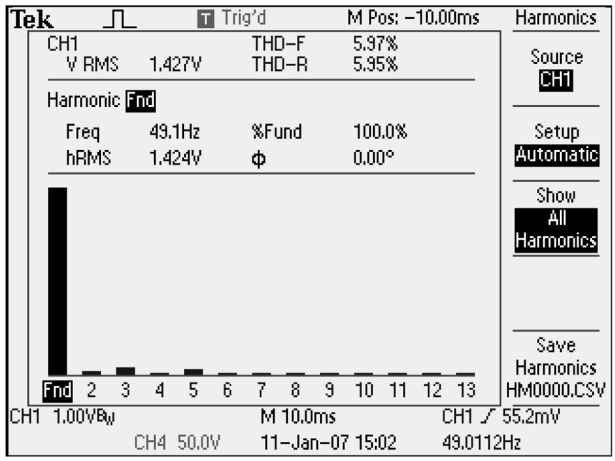


Fig. 17. FFT plots and the THD value of the grid current shown in Fig. 16, obtained using Tektronix TPS 2014 oscilloscope.

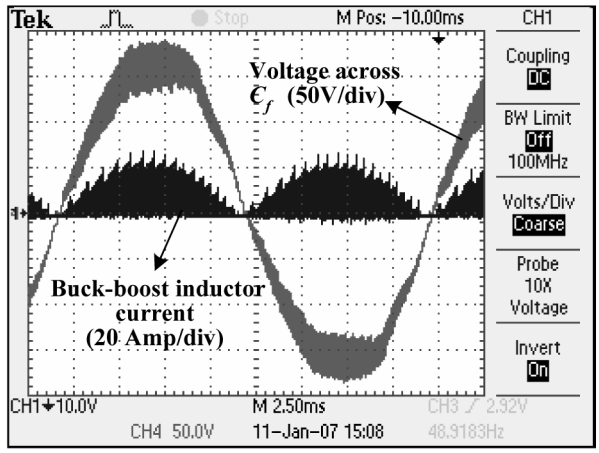


Fig. 18. Experimental waveforms of the buck-boost inductor current and filter capacitor $(C_f)$ voltage. Horizontal $x$ axis has a time scale of 2.5 ms/div.

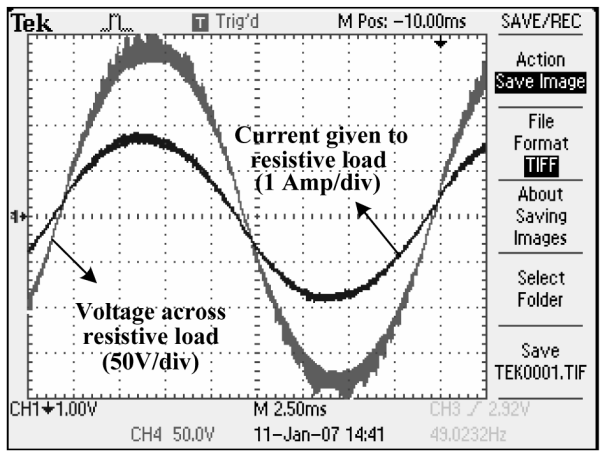


Fig. 19. Experimental results showing voltage and current waveforms across a resistive load (grid is replaced by a stand-alone resistive load).

the grid voltage must be filtered to obtain the fundamental component. Hence, the generation of sine wave (used in SPWM) is done by attenuating the sensed grid voltage and then passing it through a 'low pass' filter to render a unit amplitude pure

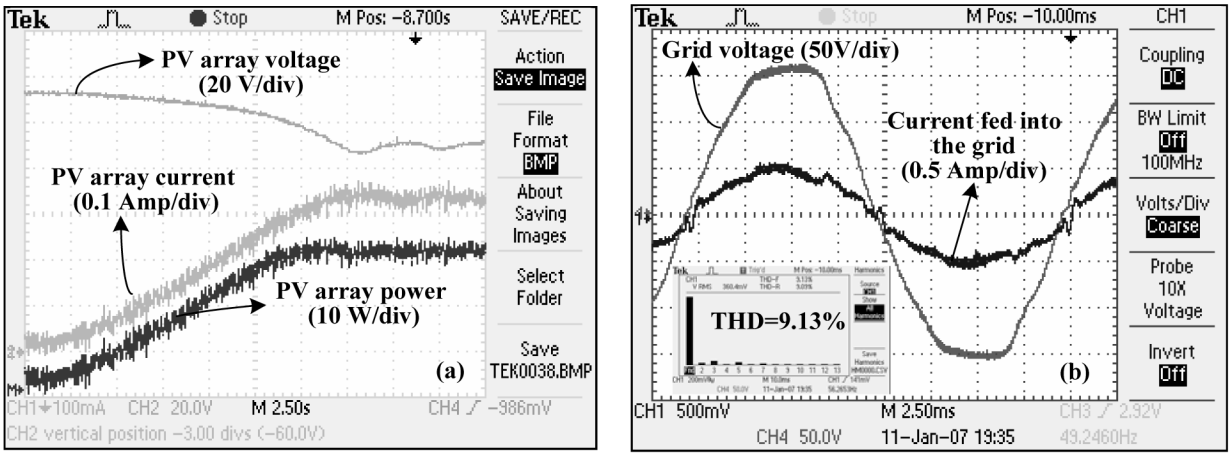


Fig. 20. Experimental plots for low insolation value (≈0.3 Suns): (a) MPP tracking plots and (b) grid current and voltage waveforms with a subplot showing the FFT and THD value of the grid current.

sine wave [Fig. 2(b)]. This waveform is then passed through an 'all-pass' filter to compensate for any phase shift.

A photograph of the experimental set up used is shown in Fig. 12. Specifications of the system are given in Table II.

Power MOSFETs (IRFP460) were used as the controllable switching devices $(SW_{p1}, SW_{p2}, SW_{n1}, SW_{n2})$. CSD20060 power diodes were used for $D_p$ and $D_n$. Grid voltage is adjusted to 150 V peak with the help of an autotransformer for the experiments. For design and selection of devices, the peak and RMS values of currents and voltages are required which were determined using expressions obtained in Section IV and verified using simulations. The RMS and peak values of the currents and voltages handled by various components and devices used in the prototype at the rated condition with $V_p = 325$ V are given in Table III.

MPPT algorithm was implemented using Texas Instruments' DSP TMS320LF2407 which computes the value of "$M$," using "hill climbing" MPPT algorithm as shown in Fig. 2. Fig. 13 shows the waveforms of the switching pulses applied to the gates of the various controllable devices in the proposed configuration obtained using Agilent's Infiniium oscilloscope (model no. 54810A). It may be noted that the density of the switching pulses (applied to $SW_{p1}$ and $SW_{n1}$) is higher for higher modulation index. Other experimental waveforms, corresponding to the power stage were obtained using Tektronix power oscilloscope TPS 2014, especially suited for such measurements. Experimental result showing MPP tracking is given in Fig. 14. Fig. 15 shows the experimental current and voltage waveforms on the PV side. Fig. 16 shows the experimental waveforms of grid voltage and the current fed into the grid. Fig. 17 shows the FFT plot and the THD value corresponding to the grid current shown in Fig. 16 while Fig. 18 shows the waveforms of the capacitor $(C_f)$ voltage and the buck-boost inductor $(L_{\rm BB})$ current. The current fed into the grid has a THD slightly higher than 5% due to the fact that the grid voltage itself is distorted which results in the distortion of the current flowing into the grid. This fact is further highlighted by Fig. 19 which shows the experimental plots obtained for a resistive load of 104 Ω (i.e., grid replaced by stand-alone resistive load). It is observed that for a resistive load, the proposed configuration feeds nearly sinusoidal current (with negligible THD).

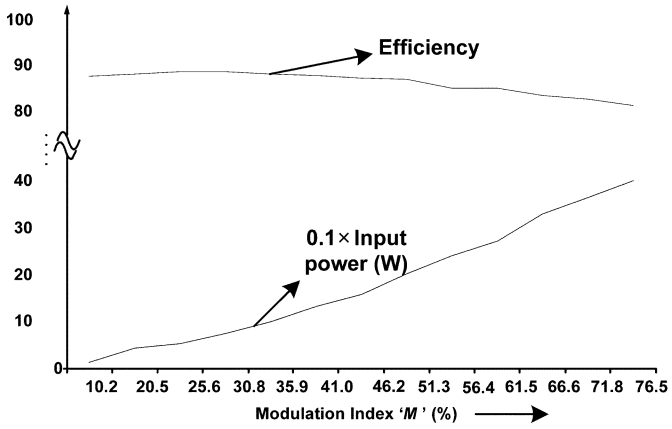


Fig. 21. Variation of efficiency and input power drawn by the proposed configuration as the modulation index "$M$" is varied.

Fig. 20(a) shows experimental plot for MPP tracking during low insolation. Fig. 20(b) shows the corresponding grid voltage and current waveforms with the grid current THD ≈9.13%. It may be noted that the THD of current fed into the grid during low insolation is significantly higher.

To determine the variation in efficiency of the proposed configuration, as it operates from low power to rated power condition, a number of experiments were performed using a resistive load of 104 Ω (in place of the grid) and by replacing the PV source by a dc source. Measurements of power on the input and output sides were made using Voltech make high bandwidth power analyzer (model PM300) and high bandwidth true RMS Tektronix multimeter's. Fig. 21 shows the experimental plot of efficiency and the input power drawn with different modulation indexes used in the SPWM. Subsequently, various other experiments were also performed by restoring back the PV source and again connecting the proposed configuration's output with the power grid for obtaining the plots of power factor and grid current THD with respect to output power fed into the grid and

TABLE IV
SUMMARY OF THE COMPARISON OF THE PROPOSED CONFIGURATION WITH EXISTING TOPOLOGIES

| Configuration | Symm-etrical | Components | | | | SW Losses | | Conduction Losses | | | | Remarks (EMI concern, power level, and cooling requirement) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | S | D | L | C | NS+ | NS – | ON | | OFF | | |
| | | | | | | | | D | S | D | S | |
| Barbi [20]* | Yes | 4 | 0 | 2 | 3 | 4 | 4 | 0 | 2 | 0 | 2 | High EMI , High Power, H igh cooling req. |
| Zeta-cuk [15] | No | 4 | 0 | 2 | 3 | 1 | 1 | 0 | 2 | 0 | 2 | Low EMI , Medium Power , Low cooling req. |
| Kasa [16] | Yes | 4 | 2 | 3 | 3 | 2 | 2 | 0 | 1 | 1 | 1 | Medium EMI , Medium Power, Medium cooling req. |
| Kasa [17] | Yes | 3 | 2 | 4 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | Medium EMI, Low Power, Medium cooling req. |
| Wang [21]* | Yes | 4 | 2 | 3 | 2 | 1 | 1 | 0 | 2 | 1 | 1 | Low EMI, Medium Power, Medium cooling req. |
| Xue [18] | No | 4 | 2 | 3 | 2 | 2 | 2 | 0 | 2 | 1 | 2 | Medium EMI, Medium Power , Medium cooling req. |
| Wang [22]* | Yes | 5 | 0 | 2 | 2 | 3 | 3 | 0 | 1 | 0 | 2 | Medium EMI, Medium Power , High cooling req. |
| Huang[19] | Yes | 6 | 1 | 5 | 5 | 6 | 6 | 1 | 6 | 1 | 6 | High EMI, High Power, High cooling req. |
| Proposed | Yes | 4 | 2 | 3 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | Low EMI, High Power, Low cooling req. |

High Power $\Rightarrow$ power $\geq$ 3kW; Medium Power $\Rightarrow$ 0.5kW $\leq$ power $\leq$ 3kW; Low Power $\Rightarrow$ power $\leq$ 0.5kW; S $\Rightarrow$ Switch; D $\Rightarrow$ Diode; L $\Rightarrow$ inductor; C $\Rightarrow$ Capacitor; NS+ and NS– $\Rightarrow$ Number of devices switching at high frequency during positive and negative half cycles of the grid voltage; Symmetrical $\Rightarrow$ whether there is symmetrical operation of the converter during the two halves of the grid voltage (asymmetrical operation may lead to DC current injection into the grid)

* This configuration is not originally intended for a grid connected application.

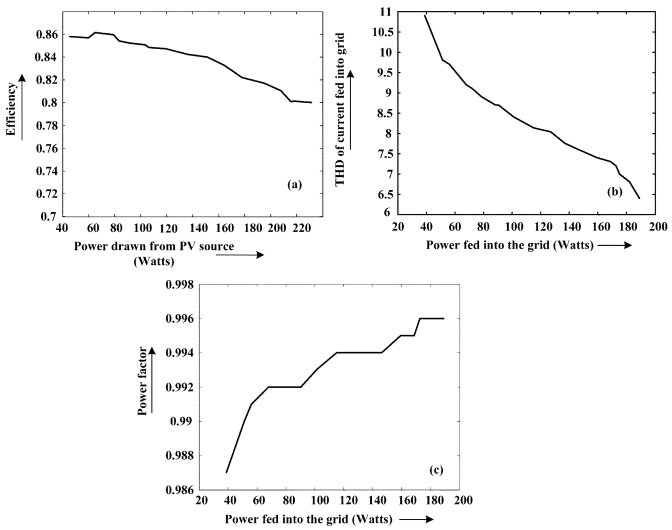


Fig. 22. Experimental plots with the PV source showing (a) efficiency versus input PV power, and (b) THD of the current versus output power fed into the grid, and (c) power factor versus power fed into the grid.

the plot of efficiency with respect to the input PV power. These plots are shown in Fig. 22.

## VII. CONCLUSION

In this work, the importance of single-stage grid connected PV systems has been highlighted. A single-stage topology with improved features has been proposed. Relevant analysis, including derivations of the expressions for peak voltage and current stresses across the switching devices, has been performed and a design procedure has been presented. The topology is simple, symmetrical and easy to control. The other desirable features include good efficiency due to optimal number of device switchings and reduced switching losses. A comparison of the proposed configuration with several existing configurations is summarized in Table IV.

The diodes ($D_p$ and $D_n$), which are inherent to the buck-boost operation, also serve to prevent any reverse power flow from the power grid to the PV array. DCM operation ensures better control apart from facilitating the generation and feeding of high quality current into the grid. DCM operation also eliminates the requirement of fast recovery diodes (i.e., $D_p$ and $D_n$). Thus, the design of the buck boost inductor is crucial, since the system must operate in DCM under any operating condition.

As per Figs. 16 and 17, the grid current THD is above 5%. But with a good grid voltage waveform (closer to a pure sine wave), the THD can be limited as per IEEE-519 (current THD $< 5\%$) and the topology will be able to feed high quality current into the grid. During low insolation, however, the current THD is observed to be high [Fig. 20(b)].

Some reactive power is also fed into the grid and its amount is found to be sensitive to the value of $C_f$. As the value of $C_f$ is decreased, the reactive power decreases and vice versa. However, reducing the value of $C_f$ increases the THD of the current fed into the grid. Thus, there is a trade-off between the reactive power and current THD and extensive computer simulations can be used to optimize the value of $C_f$. In fact, an optimization of the other design parameters is also possible using the plots of peak grid current and capacitor voltage stresses versus $z_o$ and $\omega_o$ presented in Section IV.

The proposed configuration, operating in DCM, along with the conventional hill climbing MPPT scheme, is highly robust. This is because the operating voltage of the PV array can be controlled by varying $M$. Also, there is a one-to-one relationship between $M$ and the average operating voltage of the PV array i.e., for each value of $M$, the system settles down to a

stable average operating point. Thus, there is no probability of the system moving into the short circuit region for higher values of $M$ [9].

Though the experimental results presented show a boosting of only about 1.5 times, the proposed system is expected to have reasonable boosting capability (typically 3–4 times), which means that low PV array voltages (typically 50–100 V range) can be boosted up to levels capable of interfacing with the grid voltage (115 V or 230 V ac systems). This has been verified using computer simulations.

Proposed configuration is highly suitable for an integrated solution (e.g., plug-and-play type ac modules) for PV systems. In this work, MOSFETs are used as switching devices. If low loss devices, like IGBTs, are used the efficiency can be further improved. Experiments with a DSP based laboratory prototype have shown encouraging results.

## REFERENCES


[1] B. K. Bose, P. M. Szezesny, and R. L. Steigerwald, "Microcontroller control of residential photovoltaic power conditioning system," *IEEE Trans. Ind. Appl.*, vol. 21, no. 5, pp. 1182–1191, Sep./Oct. 1985.

[2] I. Anton, F. Perez, I. Luque, and G. Sala, "Interaction between Sun tracking deviations and inverter MPP strategy in concentrators connected to grid," in *Proc. IEEE Photovolt. Spec. Conf.*, 2002, pp. 1592–1595.

[3] S. Saha and V. P. Sundarsingh, "Novel grid-connected photovoltaic inverter," *Proc. Inst. Elect. Eng.*, vol. 143, no. 2, pp. 143–56, 1996.

[4] P. G. Barbosa, H. A. C. Braga, M. do Carmo Barbosa Rodrigues, and E. C. Teixeira, "Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1116–1124, Jul. 2006.

[5] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, "Auto-calibrating dc link current sensing technique for transformerless, grid connected, H-bridge inverter systems," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1385–1396, Sep. 2006.

[6] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup, "Implementation and test of an online embedded grid impedance estimation technique for PV inverters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1136–1144, Aug. 2005.

[7] B. M. T. Ho and H. S.-H. Chung, "An integrated inverter with maximum power tracking for grid-connected pv systems," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 953–962, Jul. 2005.

[8] F. S. Kang, S. Cho, S. J. Park, C. U. Kim, and T. Ise, "A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system," *Solar Energy*, vol. 78, no. 6, pp. 727–738, 2005.

[9] T. J. Liang, Y. C. Kuo, and J. F. Chen, "Single-stage photovoltaic energy conversion system," *Proc. Inst. Elect. Eng.*, vol. 148, no. 4, pp. 339–344, 2001.

[10] Y. Chen and K. Ma-Smedley, "A cost-effective single-stage inverter with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1289–1294, Sep. 2004.

[11] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation Systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[12] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic Modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[13] F. Blaabjerg, A. Consoli, J. A. Ferreira, and J. D. Van Wyk, "The future of electronic power processing and conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 715–720, May 2005.

[14] M. Meinhardt, V. Leonavicius, J. Flannery, and S. C. Ó. Mathúna, "Impact of power electronics packaging on the reliability of grid connected photovoltaic converters for outdoor applications," *Microelectron. Rel.*, vol. 39, no. 10, pp. 1461–1472, 1999.

[15] D. Schekulin, "Grid-Connected Photovoltaic System," Germany patent DE197 32 218 Cl, Mar. 1999.

[16] N. Kasa, T. Iida, and H. Iwamoto, "Maximum power point tracking with capacitor identifier for photovoltaic power system," *Proc. Inst. Elect. Eng.*, vol. 147, no. 6, pp. 497–502, Nov. 2000.

[17] N. Kasa and T. Iida, "Flyback type inverter for small scale photovoltaic power system," in *Proc. IEEE IECON*, 2002, vol. 2, pp. 1089–1094.

[18] Y. Xue and L. Chang, "Closed-loop SPWM control for grid-connected buck-boost inverters," in *Proc. IEEE PESC*, 2004, vol. 5, pp. 3366–3371.

[19] Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z-source inverter for residential photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1776–1782, Nov. 2006.

[20] R. O. Caceres and I. Barbi, "A boost dc-ac converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.

[21] W. Chien-Ming, "A novel single-stage full-bridge buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.

[22] W. Chien-Ming, "A novel single-stage series-resonant buck–boost inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1099–1108, Aug. 2005.

[23] L. Meysenc, M. Jylhakallio, and P. Barbosa, "Power electronics cooling effectiveness versus thermal inertia," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 687–693, May 2005.

[24] R. Henk, *Practical Design of Power Supplies*. New York: McGraw Hill, 1998, pp. 95–96.

[25] Y. Xue, L. Chang, S. B. Kjær, J. Bordonau, and T. Shimizu, "Topologies of single phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.

[26] V. F. Pires and J. F. Silva, "Teaching non linear modeling, simulation, and control of electronic power converters using MATLAB/SIMULINK," *IEEE Trans. Education*, vol. 45, no. 3, pp. 253–261, Aut. 2002.

[27] G. Walker, "Evaluating MPPT converter topologies using a MATLAB PV model," *J. Electr. Electron. Eng., Australia*, vol. 21, no. 1, pp. 49–56, 2001.


**Sachin Jain,** photograph and biography not available at the time of publication.

**Vivek Agarwal,** photograph and biography not available at the time of publication.