Remember to bring this along to your lab!

[This document is available on LumiNUS and module website http://www.comp.nus.edu.sg/~cs2100]

Name: _____   Student No.: _____
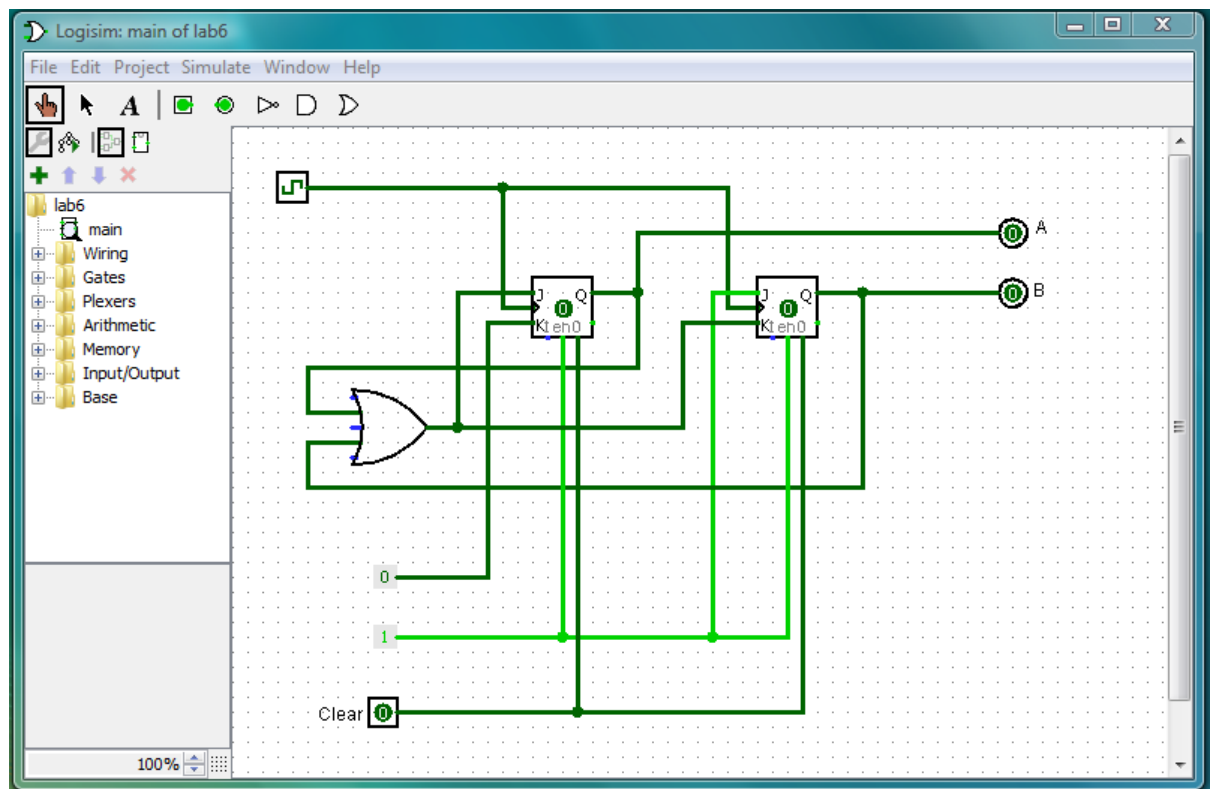
Lab Group: _____

Objective:

In this experiment, you will use **Logisim** to analyse and design sequential circuits.

Part I

1. Run Logisim, open the file **lab10part1.circ**. The circuit is shown below.

2. The circuit consists of two JK flip-flop and an OR gate. Note the following:

   ▪ The outputs of the two JK flip-flops are labelled *A* and *B*, which form the state of the circuit.

   ▪ The Clock ⬛ is connected to the clock inputs of the flip-flops.

   ▪ The logic constant 1 is connected to the Enable inputs of the flip-flops.

   ▪ The Clear switch ⬛ is connected to the clear inputs of the flip-flops. Hence when Clear = 1, it clears the contents of both flip-flips to 0, bringing the circuit to the initial state of *AB*=00.

   ▪ The flip-flop inputs are as follows:

For flip-flop *A*: **JA = A + B;**   **KA = 0**

For flip-flop *B*: **JB = 1;**   **KB = A + B**
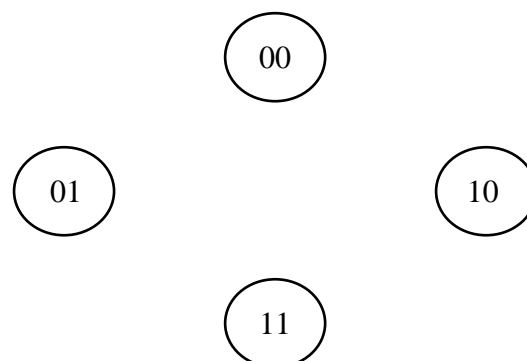
3. Complete the following table: [6 marks]

Present state		Flip-flop inputs				Next state	
A	**B**	**JA**	**KA**	**JB**	**KB**	**A⁺**	**B⁺**
0	0						
0	1						
1	0						
1	1						

4. Verify the correctness of your table above by testing the circuit in Logisim.

   a) Click on "Clear" input to get 1. This clears both flip-flops to 0, bringing the circuit to the initial state of *AB*=00.

   b) Click on "Clear" input to get 0 before you proceed. This puts the flip-flops in their normal operation mode.

   c) Clicking the "Clock" input toggles its value. When the "Clock" value changes from 0 to 1 (i.e. a rising edge), the flip-flops react according to the commands at their J and K inputs.

   d) Click the "Clock" input several times to simulate the square wave, and watch the outputs of the flip-flops change their values. Do the values follow your table above?

   e) If at any point of time you want to reset the flip-flops to the initial state of 00, go to step (a) above.

5. Complete the state diagram below. [4 marks]

Part II

6. You will design a sequential circuit using JK flip-flops. The flip-flop inputs are given below:

For flip-flop *A*:   *JA* = **1;**   *KA* = *A* · *B*

For flip-flop *B*:   *JB* = **0;**   *KB* = (*A* · *B*)'

7. Complete the following table: [6 marks]

Present state		Flip-flop inputs				Next state	
A	*B*	*JA*	*KA*	*JB*	*KB*	A^+	B^+
0	0						
0	1						
1	0						
1	1						

8. Complete the state diagram below.   [4 marks]

00

01   10

11
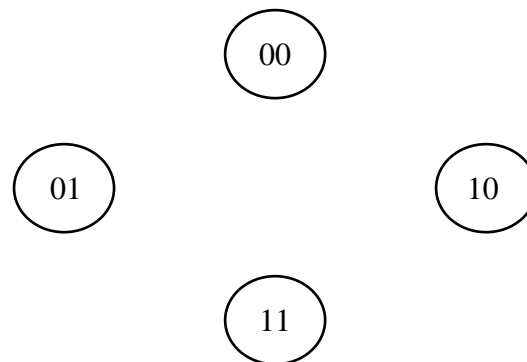
9. Implement the circuit on Logisim and show it to your lab TA. In your circuit, you should also include a "Preset" input so that you can set both flip-flops to 1.   [5 marks]

10. As this is your final lab, your lab report will not be returned to you.

Total: 25 marks