KOCAELİ UNIVERSITY

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI DESIGN TERM PROJECT

4 BIT ADDER

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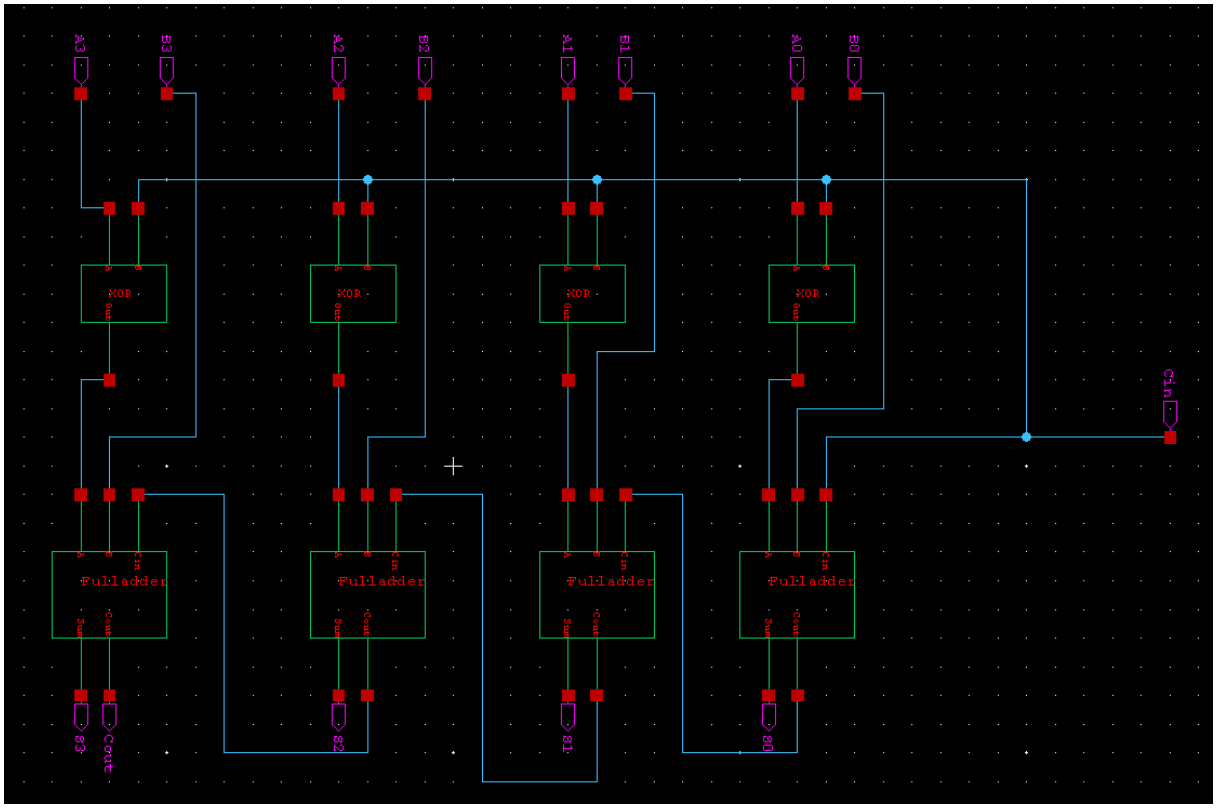
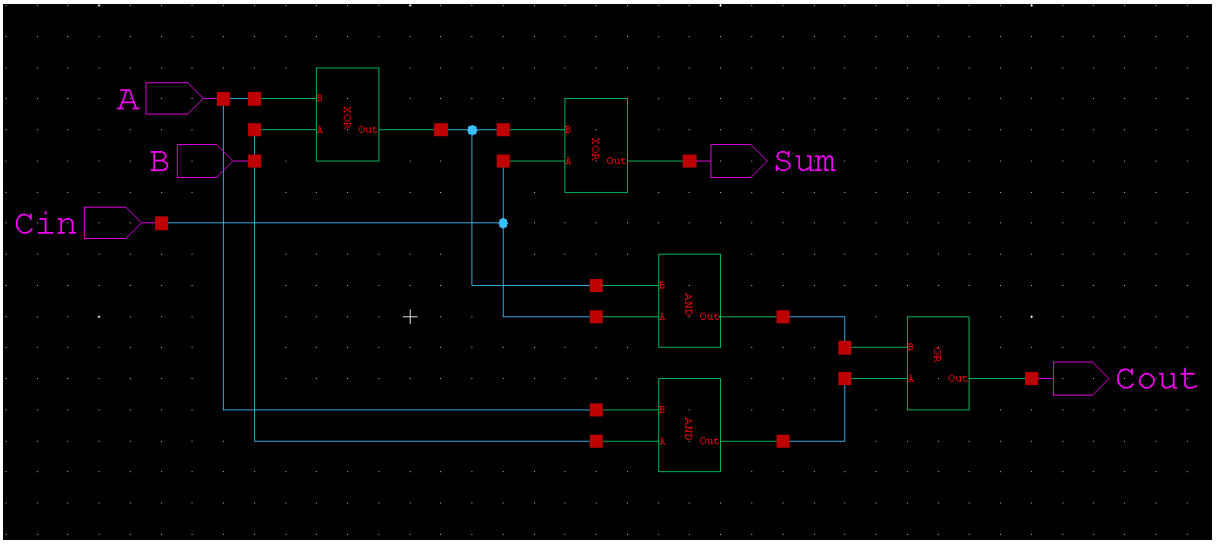
KOCAELİ 2020

Contents

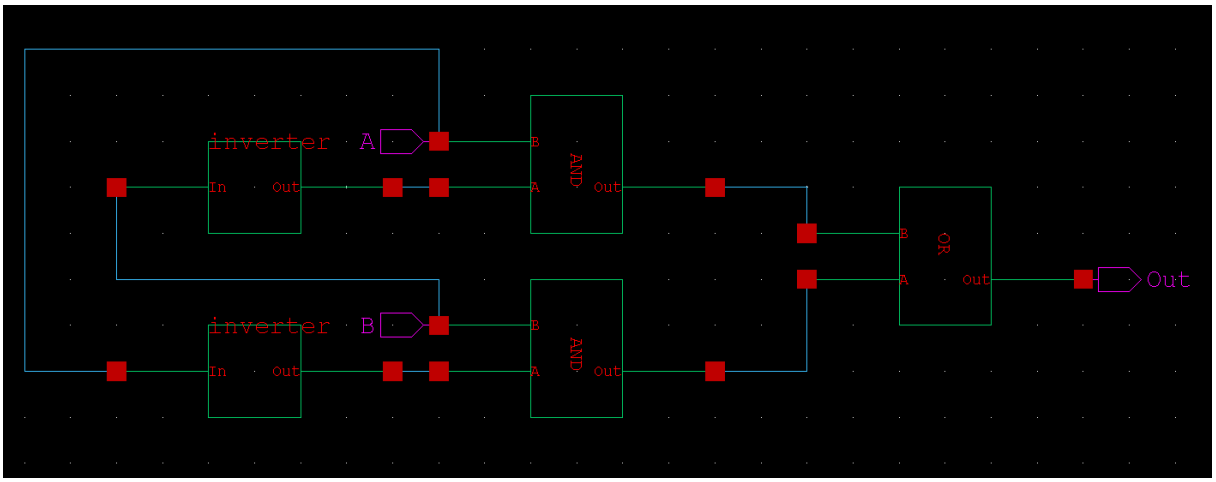
SCHEMATIC DESIGNS



Şekil 1 - 4 Bit Adder Schematic



Şekil 2 - Fulladder Schematic used by 4 Bit Adder



Şekil 3 - XOR Gate used by Fulladder

NETLIST FILE GENERATED FROM SCHEMATIC

```
* SPICE export by:  SEDIT 13.00
* Export time:      Tue Dec 15 21:46:17 2020
* Design:           lab2
* Cell:             adder
* View:             view0
* Export as:        top-level cell
* Export mode:      hierarchical
* Exclude .model:   no
* Exclude .end:     no
* Expand paths:     yes
* Wrap lines:       no
* Root path:        C:\Users\Ck_sy\Desktop\VLSI\lab2
* Exclude global pins:   no
* Control property name: SPICE

********** Simulation Settings - General section **********

*************** Subcircuits ******************
.subckt and A B Out Gnd Vdd
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 N_2 A N_1 Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 N_1 B Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_3 Out N_2 Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 N_2 A Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_2 N_2 B Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_3 Out N_2 Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

.subckt inverter In Out Gnd Vdd
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 Out In Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

.subckt or A B Out Gnd Vdd
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 N_3 A Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 N_3 B Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
```

```
MNMOS_3 Out N_3 Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 N_1 A Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_2 N_3 B N_1 N_2 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_3 Out N_3 Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

.subckt XOR A B Out Gnd Vdd
Xand_2 N_3 B N_4 Gnd Vdd and
Xand_1 N_1 A N_2 Gnd Vdd and
Xor_1 N_4 N_2 Out Gnd Vdd or
Xinverter_1 B N_1 Gnd Vdd inverter
Xinverter_2 A N_3 Gnd Vdd inverter
.ends

.subckt full_adder A B Cin Cout Sum Gnd Vdd
Xand_1 Cin N_1 N_3 Gnd Vdd and
Xor_1 N_2 N_3 Cout Gnd Vdd or
Xand_2 B A N_2 Gnd Vdd and
XXOR_1 B A N_1 Gnd Vdd XOR
XXOR_2 Cin N_1 Sum Gnd Vdd XOR
.ends


********** Simulation Settings - Parameters and SPICE Options **********

Xfull_adder_1 N_2 B1 N_1 N_4 S1 Gnd Vdd full_adder
Xfull_adder_2 N_3 B0 Cin N_1 S0 Gnd Vdd full_adder
XXOR_1 A1 Cin N_2 Gnd Vdd XOR
XXOR_2 A0 Cin N_3 Gnd Vdd XOR
Xfull_adder_3 N_5 B2 N_4 N_8 S2 Gnd Vdd full_adder
Xfull_adder_4 N_6 B3 N_8 Cout S3 Gnd Vdd full_adder
XXOR_3 A2 Cin N_5 Gnd Vdd XOR
XXOR_4 A3 Cin N_6 Gnd Vdd XOR

********** Simulation Settings - Analysis section **********
Vpower Vdd Gnd 5V
.include "C:\Users\Ck_sy\Desktop\VLSI_tech_files\SCN_0.25u_CMOS.md"
Vbit  A0 Gnd dc 0 BIT ({0100} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit2 A1 Gnd dc 0 BIT ({0011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit3 A2 Gnd dc 0 BIT ({0000} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit4 A3 Gnd dc 0 BIT ({0010} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

Vbit5 B0 Gnd dc 0 BIT ({0111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit6 B1 Gnd dc 0 BIT ({0001} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit7 B2 Gnd dc 0 BIT ({0001} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit8 B3 Gnd dc 0 BIT ({0001} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

Vbit9 Cin Gnd dc 0 BIT ({0000} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
.print tran v(S0) v(S1) v(S2) v(S3) v(Cout)
*.print tran v(B0) v(B1) v(B2) v(B3)
*.print tran v(A0) v(A1) v(A2) v(A3)
.tran 40p 40n
.print tran p(Vpower)
.power Vpower 0 40n
********** Simulation Settings - Additional SPICE commands **********

.end
```

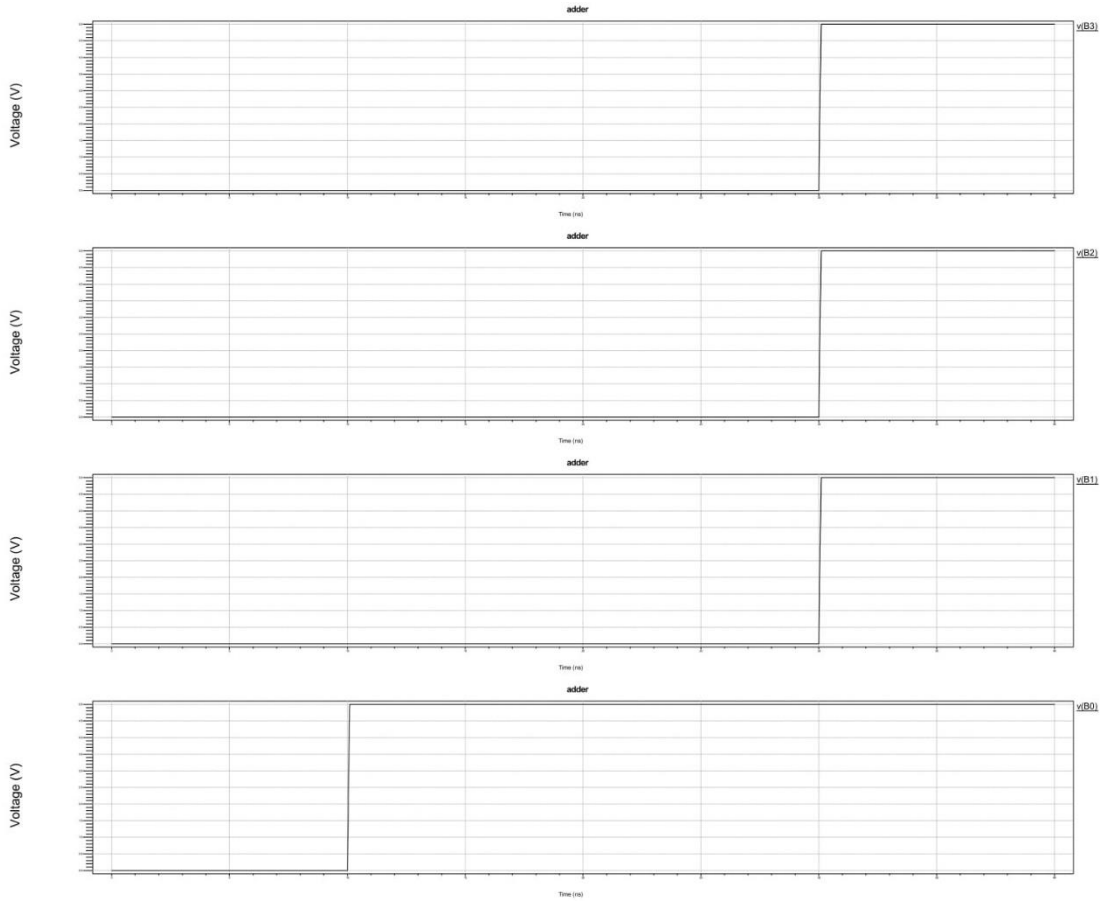
SIMULATION RESULTS

Adder performed both addition and substraction operations for following numbers in simulation; A=0 and B=0 , A=1 and B=1 , A=10 and B=1 , A=2 and B= 15.

Adder circuit was simulated for 100mbps. Further more, circuit was simulated for 1gbps but results were not satisfactory.

4 Bit Adder , A and B Inputs

Şekil 4 Input A



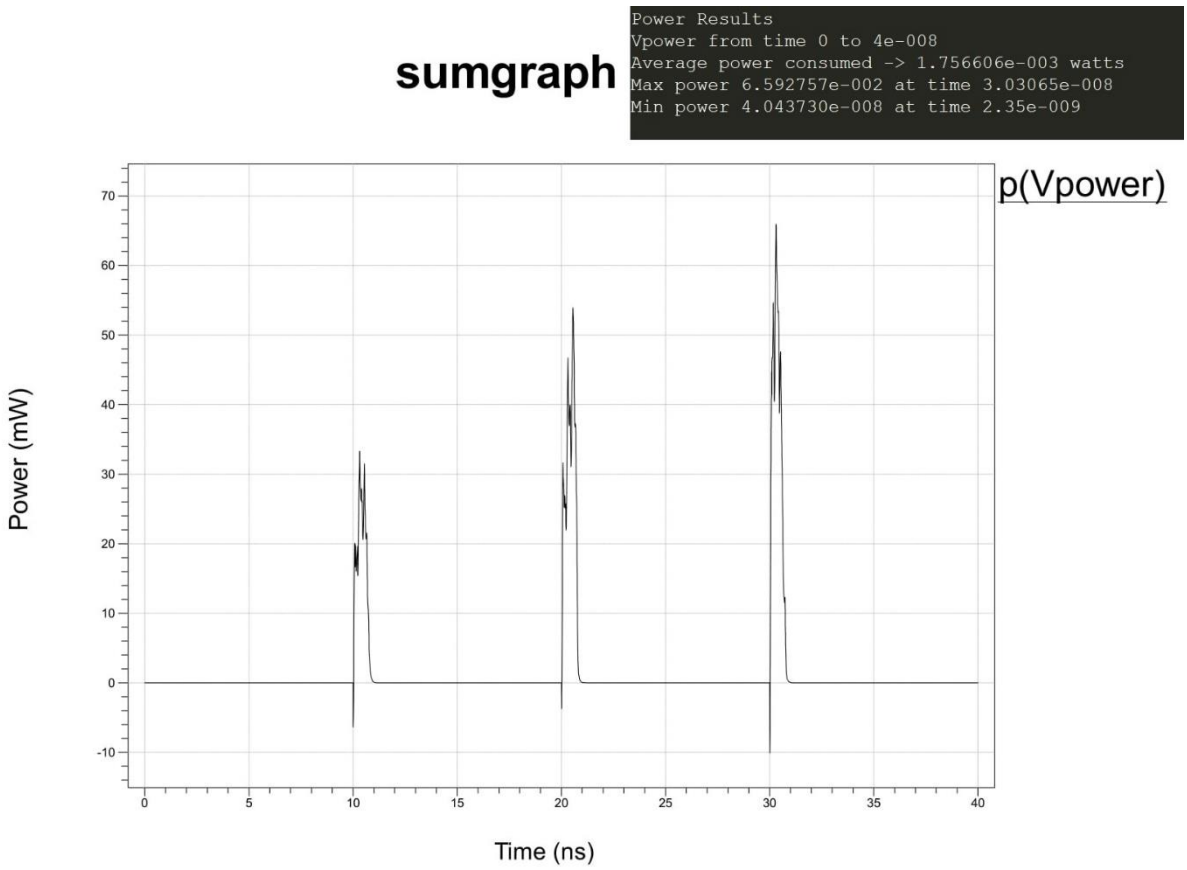
Şekil 5 Input B

4 Bit Adder Output for Addition

Cin (K) is 0 for all time.

Şekil 6 Adder Output

Power Analysis for Addition



Şekil 7 Transient Power Analysis for Addition

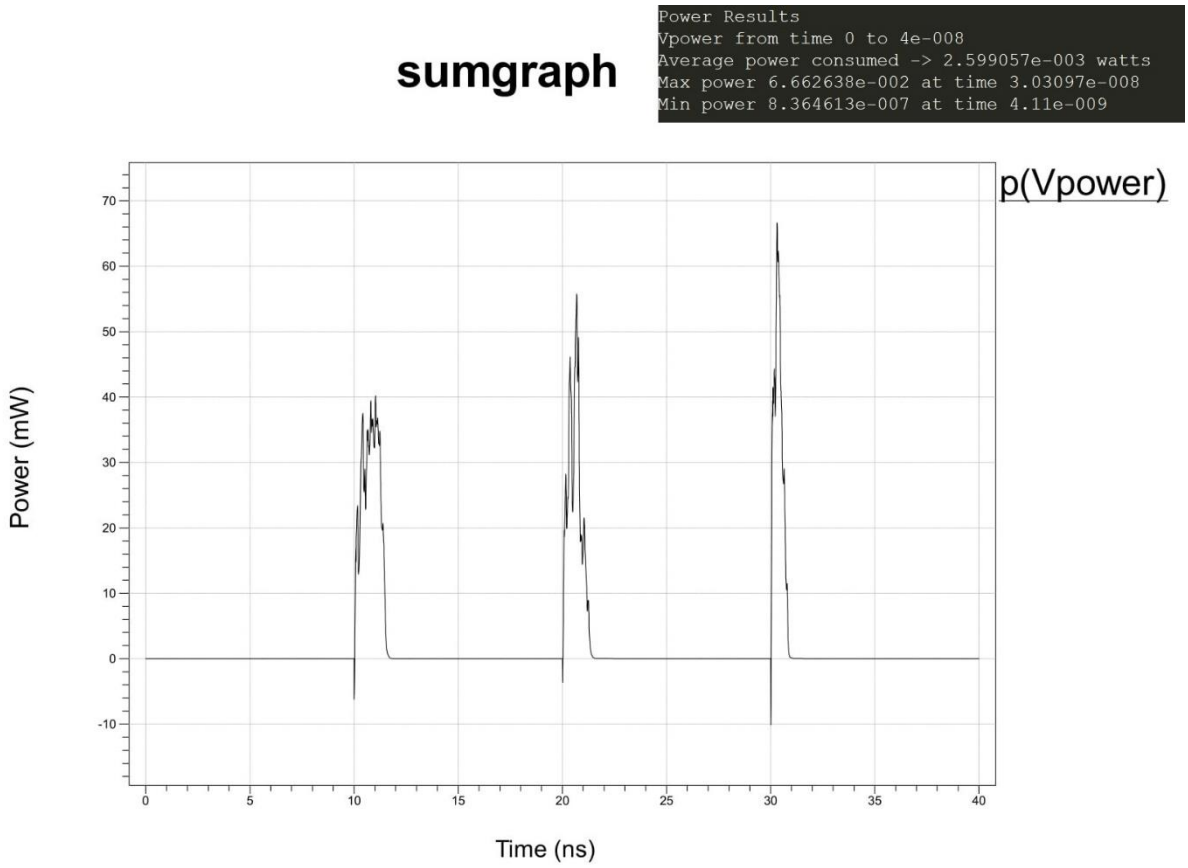
4 Bit Adder Output for Substraction

Cin (K) is 1 for all time.

Şekil 8 Adder Output

At Şekil 7 we see that output is 7 but adder substract 10 from 1 , result would have been -9 but 7 is 2's complement of 9. Circuit gives output as 2's complement for substraction.

Power Analysis for Substraction

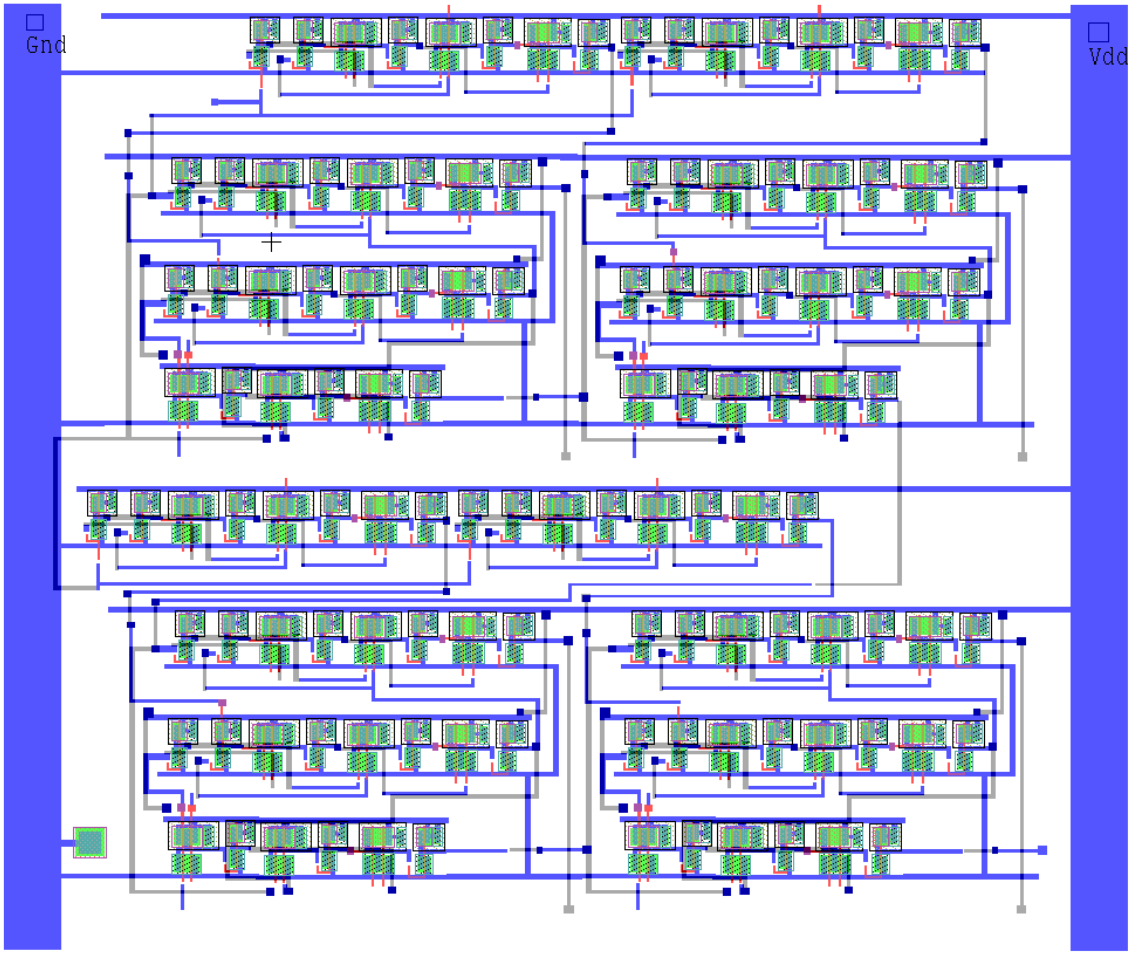


Şekil 9 Transient Power Analysis for Substraction

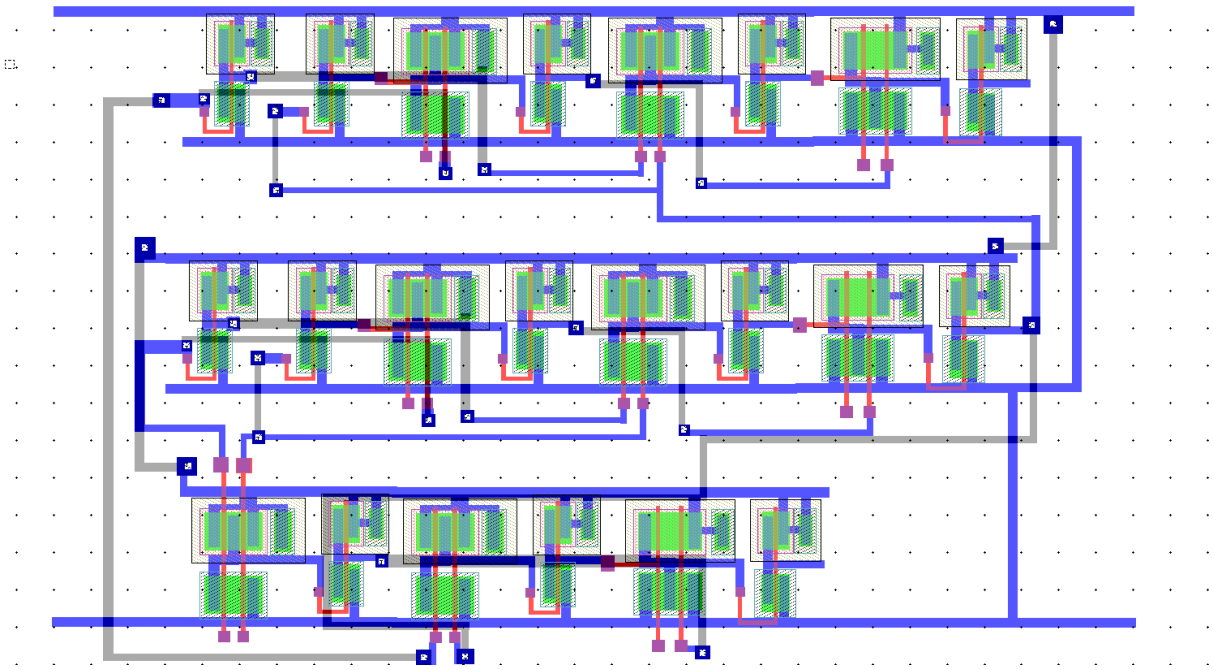
RESULTS

As wee can see at the graphs above , we have little glitches at 100mbps which is acceptable. We can design a layout for this circuit.

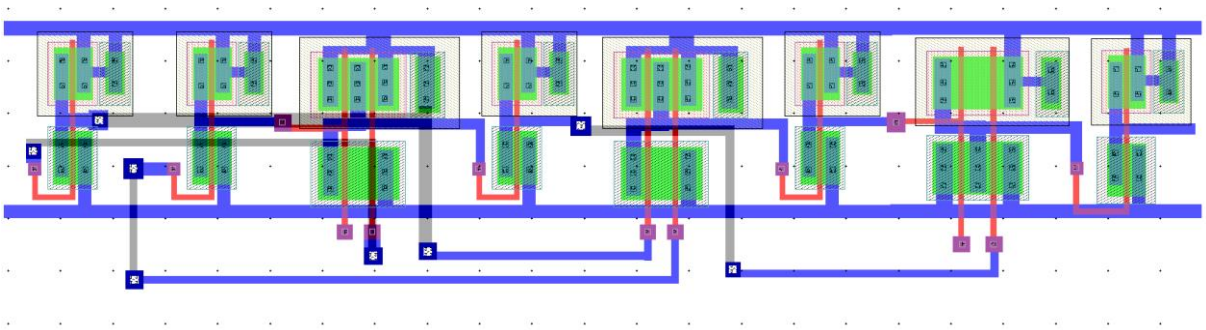
LAYOUT DESIGNS



Şekil 10 4 Bit Adder Layout



Şekil 11 Fulladder Layout



Şekil 12 XOR Layout

SIMULATION SETTINGS FOR T-SPICE

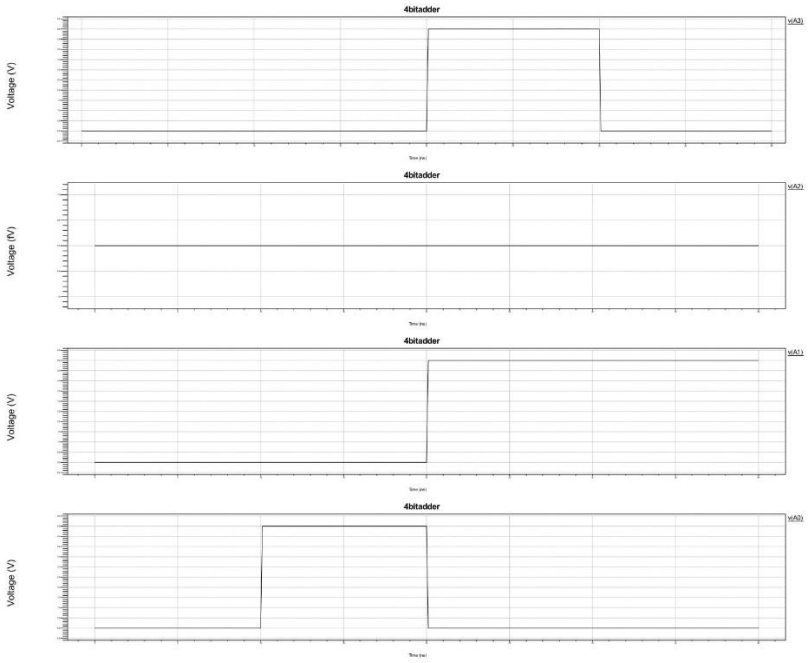
Netlist file extracted from layout is attached that's why will be not fully shown here.

```
Vpower Vdd Gnd 5V
.include "C:\Users\Ck_sy\Desktop\VLSI_tech_files\SCN_0.25u_CMOS.md"
Vbit  A0 Gnd dc 0 BIT ({1000} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit2 A1 Gnd dc 0 BIT ({0010} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit3 A2 Gnd dc 0 BIT ({0101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit4 A3 Gnd dc 0 BIT ({0010} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0

Vbit5 B0 Gnd dc 0 BIT ({1011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit6 B1 Gnd dc 0 BIT ({0011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit7 B2 Gnd dc 0 BIT ({1111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
Vbit8 B3 Gnd dc 0 BIT ({0001} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0

Vbit9 K Gnd dc 0 BIT ({0000} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0
ROUND=0
.tran 40p 40n
*.print tran v(S0) v(S1) v(S2) v(S3) v(Cout)
*.print tran v(B0) v(B1) v(B2) v(B3)
*.print tran v(A0) v(A1) v(A2) v(A3)
.print tran p(Vpower)
.power Vpower 0 40n
```

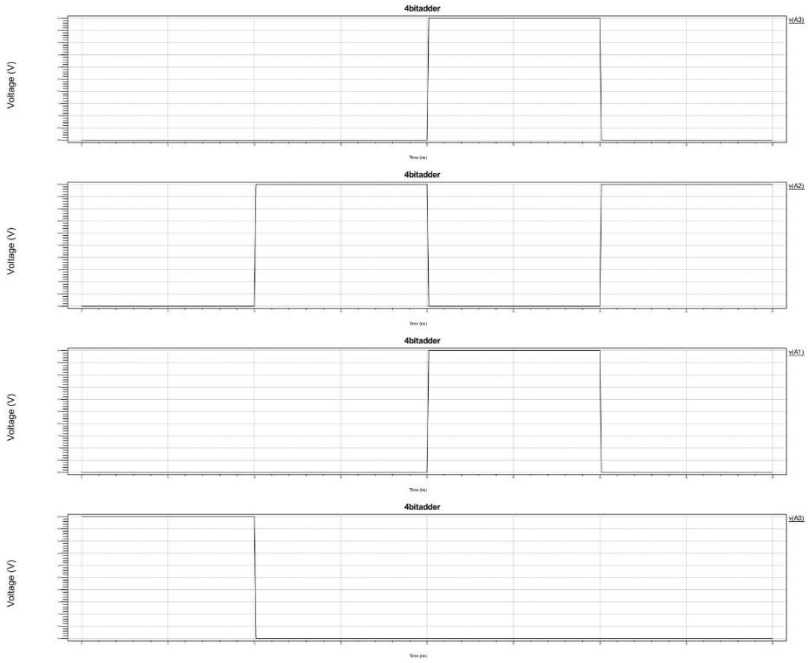
SIMULATION RESULTS

4 Bit Adder , A and B Inputs

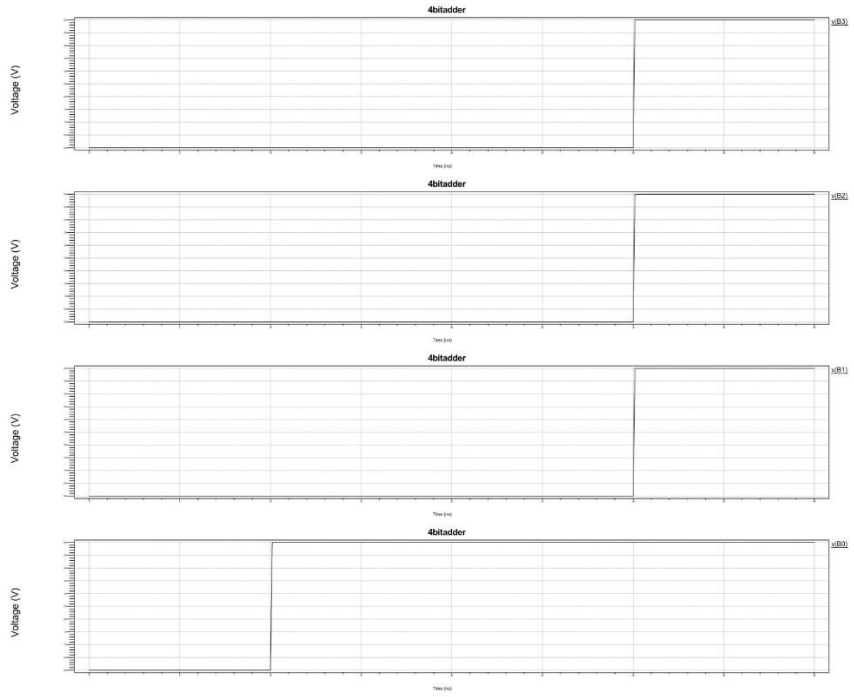
Device was tested for 8 different scenarios.



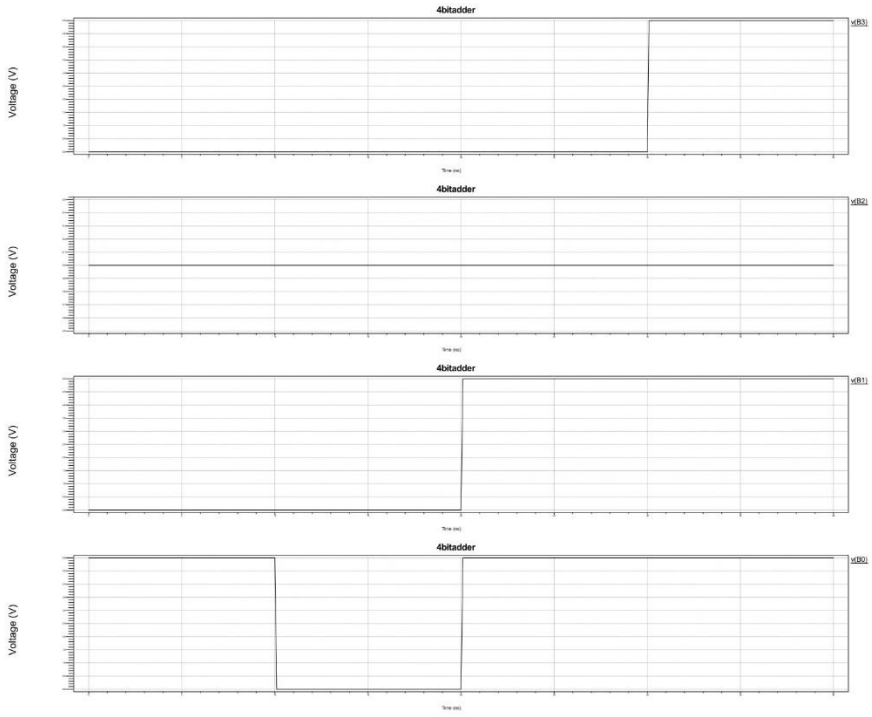
Şekil 13 Input Sequence 1 for A



Şekil 14 Input Sequence 2 for A



Şekil 15 Input Sequence 1 for B



Şekil 16 Input Sequence 2 for B

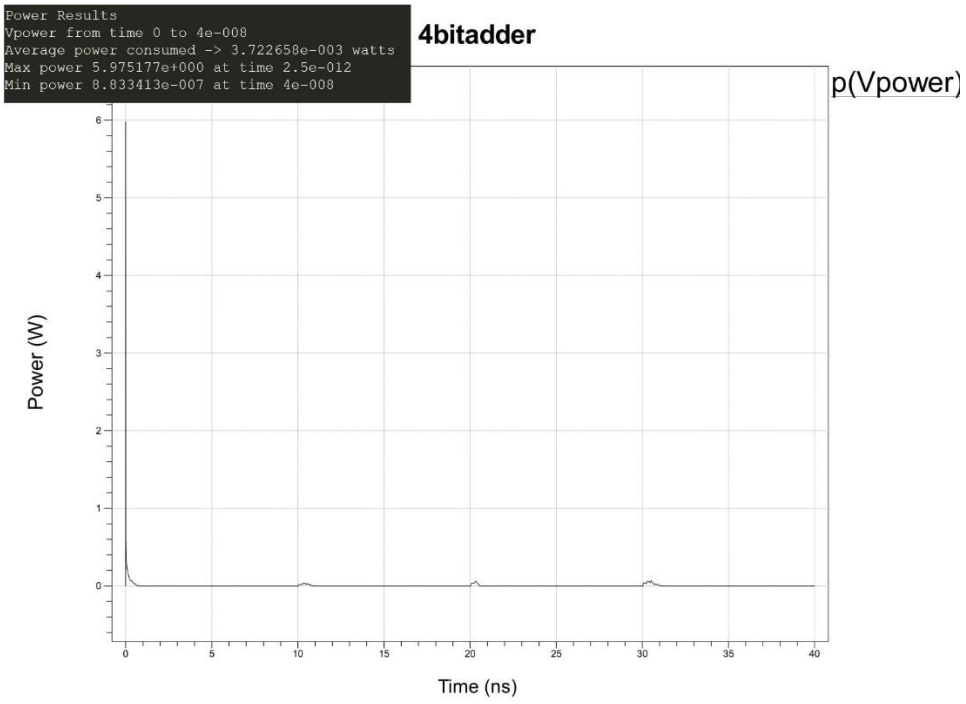
4 Bit Adder Outputs for Addition

Şekil 17 Adder Output for Input Sequence 1 (Addition)

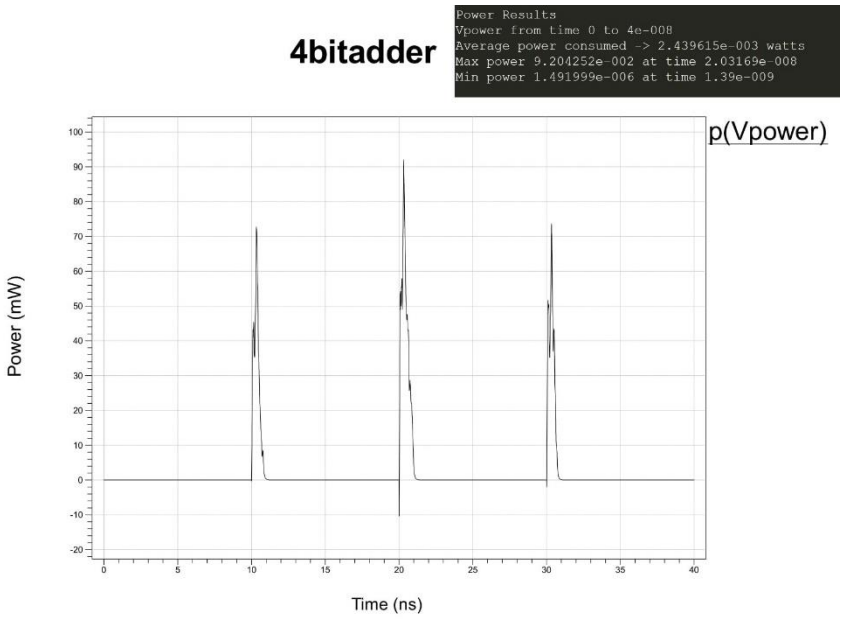
Şekil 18 Adder Output for Input Sequence 2 (Addition)

Cin(K) is 0 for all time.

Power Analysis for Addition



Şekil 19 Transient Power Analysis for Input Sequence 1

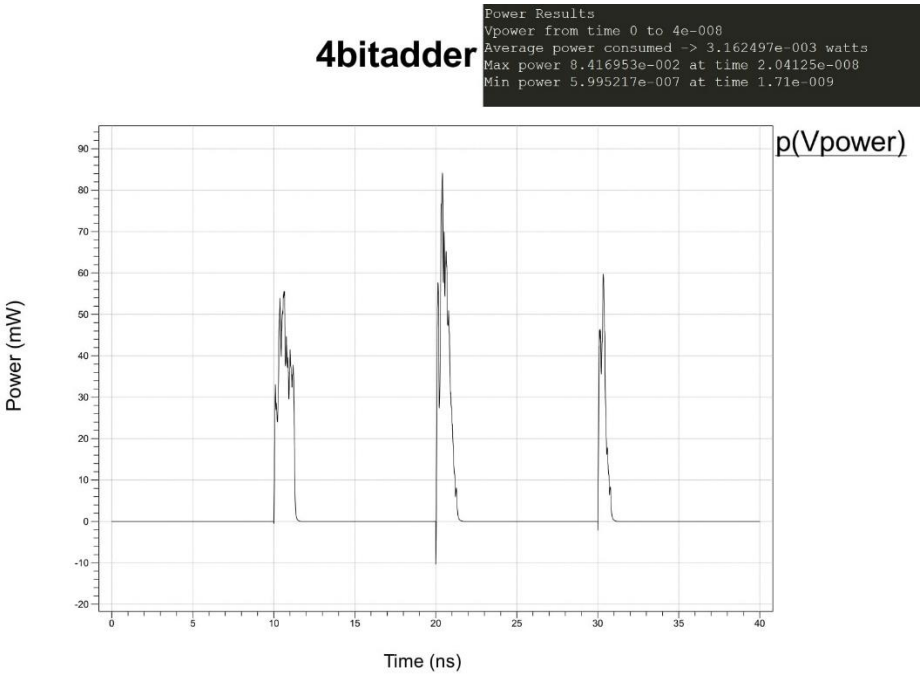


Şekil 20 Transient Power Analysis for Input Sequence 2

4 Bit Adder Outputs for Substraction

Şekil 21 Adder Output for Input Sequence 2 (Substraction)

Power Analysis for Substraction



Şekil 22 Transient Power Analysis for Input Sequence 2 (Substraction)