KOCAELİ UNIVERSITY

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI DESIGN TERM PROJECT

4x16 Decoder

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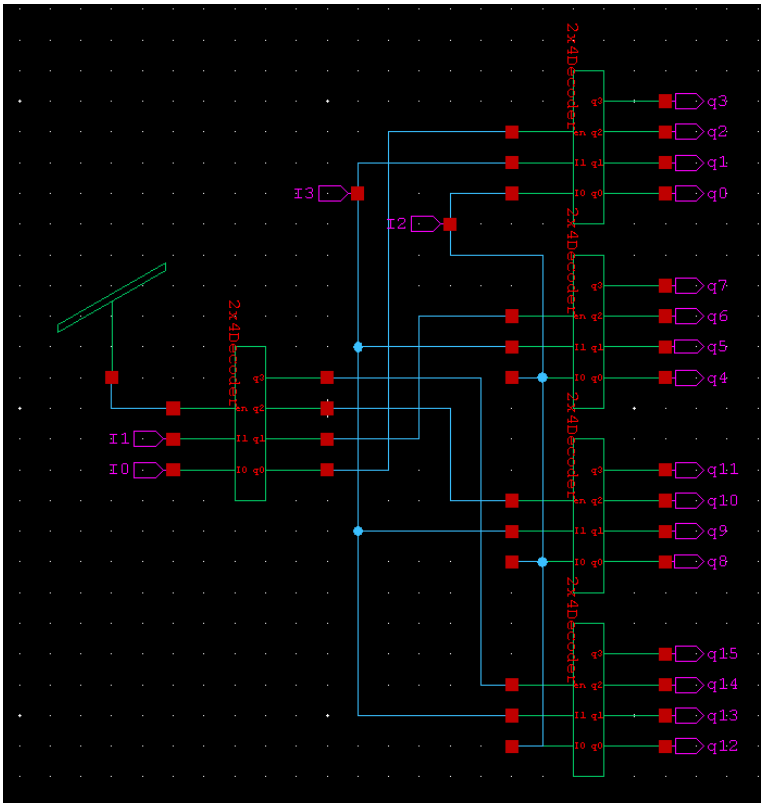
160207055

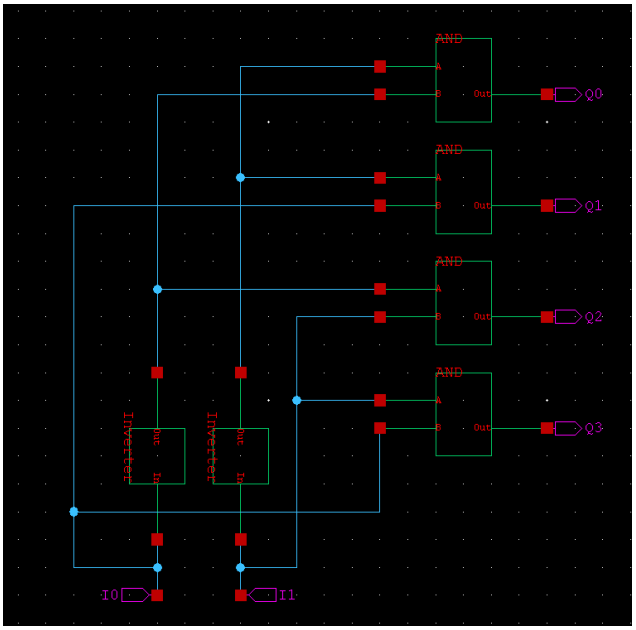
KOCAELİ 2020

Contents

SCHEMATIC DESIGNS



Şekil 1 - 4x16 Decoder Schematic



Şekil 2 – 2x4 Decoder Schematic

NETLIST FILE GENERATED FROM SCHEMATIC

```
* SPICE export by:  SEDIT 13.00
* Export time:      Wed Dec 30 16:01:03 2020
* Design:           Decoder
* Cell:             Cell1
* View:             view0
* Export as:        top-level cell
* Export mode:      hierarchical
* Exclude .model:   no
* Exclude .end:     no
* Expand paths:     yes
* Wrap lines:       no
* Root path:        C:\Users\Ck_sy\Desktop\VLSI\Decoder
* Exclude global pins:   no
* Control property name: SPICE

********* Simulation Settings - General section *********

********** Subcircuits **********
.subckt Inv In Out Gnd Vdd
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 Out In Gnd Gnd NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

.subckt 3AND A B C Out Gnd Vdd
*-------- Devices: SPICE.ORDER == 0 --------
XInv_1 N_6 Out Gnd Vdd Inv
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 N_2 B N_3 N_1 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 N_3 C Gnd N_4 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_3 N_6 A N_2 N_5 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 N_6 A Vdd N_7 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_2 N_6 B Vdd N_8 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_3 N_6 C Vdd N_9 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

.subckt 2x4decoder_en I0 I1 en q0 q1 q2 q3 Gnd Vdd
XInv_1 I0 N_2 Gnd Vdd Inv
XInv_2 I1 N_1 Gnd Vdd Inv
X3AND_1 en N_1 N_2 q0 Gnd Vdd 3AND
X3AND_2 en I0 N_1 q1 Gnd Vdd 3AND
X3AND_3 en I1 N_2 q2 Gnd Vdd 3AND
X3AND_4 en I1 I0 q3 Gnd Vdd 3AND
.ends


********* Simulation Settings - Parameters and SPICE Options *********

X2x4decoder_en_2 I2 I3 N_1 q0 q1 q2 q3 Gnd Vdd 2x4decoder_en
X2x4decoder_en_3 I2 I3 N_2 q4 q5 q6 q7 Gnd Vdd 2x4decoder_en
X2x4decoder_en_4 I2 I3 N_3 q8 q9 q10 q11 Gnd Vdd 2x4decoder_en
X2x4decoder_en_5 I2 I3 N_4 q12 q13 q14 q15 Gnd Vdd 2x4decoder_en
X2x4decoder_en_1 I0 I1 Vdd N_1 N_2 N_3 N_4 Gnd Vdd 2x4decoder_en

********* Simulation Settings - Analysis section *********
Vpower Vdd Gnd 5V
```

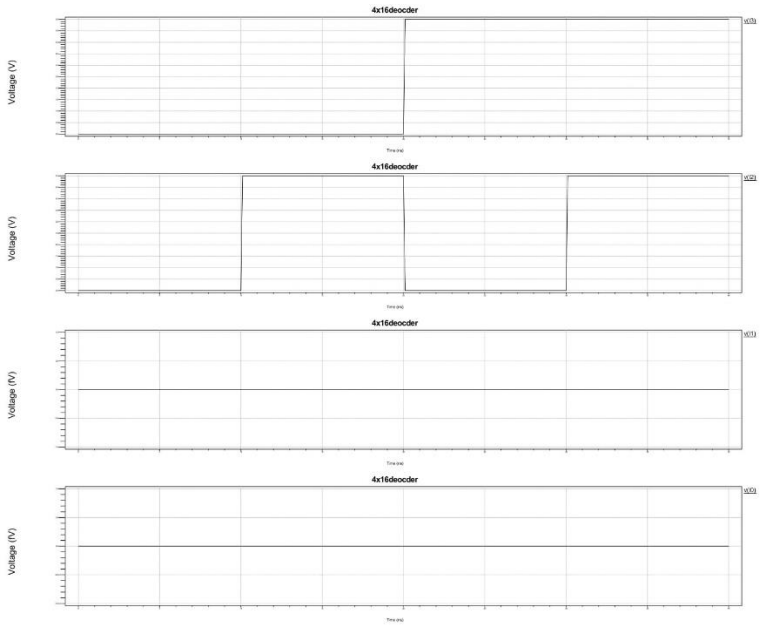
```
*IO ve I1 4lük seçim için 00,01,10,11 sırasıyla dene 3 ve 4 elleme.
Vbit1 I0 Gnd dc 0 BIT ({1111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit2 I1 Gnd dc 0 BIT ({1111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

Vbit3 I2 Gnd dc 0 BIT ({0101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit4 I3 Gnd dc 0 BIT ({0011}pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

.include "C:\Users\Ck_sy\Desktop\Programlar\VLSI PROGRAMLAR VE
KURULUMLARI\VLSI_tech_files\SCN_0.25u_CMOS.md"
.tran 40p 40n start=0
*.print tran v(I0) v(I1) v(I2) v(I3)
*.print tran v(q0) v(q1) v(q2) v(q3)
*.print tranv(q4) v(q5) v(q6) v(q7)
*.print tran v(q8) v(q9) v(q10) v(q11)
*.print tran v(q12) v(q13) v(q14) v(q15)
.print tran p(Vpower)
.power Vpower 0 40n

********* Simulation Settings - Additional SPICE commands *********

.end
```

SIMULATION RESULTS

I0 and I1 bits are used for enable one of 2x4 decoders at output stage. For examle, “00” enables the outputs q0-q3 ; “01” enables the outputs q4-q7 ..etc. I2 and I3 bits are used to select the enabled decoder output from 0-3.

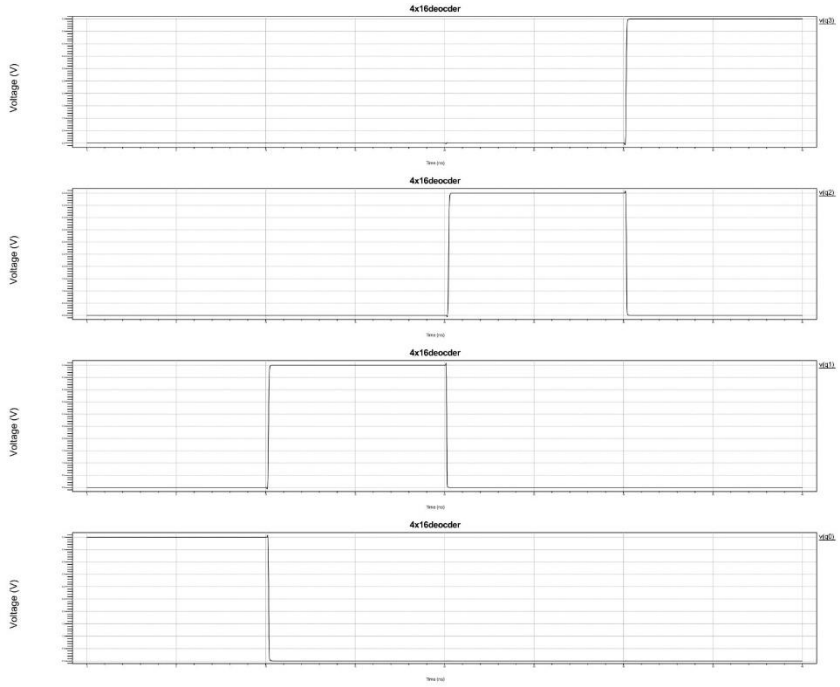
Circuit was simulated for 100mbps.

Decoder Inputs and Outputs

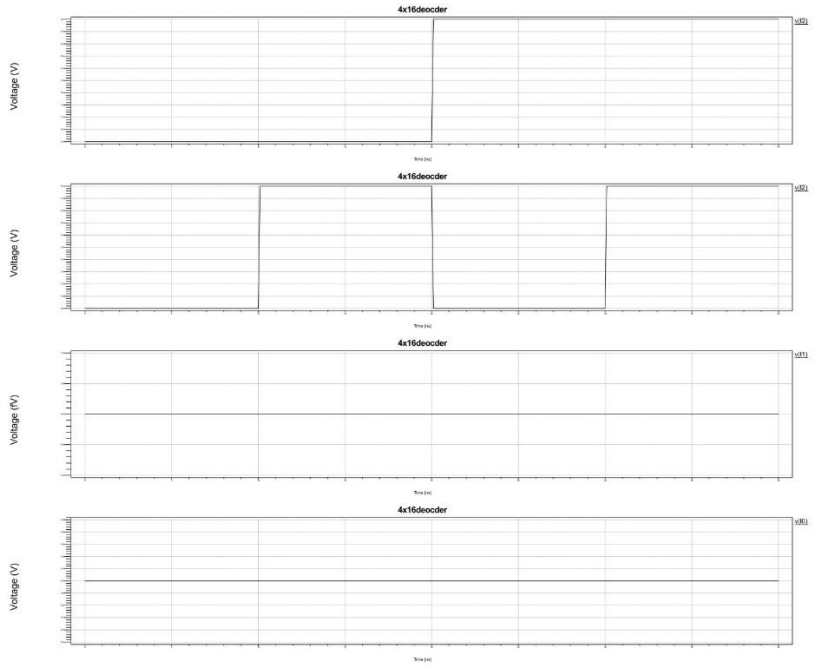


Şekil 3 Input I1 and I0 is "00"

I1 and I0 are “00” so, this will enable the outputs q0-q3.

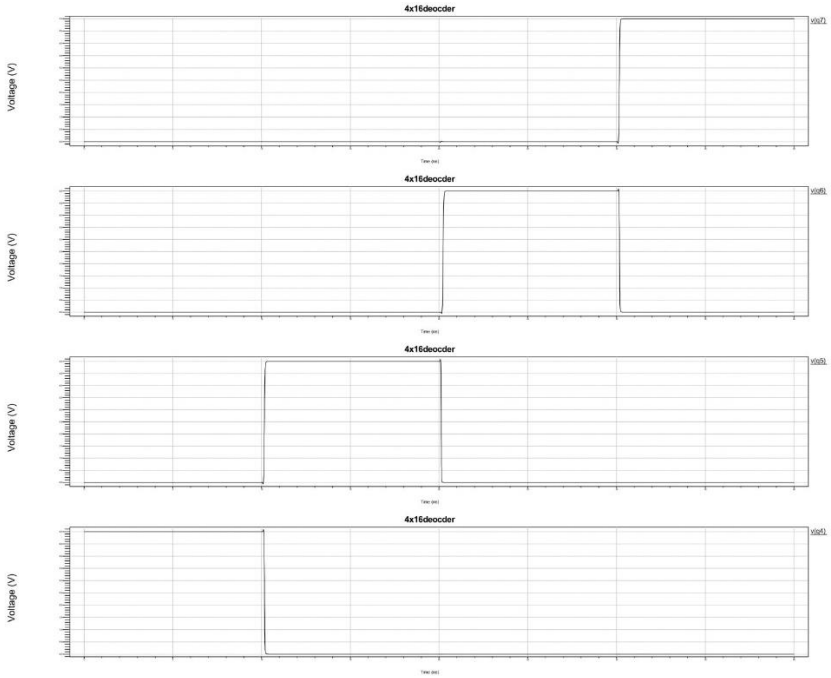


Şekil 4 Outputs q0-q3

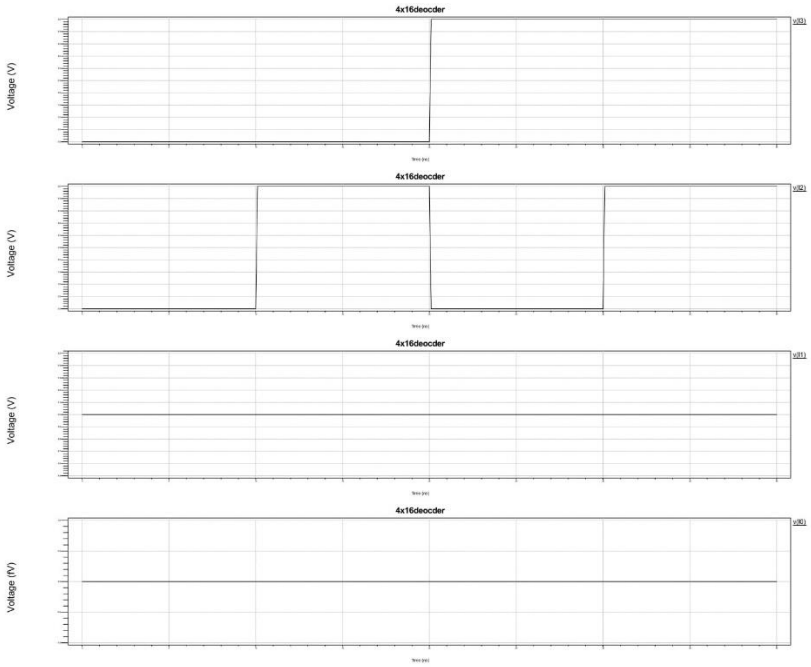


Şekil 5 Input I1 and I0 is "01"

I1 and I0 are “01” so, this will enable the outputs q4-q7.

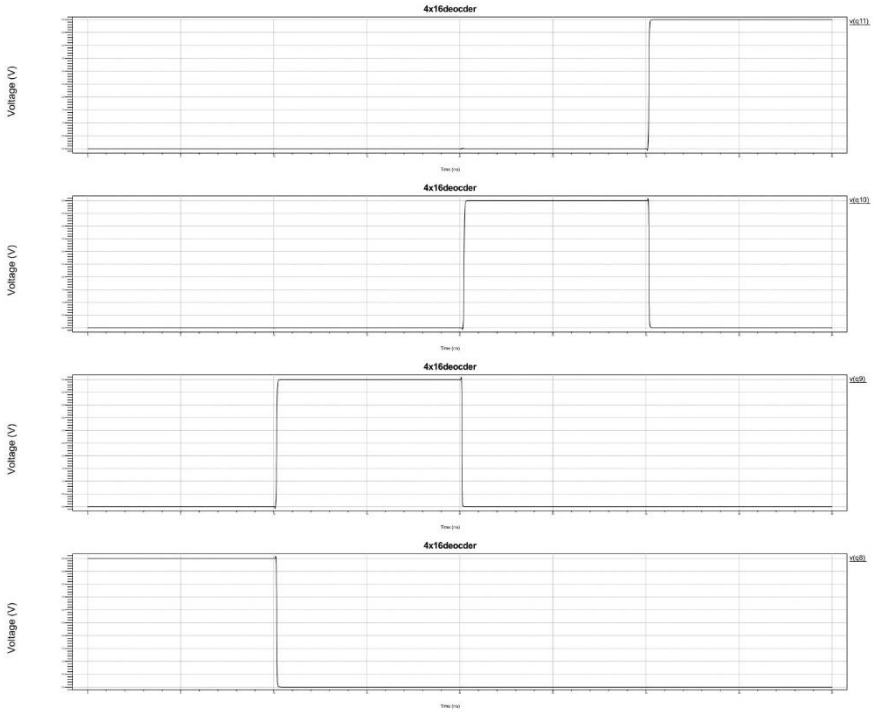


Şekil 6 Outputs q4-q7

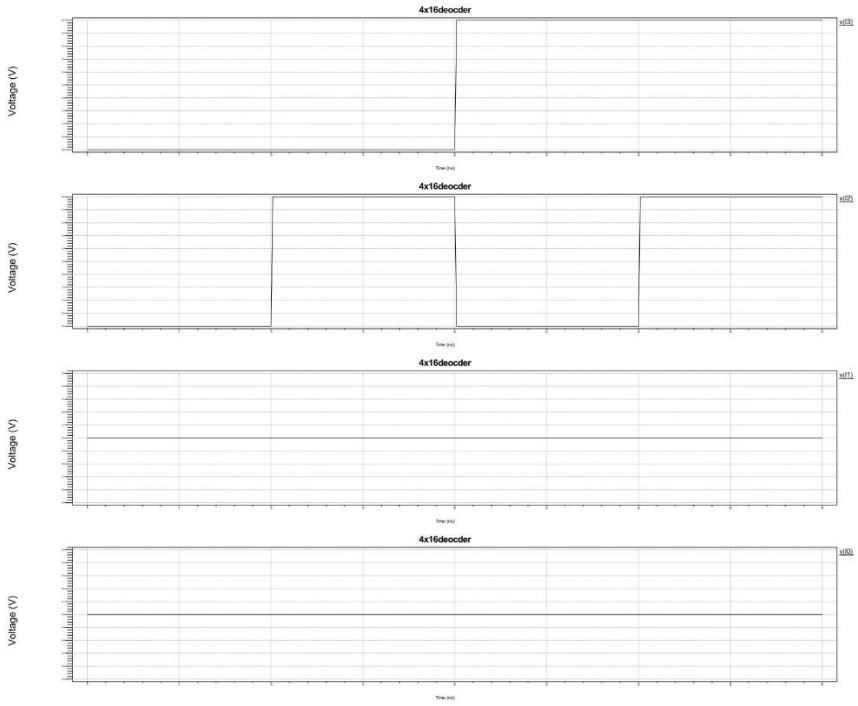


Şekil 7 Input I1 and I0 is "10"

I1 and I0 are “10” so, this will enable the outputs q8-q11.

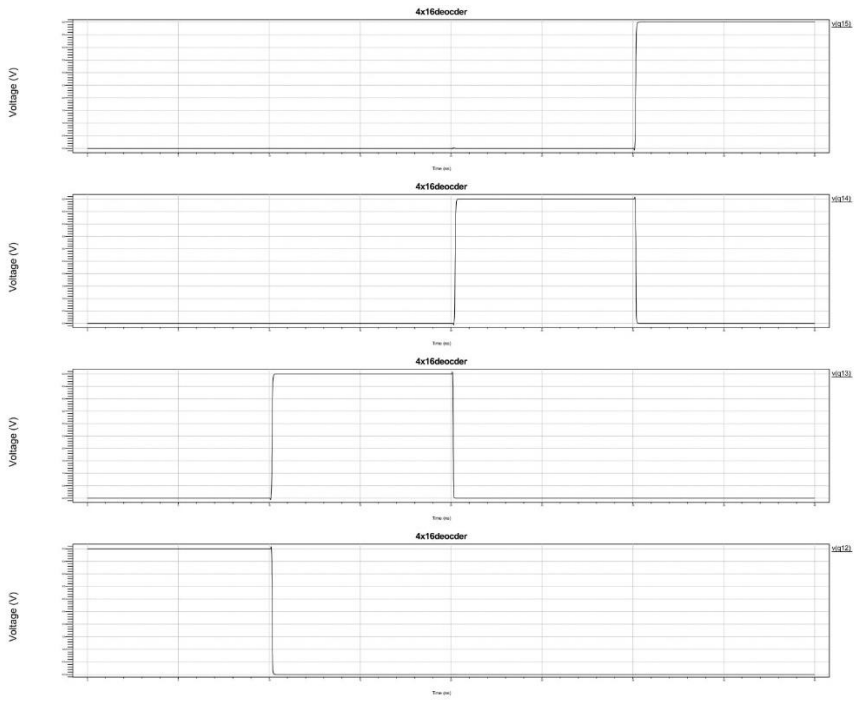


Şekil 8 Outputs q8-q11



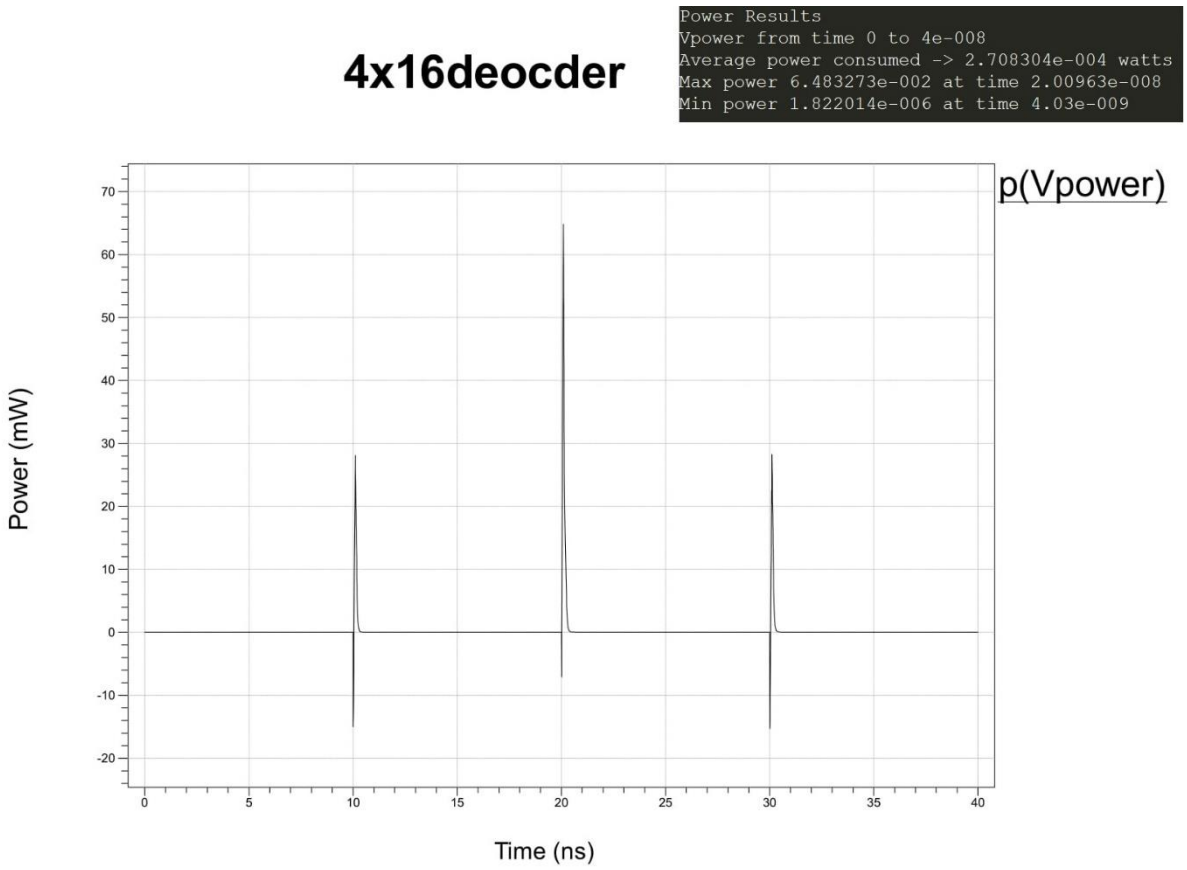
Şekil 9 Input I1 and I0 is "11"

I1 and I0 are “11” so, this will enable the outputs q12-q15.



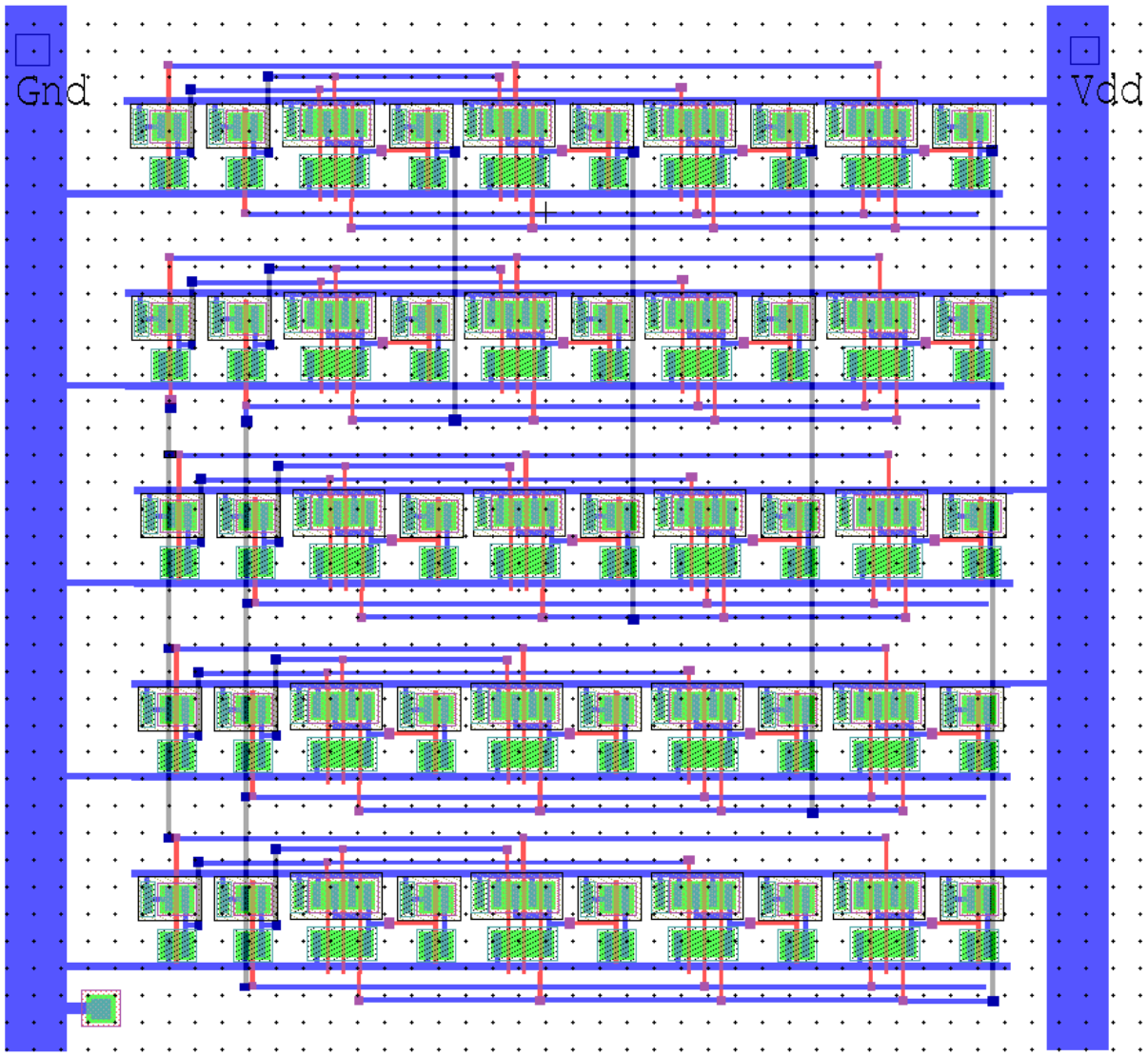
Şekil 10 Outputs q12-q15

Power Analysis

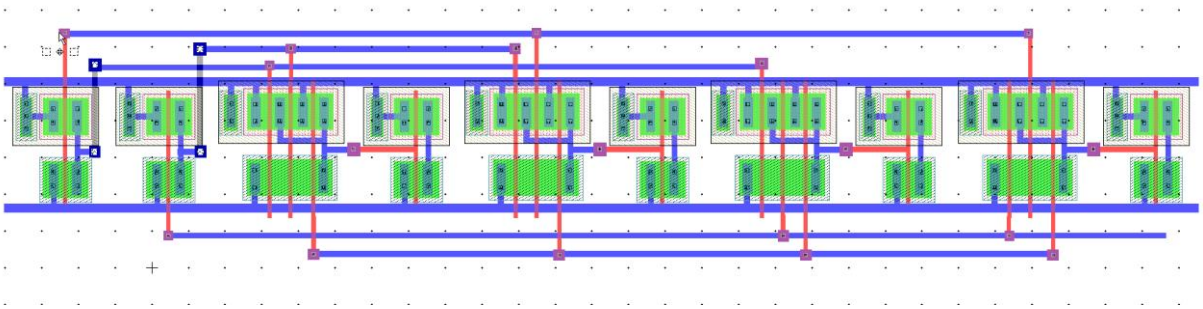


Şekil 11 Peak and Average Power

LAYOUT DESIGNS



Şekil 12 4x16 Decoder



Şekil 13 2x4 Decoder

NETLIST FILE

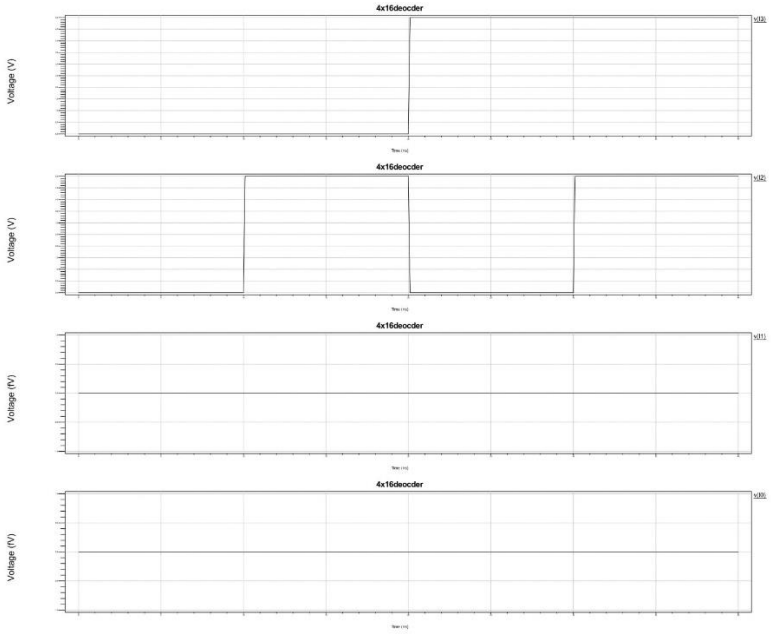
Extracted netlist file is already attached that’s why it will be not shown fully here.

SIMULATION SETTINGS

```
Vpower Vdd Gnd 5V
*IO ve I1 4lük seçim için 00,01,10,11 sırasıyla dene 3 ve 4 elleme.
Vbit1 I0 Gnd dc 0 BIT ({1111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit2 I1 Gnd dc 0 BIT ({1111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

Vbit3 I2 Gnd dc 0 BIT ({0101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0
Vbit4 I3 Gnd dc 0 BIT ({0011}pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n delay=0) AC 0 0 ROUND=0

.include "C:\Users\Ck_sy\Desktop\Programlar\VLSI PROGRAMLAR VE
KURULUMLARI\VLSI_tech_files\SCN_0.25u_CMOS.md"
.tran 40p 40n start=0
*.print tran v(I0) v(I1) v(I2) v(I3)
*.print tran v(q0) v(q1) v(q2) v(q3)
*.print tranv(q4) v(q5) v(q6) v(q7)
*.print tran v(q8) v(q9) v(q10) v(q11)
*.print tran v(q12) v(q13) v(q14) v(q15)
.print tran p(Vpower)
.power Vpower 0 40n
```

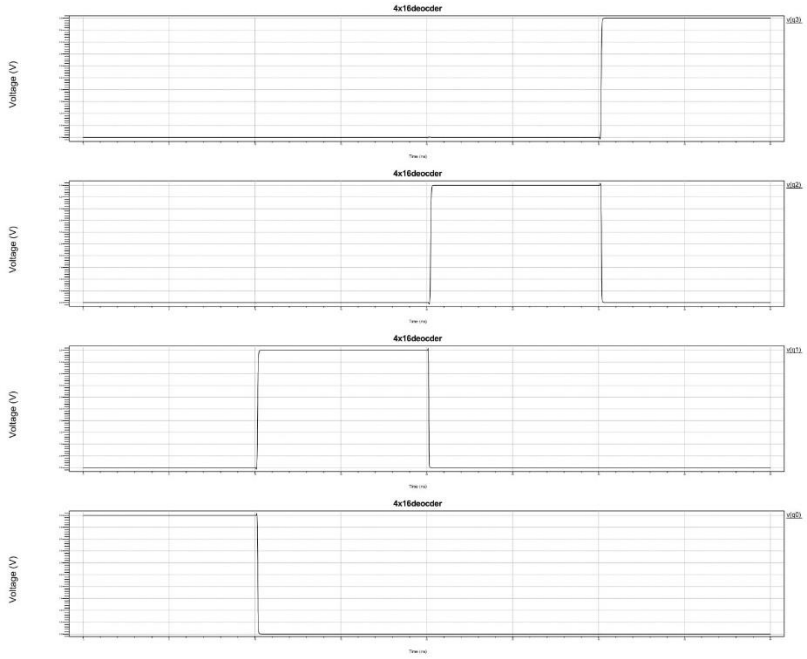
SIMULATION RESULTS

Decoder Inputs and Outputs

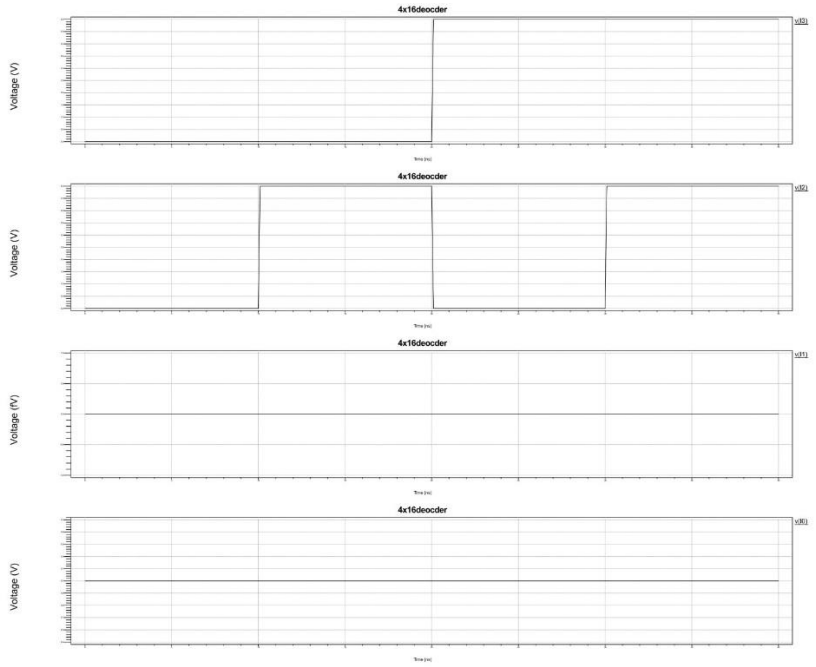


Şekil 14 Input I1 and I0 is "00"

I1 and I0 are “00” so, this will enable the outputs q0-q3.

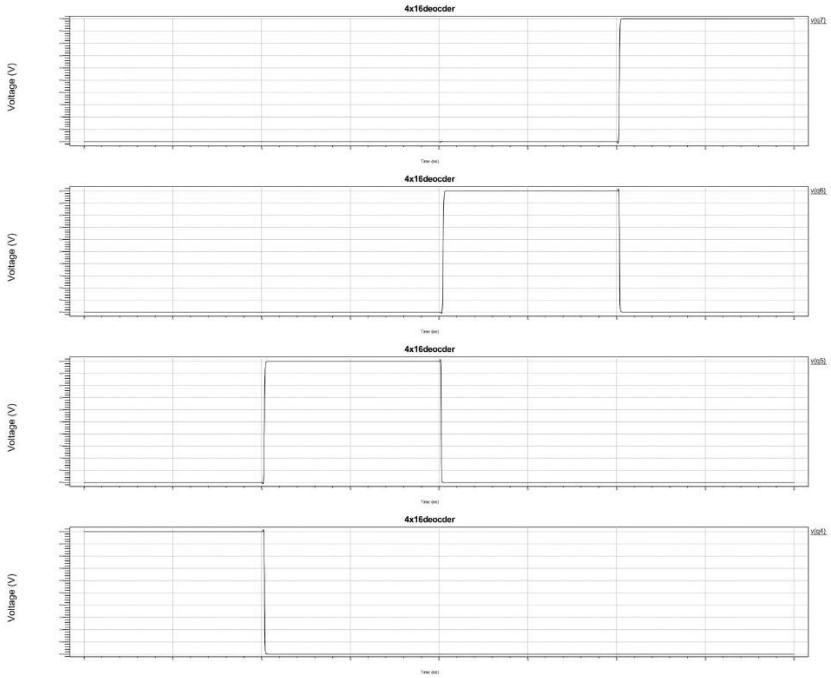


Şekil 15 Outputs q0-q3

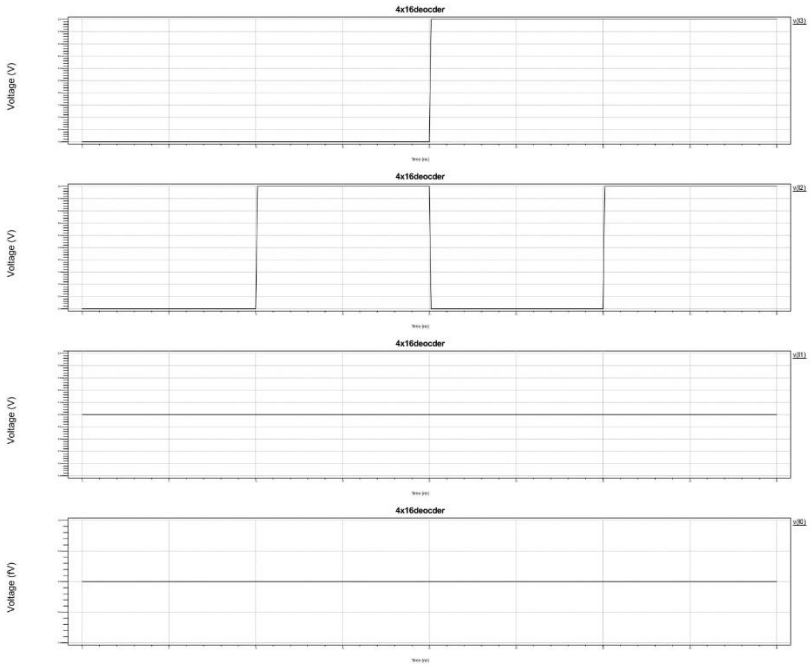


Şekil 16 Input I1 and I0 is "01"

I1 and I0 are “01” so, this will enable the outputs q4-q7.

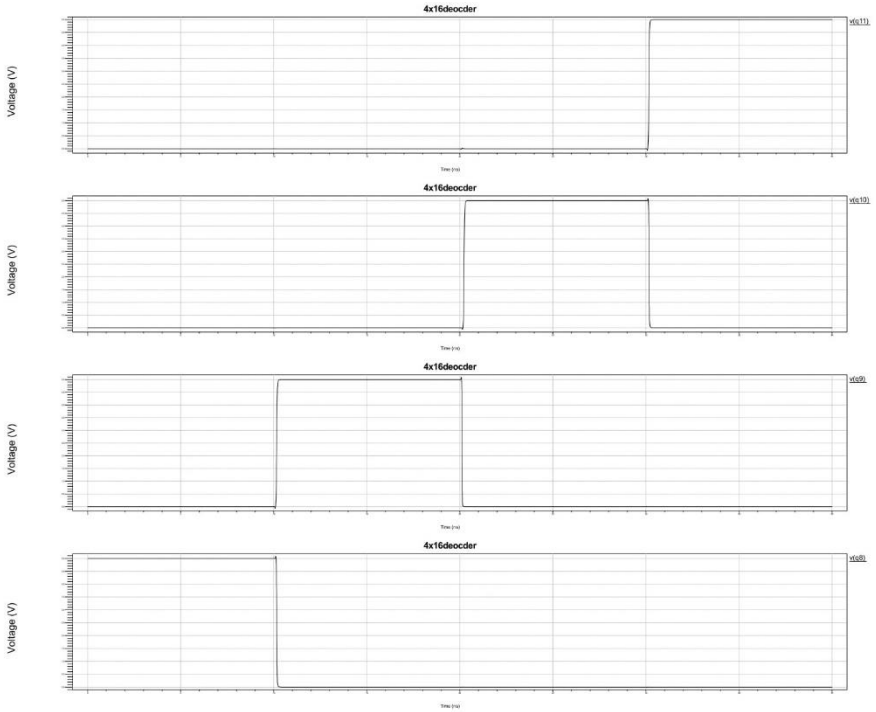


Şekil 17 Outputs q4-q7

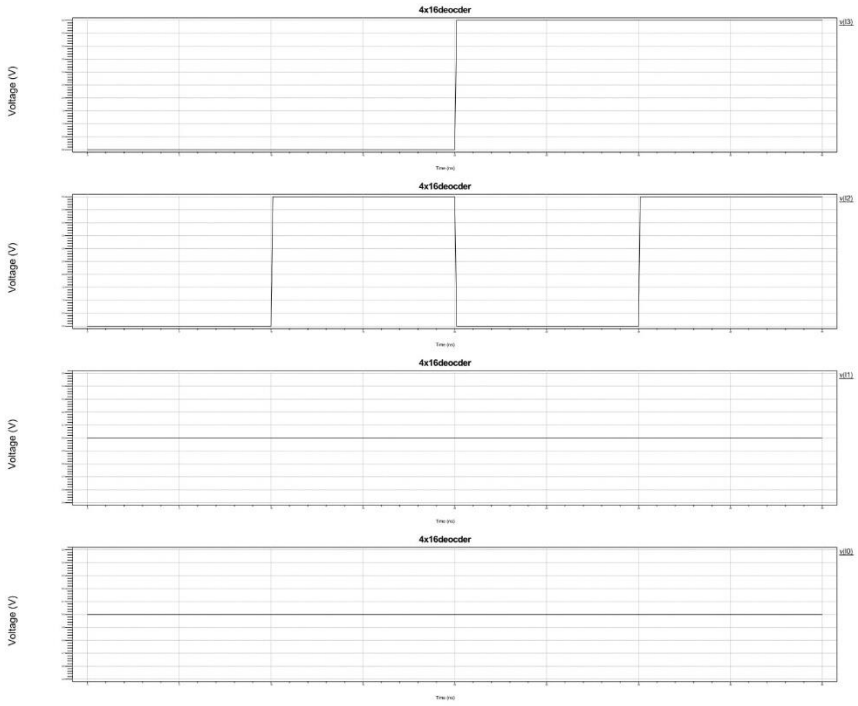


Şekil 18 Input I1 and I0 is "10"

I1 and I0 are “10” so, this will enable the outputs q8-q11.

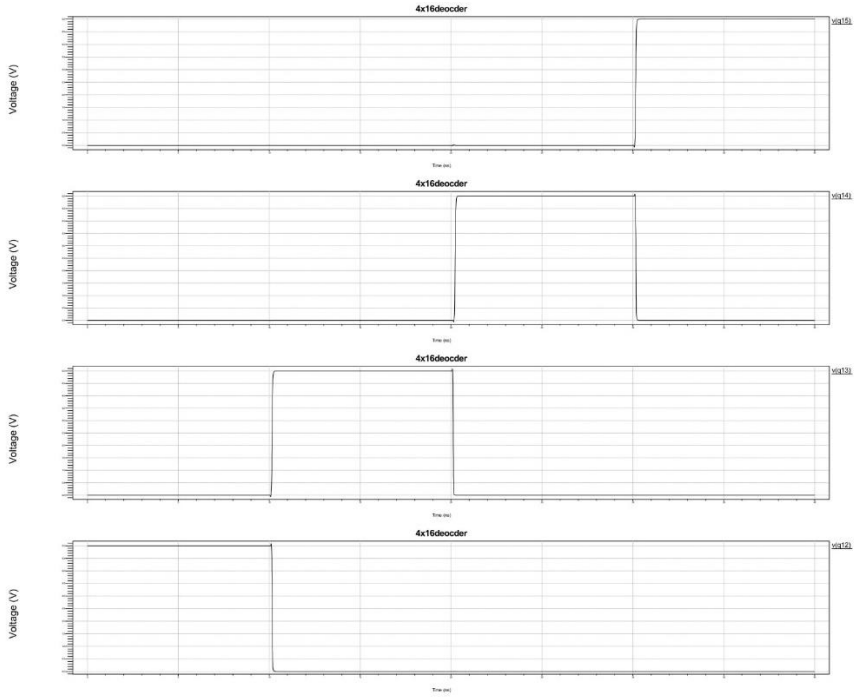


Şekil 19 Outputs q8-q11



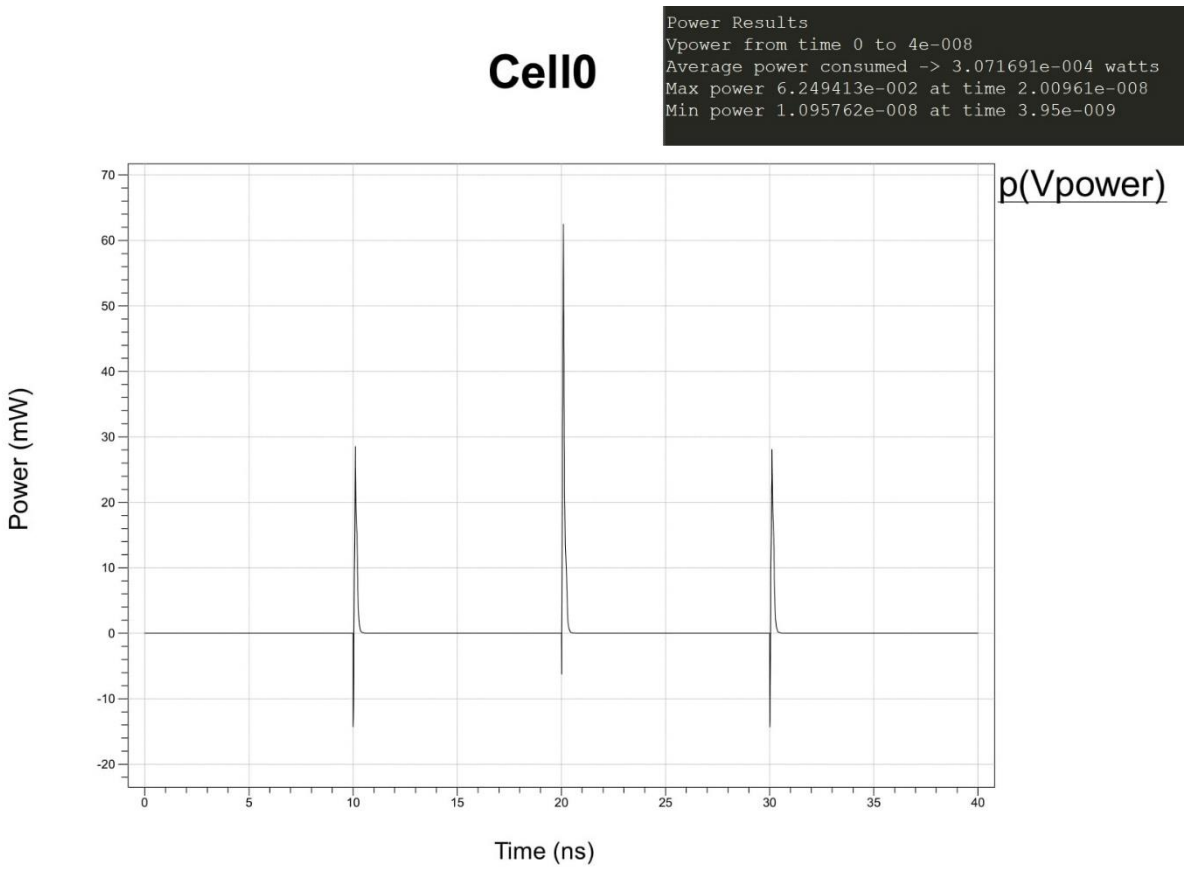
Şekil 20 Input I1 and I0 is "11"

I1 and I0 are “11” so, this will enable the outputs q12-q15.



Şekil 21 Outputs q12-q15

Power Analysis



Şekil 22 Peak and Average Power