	idle	load	precRes	signedMult	unsignedMult	multKernelS	multDone	exepByDiv0	overflow d	livisorX2	loadCnt1	savelterLoop	divKernelS	computeQ	wait4signals	correctDown	correctUp	saveQl	saveQ	loadIterLoop	remCor	divDone	reset
reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
pDR en	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rev_en	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sumL_sel	0 0	0 0	0 0	0 0	0.0	0 1	0 0	0 0	0 0	0 0	0 0	0.0	10	0 0	0.0	0 0	0 0	0 0	10	0 0	0 0	0 0	0 0
sumH_sel	0 0	0 0	0 0	0 0	0 0	10	0 0	0 0	0 0	0 0	0 0	0.0	0 1	0 0	0 0	0 0	10	0 0	10	0 0	0 0	0 0	0 0
sumL_en	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0
sumH_en	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
divisor_IShift	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
divisor_en	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
curryH_sel	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
curryL_sel	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
curryH_en	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
curryL_en	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
invBits_shift_en	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
carrySaveA_sel	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0
carrySaveB_sel	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
counterRegn_en	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
counter_sel	0	0	0	0 1	0 0	0	0	0	0	0	10	0	0	0	0	0	0	0	0	11	0	0	0
ldCounter_en	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
counter_upDown	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
counter_en	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0
correction_sel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1 0	1 0	0	0	0	0
sxOp_rxAdd_sel	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
rxOp_rxAdd_sel	0 0	0 0	0 0	0 0	0 0	0 0	0 1	0 0	0 0	0 0	0 0	0 0	10	0 0	0 0	10	10	1 0	1 0	0 0	0 0	0 0	0 0
addMode_sel	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
leftAdd_mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rightAdd_mode	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0
pLr_rShift	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
pLr_en	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
pHq_en	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
done	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
div0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ovf	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0