**实验2-Buliding Basic Elements for IPI**

课程名称:数字逻辑

实验教学学时：

学时 ；

年级/班级：16级6班

分组学生人数：2

专业：软件工程

1. **实验目的**

(1) Use Create and Package IP feature of Vivado to create IP

(2) Simulate and verify IP functionality

(3) Generate the bitstream and verify the functionality in hardware

(4)Mastering how to bound pins.

**二、实验原理或预习内容**

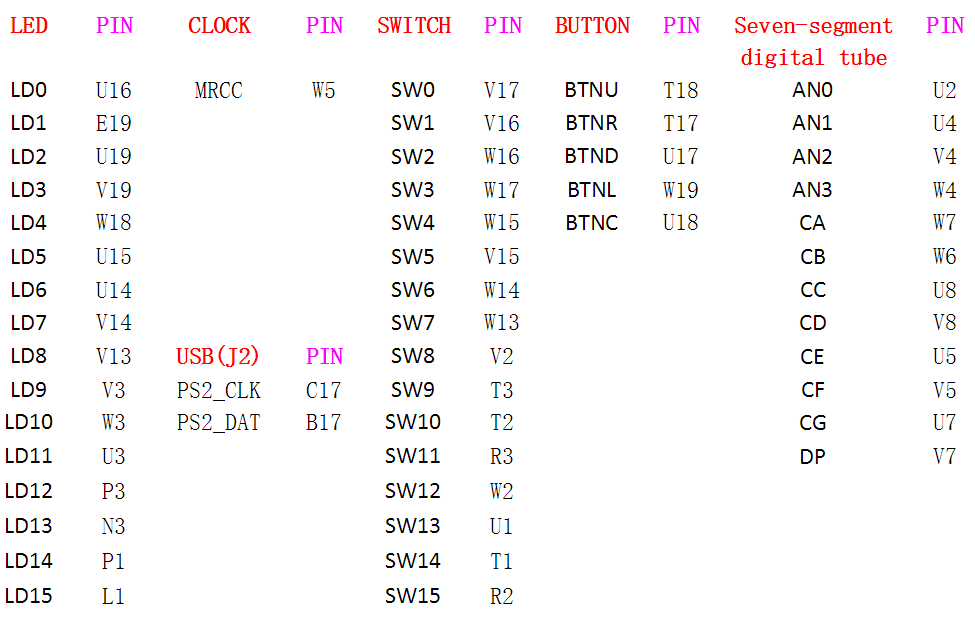
（1）Operating the inputs logcially according to the digital circuit’s rules.The switch is one(true)when it is on and the LED is light when the output is one(right).We can observe the LEDs to test our circuit.

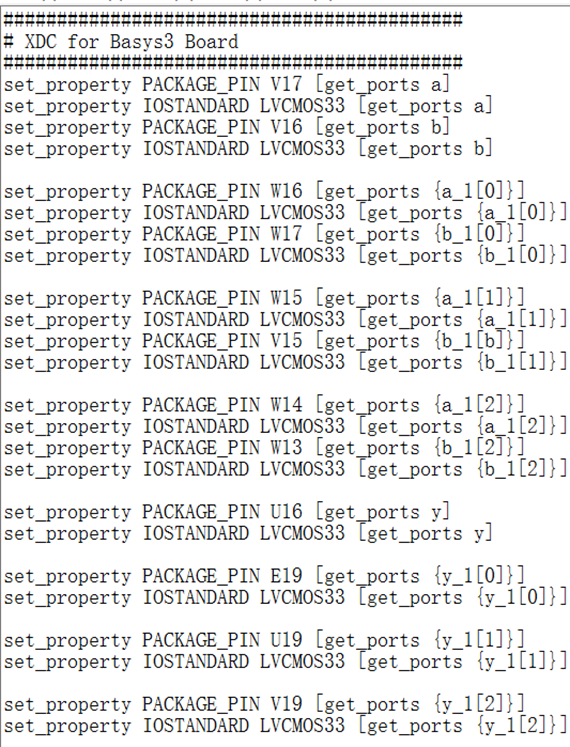
**三、实验环境**

（1）Basys3 board

（2）Vivado

**四、实验内容**

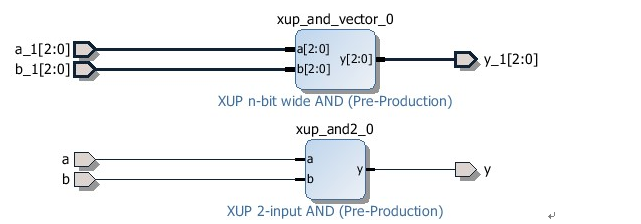
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**As the picture shows,we connect the SW0 to a and the SW1 to b from the first sentence to the fourth sentence, connect the sw2 to a\_1[0] and the sw3 to b\_1[0] from the fifth sentence to the eighth sentence, connect the sw4 to a\_1[1] and the sw5 to b\_1[1] from the ninth sentence to the twelfth sentence,**

**and connect the sw6 to a\_1[2] and the sw7 to b\_1[2] from the thirteenth sentence to the sixteenth sentence.**

**Then the following sentences finish connecting LD0 to y,LD1 to y\_1[0],LD2 to y\_1[1],and LD3 to y\_1[2].**

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The truth tables are listed as follows.

SW0 SW1 LD0 SW2 SW3 LD1 SW4 SW5 LD2

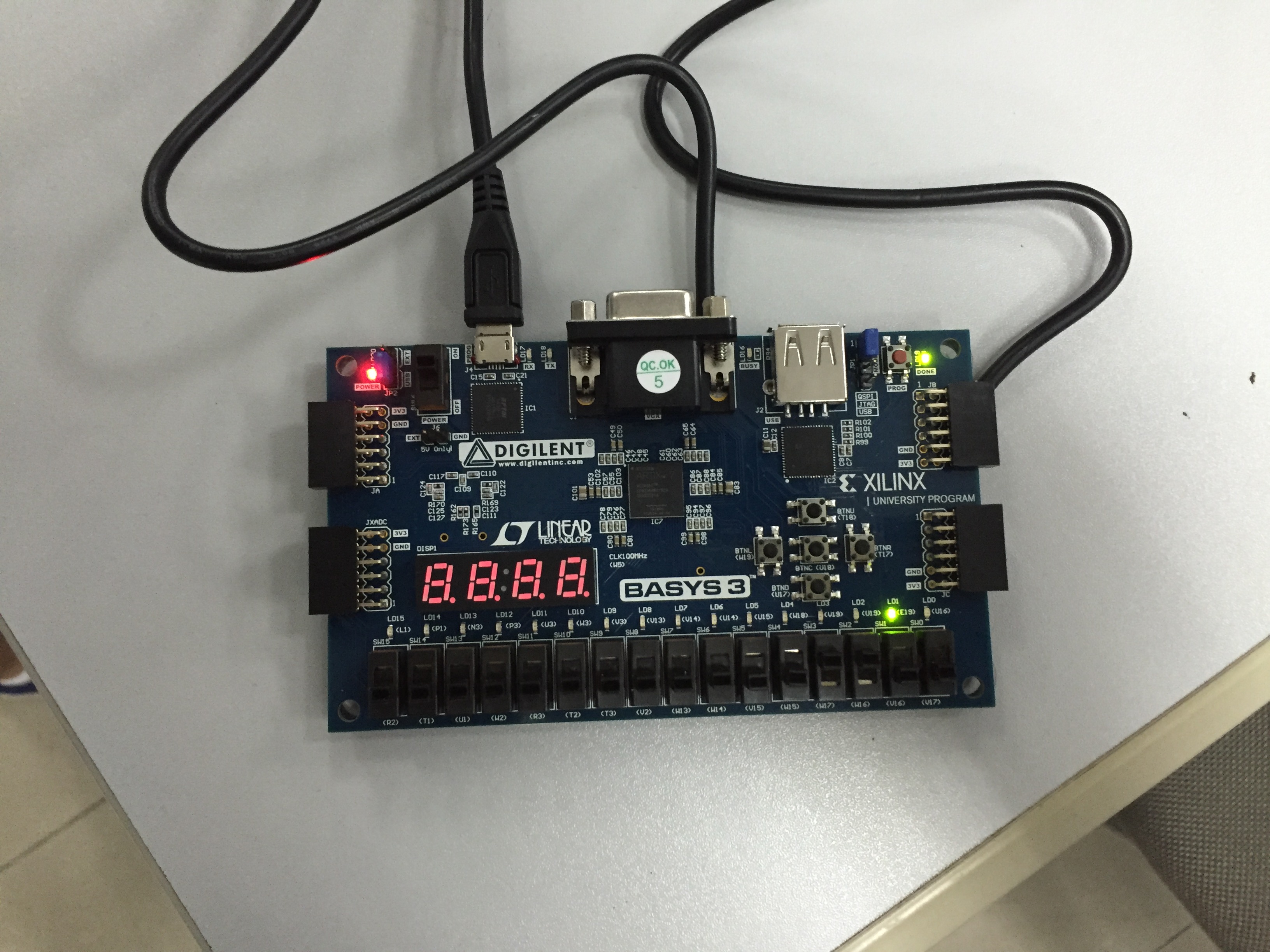
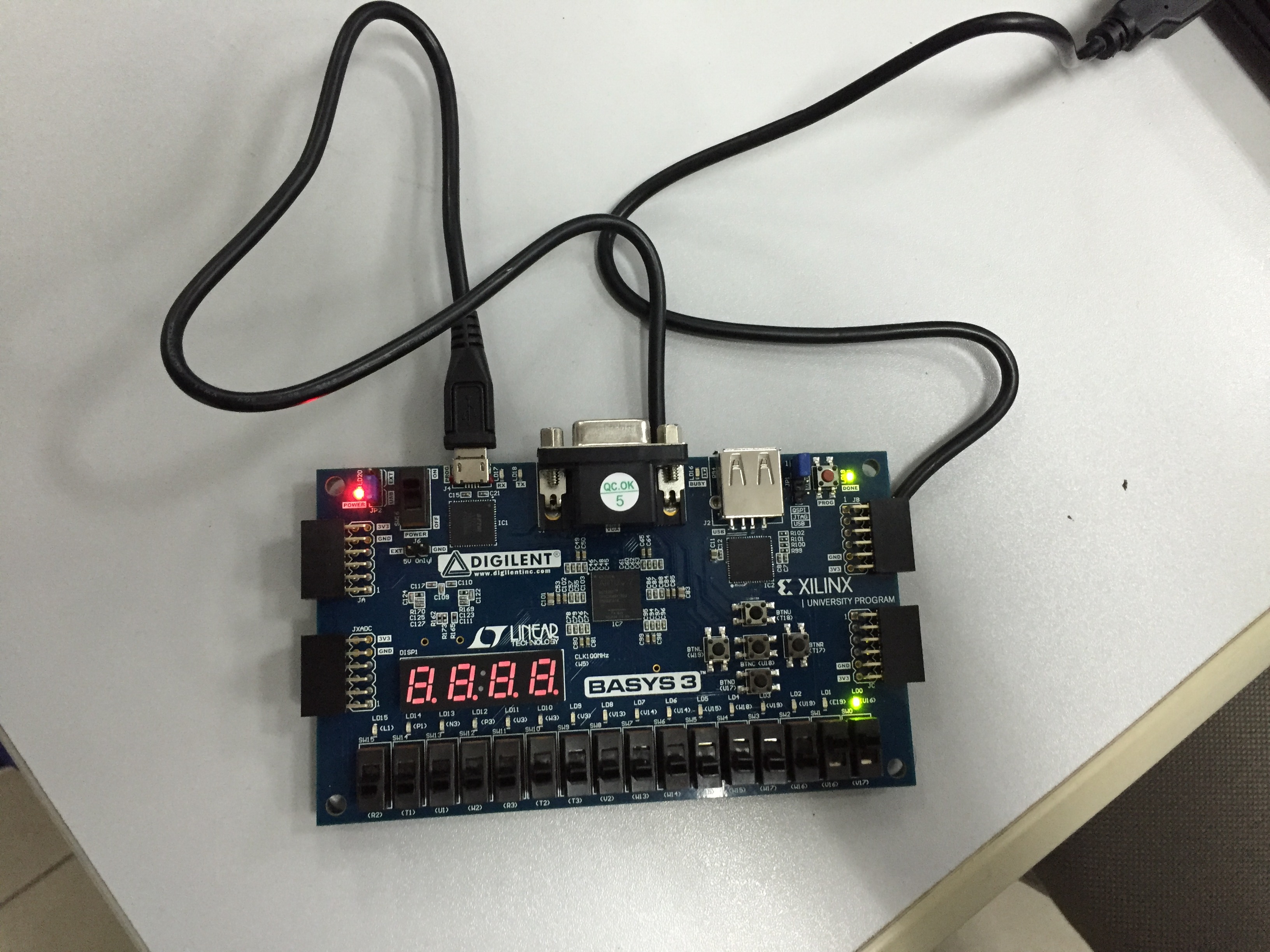
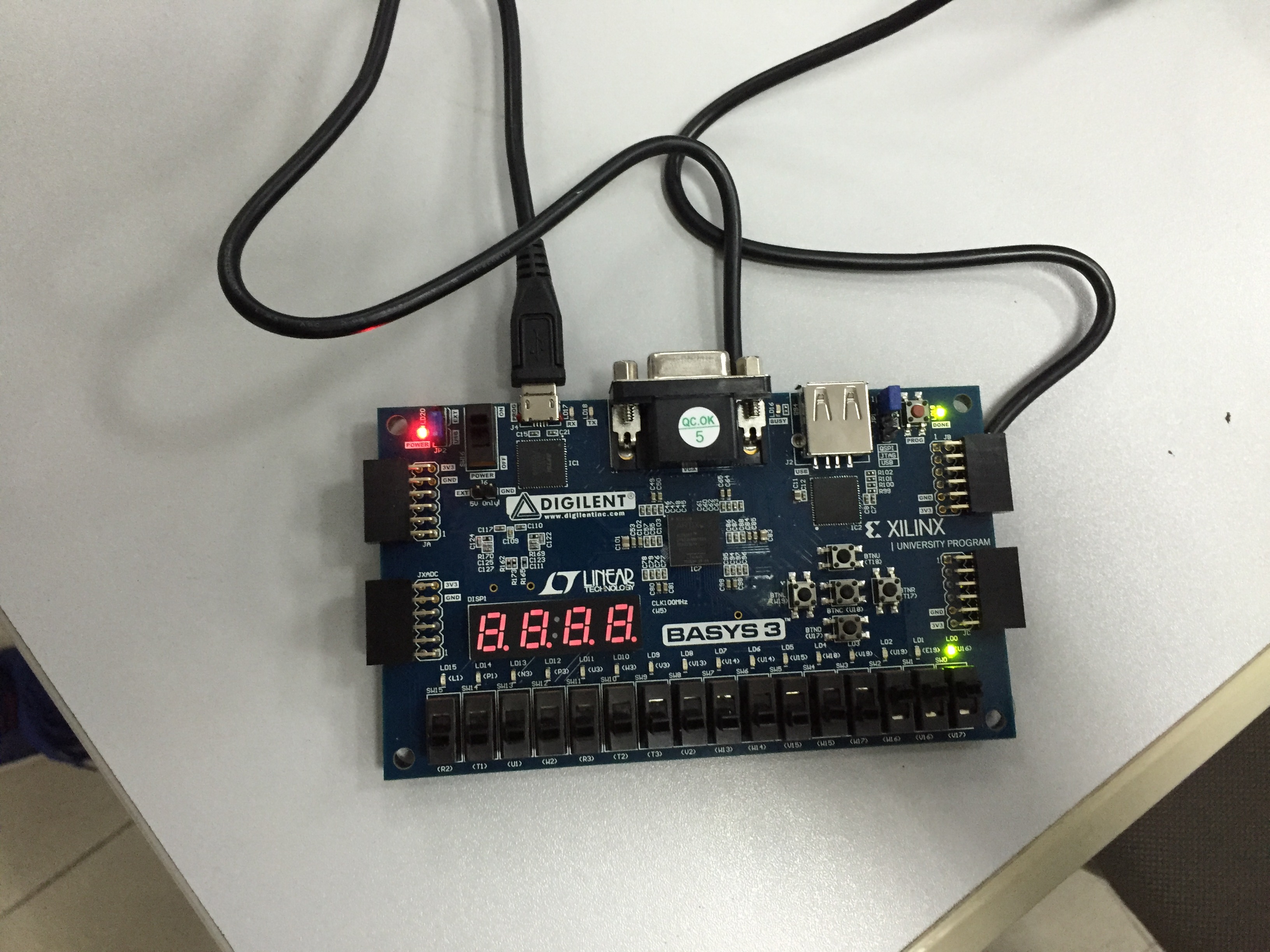
**0 0 0**   **0 0 0 0 0 0**

**0 1 0**   **0 1 0 0 1 0**

**1 1 1**   **1 1 1 1 1 0**

**1 0 0**   **1 0 0 1 0 1**

**The following pictures show us the outputs.**



**五、实验结论及思考题**

（1）According to the outputs of Basys3 board,we can draw a conclusion that we have successed in creating a Vivado project targeting a specific FPGA device located on the Basys3 board,which revealed that The Vivado software tool can be used to perform a complete design flow.

（2）The perfect outputs show that the digital circuit we design can work well and we have successed in bounding pins.