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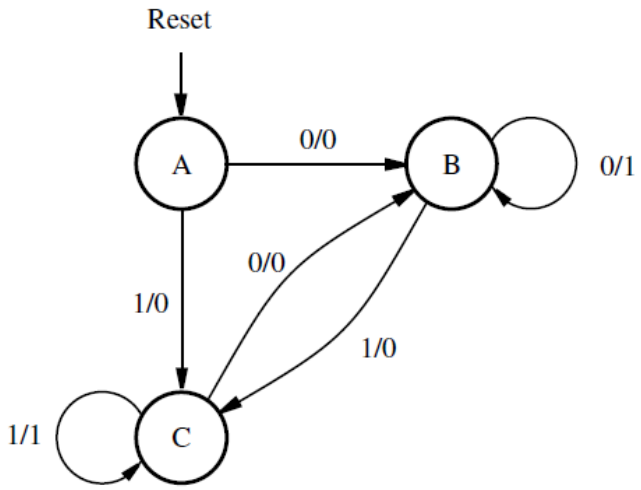
ECE 426/516 **Implementation of VLSI Systems with HDL**
Homework #5 Verilog Code for digital circuits and systems
Due date: March 11th, 2024 11:30 pm

Question 1: Design a Mealy-type FSM that can act as a sequence detector described in the following figure.

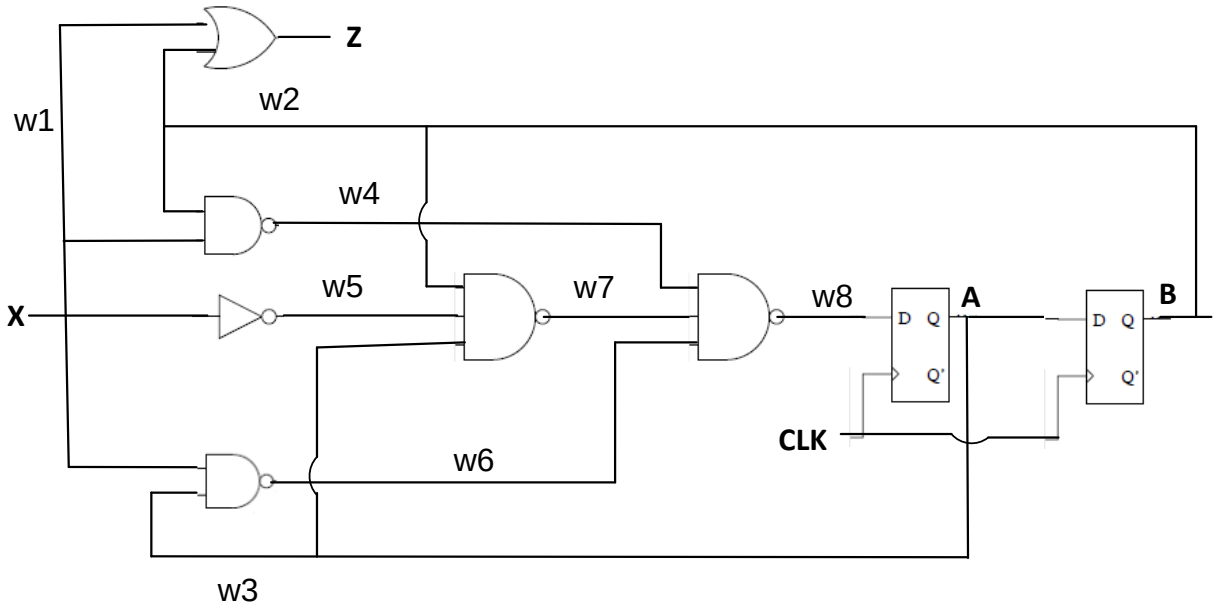


(a) Complete the corresponding state table below.

Present State	Next State		Output	
	W=0	W=1	W=0	W=1
A	B	C	0	0
B	B	C	1	0
C	B	C	0	1

(b) Write Verilog code for this FSM with behavior modeling, instead of gate-level modeling. Simulate your design with a test bench and include your simulation results.

Question 2: A finite state machine shown below has one input, X, and one output, Z, and two state variables, A and B, and a clock input. You may add "set" or "reset" pins to the D Flip-flops to initialize the status of A, and B.



Implement this FSM and its testbench in Verilog. Hand in your code and a printout of part of your simulation showing the correct operation of this FSM.

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To make w8 = 1:


w4 == 0 (b == 1, x == 1)

w7 == 0 (A == 0, x ==1, B == 0)

w6 == 0 (A == 0, x == 0)
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