Arithmetic Circuit Designs with Pipelines

Verilog Lab 6

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Section A: 16-bit adder without pipelining.

```
1  // chase lotito - ece426 lab 6 - adder a
2
3  // Addition of two 16 bits, 2's complement nos., n1 and n2.  All the 16
       bits addition at one stroke without any pipeline.
4  // Result is 17 bits.
5
6  `timescale 1us / 1us
7
8  module adder_a (clk, n1, n2, sum);
9
10 // i/o
11 input clk;
12 input [15:0] n1, n2;
13 output [16:0] sum ;
14
15 reg [16:0] sum;
16 wire [16:0] sum_i;
17
18 assign sum_i = {n1[15], n1} + {n2[15], n2};    // Add after sign
       extension - Result (i).
19
20 // Frequency of operation is not relevant since this is a combination
       circuit.
21 // Pipeline 1, clk (1), register final result (i).
22 always @ (posedge clk) begin
23     sum <= sum_i;
24 end
25
26 endmodule
```

```
1  // Test bench for adder_a design
2
3  `define CLKPERIODBY2 5 // Operate at 50 MHz.
4
5  `timescale 1us / 1us
6  `include "adder_a.v" // This is the design.
7
8  module adder_a_testbench;
9
```

```
10 reg clk;
11 reg [15:0] n1;
12 reg [15:0] n2;
13 wire [16:0] sum;
14
15 adder_a U1 (.clk(clk), .n1(n1), .n2(n2), .sum(sum) );
16
17 // GTKWAVE (waveform simulator)
18 initial begin : GTKWAVE
19     $dumpfile("adder_a.vcd");
20     $dumpvars(0, adder_a_testbench);
21 end
22
23 initial begin // Apply different sets of inputs.
24     clk = 1'b0; n1 = 16'h0; n2 = 16'h0;
25
26     #10 n1 = 16'h0001; n2 = 16'h0101;
27     #10 n1 = 16'h0fff; n2 = 16'h0fff;
28     #10 n1 = 16'h7fff; n2 = 16'h7fff;
29     #10 n1 = 16'h8000; n2 = 16'h8000;
30     #10 n1 = 16'h0001; n2 = 16'h0001;
31     #10 n1 = 16'hffff; n2 = 16'h0001;
32     #10 n1 = 16'h7fff; n2 = 16'h7fff;
33     #10 n1 = 16'h5555; n2 = 16'haaaa;
34     #10 n1 = 16'h0000; n2 = 16'h0000;
35
36     #20 $finish;
37 end
38
39 initial $monitor("[%0t us] clk =%b n1 = %h n2 = %h sum = %h", $time,
       clk, n1, n2, sum);
40
41 always #`CLKPERIODBY2 clk <= ~clk;  // Toggle the clock.
42
43 endmodule
```

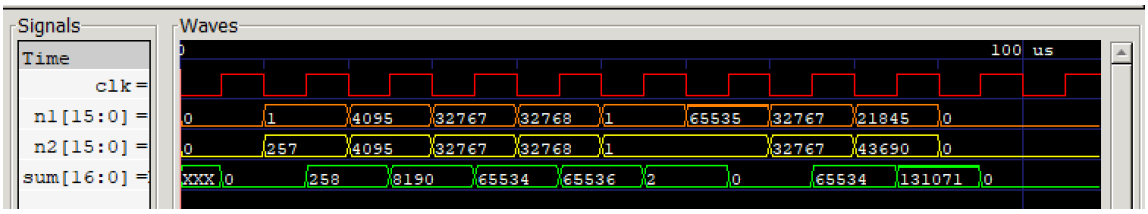

Figure 1: Adder A Waveforms

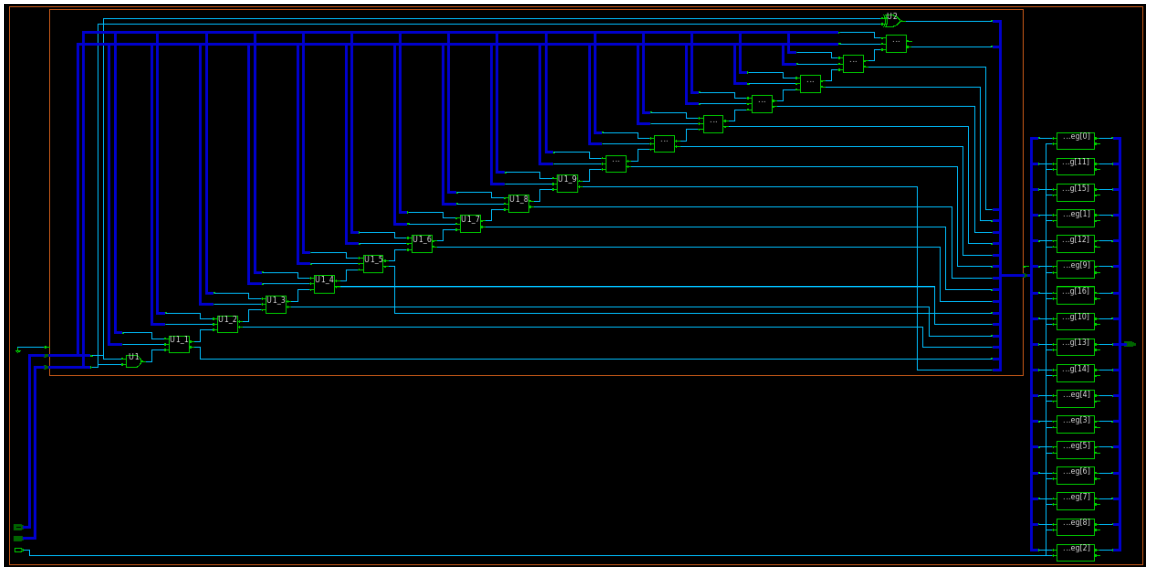

Figure 2: Adder A Circuit

```
****************************************
Report : area
Design : adder_a
Version: S-2021.06-SP5-4
Date   : Sat Apr 27 16:40:54 2024
****************************************

Library(s) Used:

    saed90nm_max (File: /synopsys/GPDK/SAED_ED

Number of ports:                          103
Number of nets:                           135
Number of cells:                           37
Number of combinational cells:             18
Number of sequential cells:                17
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:                493.055992
Buf/Inv area:                        0.000000
Noncombinational area:             423.014395
Macro/Black Box area:                0.000000
Net Interconnect area:              18.859402

Total cell area:                   916.070387
Total area:                        934.929789
1
```

Figure 3: Adder A Area Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : adder_a
Version: S-2021.06-SP5-4
Date   : Sat Apr 27 16:41:01 2024
****************************************

Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

  Startpoint: sum_reg[16]
              (rising edge-triggered flip-flop)
  Endpoint: sum[16] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  adder_a            8000                  saed90nm_max

  Point                                    Incr       Path
  -----------------------------------------------------------
  sum_reg[16]/CLK (DFFX1)                  0.00       0.00 r
  sum_reg[16]/Q (DFFX1)                    0.63       0.63 f
  sum[16] (out)                            0.00       0.63 f
  data arrival time                                   0.63
  -----------------------------------------------------------
  (Path is unconstrained)
```

Figure 4: Adder A Timing Report

Section B: 16-bit adder with pipelining.

```
1  // chase lotito - ece426 lab 6 - adder b
2  // Addition of two 16 bit, 2's complement nos., n1 and n2. 8 bits
       addition at a time. Result is 17 bits.
3
4  module adder_b ( clk, n1, n2, sum);
5
6  // i/o
7  input clk;
8  input [15:0] n1;
9  input [15:0] n2;
10 output [16:0] sum;
11
12 reg [16:0] sum;
13 wire [8:0] sum_LSB;
14 reg [8:0] sum_LSB_1;
15
16 reg [15:8] n1_reg1;
17 reg [15:8] n2_reg1;
18
19 wire [16:8] sum_MSB;
20 wire [16:0] sum_next;
21
22 assign sum_LSB = n1[7:0] + n2[7:0]; // Add least significant byte.
       sum_LSB [8] is the carry.
23
24 always @ (posedge clk)  // Pipeline 1, clk (1), register LSB to
       continue addition of MSB.
25 begin
26     sum_LSB_1 <= sum_LSB;   // Preserve LSB sum
27     n1_reg1 <= n1[15:8];    // Preserve MSBs
28     n2_reg1 <= n2[15:8];
29 end
30
31 // Extend sign & add msbs with carry.
32 assign sum_MSB = {n1_reg1[15], n1_reg1[15:8]} + {n2_reg1[15], n2_reg1
       [15:8]} + sum_LSB_1 [8];// Add MSBs with carry.
33 assign sum_next = {sum_MSB, sum_LSB_1 [7:0]};
34
35 always @ (posedge clk)// Pipeline 2, clk (2), register result.
36 begin
37     sum <= sum_next;
38 end
39
40 endmodule
```

```
// chase lotito - ece426 adder_b testbench

`define CLKBYPERIOD2 5// Operate at 50 MHz.
`include "adder_b.v" // This is the design.

module adder_b_testbench;

reg clk;
reg [15:0] n1;
reg [15:0] n2;

wire [16:0] sum;

adder_b U1 (.clk(clk), .n1(n1), .n2(n2), .sum(sum) );

// GTKWAVE (waveform simulator)
initial begin : GTKWAVE
    $dumpfile("adder_b.vcd");
    $dumpvars(0, adder_b_testbench);
end

initial begin// Apply different sets of inputs.
 clk = 1'b0; n1 = 16'h0; n2 = 16'h0;

 #10 n1 = 16'h0001; n2 = 16'h0101;
 #10 n1 = 16'h0fff; n2 = 16'h0fff;
 #10 n1 = 16'h7fff; n2 = 16'h7fff;
 #10 n1 = 16'h8000; n2 = 16'h8000;
 #10 n1 = 16'h0001; n2 = 16'h0001;
 #10 n1 = 16'hffff; n2 = 16'h0001;
 #10 n1 = 16'h7fff; n2 = 16'h7fff;
 #10 n1 = 16'h5555; n2 = 16'haaaa;
 #10 n1 = 16'h0000; n2 = 16'h0000;

 #10 $stop;
 $finish;
end

initial $monitor("[%0t us] clk =%b n1 = %h n2 = %h sum = %h", $time,
    clk, n1, n2, sum);

always #`CLKBYPERIOD2 clk <= ~clk;// Toggle the clock.

endmodule
```

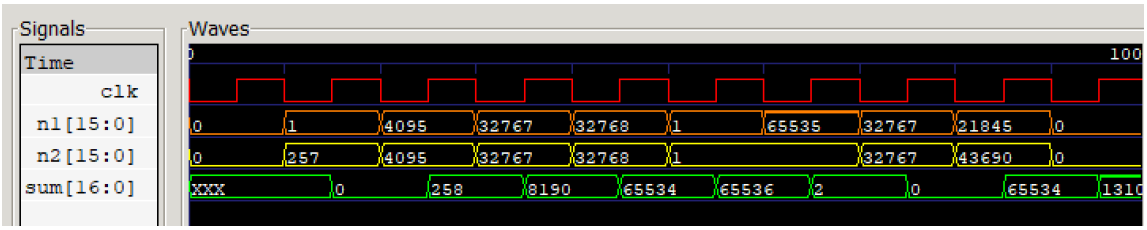

Figure 5: Adder B Waveforms

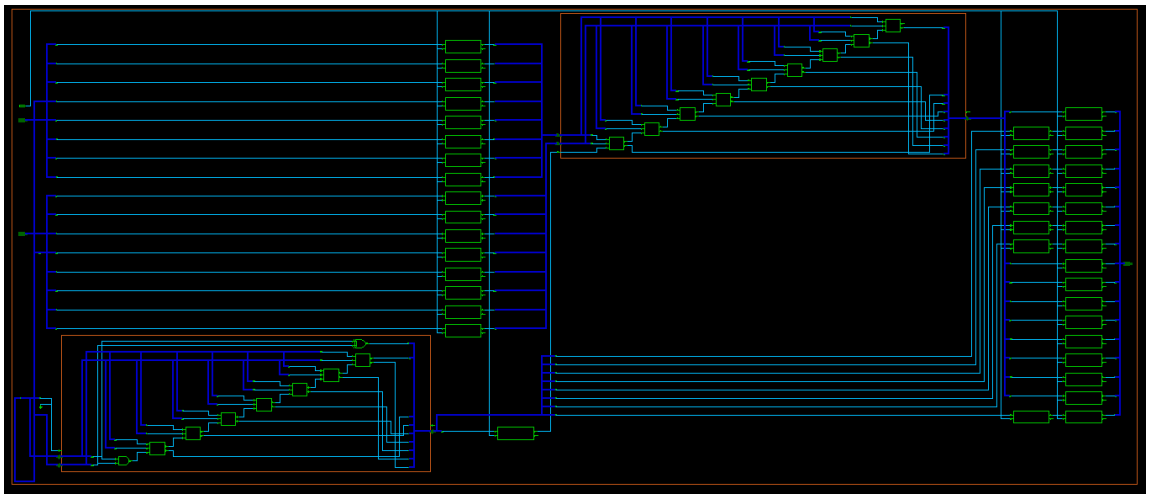

Figure 6: Adder B Circuit

```
****************************************
Report : area
Design : adder_b
Version: S-2021.06-SP5-4
Date   : Sat Apr 27 16:44:27 2024
****************************************

Information: Updating design information... (U
Library(s) Used:

    saed90nm_max (File: /synopsys/GPDK/SAED_ED

Number of ports:                          108
Number of nets:                           162
Number of cells:                           63
Number of combinational cells:             18
Number of sequential cells:                42
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       3

Combinational area:                493.055992
Buf/Inv area:                        0.000000
Noncombinational area:            1045.094387
Macro/Black Box area:                0.000000
Net Interconnect area:              44.824272

Total cell area:                  1538.150379
Total area:                       1582.974651
1
```

Figure 7: Adder B Area Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : adder_b
Version: S-2021.06-SP5-4
Date   : Sat Apr 27 16:44:29 2024
****************************************

Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

  Startpoint: sum_reg[16]
              (rising edge-triggered flip-flop)
  Endpoint: sum[16] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  adder_b            8000                  saed90nm_max

  Point                                    Incr       Path
  -----------------------------------------------------------
  sum_reg[16]/CLK (DFFX1)                  0.00       0.00 r
  sum_reg[16]/Q (DFFX1)                    0.63       0.63 f
  sum[16] (out)                            0.00       0.63 f
  data arrival time                                   0.63
  -----------------------------------------------------------
```

Figure 8: Adder B Timing Report