ECE 447/547 (Semiconductor Devices)

Southern Illinois University Carbondale

Designing an n-Type MOSFET using a Simulator

Using the MOSFET simulator on nanoHUB (https://nanohub.org/tools/mosfet/) design an *n-type* silicon MOSFET that would meet the following figures-of-merits:

ON current (for $V_G = V_D = 0.8V$) $\geq 600\ \mu A/\mu m$
OFF current (for $V_G = 0V$, $V_D = 0.8V$) $\leq 10\ \mu A/\mu m$
Subthreshold Swing, $S \leq 200$ mV/dec
Drain Induced Barrier Lowering (DIBL) ≤ 250 mv/V

For your design, use the following specifications:

On the "Structural Properties" phase:
Doping density: *Uniform*
Channel length = 22 nm
Oxide thickness ≥ 0.7 nm
S/D length = 2×Channel length
Junction depth = Channel length
Substrate thickness = 50 nm
Device width = 1000 nm
S/D doping concentration = 2×10^{20} cm^{-3}
Channel doping concentration $\leq 1\times10^{19}$ cm^{-3}
Substrate doping concentration = 5×10^{16} cm^{-3}

On the **"Model" phase**, carefully look through the input parameters. Use the following:
Gate type: *n*+ polysilicon
Activate the following models (set 'yes'):
Concentration dependent scattering (ionized impurity scattering)
Vertical field dependent mobility (this takes care of surface roughness)
Parallel field dependence

On the "Voltage Sweep" phase:
Maximum supply voltage (V_G and V_D) = 0.8 V
Note that you need to obtain two curves for the I_D-V_{GS} characteristic, for V_D = 0.05 and 0.8 V. Also, sweep your gate voltage from -0.5V to 0.8 V (threshold voltage can be negative with *n*+ polysilicon gates!).
Plot along length = "yes"
Plot along depth = "yes"
Where to plot 1-D plots along length ≡ 2 nm
Where to plot 1-D plots along depth ≡ 55 nm

Hints:
You should mainly be adjusting (fine-tuning) "oxide thickness" and/or "channel doping density".
If you see no I_D-V_{GS} curves in the output drop-down menu (that is, the simulation has some convergence issues), you need to rerun the simulation with little different values.

Report:

1) Using appropriate equations/formulae (from textbook or lecture notes) and the device parameters used in your calculations, *analytically* calculate the following:
    a. Threshold voltage, V_{th}
    b. ON current
    c. OFF current
2) Are the results obtained from (1) different from those that you extracted from simulation? Why or why not? Comment specifically on V_{th}.
3) Comment on the following: When designing a nanoscale MOSFET, why (or how) do engineers consider public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (if applicable)?
4) Read the attached document on Engineering Ethics. Why do you think it is important to consider ethics (identifying the important and relevant ones) in engineering design projects?

Attach appropriate images/figures with your write-up.