SOUTHERN ILLINOIS UNIVERSITY
CARBONDALE

ECE 426 Implementation of VLSI Systems

Lab 3: Ripple-Carry and Carry-Lookahead Adders

Performed by:

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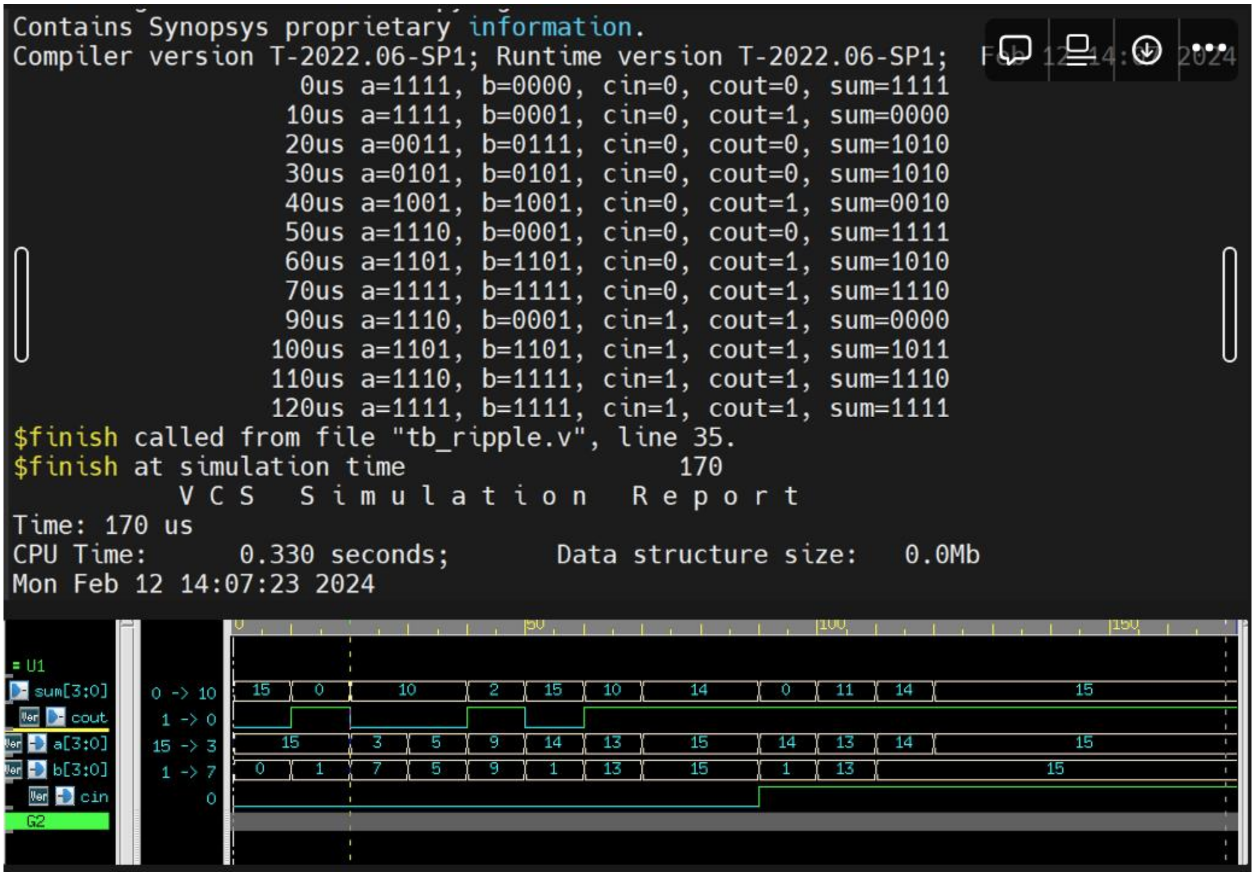
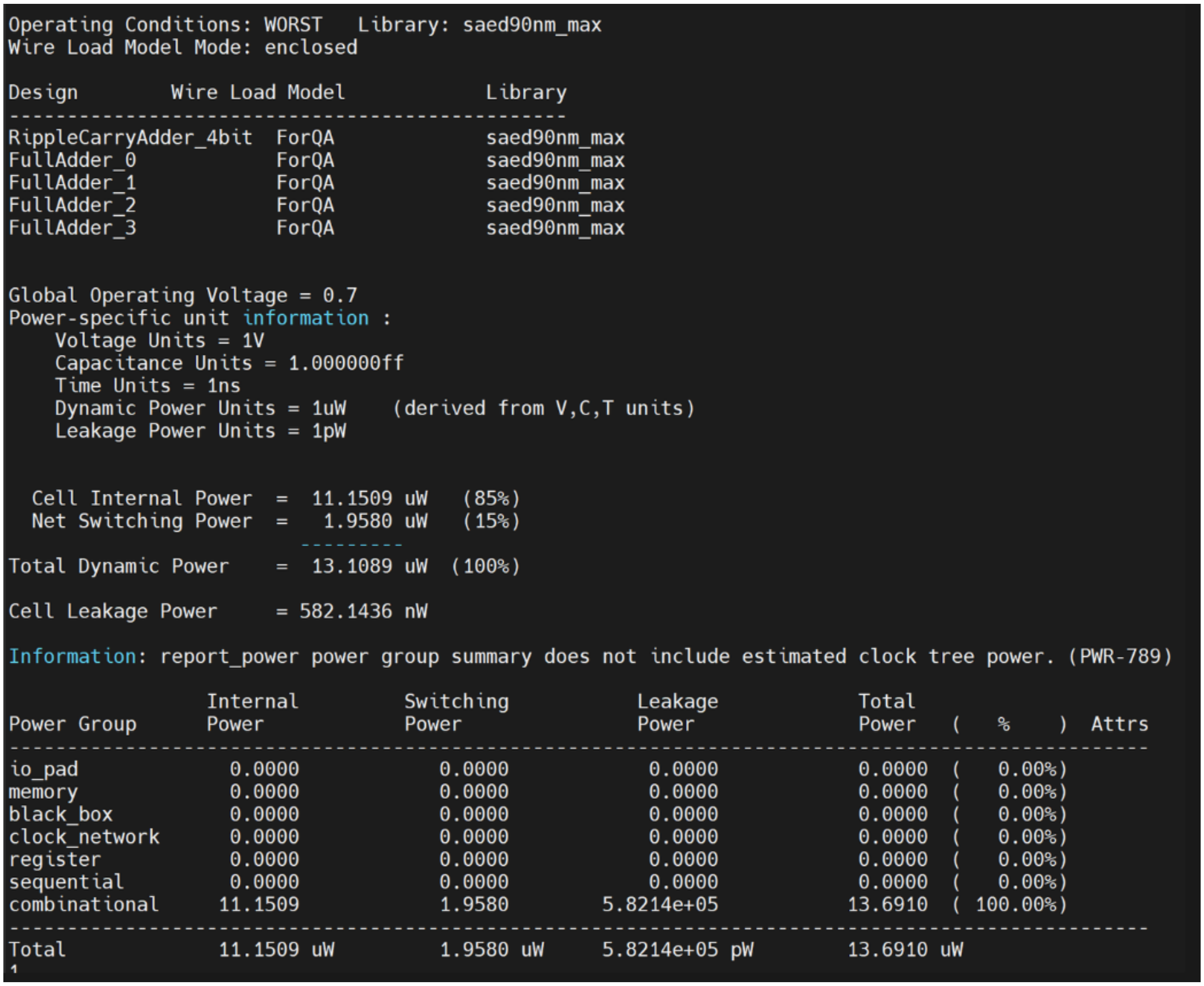
Ripple-Carry Adder Demo



```
Contains Synopsys proprietary information.
Compiler version T-2022.06-SP1; Runtime version T-2022.06-SP1;  F    12  4:   2024
                      0us a=1111, b=0000, cin=0, cout=0, sum=1111
                     10us a=1111, b=0001, cin=0, cout=1, sum=0000
                     20us a=0011, b=0111, cin=0, cout=0, sum=1010
                     30us a=0101, b=0101, cin=0, cout=0, sum=1010
                     40us a=1001, b=1001, cin=0, cout=1, sum=0010
                     50us a=1110, b=0001, cin=0, cout=0, sum=1111
                     60us a=1101, b=1101, cin=0, cout=1, sum=1010
                     70us a=1111, b=1111, cin=0, cout=1, sum=1110
                     90us a=1110, b=0001, cin=1, cout=1, sum=0000
                    100us a=1101, b=1101, cin=1, cout=1, sum=1011
                    110us a=1110, b=1111, cin=1, cout=1, sum=1110
                    120us a=1111, b=1111, cin=1, cout=1, sum=1111
$finish called from file "tb_ripple.v", line 35.
$finish at simulation time                  170
           V C S   S i m u l a t i o n   R e p o r t
Time: 170 us
CPU Time:      0.330 seconds;       Data structure size:   0.0Mb
Mon Feb 12 14:07:23 2024
```

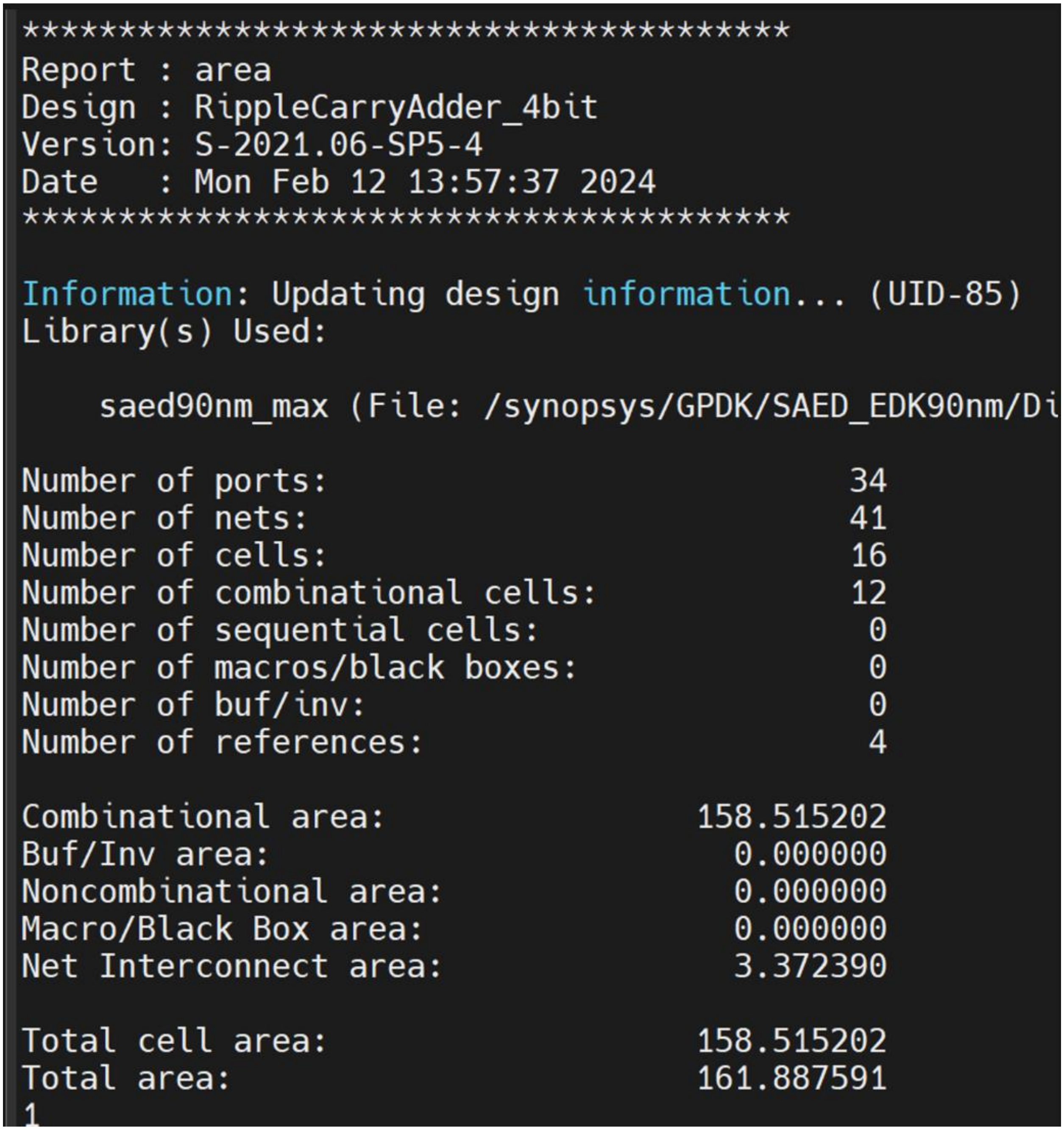
Figure 1: Ripple-Carry Simulation



```
Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
RippleCarryAdder_4bit  ForQA             saed90nm_max
FullAdder_0            ForQA             saed90nm_max
FullAdder_1            ForQA             saed90nm_max
FullAdder_2            ForQA             saed90nm_max
FullAdder_3            ForQA             saed90nm_max


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  11.1509 uW   (85%)
  Net Switching Power  =   1.9580 uW   (15%)
                         ---------
Total Dynamic Power    =  13.1089 uW  (100%)

Cell Leakage Power     = 582.1436 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.0000           0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational     11.1509           1.9580        5.8214e+05           13.6910  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             11.1509 uW        1.9580 uW     5.8214e+05 pW        13.6910 uW
```

Figure 2: Ripple-Carry Power

e



```
****************************************
Report : area
Design : RippleCarryAdder_4bit
Version: S-2021.06-SP5-4
Date   : Mon Feb 12 13:57:37 2024
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_max (File: /synopsys/GPDK/SAED_EDK90nm/Di

Number of ports:                           34
Number of nets:                            41
Number of cells:                           16
Number of combinational cells:             12
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       4

Combinational area:                158.515202
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:               3.372390

Total cell area:                   158.515202
Total area:                        161.887591
1
```

Figure 3: Ripple-Carry Area

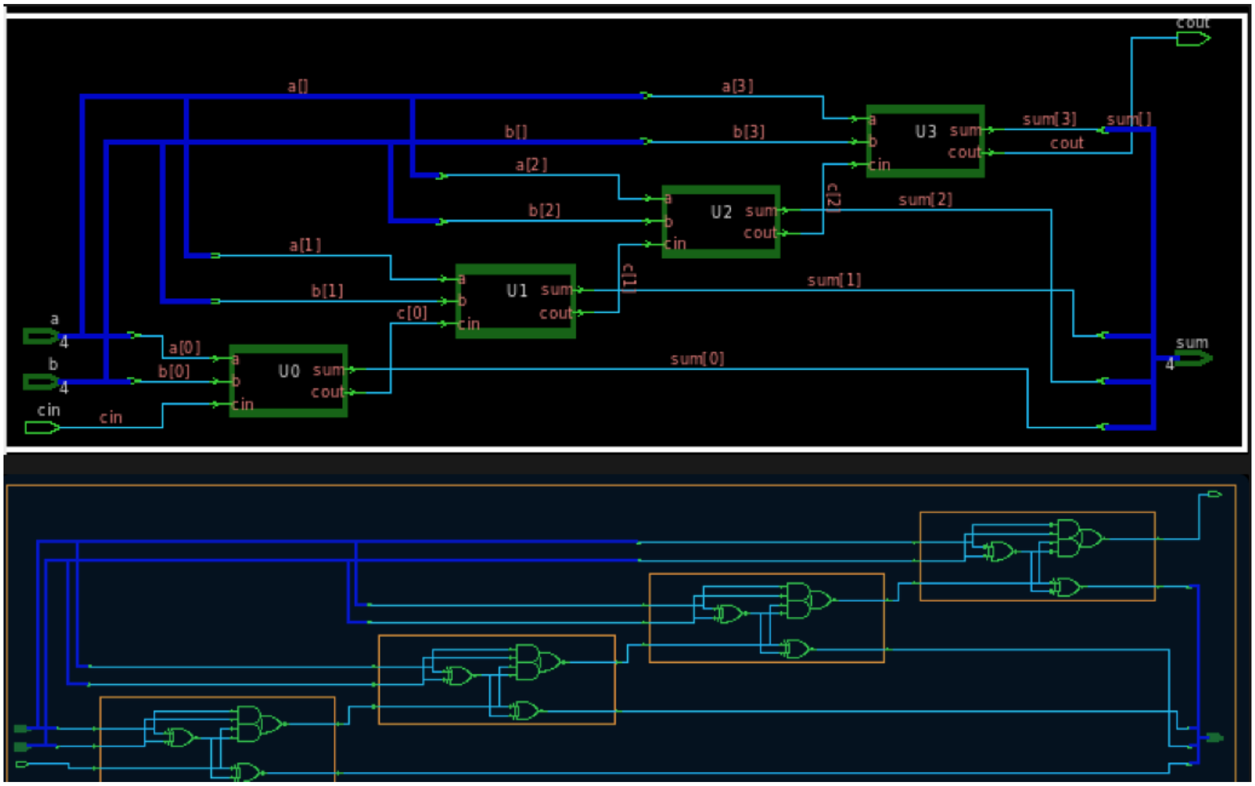
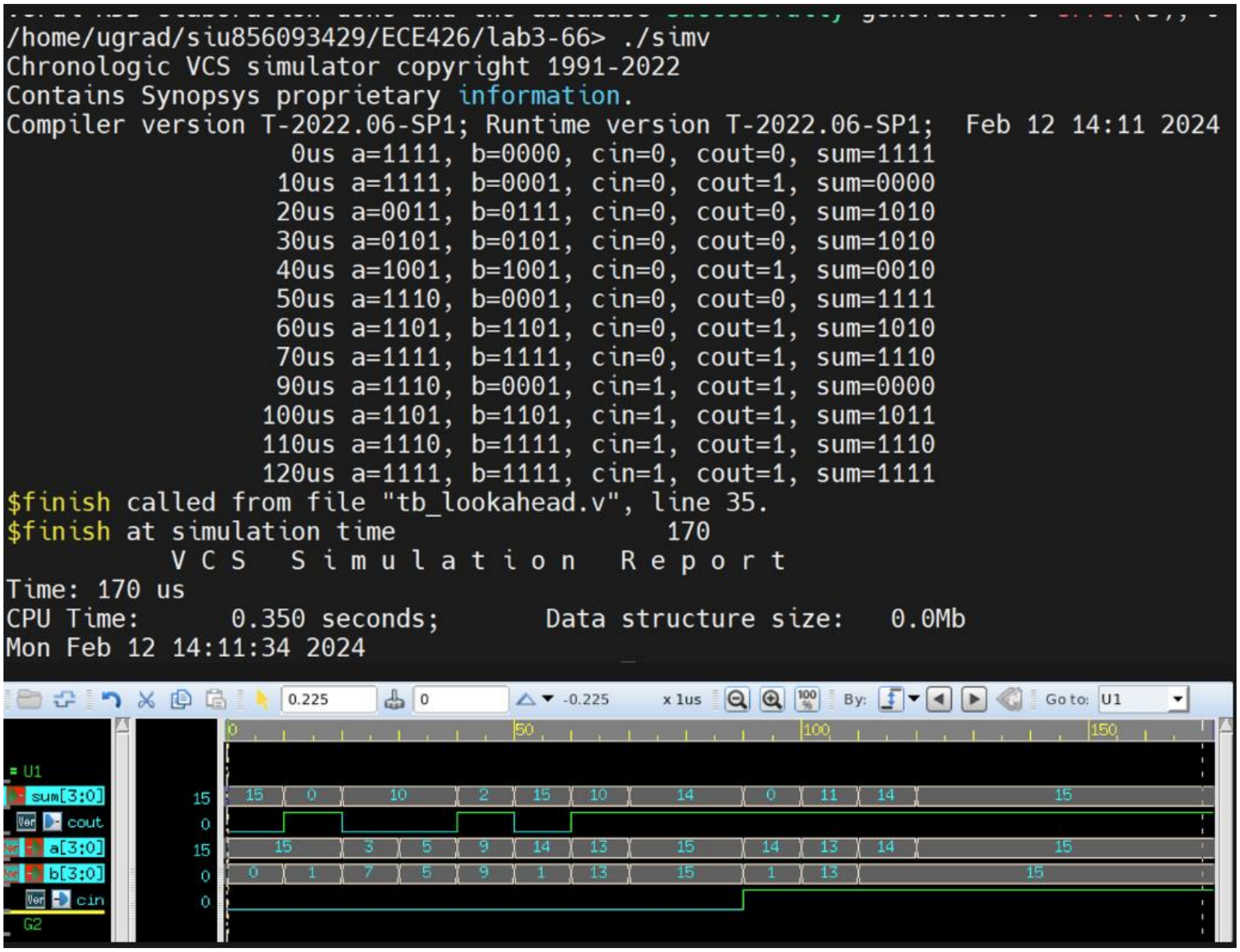


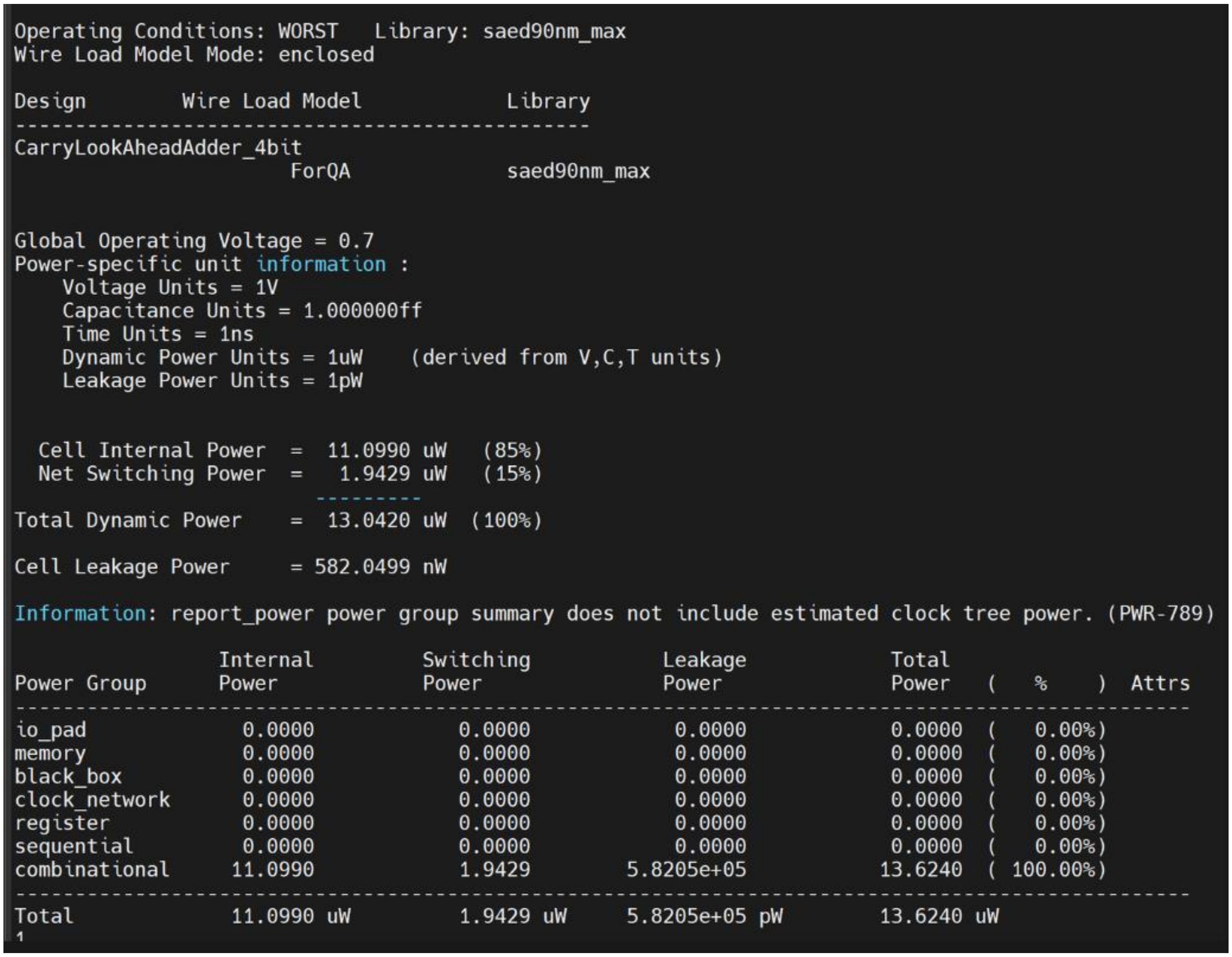
Figure 4: Ripple-Carry Synthesized Circuit

Carry-Lookahead Adder Demo



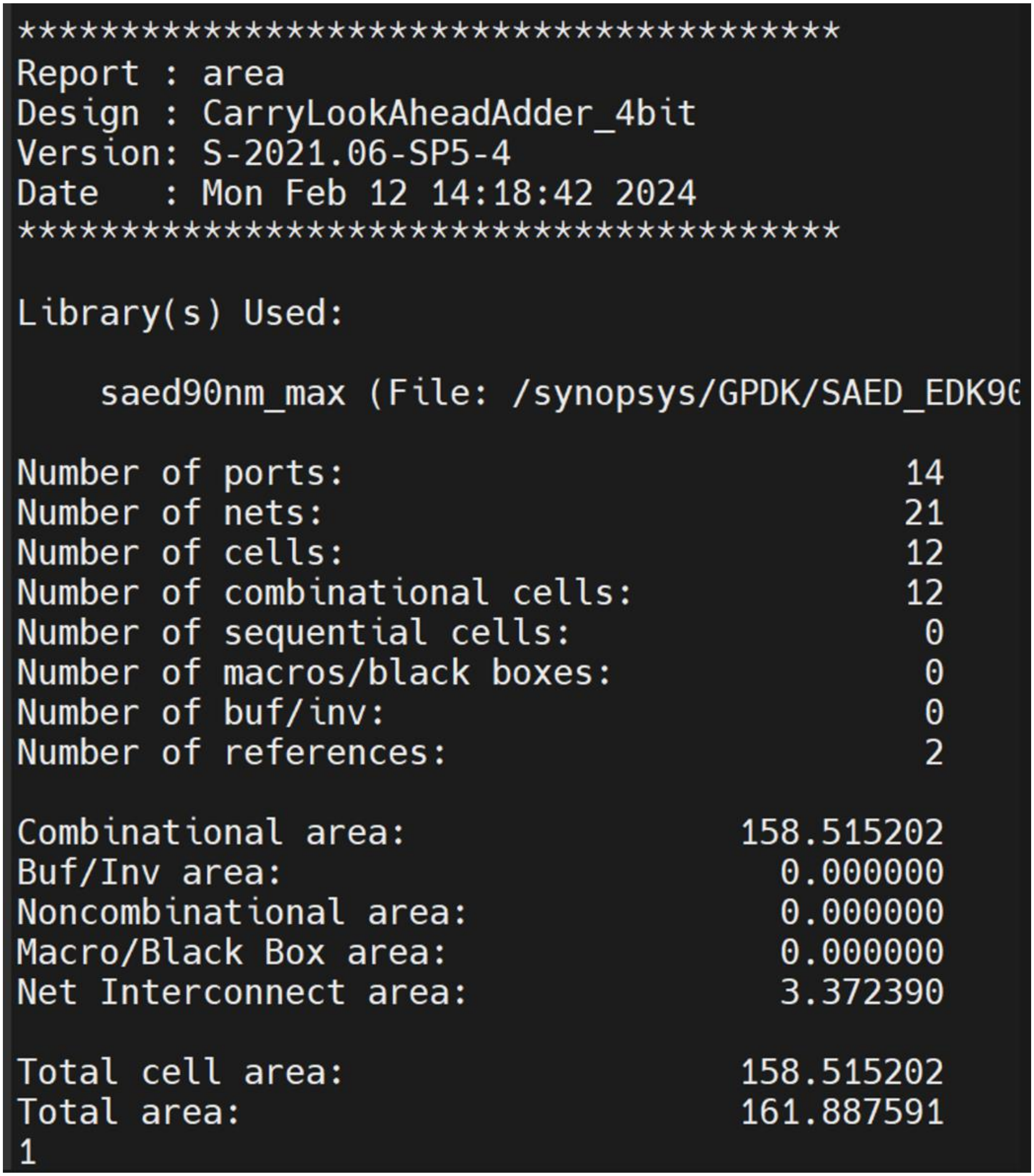
```
/home/ugrad/siu856093429/ECE426/lab3-66> ./simv
Chronologic VCS simulator copyright 1991-2022
Contains Synopsys proprietary information.
Compiler version T-2022.06-SP1; Runtime version T-2022.06-SP1;  Feb 12 14:11 2024
                   0us a=1111, b=0000, cin=0, cout=0, sum=1111
                  10us a=1111, b=0001, cin=0, cout=1, sum=0000
                  20us a=0011, b=0111, cin=0, cout=0, sum=1010
                  30us a=0101, b=0101, cin=0, cout=0, sum=1010
                  40us a=1001, b=1001, cin=0, cout=1, sum=0010
                  50us a=1110, b=0001, cin=0, cout=0, sum=1111
                  60us a=1101, b=1101, cin=0, cout=1, sum=1010
                  70us a=1111, b=1111, cin=0, cout=1, sum=1110
                  90us a=1110, b=0001, cin=1, cout=1, sum=0000
                 100us a=1101, b=1101, cin=1, cout=1, sum=1011
                 110us a=1110, b=1111, cin=1, cout=1, sum=1110
                 120us a=1111, b=1111, cin=1, cout=1, sum=1111
$finish called from file "tb_lookahead.v", line 35.
$finish at simulation time                   170
           V C S   S i m u l a t i o n   R e p o r t
Time: 170 us
CPU Time:      0.350 seconds;       Data structure size:   0.0Mb
Mon Feb 12 14:11:34 2024
```

Figure 5: Carry-Lookahead Simulation



```
Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
CarryLookAheadAdder_4bit
                       ForQA              saed90nm_max


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  11.0990 uW   (85%)
  Net Switching Power  =   1.9429 uW   (15%)
                         ---------
Total Dynamic Power    =  13.0420 uW  (100%)

Cell Leakage Power     = 582.0499 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational     11.0990           1.9429        5.8205e+05            13.6240  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             11.0990 uW        1.9429 uW     5.8205e+05 pW         13.6240 uW
1
```

Figure 6: Carry-Lookahead Power



```
****************************************
Report : area
Design : CarryLookAheadAdder_4bit
Version: S-2021.06-SP5-4
Date   : Mon Feb 12 14:18:42 2024
****************************************

Library(s) Used:

    saed90nm_max (File: /synopsys/GPDK/SAED_EDK90

Number of ports:                             14
Number of nets:                              21
Number of cells:                             12
Number of combinational cells:               12
Number of sequential cells:                   0
Number of macros/black boxes:                 0
Number of buf/inv:                            0
Number of references:                         2

Combinational area:                  158.515202
Buf/Inv area:                          0.000000
Noncombinational area:                 0.000000
Macro/Black Box area:                  0.000000
Net Interconnect area:                 3.372390

Total cell area:                     158.515202
Total area:                          161.887591
1
```

Figure 7: Carry-Lookahead Area

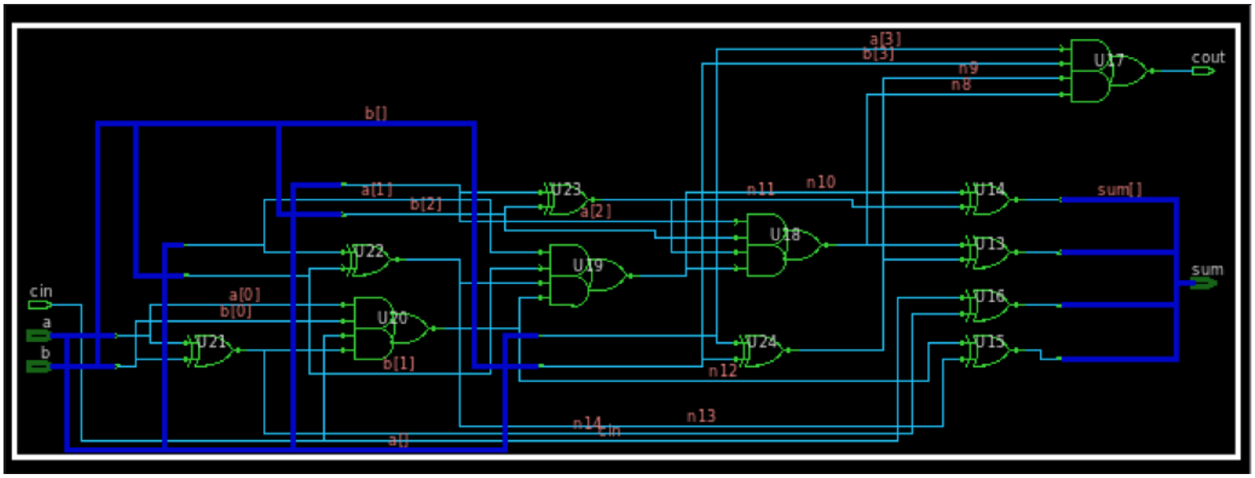


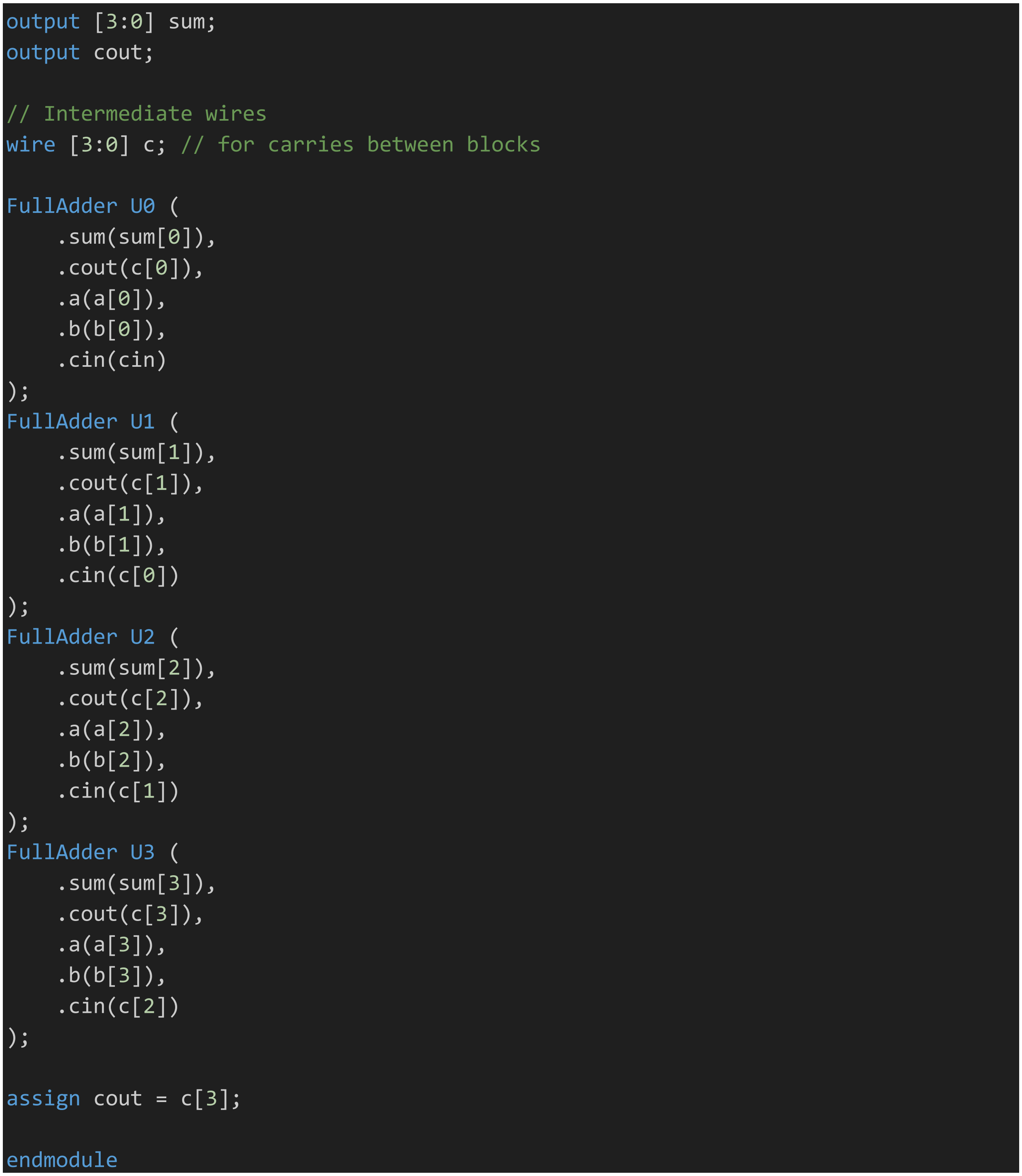
Figure 8: Carry-Lookahead Synthesized Circuit

The only problem is we cannot prove that the Carry-Lookahead is faster just off of power and area reports. We would need to set up a simulation targeted at testing the speed between the two. From QOR reports, we see that the critical path lengths of the circuits are nearly identical, so I'm not sure what to make of that without a specific timing simulation.

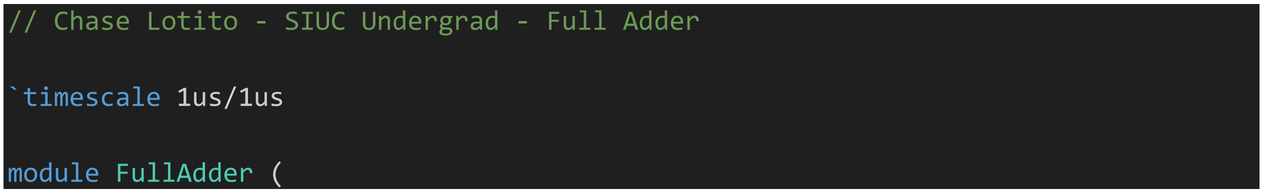
The similarities in critical paths are most likely due to the testbenches for each circuit testing over the same time range and the delays of the inputs being the same for both circuits.

Appendix A: Ripple-Carry Adder Code

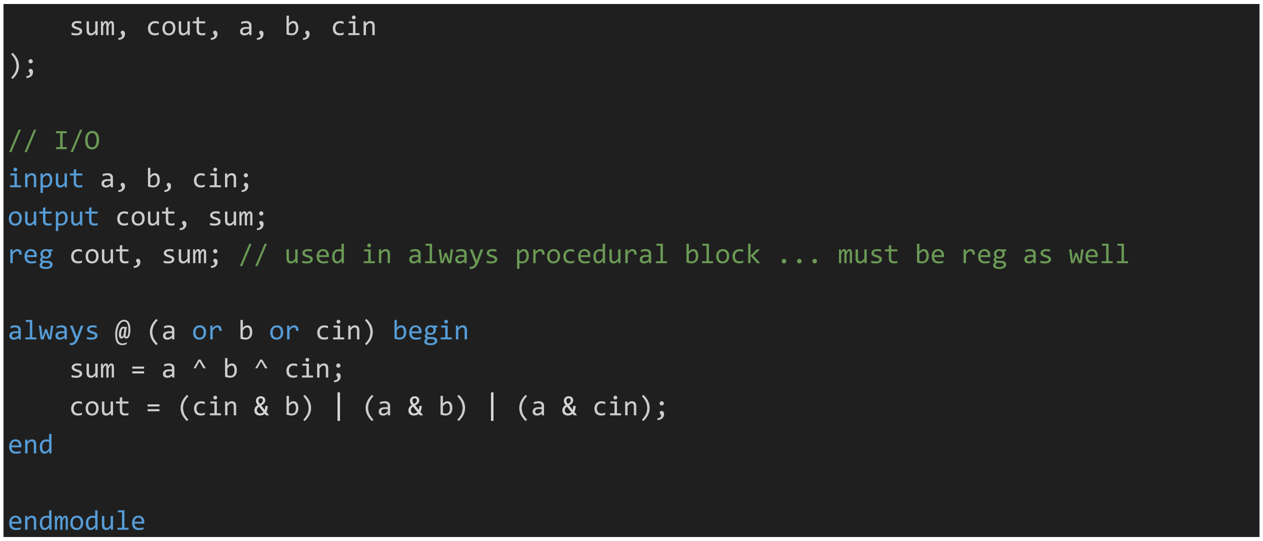
```
/*
Chase Lotito - SIUC Undergraduate - SP2024
ECE426 - Chao Lu
LAB3 - 4-bit Adders
*/

// 4-BIT RIPPLE-CARRY ADDER

// Full Adder Block

`include "FullAdder.v"
`timescale 1us/1us

module RippleCarryAdder_4bit (
    sum, cout, a, b, cin
);

// I/O
input [3:0] a, b;
input cin;
```



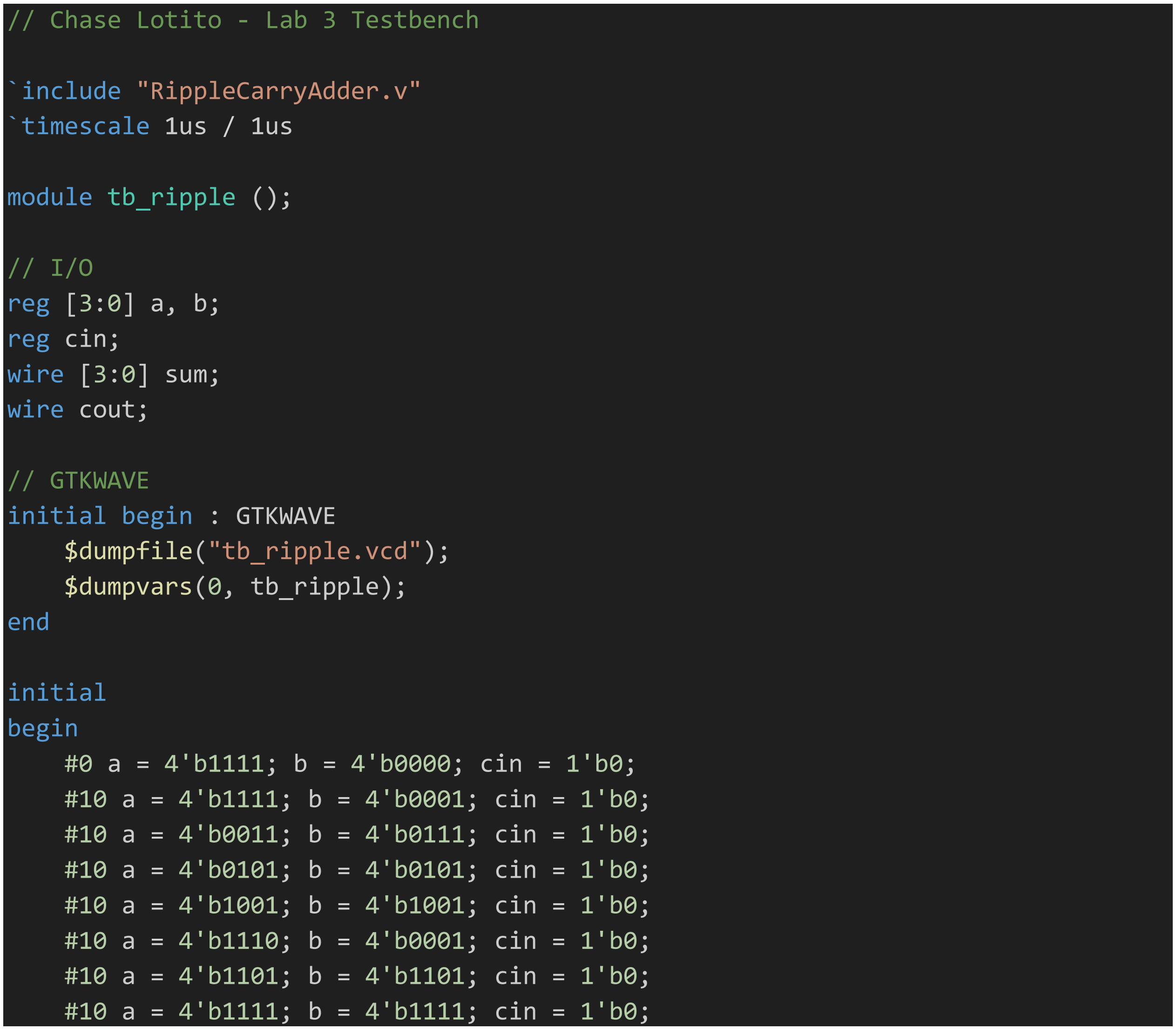
```
output [3:0] sum;
output cout;

// Intermediate wires
wire [3:0] c; // for carries between blocks

FullAdder U0 (
    .sum(sum[0]),
    .cout(c[0]),
    .a(a[0]),
    .b(b[0]),
    .cin(cin)
);
FullAdder U1 (
    .sum(sum[1]),
    .cout(c[1]),
    .a(a[1]),
    .b(b[1]),
    .cin(c[0])
);
FullAdder U2 (
    .sum(sum[2]),
    .cout(c[2]),
    .a(a[2]),
    .b(b[2]),
    .cin(c[1])
);
FullAdder U3 (
    .sum(sum[3]),
    .cout(c[3]),
    .a(a[3]),
    .b(b[3]),
    .cin(c[2])
);

assign cout = c[3];

endmodule
```



```
// Chase Lotito - SIUC Undergrad - Full Adder

`timescale 1us/1us

module FullAdder (
```



```
    sum, cout, a, b, cin
);

// I/O
input a, b, cin;
output cout, sum;
reg cout, sum; // used in always procedural block ... must be reg as well

always @ (a or b or cin) begin
    sum = a ^ b ^ cin;
    cout = (cin & b) | (a & b) | (a & cin);
end

endmodule
```

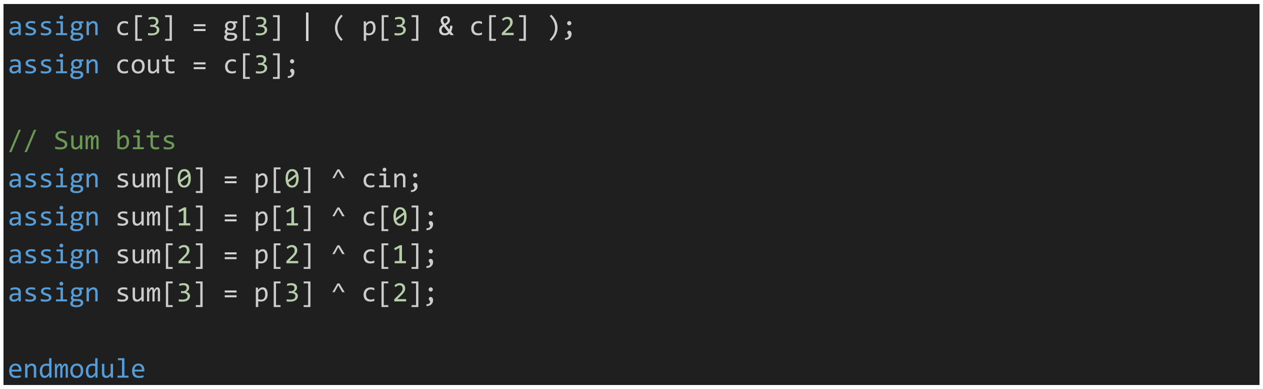


```
// Chase Lotito - Lab 3 Testbench

`include "RippleCarryAdder.v"
`timescale 1us / 1us

module tb_ripple ();

// I/O
reg [3:0] a, b;
reg cin;
wire [3:0] sum;
wire cout;

// GTKWAVE
initial begin : GTKWAVE
    $dumpfile("tb_ripple.vcd");
    $dumpvars(0, tb_ripple);
end

initial
begin
    #0 a = 4'b1111; b = 4'b0000; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b0001; cin = 1'b0;
    #10 a = 4'b0011; b = 4'b0111; cin = 1'b0;
    #10 a = 4'b0101; b = 4'b0101; cin = 1'b0;
    #10 a = 4'b1001; b = 4'b1001; cin = 1'b0;
    #10 a = 4'b1110; b = 4'b0001; cin = 1'b0;
    #10 a = 4'b1101; b = 4'b1101; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b0;
    #10 a = 4'b1110; b = 4'b0001; cin = 1'b1;
    #10 a = 4'b1101; b = 4'b1101; cin = 1'b1;
    #10 a = 4'b1110; b = 4'b1111; cin = 1'b1;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b1;
    #50 $finish;
end

 //instantiate the module into the test bench
RippleCarryAdder_4bit U1 (
    .a(a),
    .b(b),
    .cin(cin),
    .sum(sum),
    .cout(cout)
);

initial
begin
 $monitor ($time, "us a=%b, b=%b, cin=%b, cout=%b, sum=%b", a, b, cin, cout,
sum);
end

endmodule
```

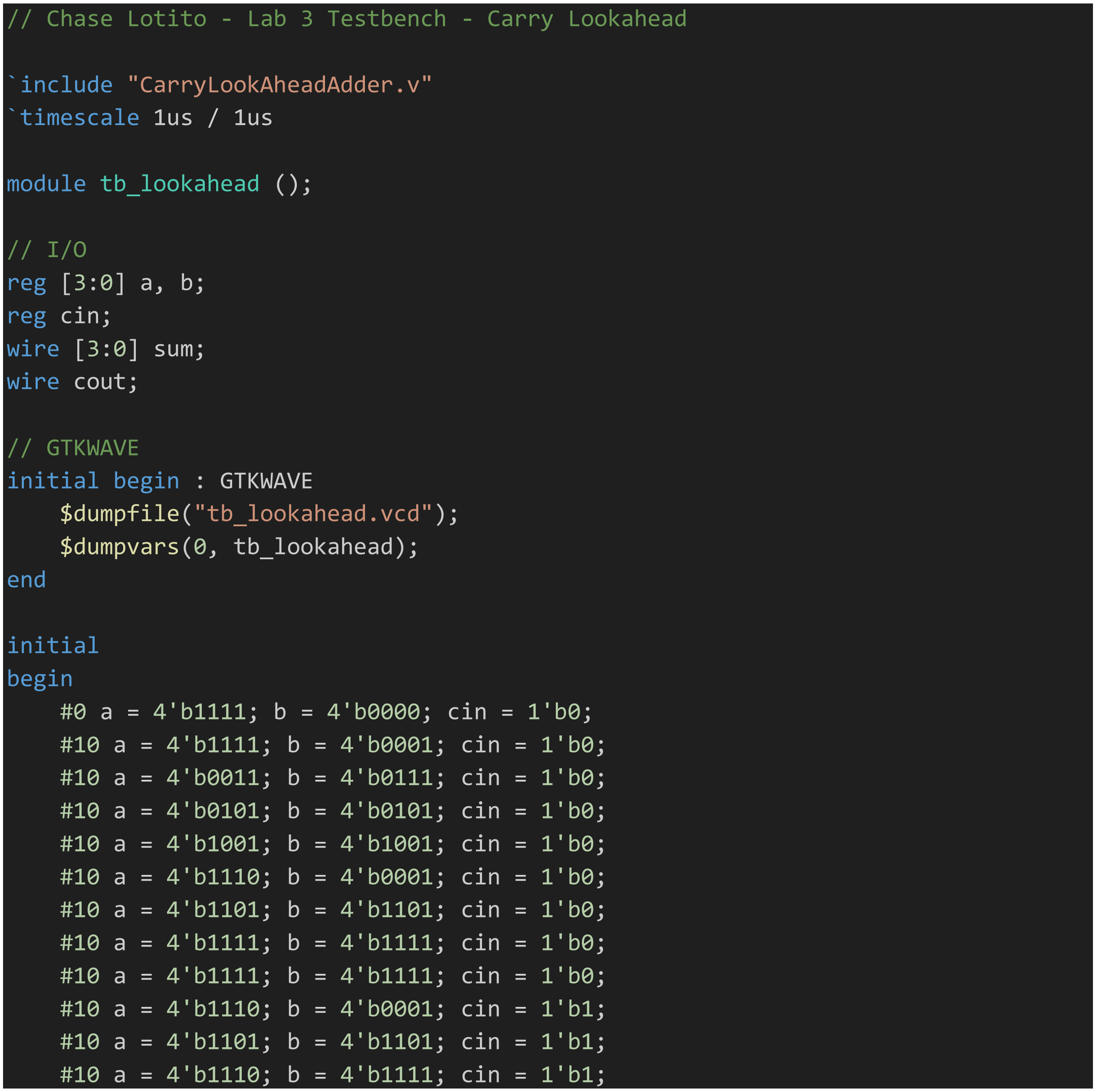
```
set search_path ".
/synopsys/GPDK/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models"
set link_library "saed90nm_max.db"
set target_library "saed90nm_max.db"
set symbol_library "saed90nm_max.db"
analyze -library WORK -format verilog
{/home/ugrad/siu856093429/ECE426/lab3/RippleCarryAdder.v}
elaborate RippleCarryAdder_4bit -library WORK
link
compile -exact_map
```

Appendix B: Carry-Lookahead Adder Code

```
// Chase Lotito - SIUC Undergrad - SP2024
// Lab 3 - Part 2 - Carry-Lookahead Adder

// CARRY LOOK AHEAD ADDER USES:
    // c[i] = g[i] | p[i] & c[i-1] (c[-1] = cin)
        // G is CARRY GENERATE --> g = a[i] & b[i]
        // P is CARRY PROPAGATE --> p[i] = a[i] ^ b[i] (xor)
// THE SUM:
    // sum[i] = p[i] ^ c[i-1] = a[i] ^ b[i] ^ c[i-1]
    //

`timescale 1us/1us

module CarryLookAheadAdder_4bit (
    sum, cout, a, b, cin
);

// I/O
input [3:0] a, b;
input cin;
output [3:0] sum;
output cout;

// Interconnections!
wire [3:0] c, g, p; // carries, generates, propogates

// Generate carry bits
assign g[0] = a[0] & b[0];
assign g[1] = a[1] & b[1];
assign g[2] = a[2] & b[2];
assign g[3] = a[3] & b[3];

// Propogate carry bits
assign p[0] = a[0] ^ b[0];
assign p[1] = a[1] ^ b[1];
assign p[2] = a[2] ^ b[2];
assign p[3] = a[3] ^ b[3];

// Carry bits
assign c[0] = g[0] | ( p[0] & cin );
assign c[1] = g[1] | ( p[1] & c[0] );
assign c[2] = g[2] | ( p[2] & c[1] );
```



```
assign c[3] = g[3] | ( p[3] & c[2] );
assign cout = c[3];

// Sum bits
assign sum[0] = p[0] ^ cin;
assign sum[1] = p[1] ^ c[0];
assign sum[2] = p[2] ^ c[1];
assign sum[3] = p[3] ^ c[2];

endmodule
```



```
// Chase Lotito - Lab 3 Testbench - Carry Lookahead

`include "CarryLookAheadAdder.v"
`timescale 1us / 1us

module tb_lookahead ();

// I/O
reg [3:0] a, b;
reg cin;
wire [3:0] sum;
wire cout;

// GTKWAVE
initial begin : GTKWAVE
    $dumpfile("tb_lookahead.vcd");
    $dumpvars(0, tb_lookahead);
end

initial
begin
    #0 a = 4'b1111; b = 4'b0000; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b0001; cin = 1'b0;
    #10 a = 4'b0011; b = 4'b0111; cin = 1'b0;
    #10 a = 4'b0101; b = 4'b0101; cin = 1'b0;
    #10 a = 4'b1001; b = 4'b1001; cin = 1'b0;
    #10 a = 4'b1110; b = 4'b0001; cin = 1'b0;
    #10 a = 4'b1101; b = 4'b1101; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b0;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b0;
    #10 a = 4'b1110; b = 4'b0001; cin = 1'b1;
    #10 a = 4'b1101; b = 4'b1101; cin = 1'b1;
    #10 a = 4'b1110; b = 4'b1111; cin = 1'b1;
    #10 a = 4'b1111; b = 4'b1111; cin = 1'b1;
    #50 $finish;
end

 //instantiate the module into the test bench
CarryLookAheadAdder_4bit U1 (
    .a(a),
    .b(b),
    .cin(cin),
    .sum(sum),
    .cout(cout)
);

initial
begin
 $monitor ($time, "us a=%b, b=%b, cin=%b, cout=%b, sum=%b", a, b, cin, cout,
sum);
end

endmodule
```

```
set search_path ".
/synopsys/GPDK/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models"
set link_library "saed90nm_max.db"
set target_library "saed90nm_max.db"
set symbol_library "saed90nm_max.db"
analyze -library WORK -format verilog
{/home/ugrad/siu856093429/ECE426/lab3/CarryLookAheadAdder.v}
elaborate CarryLookAheadAdder_4bit -library WORK
link
compile -exact_map
```