MOSFET Design

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***Abstract*—For this MOSFET experiment, we want to analytically design, and numerically verify the design for a n-type MOSFET. Parameters to design for are on current, off current, subthreshold swing, and drain-induced barrier lowering (DIBL).**

I. Analytical Approach

Given the flat-band voltage V_{FB}, the difference between Fermi and Instrinic level ϕ_{fp}, oxide capacitance C_{ox}, and acceptor doping concentration, the threshold voltage in a MOSFET is:

$$V_T = V_{FB} + 2\phi_{fp} + \frac{\sqrt{2q\epsilon N_a(2\phi_{fp})}}{C_{ox}}$$

If we assume there isn't too much band bending from work function differences, then let $V_{FB} = 0V$. Then we can iterate through values knowing $C_{ox} = k_{ox}\epsilon_0/t_{ox}$. Also:

$$\phi_{fp} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

Question 1.

We can backsolve for off current using the triode version of the mosfet drain current, and get that $V_T = 0.8V$ for $\leq 10\mu A/\mu m$. By iterating different values, this requires $N_a = 7e+16cm^{-3}$ and I set $t_{ox} = 4nm$.

However, if I solve for on current, I get about 1.165μA. This part I am not sure on, it would take me more time to fit all the parameters correctly. Also, V_{GS} for this is very close to V_T in value, which decreases the analytical value for I_D.

We can calculate for subthreshold swing using:

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_b}{C_{ox}}\right)$$

We can also solve for current in the triode mode, drain current is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(2(V_{GS} - V_T)V_{DS} - V_{DS}^2)$$

And in saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

Given the currents and associated voltages, we can account for drain-induced barrier lowering (DIBL):

$$\text{DIBL} = \frac{|\Delta V_T|}{\Delta V_{DS}}$$

II. Design Method

For this MOSFET experiment, the *MOSFet* simulator from nanoHUB.org was used [1].

The MOSFET must:

1) ON current ($V_G = V_D = 0.8V$) $\geq 600\mu A/\mu m$
2) OFF current ($V_G = 0V, V_D = 0.8V$) $\leq 10\mu A/\mu m$
3) Subthreshold Swing, $S \leq 200mV/\text{dec}$
4) Drain Induced Barrier Lowering (DIBL) $\leq 250mV/V$

III. Discussions on Design and Analysis

To follow the anayltical, after setting the given parameters, I set $N_a = 7 \times 10^{16}cm^{-3}$, and $t_{ox} = 4nm$. 4nm since values needed to be shifted to get convergence.

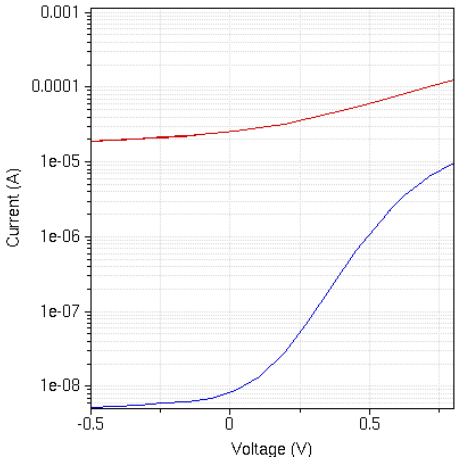

Fig. 1. $I_D - V_{GS}$ curve for $t_{ox} = 4nm$, and $N_a = 7 \times 10^{16}cm^{-3}$

Question 2.

For this design, we get off current to be 6.95μA, which satisfies our requirements. The on current is off by a single order of magnitude at 14.5μA, which does not satisfy the requirements. It was difficult to simulate these IV curves that weren't mostly flat across the voltage sweep.

Though, if we look at Figure 1, the subthreshold begins to flatten for the blue IV-curve near 0.75-0.8V, so the threshold voltage we found analytically follows in simulation.

Major differences will come in the higher accuracy of the simulator, which solves more complex models of the MOSFET while taking quantum effects into account.

Question 3.

Nanoscale device engineers design devices that are applied to every sector's technology, so it is paramount that design decisions are made with the public in mind.

Critically, devices should be designed to first deliver the highest reliability possible. For public health, reliable semiconductor sensors and transistors which monitor the health of high-risk patients must provide robust functionality guaranteed.

For the general welfare, smaller and cheaper devices that don't skimp on power efficiency, and deliver on high switching speed can be large boosts to economic growth. If a nation can spearhead innovative semiconductor device designs, then the people of that nation can benefit from the device's gains. Also, reducing in off current, and therefore leakage power, is critical in reducing small and unnecessary carbon emissions—good for reducing the need for electricity mostly generated from coal mines in the United States.

Question 4.

As engineers, making products or designing infrastructure for people requires standards to make sure the public that interacts with a design are safe and better off with the design than before.

It is right to put the safety of others on a pedestal as an engineer. Lives rely on your work, so it is imperative engineers put safety on top. This also ensures that progress made is worth pursuing, since it would have already passed safety standards in approach.

Secondly, it is right to design in aims of making people better off than they were before. More than ever, we need to reduce superfluous junk, and be in search of useful and life-improving tools. For nanoscale devices, making sure to not reinvent another smaller transistor, but instead a transistor that reduces leakage or can withstand greater electric fields.

REFERENCES

[1] e. a. Shaikh S Ahmed, "Mosfet," https://nanohub.org/resources/mosfet, 2017.