Design of a MOS Capacitor structure adjacent to finFET

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***Abstract*—This experiment is to design a dual-gate MOS capacitor with a threshold voltage $V_{th} = 0.7V$.**

I. Introduction

This project is an important case study in engineering the threshold voltage in a MOS capacitor (MOSCAP). Specifically, a dual-gate MOSCAP which resembles the active channel region in a finFET device. finFETs are transistors with better gate control and low power consumption, and they're an extremely prominent device in current industry.

II. Design Method

For this MOSCAP experiment, the *SCHRED 1.0* simulator from nanoHUB.org was used [1].

The MOSCAP must:

1) Threshold voltage V_{th} of 0.7V (±10%).
2) Body thickness T_b of 5nm.
3) $2 \times 10^{17}\text{cm}^{-3} \leq N_A \leq 6 \times 10^{17}\text{cm}^{-3}$
4) HfO_2 as gate dielectric.
5) Aluminum as gate contact material.
6) Silicon wafer in (100) orientation.

III. Discussions on Design and Analysis

To simulate HfO_2, the gate oxide dielectric constant $\epsilon_r = 25.1$. To simulate aluminum, the necessary work function $\phi_{Al} = 4.28$eV.

I chose an iterative approach to find the proper device parameters. Where the capacitance of the function seemed to be a weak function of the doping density, so I set the acceptor doping density $N_A = 4 \times 10^{17}\text{cm}^{-3}$. Then, I varied the oxide thickness, and I always kept $t_{ox} = t_{box}$ to better follow a finFET.

Figure 1 shows at $V_g = 2$V, we get $C_{tot} = 4.429\mu F/\text{cm}^2$, and at $V_g = 0.7V$ we get $C_{tot} = 3.965\mu F/\text{cm}^2$; here, this capacitance is 89.5% the 2V value, so we have designed for $V_{th} = 0.7V$. The green C-V curve in Figure 1 shows the curve of the MOSCAP with $t_{ox} = 8$nm.

Figures 2 and 3 show the biased MOSCAP's conduction band and electric field across the device. The E-field spikes at the locations of inversion in the conduction band near the oxide-semiconductor interfaces. Via $E = -dV/dx$, we see the large drop in potential at 0nm, a spike in the E-field, and the same occurs at the next oxide-semiconductor interface, but instead a large potential increase leads to a negative E-field spike.

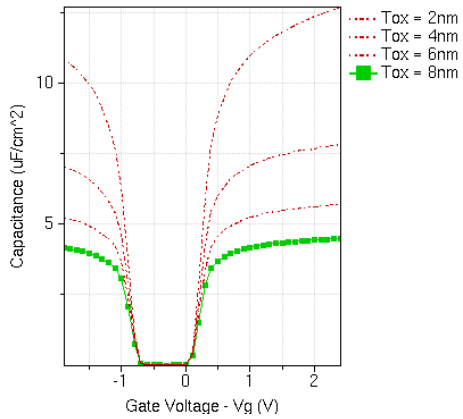

Fig. 1. C-V Characteristics of MOSCAPs, sweep of t_{ox}.

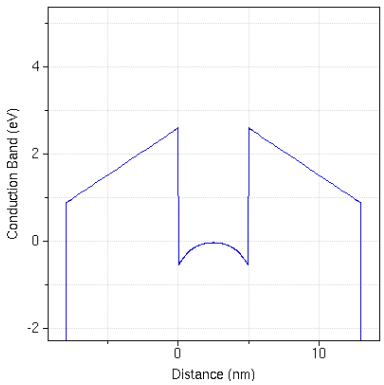

Fig. 2. Conduction band for biased MOSCAP.

Figure 4 shows the difference between the classical conduction band partnered with the quantized energy states. At full bias, the CBM is at -539meV, but the lowest quantized energy state is at -128meV. This difference of near 400meV will cause the threshold voltage to inevitably increase, and shift the C-V curve to the right.

Rerunning the simulation with the *Semiclassical* charge model, we get at $V_g = 2V$, $C_{tot} = 4.941\mu F/\text{cm}^2$. 90% of that capacitance is found at $Vg = V_T = 0.5V$. With respect to the quantum mechanical charge model, the semiclassical gives a threshold voltage 0.2V lower.

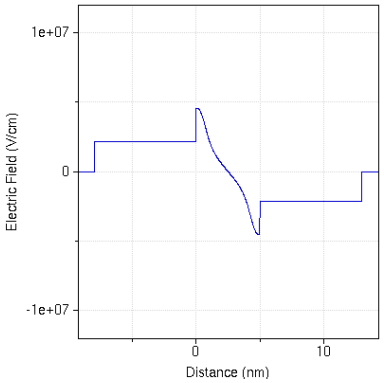

Fig. 3. Electric field profile in biased MOSCAP.

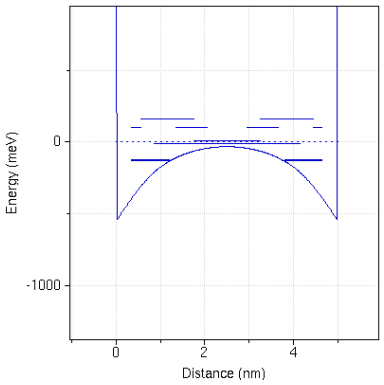

Fig. 4. Conduction band minimum and quantum energy states.

Figure 5 shows the decrease in capacitance as the body gets thicker, which follows as $C = \epsilon_0 A/d$. But, we know that $C \sim V_T$, so increases in body thickness cause decreases in the threshold voltage for a device. This is also shown in the C-V characteristic curve shifting to the left as the body thickness increases.

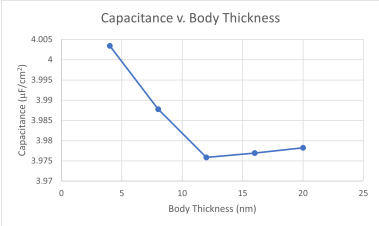

Fig. 5. Capacitance versus Body Thickness

IV. Conclusion

Interestingly, increases in device size lead to decreased threshold voltages—better control even with more device to operate. Here, we are fighting with the nanoscale quantum effects, and the increases in energy that are caused by compacting charge carriers.

We have to have a thick oxide layer since the permittivity of HfO_2 is so much greater than conventional oxide materials. This is good since we want to decrease leakage currents, and this also causes decreases in device capacitance. Ultimately, this is also good since we now require less energy to switch our device. Also, for digital circuits, this device could operate at higher frequencies as compared to thinner-oxide devices.

So, if we want to design a finFET, then we want thicker gate-oxides that can still permit the proper amount of electric flux into the channel region as before. This is so we can reduce capacitance to take advantage of greater gate control.

References

[1] e. a. Vasileska, Dragica, "Schred," https://nanohub.org/resources/schred, 2022.