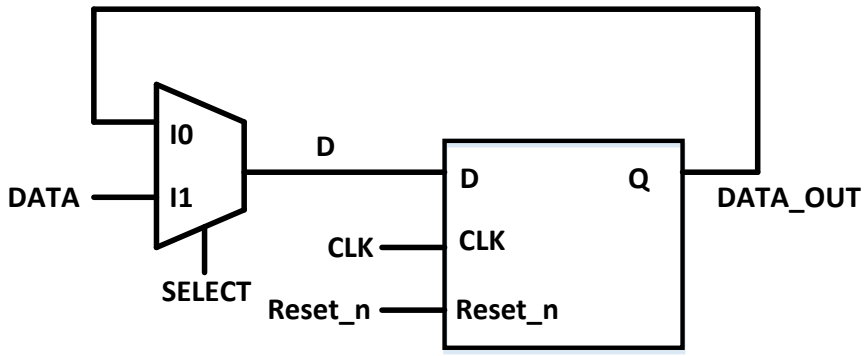
ECE 426/516 **Implementation of VLSI Systems with HDL**

Homework #4 Verilog Code for digital circuits and systems
Due date: March 4th, 2024, 11:30PM

Question 1: **Complete Verilog code for the following circuit, and write a test bench to verify its function.**

When "reset_n" is 0, "DATA_OUT" will be asynchronously reset to 0. When "SELECT" is 1, "DATA" will be assigned to "D". When "SELECT" is 0, "DATA_OUT" will be assigned to "D". At the rising edge of "CLK", "D" is synchronously loaded to "DATA_OUT".

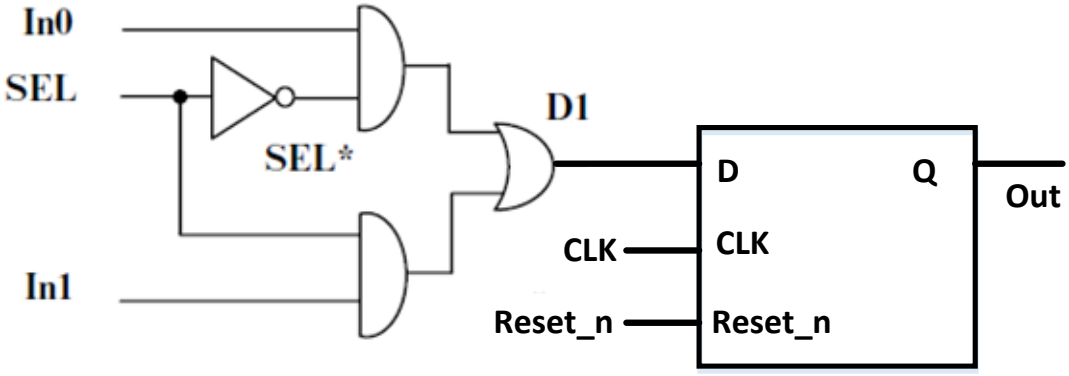



```
module ff (Reset_n, CLK, DATA, SELECT, D, DATA_OUT) ;

input   Reset_n ;
input   CLK;
input   DATA;
input   SELECT ;
output  DATA_OUT ;
output D;

reg  DATA_OUT ;
wire  D ;
assign D  = _____________________________;
always @ (_____________________________)
        begin
                if (_________________)  _____________________;
                else          _____________________________:
end
endmodule
```

Question 2: **Complete Verilog code for the following circuit, and write a test bench to verify its function.** When "reset_n" is 0, "Out" will be asynchronously reset to 0.




```
module ss (Reset_n, CLK, In0, In1, SEL, D1, Out) ;

input   Reset_n ;
input   CLK;
input   In0 ;
input   In1 ;
input   SEL ;
output D1;
output  Out ;

reg          Out ;
wire          D1 ;

assign D1  = _____________________________ ;
always @ (_____________________)
          begin
                if (_________________) _____________________;
                else  _____________________________;
          end
endmodule
```