ECE 447/547 (Semiconductor Devices)

Southern Illinois University Carbondale

Project #4: Design a MOS Capacitor Structure using SCHRED 1.0

Introduction:

Schred calculates the *C-V* characteristic and associated profiles and the quantum states in a typical MOS (Metal-Oxide-Semiconductor) or SOS (Semiconductor-Oxide-Semiconductor) structure and a typical SOI (Semiconductor-on-Insulator) structure by solving self-consistently the one-dimensional (1D) Poisson equation and the 1-D Schrodinger equation. (The effects of many-body exchange-correlation on the energetics and wavefunctions can also be studied, but this is the subject of an advanced graduate level course).

Simulation Experiments:

Part I (Numerical Design)

A dual-gate MOS structure resembles the active channel region of a modern FinFET device. Using the *Schred* simulator (version *1.0*) as available at https://nanohub.org/resources/schred, design a *dual-gate* MOS capacitor structure with a *p*-doped body that meets the following specifications:

- *Threshold voltage*, V_{th} = 0.7 V (a 10% design tolerance is allowed)
- *Semiconductor body thickness* = 5 nm
- 2×10^{17} cm^{-3} < *Semiconductor body doping* <6×10^{17} cm^{-3}
- Use HfO_2 as gate dielectric material
- Use *aluminum* as gate contact material
- Use silicon wafer in (100) orientation

Hints:

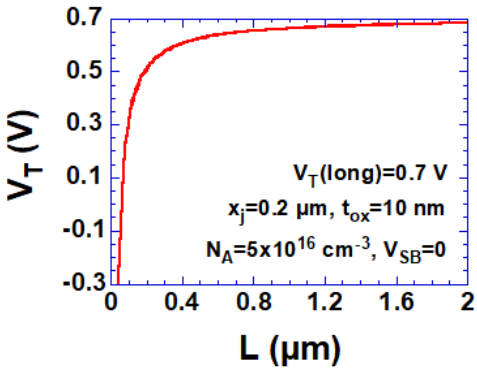
- Definition of V_{th}: Assume that V_{th} is the gate voltage at which the capacitance (in *inversion*) becomes equal to 0.9×the capacitance at V_g = 2V.
- Mainly, you need to determine reasonable values for *gate oxide thickness* and *body doping density*.

Notes:

- In the simulator, on *Device Parameters* phase, you need to set *Vary Both Gate Voltages* to "yes" (that is, it is a *common* multi-gate device).
- Also, the device should be symmetric, that is, use the same materials and thickness for top and bottom gate contacts and insulators.
- You must activate the *Quantum Mechanical* model in your simulation and use *Fermi-Dirac* statistics.
- At this stage, set "no" for *Partial Ionization*, *Exchange Interaction*, and *"Quantum Calculation in Accumulation Region"*. Use default values for other device parameters and models.

Part II (Analysis)

1) Comment on the correspondence between the *Conduction Band* and the *Electric Field* profiles.
2) Comment on the symmetry/asymmetry in electron distribution in the channel region in inversion.
3) Obtain the ground state (lowest) quantized energy for the structure from Schred output drop down menu. Determine the *shift* in conduction band minimum with respect to the classical band edge.
4) For your design, re-run the simulator using the *Semiclassical* charge model. Extract V_{th} and obtain the shift with respect to the quantum mechanical counterpart.
5) Starting with your original design, vary body thickness from 4 nm to 20 nm (in a step of 4 nm), and extract and plot V_{th} as a function of body thickness. Comment on your finding.
6) *For ECE 547 Students*: When your designed MOS structure is incorporated within a real nanoscale MOSFET (that is, with the addition of the source and drain regions), there will be a negative shift (lowering) in the threshold voltage as compared to the V_{th} obtained from the MOS capacitor structure due to short-channel charge-sharing effect. Assuming a MOSFET channel length of 100 nm, determine the V_{th} for the actual MOSFET. Use the graph shown on the right for extracting useful data.



Report:

Follow the *IEEE* style (https://www.ieee.org/conferences/publishing/templates.html) and write on the following aspects, as much as possible:

- *Abstract (a brief statement on what you plan to do in this project)*
- *Introduction (why this project and related device is important)*
- *Design Method (i.e. the simulator used and a reference to it)*
- *Discussions on Design and Analysis*
  - *Here, while describing your design and analysis, attach necessary graphs, snapshots of the simulator pages, and/or codes (if used).*
- *Conclusion*
  - *Here, in short state what you have learnt from this project*
- *References (as needed)*