ECE 426/516 **Implementation of VLSI Systems with HDL**

Homework #8 Arithmetic Circuit Designs

Due Date: April 30, 2024, by 11:30pm

Please upload your solution to D2L

Question: Write a Verilog code for subtracting two 12-bit numbers in 2's complement. Subtract 6 bits at a time to pipeline your design. Compete the following Verilog code and write a test bench to test your design.

```
// Subtraction of two 12 bit, 2's complement numbers.
// Evaluate n1 - n2 = n1+(-n2).
// Algorithm: Sign extend n1 & n2. Evaluate n1 + (two's complement of n2). Result is 13 bits.

module subtractor (clk, n1, n2, subtract) ;

input  clk ;
input  [11:0]  n1 ;
input  [11:0]  n2 ;
output  [12:0]  subtract ;

reg [12:0]  subtract ;
wire [12:0]  signe_n1 ;
wire [12:0]  signe_n2 ;

reg  [12:0]  twosc_n2 ;
reg  [12:0]  n1_reg1 ;

wire [6:0]   sub_lsb ;
reg   [6:0]   sub_lsb_2 ;
reg   [12:6]  twosc_n2_2;
reg   [12:6]  n1_reg2 ;

wire  [12:6]  sub_msb ;
wire  [12:0]  sub_next ;

assign  signe_n1 = _____ ;  // sign extend n1
assign  signe_n2 = _____ ;  // sign extend n2

always @ (posedge clk)    // Pipeline 1, clk (1)
```

```
begin
        twosc_n2 <= _____; // compute twos complement of signe_n2
        n1_reg1 <= _____; // preserve n1
end

assign  sub_lsb  = _____;  // Add least 6 significant bits, sub_lsb [6] is the carry.

always @ (posedge clk) //pipeline 1, clk (2), register LSB to continue addition of MSB.

begin
 sub_lsb_2 <= _____; // preserve LSB sum, sum_lsb_2 [6] is the carry.
 twosc_n2_2 <= _____; // preserve MSB of n2 for further processing.
 n1_reg2   <= _____;   // preserve MSB of n1_reg1
end

// Add msbs with carry.
assign  sub_msb = _____; // add MSBs with carry
assign sub_next = _____;  // put together MSB & LSB of the final result

always @ (posedge clk)          // Pipeline 2, clk (2), register the final result

begin
subtract  <= _____;
end

endmodule
```