ECE 426/516 **Implementation of VLSI Systems with HDL**

Homework #6 RTL Verilog Coding

Due date: March 25th 2024, by 11:30pm

Please upload your homework solution to D2L

Question 1: Realize Verilog code to multiply an 8-bit input called 'data' by a fixed constant, 11 and 15 respectively in decimal. Complete the following Verilog code, write a test bench, and include your simulation results.

```
module multiply (data, product_11, product_15);

input [7:0] data ;
output [11:0] product_11 ;
output [11:0] product_15 ;

wire [11:0] product_11 ;
wire [11:0] product_15 ;

assign product_11 = _____; // 8 x data + 2 x data + data

assign product_15 = _____; // 8 x data + 4 x data + 2 x data + data

endmodule
```

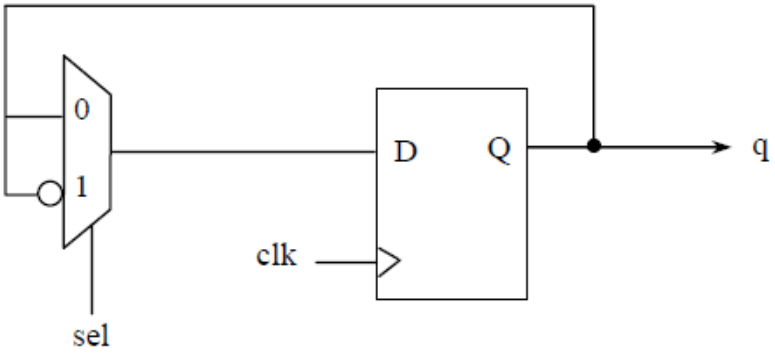
Question 2: An intermediate data called 'dct [11:0]' needs to be scaled down by 8. For example, if dct = 1280, then the scaled output called 'dctq' is 160. Complete the following Verilog code for implementation the scaling, write a test bench and include your simulation results.

```
module a5_9 (dct, dctq) ;

input [11:0] dct ;
output [8:0] dctq;
wire [8:0] dctq;

assign dctq = _____; // data/8
endmodule
```

Question 3: Realize the circuit below using Verilog. Include a signal "reset_n" for asynchronously clearing the flip-flop. What type of circuit is this? Complete the following Verilog code. Write a test bench to test it.




```
module tff (clk, reset_n, sel, q);

input clk ; // Declare the inputs and outputs of the module.
input reset_n ;
input sel ;
output q ;
reg q ;
wire D ;

assign D = _____; // model the combinational logic
always @ (_____)

begin
if (_____) _____;
else _____;

end
endmodule
```