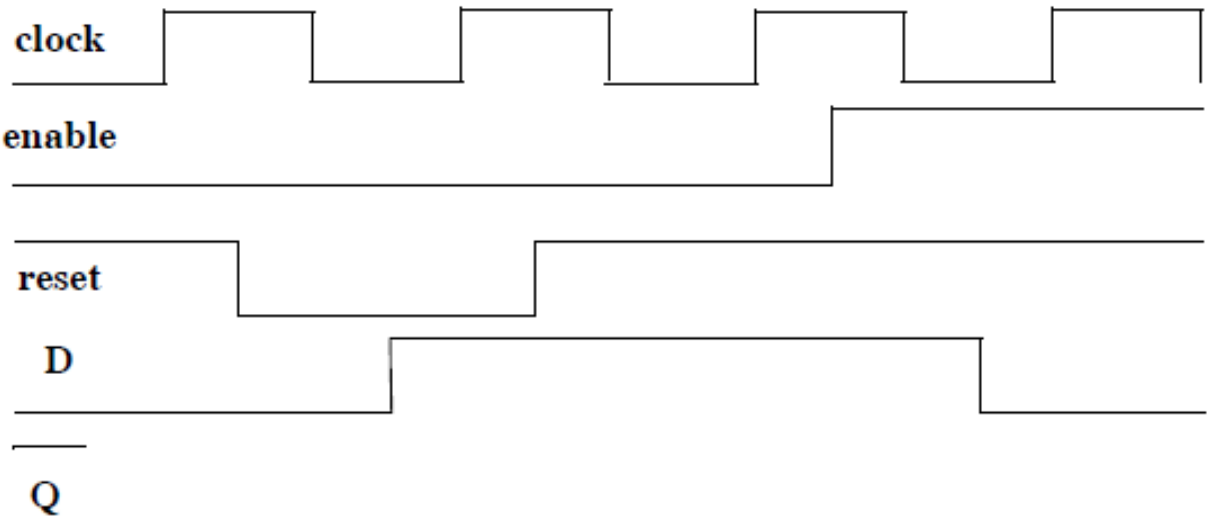
ECE 426/516 Implementation of VLSI Systems Fall 2016

Mid-Term Practice Paper

Question 1 (10 marks)

(a) Complete the timing diagram for the following piece of code. Assume Q starts at 1 and that Q is a signal. Assume that all delays are negligible. (4 marks)

```
always @ (reset, enable, clock, D)
if (reset == '0') then
        Q <='0';
else if (enable == '1' and clock == '1') then
        Q <= D;
else
        Q <= Q;
end;
end;
```



(b) Draw the circuit for the following Verilog code. (6 marks)

```
module combinational (a, b, sel, out);
input a, b;
input sel;
output out;
reg out;

always @ (a or b or sel)
begin
        if (sel) out = a & b;
        else out = b;
end

endmodule
```

```
module combinational (a, b, sel, out);
input a, b;
input sel;
output out;
reg out;

always @ (a or b or sel)
begin
        if (sel) out = a & b;
end

endmodule
```

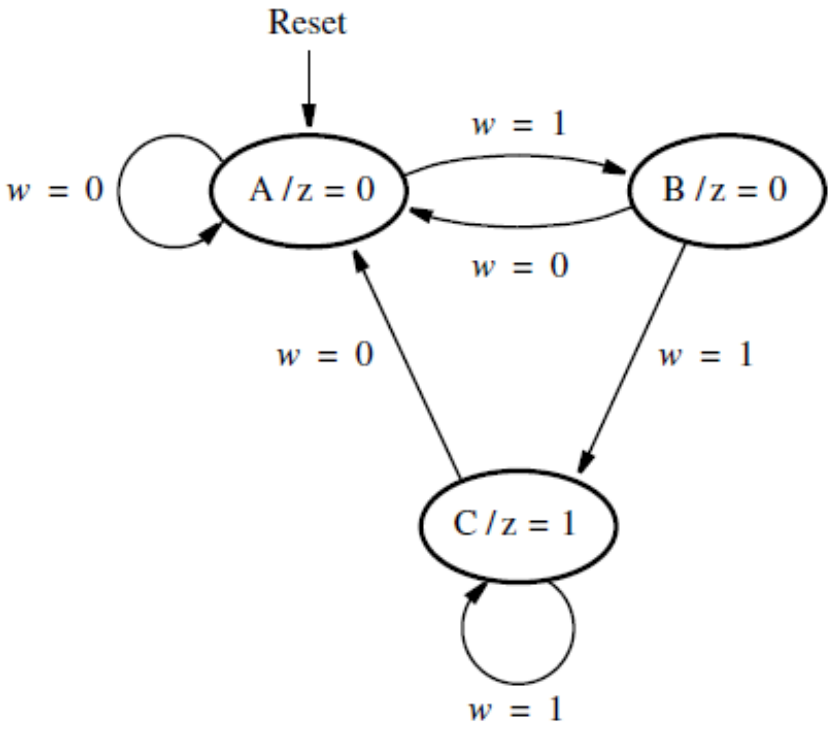
Question 2 (10 marks)

(a) Complete the behavioral description in Verilog for a synchronous 4-bit counter. When RESET = 0, output will become to 0 at the next rising edge of clock. When output = 14, output will become to 0 at the next rising edge of clock.

The basic template is shown below – fill in the necessary code to complete the description. (4 marks)

```
module counter (CLK, Q, RESET);

input RESET, CLK;

output [3:0] Q;

reg [3:0] Q;




endmodule
```

(b) Fill in the follow Verilog code to realize the following state transition diagram (6 marks)



Module simple (w, Clock, Resetn, z);

Input Clock, Resetn, w;

Output z;

Reg [2:1] y, Y;

Parameter [2:1] A=2’ b00, B=2’ b01, C=2’ b10;

// define the next state combinational circuit

always@ (w, y)

case (y)

A: **if** (w) _____ (your code here)

else _____ (your code here)

B: if (w) _____ (your code here)

else _____ (your code here)

C: if (w) _____ (your code here);

else _____ (your code here);

_____ (your code here)

endcase

// define the sequential block

always@ (_____) (your code here)

if (Resetn == 0)

_____ (your code here)

else _____ (your code here)

// define output

_____ (your code here)

endmodule