SOUTHERN ILLINOIS UNIVERSITY
CARBONDALE

ECE 426 Implementation of VLSI Systems

Lab #2: 3-to-8 Bit Decoder

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A: Testbench

This testbench was used for both the structural and the behavioral 3:8 decoder.

```
/*
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Lab 2 - Testbench
*/

// Set time scale: 1ns units / 1ns precision
`timescale 1ns / 1ns

// Import the design files
`include "decoder_3to8_structural.v"
`include "decoder_3to8_behavioral.v"

// Create testbench module
module testbench();

// Initialize I/O
reg [2:0] I; // reg is a storage element in procedural blocks (like initial!)
reg EN;
wire [7:0] D_STRUCTURAL; // wire is for continuous assignments
wire [7:0] D_BEHAVIORAL;

// Start-up procedures:
initial

begin: tb_stimulus // tb_stimulus = [name_of_block], necessary for blocks with
variables
    // Creating a input vector that will act as the left-hand side of a truth
table
    reg [4:0] invect;

    // The for-loop will automatically cycle each input from 0 to 16 (0000 to
1111)
    for (invect = 0; invect < 16; invect = invect + 1)
        begin
            {EN, I[2], I[1], I[0]} = invect[4:0];

            // Display both Structural and Behavioral designs to terminal
            #10 $display ("[STRUCTURAL] EN = %b, INPUT = %b, OUTPUT = %b ||
```

```
                [BEHAVIORAL] EN = %b, INPUT = %b, OUTPUT = %b", EN, I,
D_STRUCTURAL, EN, I, D_BEHAVIORAL);
        end
end

// Initialize modules!
decoder_3to8_structural U1 (
    .EN(EN),
    .I(I),
    .D(D_STRUCTURAL)
);

decoder_3to8_behavioral U2 (
    .EN(EN),
    .I(I),
    .D(D_BEHAVIORAL)
);
endmodule
```

I: Code for Structural 3:8 Decoder

```
/*
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Lab 2: 3-to-8 Decoder - Structural Design
*/


// The 3-to-8 Decoder takes a 3-bit binary input
// then outputs the associated decimal number (d0-d7)
// The encoder has an enable pin
module decoder_3to8_structural (EN, I, D);

// I/O
input EN;
input [2:0] I;
output [7:0] D;

// This will contain the inverted input
wire [2:0] I_;

// Inverting the input for later
```

```
not N0 (I_[0], I[0]); // first bit of input inverted and lives on first bit of I_
wire
not N1 (I_[1], I[1]);
not N2 (I_[2], I[2]);

// Boolean expressions gotten from 3-to-8 decoder truth table
and A0 (D[0], EN, I_[2], I_[1], I_[0]); // 000 D[0] is the first output
and A1 (D[1], EN, I_[2], I_[1], I[0]); // 001
and A2 (D[2], EN, I_[2], I[1], I_[0]); // 010
and A3 (D[3], EN, I_[2], I[1], I[0]); // 011
and A4 (D[4], EN, I[2], I_[1], I_[0]); // 100
and A5 (D[5], EN, I[2], I_[1], I[0]); // 101
and A6 (D[6], EN, I[2], I[1], I_[0]); // 110
and A7 (D[7], EN, I[2], I[1], I[0]); // 111

// For the last case, the decoder will automatically
// output nothing, which is what we want!

endmodule
```

```
set search_path ".
/synopsys/GPDK/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models"
set link_library "saed90nm_max.db"
set target_library "saed90nm_max.db"
set symbol_library "saed90nm_max.db"
analyze -library WORK -format verilog
{/home/ugrad/siu856093429/ECE426/lab2/decoder_3to8_behavioral.v}
elaborate 3to8_decoder_structural -library WORK
link
compile -exact_map
```

II: Simulation of Structural 3:8 Decoder

```
/home/ugrad/siu856093429/ECE426/lab2-56> ./simv
Chronologic VCS simulator copyright 1991-2022
Contains Synopsys proprietary information.
Compiler version T-2022.06-SP1; Runtime version T-2022.06-SP1;  Jan 30 15:21 2024
[STRUCTURAL] EN = 0, INPUT = 000, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 000, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 001, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 001, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 010, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 010, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 011, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 011, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 100, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 100, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 101, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 101, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 110, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 110, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 111, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 111, OUTPUT = 00000000
[STRUCTURAL] EN = 1, INPUT = 000, OUTPUT = 00000001 || [BEHAVIORAL] EN = 1, INPUT = 000, OUTPUT = 00000001
[STRUCTURAL] EN = 1, INPUT = 001, OUTPUT = 00000010 || [BEHAVIORAL] EN = 1, INPUT = 001, OUTPUT = 00000010
[STRUCTURAL] EN = 1, INPUT = 010, OUTPUT = 00000100 || [BEHAVIORAL] EN = 1, INPUT = 010, OUTPUT = 00000100
[STRUCTURAL] EN = 1, INPUT = 011, OUTPUT = 00001000 || [BEHAVIORAL] EN = 1, INPUT = 011, OUTPUT = 00001000
[STRUCTURAL] EN = 1, INPUT = 100, OUTPUT = 00010000 || [BEHAVIORAL] EN = 1, INPUT = 100, OUTPUT = 00010000
[STRUCTURAL] EN = 1, INPUT = 101, OUTPUT = 00100000 || [BEHAVIORAL] EN = 1, INPUT = 101, OUTPUT = 00100000
[STRUCTURAL] EN = 1, INPUT = 110, OUTPUT = 01000000 || [BEHAVIORAL] EN = 1, INPUT = 110, OUTPUT = 01000000
[STRUCTURAL] EN = 1, INPUT = 111, OUTPUT = 10000000 || [BEHAVIORAL] EN = 1, INPUT = 111, OUTPUT = 10000000
          V C S   S i m u l a t i o n   R e p o r t
Time: 160 ns
CPU Time:      0.890 seconds;       Data structure size:   0.0Mb
Tue Jan 30 15:21:32 2024
/home/ugrad/siu856093429/ECE426/lab2-57>
```

Figure 1: U1 is 3:8 Structural

III: Code for Behavioral 3:8 Decoder

```
/*
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ECE426L - Chao Lu

Lab 2: 3-to-8 Decoder - Behavioral Design
*/

module decoder_3to8_behavioral (EN, I, D);

// I/O
input EN;
input [2:0] I;
output [7:0] D;
```

```
// This allows us to set the value of D
reg [7:0] D;

// Check if EN or I changes (enable on or off, new input)
always @(EN or I) begin

    // Clears output vector to 00000000
    D = 8'h00;

    // Check if EN is HIGH
    if (EN == 1) begin
        // Check input then set output bit accordingly
        if (I[2] == 0 & I[1] == 0 & I[0] == 0) // e.g. sees input of 000
            D[0] = 1; // 000000001
        else if (I[2] == 0 & I[1] == 0 & I[0] == 1)
            D[1] = 1;
        else if (I[2] == 0 & I[1] == 1 & I[0] == 0)
            D[2] = 1;
        else if (I[2] == 0 & I[1] == 1 & I[0] == 1)
            D[3] = 1;
        else if (I[2] == 1 & I[1] == 0 & I[0] == 0)
            D[4] = 1;
        else if (I[2] == 1 & I[1] == 0 & I[0] == 1)
            D[5] = 1;
        else if (I[2] == 1 & I[1] == 1 & I[0] == 0)
            D[6] = 1;
        else if (I[2] == 1 & I[1] == 1 & I[0] == 1)
            D[7] = 1;
    end
end

endmodule
```

```
set search_path ".
/synopsys/GPDK/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models"
set link_library "saed90nm_max.db"
set target_library "saed90nm_max.db"
set symbol_library "saed90nm_max.db"
analyze -library WORK -format verilog
{/home/ugrad/siu856093429/ECE426/lab2/decoder_3to8_behavioral.v}
elaborate 3to8_decoder_behavioral -library WORK
link
compile -exact_map
```

IV: Simulation for Behavioral 3:8 Decoder

```
PS C:\Users\Chase Lotito\Desktop\SIUC\SPRING 2024\426 - VLSI SYSTEMS\LABS\ece427_lab2> vvp tb.vvp
VCD info: dumpfile tb.vcd opened for output.
[STRUCTURAL] EN = 0, INPUT = 000, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 000, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 001, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 001, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 010, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 010, OUTPUT = 00000000
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[STRUCTURAL] EN = 0, INPUT = 100, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 100, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 101, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 101, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 110, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 110, OUTPUT = 00000000
[STRUCTURAL] EN = 0, INPUT = 111, OUTPUT = 00000000 || [BEHAVIORAL] EN = 0, INPUT = 111, OUTPUT = 00000000
[STRUCTURAL] EN = 1, INPUT = 000, OUTPUT = 00000001 || [BEHAVIORAL] EN = 1, INPUT = 000, OUTPUT = 00000001
[STRUCTURAL] EN = 1, INPUT = 001, OUTPUT = 00000010 || [BEHAVIORAL] EN = 1, INPUT = 001, OUTPUT = 00000010
[STRUCTURAL] EN = 1, INPUT = 010, OUTPUT = 00000100 || [BEHAVIORAL] EN = 1, INPUT = 010, OUTPUT = 00000100
[STRUCTURAL] EN = 1, INPUT = 011, OUTPUT = 00001000 || [BEHAVIORAL] EN = 1, INPUT = 011, OUTPUT = 00001000
[STRUCTURAL] EN = 1, INPUT = 100, OUTPUT = 00010000 || [BEHAVIORAL] EN = 1, INPUT = 100, OUTPUT = 00010000
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[STRUCTURAL] EN = 1, INPUT = 110, OUTPUT = 01000000 || [BEHAVIORAL] EN = 1, INPUT = 110, OUTPUT = 01000000
[STRUCTURAL] EN = 1, INPUT = 111, OUTPUT = 10000000 || [BEHAVIORAL] EN = 1, INPUT = 111, OUTPUT = 10000000
PS C:\Users\Chase Lotito\Desktop\SIUC\SPRING 2024\426 - VLSI SYSTEMS\LABS\ece427_lab2>
```
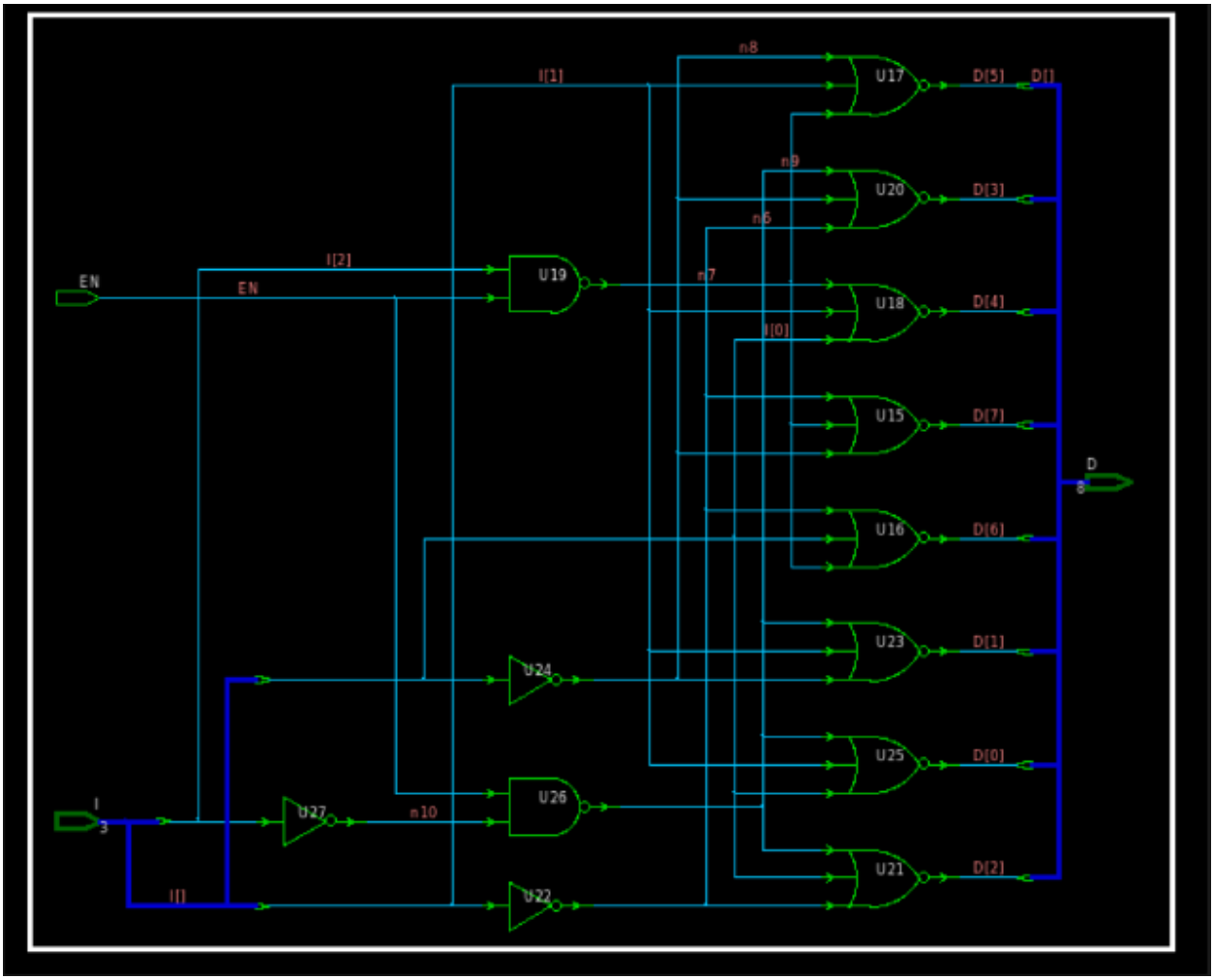

Figure 2: U2 is 3:8 Behavioral

V: Synthesis of Designs



This is the synthesized circuit from the behavioral design, and it is worth noting it is basically identical to the structural circuit.

```
Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.2889 uW   (48%)
  Net Switching Power  =   1.4057 uW   (52%)
                         ---------
Total Dynamic Power    =   2.6946 uW  (100%)

Cell Leakage Power     = 189.6322 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000           0.0000  (   0.00%)
register           0.0000           0.0000              0.0000           0.0000  (   0.00%)
sequential         0.0000           0.0000              0.0000           0.0000  (   0.00%)
combinational      1.2889           1.4057          1.8963e+05           2.8842  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total              1.2889 uW        1.4057 uW       1.8963e+05 pW        2.8842 uW
1
dc_shell>
```

Figure 3: Behavioral Report Power

```
****************************************
Report : area
Design : decoder_3to8_behavioral
Version: S-2021.06-SP5-4
Date   : Tue Jan 30 15:40:33 2024
****************************************

Library(s) Used:

    saed90nm_max (File: /synopsys/GPDK/SAED_EDK90nm/D

Number of ports:                           12
Number of nets:                            17
Number of cells:                           13
Number of combinational cells:             13
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          3
Number of references:                       3

Combinational area:                94.003202
Buf/Inv area:                      16.588800
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:              3.815851

Total cell area:                   94.003202
Total area:                        97.819053
1
dc_shell>
```

Figure 4: Behavioral Report Area