ELE447 HW1 CHASE LOTITO

(1) IV Characteristics. Current is generally dependent on carrier density and carrier velocity : $I \sim nv$.

Using an expression for electron density in terms of the density-of-states and the Fermi distribution function, explain how in a MOSFET current is controlled by gate voltage.

From class the equilibrium electron concentration is:

$$n_0 = \int_{-\infty}^{\infty} g(E) f(E)\, dE$$

This integral tells us that $n_0$ is proportional to both the density of energy states in a system and the distribution of electrons within those states over a energy range in question, $(-\infty, \infty)$ meaning all energy in the system.

We want to control the electrons we have in the MOSFET, so we must control g and f, therefore we must control energy, E.

$V = \frac{PE}{Q}$

The definition of voltage is the electric potential energy per unit charge. So, if we apply voltage to our semiconductor, we hope to increase energy in our system causing more energy states for electrons to occupy and distribute them within the states.

Specifically, we apply a voltage at the GATE, which provides electric potential across the channel region. The channel region then gains more energy states for $e^-$ to occupy, they're more likely to enter those states, so we have increased $e^-$ presence in the channel region and we have ↑current flow.

This is assuming g(E) and f(E) are proportional to E.

② How does device scaling (reducing FET size) lead to cheaper and high-performance systems (eg. microprocessors)?

By reducing the size of devices we can reduce cost in a few ways: and increase performance

① Less material

①a Less material waste

② Reduced time delay

③ Reduced power consumption

cost reduction

① By using smaller devices we naturally need less material to construct the same number of devices as before, so production costs are lowered. But due to the nature of semiconductor manufacturing, reducing the size of the devices allows the cross-sectional area of a Si wafer to be populated optimally, and we get more out of the same material.

② We know $\Delta t = \frac{CV}{I}$ for a device. The best thing we can do as of yet to reduce this delay is to reduce the capacitance, C. $C = \frac{\varepsilon A}{d}$. Specifically in reducing size, if the area A of the device is smaller, then we have reduced capacitance and reduced time delay. Now the device has higher-performance.

③ But if we've reduced time-delay, then we have the same I/V happening over less time. In other words, same energy over less time. This means we also reduce average power consumption. This reduces cost and increases performance.

(3) Read examples 1.1, 1.2, and 1.4. Then work out:

[1.3] Lattice constant of Si is ~~[illegible]~~ 5.43 Å. Calculate:

A) Distance from the center of one Si atom to the center of its nearest neighbor

B) The number density (#/cm³) of Si atoms.

c) The mass density (g/cm³) of Si.

(A) Si crystallizes in a diamond structure, Zincblende. The diamond structure is composed of smaller tetrahedral structures:

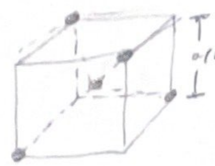
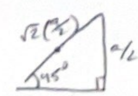



Fig 1.12 in book.

4 of these makes one diamond structure. (+4 corner atoms) (+6

• → Si atom

For all of these atoms, the nearest is corner-to-center. This distance d. is half the diagonal of a square.




$$\Rightarrow d = \frac{1}{2}(\sqrt{2})(a/2) = \frac{1}{2}(\sqrt{2})\left(\frac{5.43\times10^{-8}\,cm}{2}\right) = 1.92\times10^{-8}\,cm = \boxed{1.92\,Å}$$

(B) A diamond structure has the following: 8 corner atoms, 6 face atoms, and 4 internal atoms.

$$\Rightarrow \#\text{ Si atoms} = \frac{1}{8}(8) + \frac{1}{2}(6) + 4 = 1+3+4 = 8\text{ atoms.}$$

1+3+8 = 12

The volume of a diamond is $V = a^3 = (5.43\times10^{-8}\,cm)^3 = 1.601\times10^{-22}\,cm^3$

$$\therefore\ n = \frac{8\text{ atoms}}{1.601\times10^{-22}\,cm^3} = 4.997\times10^{22}\,\frac{\text{Si atoms}}{cm^3} = \boxed{5.00\times10^{22}\,\frac{\text{Si atoms}}{cm^3}}$$

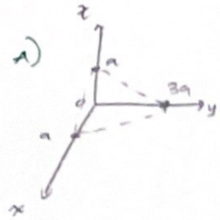
(C) From a periodic table, the molar mass of Si is 28.086 g/mol.

$$\Rightarrow \frac{5.00\times10^{22}\text{ Si atoms}}{1\,cm^3}\cdot\frac{1\text{ mol Si}}{6.02\times10^{23}\text{ Si atoms}}\cdot\frac{28.086\,g}{mol} = 2.333\,g/cm^3$$

∴ the mass density of Si is $\boxed{2.33\,g/cm^3}$

$\boxed{1.16}$ For a cubic lattice, determine the Miller Indices of the planes below.

A)



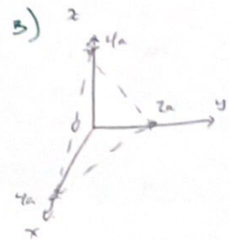

INTERCEPTS: $x = a,\ y = 3a,\ z = a$

$$\Rightarrow \left(\frac{1}{a}, \frac{1}{3a}, \frac{1}{a}\right) \cdot 3a$$

$$= (3, 1, 3)$$

$\therefore$ plane a is a $\boxed{(313) \text{ plane}}$

B)




INTERCEPTS: $x = 4a,\ y = 2a,\ z = 4a.$

$$\Rightarrow \left(\frac{1}{4a}, \frac{1}{2a}, \frac{1}{4a}\right) \cdot 4a$$

$$= (1, 2, 1)$$

$\therefore$ plane B is a $\boxed{(121) \text{ plane}}$.

# Chase Lotito - ECE447 - HW1

> Q4: Based on your understanding of semiconductor manufacturing, write 3 multiple choice questions.

### Q1: If you're looking to start making silicon semiconductors, from what two groups on the periodic table will you choose atoms for your n-type and p-type semiconductor regions?

    (A) N-TYPE: GROUP 13, P-TYPE: GROUP 14
    (B) N-TYPE: GROUP 14, P-TYPE: GROUP 15
    (C) N-TYPE: GROUP 15, P-TYPE: GROUP 13
    (D) N-TYPE: GROUP 16, P-TYPE: GROUP 12
    [ANS: C]

### Q2: Semiconductor manufacturing is both an additive and subtractive process. For the subtractive part, what steps are taken to reveal devices on a silicon wafer?

    (A) 1. SiO2 Layer, 2. Photoresist, 3. Expose through Photomask, 4. Plasma etch.
    (B) 1. Pure Si layer, 2. Photoresist, 3. Expose through Photomask, 4. Plasma etch.
    (C) 1. SiO2 Layer, 2. Photoresist and expose 3. Plasma etch, 4. Ion implant exposed regions
    (D) 1. SiO2 Layer, 2. Photomask, 3. Machine away template, 4. Chemically smooth machining impurities
    [ANS: A, not C since last is additive]

### Q3: There are many ways to test if a semiconductor device was manufactured properly. What are tools or methods that are used in the testing process?

    (A) Electron microscopy.
    (B) Sputtering machines.
    (C) Clean rooms.
    (D) Ion implantation.
    [ANS: A]