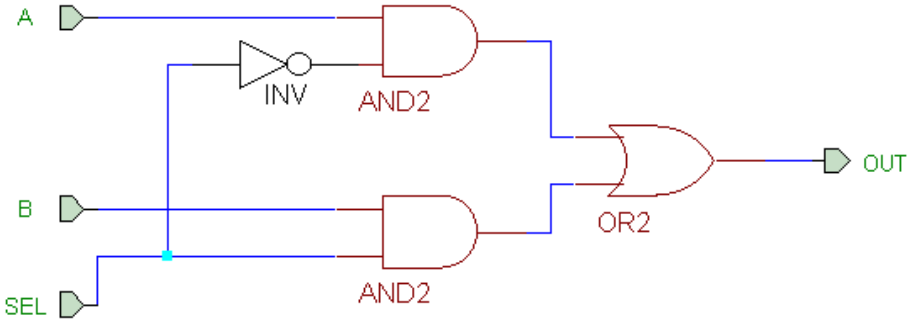
ECE 426/516 **Implementation of VLSI Systems with HDL**

HW#2 Design of Combinational Circuits Using Verilog

Due Date: 11:30pm Feb 5th, 2024

Question 1 Use Verilog to describe the following 2:1 multiplexer.



a) Use gate-level modeling.

```
module mux2_1 (SEL, A, B, OUT)
input SEL, A, B;
output OUT ;
NOT (_____) ;
AND (_____) ;
AND (_____) ;
OR (_____) ;
endmodule
```

b) Use continuous assignment statements

```
module mux2_1 (SEL, A, B, OUT)
input SEL, A, B;
output OUT;
assign Out = _____;
endmodule
```

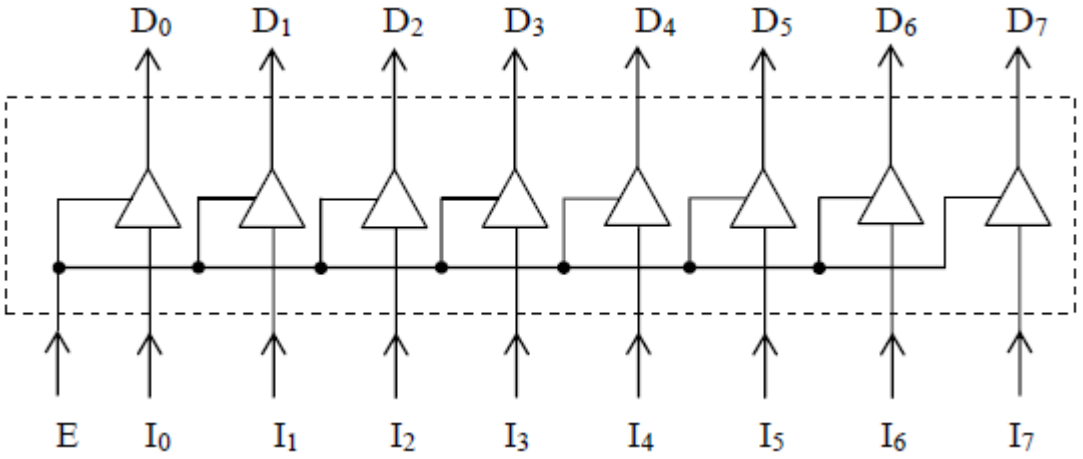
c) Use an "always" procedure block.

```
module mux2_1 (SEL, A, B, OUT)
input SEL, A, B;
output OUT;
reg OUT;
always @ (_____) begin
if (SEL)  _____;
else      _____;
end
endmodule
```

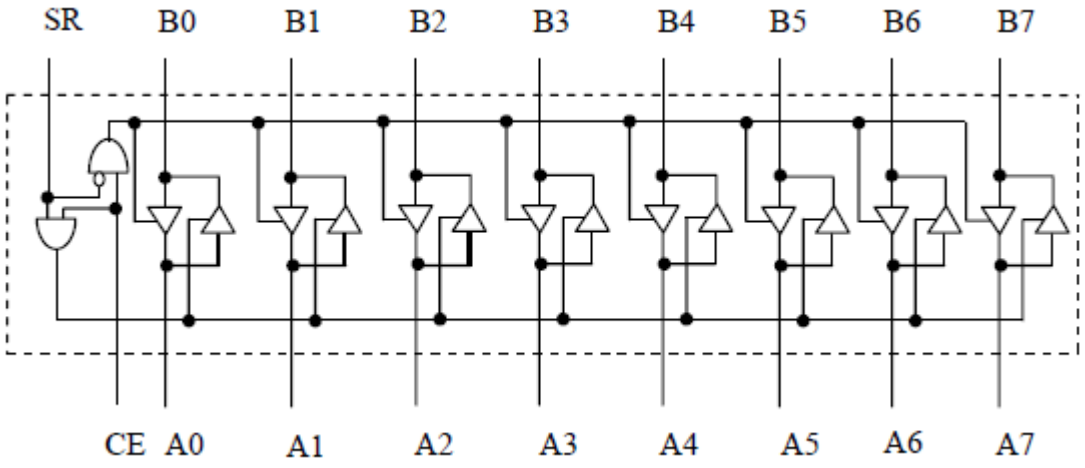
Question 2 (**Verilog using structural gates**): tristate buffers can be implemented with primitive gates. Assume primitive buffer, inverter, and AND gates are available as:

bufif1 (output_port_name, input_port_name, enable_port_name)
not (output_port_name, input_port_name)
and (output_port_name, input_port_name, input_port_name)

Write Verilog codes for the following circuits using these primitive gates. Please write a test bench to simulate your Verilog code. Include your Verilog code, test bench and simulation waveforms in your solution.



(a) Eight-bit buffer array



(b) Eight-bit bi-directional buffer array

Question 3: (**Verilog using structural gates**): A minority function is generated if the input signals have less 1's than 0's. Realize such a function in Verilog for 4 inputs using structural gates. These structural gates may include nor, or, xor, xnor, and, nand gates. Please write a test bench to

simulate your Verilog code. Include your Verilog code, test bench and simulation waveforms in your solution.

Question 4: (**Verilog using structural gates):** Parity generator/checker is commonly used to detect errors in data communication. "Even' parity output, OP, goes high when an even number of data inputs among I0 through I7 are high. Write a Verilog code to implement such an even parity generator using primitive gates.

Question 5: (**Verilog for min-term realization):**
Write Verilog codes to realize the function Σ (0, 2, 4, 6, 9, 10, 13, 15).

Question 6: (**Verilog for circuit schematic implementation**):