

A Self-Triggered Pulsed-Mode Flyback Converter for Electric-Field Energy Harvesting

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Abstract—Electric-field energy harvesting (EFEH) from medium-voltage (MV) power lines is an emerging technology to energize the low-cost distributed electronic measurement systems that are needed to monitor vital line parameters for smart grid systems. The challenge with EFEH is to extract energy without requiring a direct connection to the power line conductor. This severely constrains the amount of continuous energy that can be obtained because of the weak capacitive coupling between the power line and the energy harvesting system. This paper addresses this challenge, by using a self-triggered discontinuously operating flyback converter to transform a high-voltage dc bus rectified from the weakly coupled ac supply down to useful low-voltage levels. The results show that over 20 mW of continuous power can be extracted from a 12.7-kV MV line using this approach. Detailed circuit analysis and matching experimental results are presented to validate the concept.

Index Terms—Electric fields, energy harvesting, power electronic converters, smart grids.

I. INTRODUCTION

ONE of the potential benefits of smart grids is the creation of decentralized electrical networks that can manage bidirectional power flow on a localized basis to match generation and demand [1]. The effective implementation of this concept requires regular monitoring of grid variables such as power line voltage, current, and temperature [2], [3]. At the distribution network level, technologies such as wireless sensor networks are popular candidates for this role [4], [5]. However, self-powering of these monitoring systems is highly desirable for the very large numbers of devices that are required, to achieve a cost-efficient implementation without requiring the use of separate energy sources such as batteries [6]. Energy harvesting, i.e., the extraction of milliwatt levels of energy from sources near to the monitoring system, offers an attractive solution to this problem [7].

For medium-voltage (MV) distribution power lines operating at voltages of 11 or 22 kV, the strong electric fields that they radiate provide the potential to extract energy using capacitive coupling from the line. This approach is called

electric-field energy harvesting (EFEH) [8], where energy is collected from the parasitic capacitive displacement current that flows from the conductor to earth. Energy scavenged in this way is always available when the distribution line is energized, which is a significant benefit compared to approaches such as magnetic field energy harvesting that depends on the magnitude of the load current flowing through the line.

The main challenge with an EFEH system is the magnitude of the parasitic capacitance between the power line conductor and ground—typically no more than a few tens of picofarads [9]. Hence, the displacement current through this capacitance is at most only several hundred μA even for a high-voltage (HV) line. Most often, the energy harvester is inserted in series between the power line or ground (i.e., either conductor referenced or ground referenced) and the parasitic coupling capacitance. The displacement current then flows through the harvester input circuit bridge rectifier, slowly charging a low-voltage dc bus capacitor [8]–[10]. However, the continuously available energy using this strategy is usually well under 1 mW, so that the stored energy in the dc-bus capacitor can only operate the monitoring circuit in a burst mode for brief periods after long intervals of charging [11], [12]. Moghe *et al.* [13] use a more advanced two plate approach with an internal power conversion system to continuously extract up to 17 mW into a 50- Ω resistive load from a 35-kV power line. However, the available continuous power falls OFF rapidly for different output load resistances. Essentially, the main limitation with all these systems is that the input voltage to the harvester is quite small, which significantly constrains the energy that is continuously available for harvesting.

A better approach is to make the harvester ac input voltage much higher, as can be done by feeding the input through an ac step-down transformer before rectification [14]. Continuously extracted power levels of up to 370 mW from a 150-kV line have been reported with this strategy, using a cylinder electrode wrapped around the HV conductor [2], [3], [15]. However, since the transformer design is challenging, and the result is bulky and heavy, this approach has its limitations.

This paper now presents a new approach for a galvanically isolated EFEH system to self-power electronic systems from an MV distribution line that addresses these limitations. A two-section topology is proposed, using a passive diode rectifier to charge a dc-bus capacitor from the incoming ac to as high a voltage as possible (limited by the switching device voltage ratings), and then a self-powered flyback converter

Manuscript received February 23, 2017; revised June 7, 2017; accepted July 5, 2017. Date of publication August 11, 2017; date of current version January 31, 2018. Recommended for publication by Associate Editor Yi Tang. (Corresponding author: Brendan McGrath.)

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Digital Object Identifier 10.1109/JESTPE.2017.2738157

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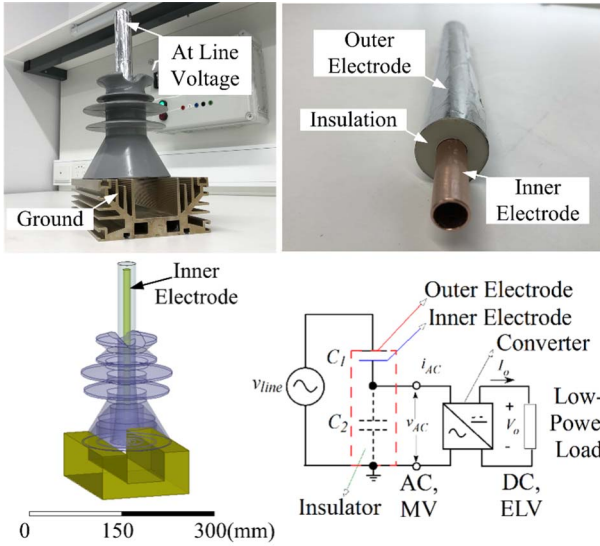


Fig. 1. Insulator-based EFEH. (Top) Experiment. (Bottom) FEA simulation model and conversion scheme.

operating in discontinuous pulse mode to extract and transform the energy from this bus capacitor down to a useful low dc voltage level. The converter pulsed energy transfer sequence operates once per half-ac fundamental cycle, and can continuously harvest over 23 mW of power from a 12.7-kV MV feeder. Detailed circuit analysis and matching experimental results are presented in this paper to confirm the approach.

II. PRINCIPLE OF AN INSULATOR-BASED EFEH

Power line insulators support and isolate the power line conductors as they pass across supporting poles. They are typically constructed as a cascaded set of porcelain “sheds” linked by an internal connecting pin. For the EFEH system, this pin is now extended beyond the top of the main insulator, surrounded by a cylindrical insulation extension, and then sheathed by an outer electrode which connects to the power line conductor. A physical proof of concept of this arrangement is shown in Fig. 1 (top). The structure forms a parasitic capacitive divider network as shown in Fig. 1 (bottom right), where C_1 represents the capacitive coupling between the outer electrode sheath and the inner electrode pin, and C_2 represents the (parasitic) coupling of the inner electrode pin to the pole earth. Energy is then scavenged by connecting an energy conversion system in parallel with C_2 , shown in Fig. 1 (bottom right) as a stylized power electronic converter that transforms the ac voltage developed across C_2 down to an appropriately extra-low dc voltage level for use by an electronic load [16]. Note that with this arrangement, galvanic contact is not required between the power line and the harvesting inner electrode. The values of the capacitances in this structure were determined as $C_1 = 43$ pF and $C_2 = 0.14$ pF, by analyzing the 3-D model shown in Fig. 1 (bottom left) using finite-element analysis (FEA). The methodology in [16] was then used to confirm these capacitances, with the outer electrode fed from a 1.22-kV source and various test resistances connected across C_2 to emulate the converter that absorbs energy from the capacitive divider. The voltage developed

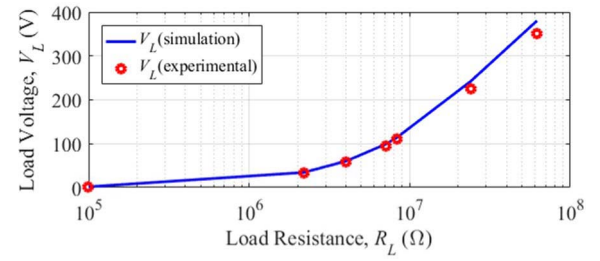


Fig. 2. Experimental validation of FEA calculated electrode capacitance using a 1.22-kV source supply [16].

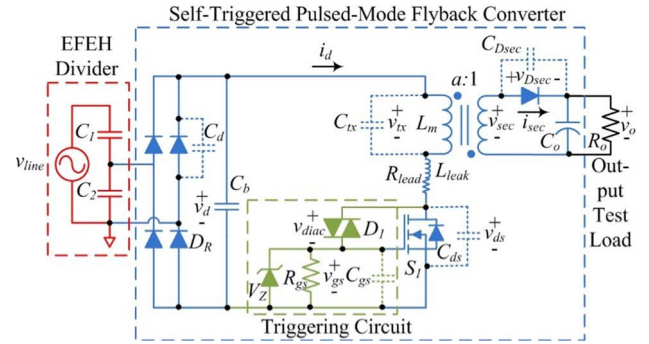


Fig. 3. EFEH with the proposed conversion system.

across each value of load resistance V_L was measured and compared against matching computer simulations using the FEA estimated values for C_1 and C_2 and including the loading effect of the experimental measurement probes. From the results shown in Fig. 2, it can be seen that the simulated and experimental load voltages are in very good agreement, confirming the theoretical coupling capacitance values.

Using this approach, the simple relationship of $P = V_L^2/R_L$ identifies that the EFEH scavenged energy is maximized by making the voltage across C_2 as large as possible. Under this condition, the primary MV supply feeding through C_1 essentially acts as a current source injecting into C_2 and the conversion system [16], with a maximum possible current of $I_{C1} = V_{ac}/X_c = 12.7 \text{ k} \times 2\pi 50 \times 43 \text{ e}^{-12} \approx 170 \text{ } \mu\text{A}$. Any realistic impedance loading, the system will reduce this input current only marginally, since the voltage across any practical power electronic converter load must be limited to about 1000 V (peak) so that it can operate with realistically rated semiconductors. For example, a 4-M Ω load resistor will limit the peak load voltage to $V_L \approx \sqrt{2} \times 170 \text{ } \mu\text{A} \times 4 \text{ M}\Omega = 970 \text{ V}_{\text{peak}}$ and in principle extract a power $P = 970^2/(2 \times 4 \text{ e}^6) = 117 \text{ mW}$, while increasing the overall impedance connected to the 12.7 kV line by only about 5%. However, it is quite challenging in practice to design a physical conversion system that will operate with this very low input current. This issue is the main focus of this paper and will now be explored in detail.

III. SELF-TRIGGERED PULSED-MODE FLYBACK CONVERTER FOR EFEH

The role of the power electronic converter shown in Fig. 1 is to create a suitable dc power supply for electronic power line monitoring systems. The design of this converter is quite

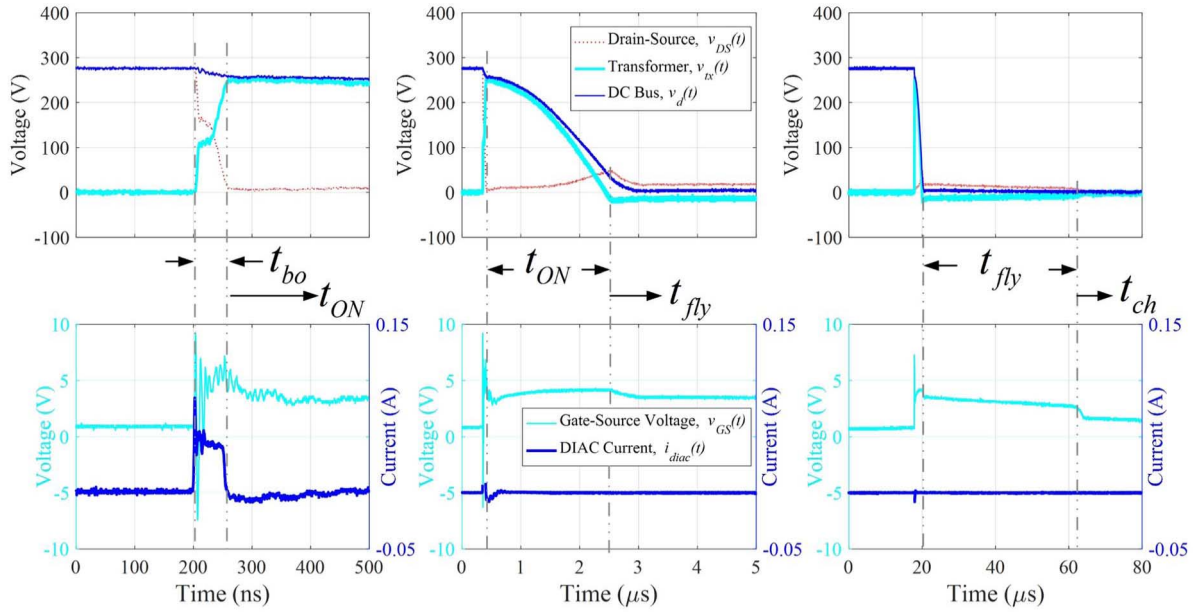


Fig. 4. Switching waveforms for one energy transfer pulse in the scale of (left) 500 ns, 10 μ s (center), and 100 μ s (right).

challenging, since it must operate at a high input voltage (with a large step-down ratio) to maximize the harvested energy. A continuously switching active converter is impractical in this role, since semiconductor devices with adequate voltage ratings usually have parasitic capacitances of the same order as the very small values of the ac input capacitor divider. To illustrate, if an active ac–dc converter phase leg was connected across C_2 , the (say) 1700-V FET devices that would be appropriate to block the 970 V+ peak input voltage, typically have drain–source capacitances of ~ 100 pF. Hence, the available 170- μ A ac input current would require nearly 0.5 ms to commutate the phase leg as the two device capacitances charge/discharge. Clearly any form of continuously switched high-frequency conversion is almost impossible with such transition times.

The conversion system presented here to overcome these challenges is shown in Fig. 3. The converter input uses a simple diode rectifier to convert the 50-Hz ac voltage developed across C_2 into a relatively high dc voltage. The second converter section then uses a pulsed operation dc–dc flyback converter to transform this voltage down to a useful low-voltage output. The converter operates as follows.

A. Principle of Operation

Each energy transfer pulse is initiated by turning ON the converter main switch S_1 when the dc-bus voltage charges up to a defined trigger voltage V_{bo} , to transfer the energy stored in the dc bus capacitance into the coupled inductance of the flyback converter. Since the rate of this energy transfer is much higher than the incoming power flow from the ac side, the dc-bus capacitor discharges, and the dc-bus voltage collapses. When it reaches a sufficiently low value, switch S_1 turns OFF, and the energy stored in the coupled inductance transfers to the secondary side rectifier and load via a conventional flyback

sequence. Once the energy transfer cycle is complete, the HV dc-bus voltage slowly recharges from the incoming ac supply until it again reaches the trigger voltage level, and another energy transfer pulse is initiated. More than one energy pulse may occur over each half-ac fundamental cycle, depending on the ac input voltage magnitude and the various capacitances shown in Fig. 3.

A primary target for this system was to directly trigger S_1 using energy taken from the dc bus, without requiring any auxiliary supply. This is achieved by connecting the DIAC string D_1 across the drain–gate of the main MOSFET S_1 . When the dc-bus voltage charges up to the DIAC string breakover voltage V_{bo} , the string triggers to a low impedance state and dumps charge into the gate of S_1 from the dc-bus capacitor via the transformer parasitic capacitance C_{tx} . This turns S_1 on to begin the pulsed energy transfer cycle. D_1 only remains in conduction until its current drops below its minimum threshold, which happens once the S_1 drain–source voltage falls. It then reverts to high impedance, ready for the next energy transfer pulse.

B. Detailed Circuit Response (LV Breakover)

To conveniently study the circuit response in detail, the conversion system described in Section II was fed from a 500-V dc supply feeding through a 10-M Ω resistor, which allowed the rectified dc bus voltage v_d to slowly charge up toward 500 V over several seconds. The DIAC string breakover voltage was reduced to 284 V (eight individual DIACs in series) so that the flyback converter would trigger at this lower dc bus voltage. This arrangement allowed detailed switching waveforms to be captured without the difficulty of measuring them at full operating voltages. Fig. 4 shows the experimental results, with switching waveforms presented over three different time scales to show the various stages of the energy transfer cycle.

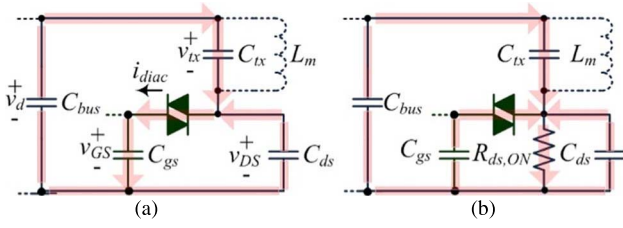


Fig. 5. DIAC breakover interval equivalent circuits. (a) Gate charge. (b) Switch turn ON.

1) *Stage #1: DIAC Breakover Interval* (t_{bo} , ~ 50 ns): Stage #1 starts when the dc-bus voltage reaches the breakover voltage of the DIAC string V_{bo} and it triggers to become a low impedance. This creates a current pulse that transfers the charge from the total effective bus capacitance C_{bus} in series with the transformer primary winding parasitic capacitance C_{tx} , and the (parallel) S_1 drain-source capacitance C_{ds} , as per the equivalent circuit shown in Fig. 5(a), into the S_1 gate-source capacitance C_{gs} . Consequently the gate voltage of S_1 rises to its threshold level, turning it ON to create a low resistance path between its drain and source terminals, as shown in Fig. 5(b). Since two of the rectifying diodes are conducting during this interval, the effective total bus capacitance is given by the parallel combination of the dc bus capacitance, the nonconducting diode parasitic capacitances, and the ac source coupling capacitance, i.e., $C_{bus} = C_b + 2C_d + C_1 + C_2$.

As shown in Fig. 4 (left), as S_1 turns ON, its drain-source voltage falls to zero, impressing the dc bus voltage across the primary winding of the flyback transformer and thus starting the energy transfer pulse. When this drain-source voltage reaches zero, the current flowing through D_1 ceases since it is now short circuited by S_1 , and it reverts to high impedance. This completes the turn-ON process, with enough charge dumped in the gate capacitance of S_1 for it to continue to conduct for the next t_{ON} period.

From Fig. 4 (left), it can also be seen how the q_{gs} charge transfer from C_{bus} to C_{tx} and C_{gs} during t_{bo} reduces the dc bus voltage from its original V_{bo} value to V_d , determined as

$$V_d \approx \frac{C_{bus}}{C_{bus} + C_{tx}} \left(V_{bo} - \frac{q_{gs}}{C_{bus} + C_{ds}} \right). \quad (1)$$

V_d is the voltage that is thus established across the transformer primary winding at the start of Stage #2.

2) *Stage #2: Energy Storage Interval* (t_{ON} , ~ 2 μ s): During Stage #2, the flyback transformer magnetising inductance L_m remains connected across the dc bus through the channel resistance $R_{ds,ON}$ of S_1 as shown in Fig. 6. This creates an LC circuit through which the energy from the dc bus new total paralleled capacitance $C_{ON} = C_1 + C_2 + 2C_d + C_b + C_{tx}$ transfers to the magnetising inductance L_m as a quarter cycle oscillation.

From the upper trace in Fig. 4(center), it can be seen how the increasing current through S_1 created by this response increases its drain-source voltage. This is because the channel resistance of S_1 is relatively high because it is not turned ON strongly. Furthermore, and somewhat paradoxically, it is

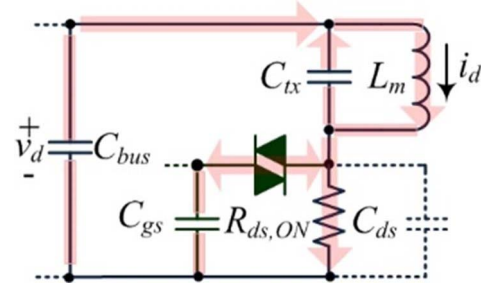


Fig. 6. Equivalent circuit during the energy storage interval.

interesting to see that this increasing drain-source voltage slightly increases the gate-source voltage of S_1 as can be seen in the lower trace of Fig. 4 (center), via coupling through the drain-gate capacitance. However, this second-order effect has little influence on t_{ON} .

The response of the LC circuit during t_{ON} can be approximately determined (ignoring the increasing drain-source voltage across S_1) as

$$v_d(t) \approx V_d \cos \left(t / \sqrt{L_m C_{ON}} \right) \approx v_{tx}(t) \quad (2a)$$

$$i_d(t) \approx V_d \sqrt{C_{ON} / L_m} \sin \left(t / \sqrt{L_m C_{ON}} \right) \quad (2b)$$

using simple ac circuit theory.

Interval t_{ON} finishes when the voltage across the transformer primary winding passes through zero, and changes polarity. Assuming that the dc-bus voltage is essentially zero at this point, t_{ON} can be calculated by determining when (2a) reaches zero, that is

$$t_{ON} = (\pi/2) \sqrt{L_m C_{ON}}. \quad (3)$$

The energy transferred to the magnetizing inductance during this energy pulse can then be calculated by

$$E_d = \int_0^{t_{ON}} v_d(t) i_d(t) dt \quad (4)$$

which, substituting from (2) and (3), solves as

$$E_d = (1/2) C_{ON} V_d^2. \quad (5)$$

Equation (5) identifies the maximum energy that can be extracted from the dc-bus consolidated capacitance for one energy transfer pulse, without taking losses into account.

3) *Stage #3: Flyback Interval* (t_{fly} , ~ 40 μ s): Fig. 4 (right) shows waveforms for the flyback interval t_{fly} , which begins when the voltage across the flyback transfer primary winding reverses and the secondary winding rises to the voltage $V_o + V_{Dsec,fw}$ (i.e., sufficient to turn ON the secondary rectifier diode with a forward voltage of $V_{Dsec,fw}$). This provides a discharge path to the output filter capacitor C_o , as shown in the equivalent circuit of Fig. 7, which allows the energy stored in the magnetizing inductance to transfer to this capacitor.

As the secondary winding current increases at the start of t_{fly} , the primary winding current correspondingly decreases by transformer action. This can be seen by the reducing drain-source voltage of S_1 in the top of Fig. 4 (center) at the start of t_{fly} . This reducing voltage decreases the

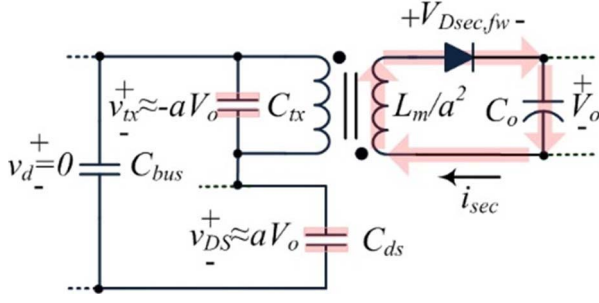


Fig. 7. Equivalent circuit during the flyback interval.

gate–source voltage of S_1 through drain–gate capacitance coupling, as shown in the bottom of Fig. 4 (center), which usefully helps to turn it OFF in preparation for the flyback energy transfer to the secondary side.

The secondary winding discharge current i_{sec} now continues until all the stored magnetic energy has been transferred to the output capacitor at the end of t_{fly} , that is

$$q_{\text{fly}}(t) = \int_0^{t_{\text{fly}}} i_{\text{sec}}(t) dt = C_o \Delta V_o \approx \frac{t_{\text{fly}} I_{\text{sec,max}}}{2} \quad (6)$$

using the conventional flyback converter assumption of a triangular approximation for the shape of $i_{\text{sec}}(t)$. The peak secondary current $i_{\text{sec,max}}$ can be determined from (2b) as

$$i_{\text{sec,max}} = a i_{d,\text{max}} = a V_d \sqrt{C_{\text{ON}}/L_m} \quad (7)$$

where a is the turns ratio of the flyback transformer.

Without considering losses, the energy stored in the magnetizing inductance during t_{ON} is equal to the energy transferred to the output capacitor, so that

$$E_o = V_o C_o \Delta V_o \approx E_d. \quad (8)$$

Combining (5)–(7) then gives an estimate of t_{fly} as

$$t_{\text{fly}} \approx \frac{V_d \sqrt{L_m C_{\text{ON}}}}{a V_o}. \quad (9)$$

At the end of this interval, the secondary rectifier diode turns OFF, the primary and secondary transformer winding voltages become zero (matching the discharged dc-bus voltage) and the HV dc bus is ready for recharge. From Fig. 4 (right), it can also be seen how the gate capacitance of S_1 has significantly discharged during this period, via the gate discharge resistance. The time constant of this RC circuit is designed so that the gate voltage is low enough at the end of t_{fly} to ensure that S_1 remains turned OFF as the HV dc bus now recharges.

4) Stage #4: Bus Recharge Interval (t_{ch}): At the end of each energy transfer pulse, the converter circuit reverts to the ac input source feeding through capacitor C_1 into the effective dc bus capacitance C_{OFF} through the conducting diodes of the input rectifier. This bus capacitance is given by the actual bus capacitance C_b in parallel with the MOSFET drain–source capacitance, the nonconducting diode parasitic capacitances and the parasitic ac side capacitance C_2 , i.e., $C_{\text{OFF}} = C_2 + 2C_d + C_b + C_{\text{ds}}$. The voltage across C_{OFF}

begins rising from zero at the start of the recharge interval t_{ch} according to the offset sinusoidal relationship of

$$v_d(t) = V_{\text{OFF,peak}} \sin(\omega_o t + \varphi) - V_{\text{OFF,peak}} \sin \varphi \quad (10)$$

where $V_{\text{OFF,PEAK}} = V_{\text{line,peak}} C_1 / (C_1 + C_{\text{OFF}})$, and $\varphi = \omega_o t$ is the phase angle of the ac input voltage at which each dc bus recharging cycle starts. Equation (10) can be linearized over each t_{ch} period as

$$v_d(t) \approx t \omega_o V_{\text{OFF,PEAK}} \cos \varphi, \quad t \in t_{\text{ch}}. \quad (11)$$

Equation (11) is always linearly increasing for each recharge interval over the range $-\pi/2 \leq \varphi \leq \pi/2$ (since the input current through C_1 leads the ac input voltage by $\pi/2$, which is the period where one diode pair of the input rectifier is conducting). Also, since the cycle of discharge and recharge is symmetrical across each ac half cycle, the recharge stage only needs to be analyzed over one half cycle.

At the end of t_{ch} , the dc-bus voltage will reach the breakover voltage of the DIAC string and start a new pulse energy transfer cycle. Hence, the number of energy transfer pulses that occur in each ac half cycle depends on the value of t_{ch} . For each pulse cycle, t_{ch} can be solved from (11) by setting $v_d(t_{\text{ch}}) = V_{\text{bo}}$. However, it is also clear from (11) that t_{ch} is not constant, but is instead a function of φ which varies as the incoming ac voltage magnitude changes. Hence, an average value for t_{ch} needs to be found by recognizing that

$$v_d(t_{\text{ch}}) = V_{\text{bo}} = \omega_o V_{\text{OFF,peak}} \overline{\cos \varphi} \times \overline{t_{\text{ch}}} \quad (12)$$

over the period $-\pi/2 \leq \varphi \leq \pi/2$. Since

$$\overline{\cos \varphi} = (1/\pi) \int_{-\pi/2}^{\pi/2} \cos \varphi d\varphi = 2/\pi \quad (13)$$

$\overline{t_{\text{ch}}}$ can then be solved as

$$\overline{t_{\text{ch}}} = \pi V_{\text{bo}} / 2 \omega_o V_{\text{OFF,peak}} \quad (14)$$

which provides an estimate for the average duration of the recharge interval. This allows the number of energy pulses expected for each fundamental half cycle to be predicted.

5) Energy Transferred: Ignoring losses, the total energy transferred through the flyback transformer in one ac source half cycle is nE_d , where n is the number of pulses that occur during that period. Since $t_{\text{ch}} \gg t_{\text{fly}} > t_{\text{ON}}$, this number can be approximately estimated as the greatest integer of the expression $(T_o/2)/\overline{t_{\text{ch}}}$ where $T_o = 1/f_o$ is the period of the input ac line voltage. Using (14), this gives

$$n \approx \lfloor (2C_1 V_{\text{line,peak}}) / (C_{\text{OFF}} V_{\text{bo}}) \rfloor. \quad (15)$$

With a total energy harvested per half cycle of nE_d , the total continuously scavenged power is then given by

$$P \approx nE_d \omega_o / \pi. \quad (16)$$

Equations (5), (15), and (16) define the relationship between the output power, the pulse transfer breakover voltage V_{bo} and the dc bus capacitance C_b . Fig. 8 shows this relationship for values of C_b up to 5 nF, and for four breakover voltages $V_{\text{bo}} = [292, 584, 860, 1140]$ V.

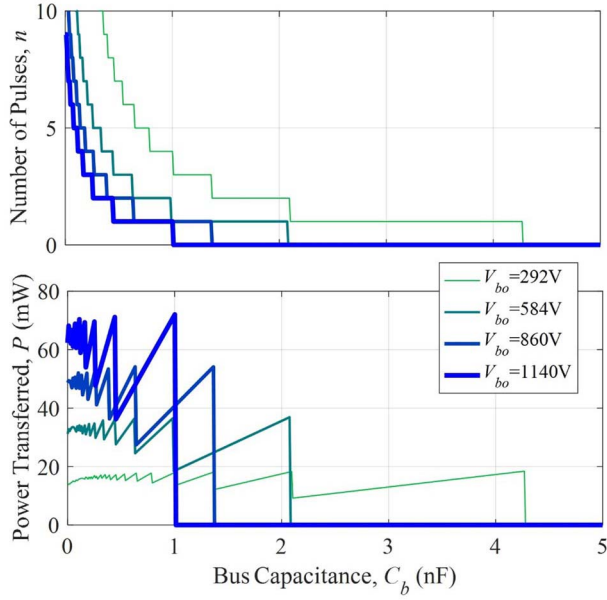


Fig. 8. Number of energy transfer pulses in half-cycle (top) and power transferred to the flyback transformer (bottom).

As can be seen in Fig. 8 (top), the number of energy transfer pulses per ac half-cycle drops with larger breakover voltage levels and larger bus capacitances, while the obtained power shown in Fig. 8 (bottom) increases as the triggering voltage and bus capacitance get higher. However, the power transfer is extremely sensitive to the changes in bus capacitance. For instance, with a breakover voltage of 292 V, the power reaches a maximum of 18 mW for about 4.3-nF capacitance. However, for a slightly larger capacitance the power abruptly collapses to zero as the number of half-period pulses drops below one.

From this analysis, the bus capacitance should be kept as low as possible to maximize the power transfer. However, even with a zero dc-bus capacitor, in practice, there will always be parasitic capacitances in the system which limits the number of energy transfer pulses that can be achieved. This issue will be illustrated in Section V. Furthermore, another important consideration for maximizing the extracted power is the system losses, which will now be considered.

IV. CIRCUIT LOSSES

The major losses that are significant for this circuit are the conduction losses in the primary MOSFET S_1 and in the secondary rectifying diode D_{sec} , with some smaller losses incurred by the self-triggering DIAC circuit. These losses can be analyzed as follows:

A. MOSFET Losses

For this circuit, the soft turn-ON of the MOSFET during the energy storage interval t_{ON} produces a significant resistive loss. This is because the channel resistance $R_{ds,ON}$ is much larger than is usual since the gate-source voltage during t_{ON} is only just above the minimum gate threshold $V_{GS(th)}$. Identifying this resistance from data sheets is not straightforward, since the

gate voltage is very hard to determine. Instead, an estimated value for $R_{ds,ON}$ was found as follows.

Using the experimental results presented in Section III, the drain-source voltage $v_{ds}(t)$ during t_{ON} was directly measured from Fig. 4 (middle), while the drain current $i_d(t)$ was determined using (2b). The instantaneous value of $R_{ds,ON}$ was then calculated as

$$R_{ds,ON}(t) \approx v_{ds}(t)/i_d(t) \quad (17)$$

which was averaged over t_{ON} . This gave a value of $R_{ds,ON}(t) \approx 620 \, \Omega$, which leads to an energy loss over t_{ON} of

$$E_{loss,sw} \approx \int_0^{t_{ON}} i_d^2 R_{ds,ON} dt = \frac{\pi C_{ON} R_{ds,ON} V_d^2 \sqrt{C_{ON}/L_m}}{4}. \quad (18)$$

Equation (18) defines the energy per pulse dissipated in $R_{ds,ON}$ during the energy storage switching interval t_{ON} , using the expressions for i_d and t_{ON} , defined in (2) and (3), respectively. Note that this loss is proportional not only to $R_{ds,ON}$ but also to the dc-bus voltage and capacitance. Experimentally, it accounts for about 44% of the total theoretically available energy, as will be seen in Section V.

B. Secondary Diode Losses

During the flyback interval t_{fly} , the secondary current through the diode D_{sec} causes an energy loss because of the diode forward voltage $V_{Dsec,fw}$. This loss is given by

$$E_{loss,Dsec} \approx \int_0^{t_{fly}} V_{Dsec,fw} i_{sec}(t) dt \quad (19)$$

and can be evaluated using (7) and (9), again under the assumption of a triangular-shaped waveform for $i_{sec}(t)$, as

$$E_{loss,Dsec} \approx V_{Dsec,fw} V_d^2 C_{ON} / 2V_o. \quad (20)$$

This loss is dependent on the forward voltage drop of the secondary diode and the maximum dc-bus voltage. Experimentally, it accounts for 25% of the total theoretically available energy, as will be seen in Section V.

C. Self-Triggering Losses

During the DIAC breakover interval, the charge necessary for S_1 to just turn ON is transferred from the dc-bus capacitance to the parasitic primary transformer winding C_{tx} and the MOSFET gate-source capacitance C_{gs} . The energy lost in this process is reflected in the bus voltage drop from V_{bo} to V_d according to (1), and is given by

$$\Delta E = 0.5 \times (C_{ds} - C_{tx})(V_{bo}^2 - V_d^2). \quad (21)$$

From the MV experimental results presented later in this paper, the drop in dc-bus voltage at the DIAC 1140-V trigger point was about 50 V, which represents an energy loss of 0.34%. Since this is significantly smaller than the major conduction losses just discussed, it was not analyzed in any more detail.

TABLE I
MAIN DESIGN PARAMETERS

Element	Parameter	Value
Flyback transformer		
Turns-ratio	a	4.47
Number of primary turns	N_l	148
Magnetising inductance	L_m	5.5mH
Inter-winding capacitance	C_{tx}	30.7pF
Core/Material		RM12/N41
DBR Diodes		
OFF Capacitance	C_d	2pF
MOSFET (nominal)		
Drain-Source capacitance	C_{ds}	50pF
Gate-Source Capacitance	C_{gs}	170pF
Secondary diode		
Forward voltage	$V_{Dsec, fw}$	1V
DIACs (each)		
Individual breakover	$V_{bo, each}$	32V
Designed lead resistance	R_{lead}	470 Ω
Output Circuit		
Output capacitor	C_o	5.6mF
Tested output load	R_o	820 Ω

TABLE II
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Description
ω_o	100 π rad/s	Grid angular frequency
V_{line}	4.5kV(rms)	AC line voltage
C_l	100pF	MV capacitor
C_2	17pF	LV capacitor
C_b	330pF	Added bus capacitance
C_{extra}	660pF	Parasitic bus lumped capacitance



Fig. 10. MV experimental setup.

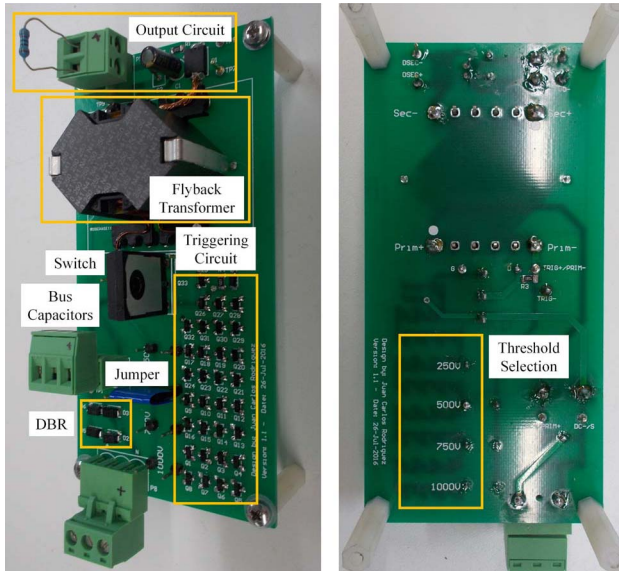


Fig. 9. Prototype converter (left) top (right) bottom.

V. EXPERIMENTAL VALIDATION (MV BREAKOVER)

A. Coupled Inductor Design

The design of the coupled inductor of the conversion system is somewhat unconventional compared to a conventional flyback converter. First, the magnetic core has to be selected as a choice between the minimum core size required to store the energy transferred in each energy transfer pulse without core saturation, and a larger core size that can accommodate more primary turns to increase L_m and thus reduce the MOSFET conduction losses as identified in (18). Consideration also needs to be given to the insulating capability of the selected core, recognizing that the primary winding must withstand nearly 1 kV until the DIAC string triggers. Taking these factors into account, an RM12 ferrite core was selected for the coupled inductor because this type of core integrates the benefits of compact pot cores (typically used in low-power SMPS) but with a large winding exit notch in the ferrite, which allows for more clearance distance [17]. In addition, the window

utilization factor of the bobbin was made smaller (24%) than is commonly used for standard flyback converters (40%) and high dielectric breakdown (7.5 kV) insulation adhesive tape were used in the design to achieve adequate insulation between windings. It should be noted, however, that the transformer only ever sees a peak voltage of 1140 V despite being nominally driven from a 12.7-kV ac supply, and hence, the insulation requirements of the winding are not as challenging as might be anticipated.

Next, the turns ratio was selected as a balance between the required reverse blocking voltage of the secondary rectifying diode, and the peak current flowing through this diode as the flyback period commences. Consideration also needed to be given to the reverse bias junction capacitance of the secondary diode, since this capacitance reduces the converter efficiency because it reflects back through the coupled inductor to the primary side during the energy charging interval t_{ON} .

The secondary diode selected was an MURS480ET3G, because of its (relatively) low forward voltage drop and low reverse-bias junction capacitance. Since this diode has a 400-V reverse blocking voltage, the turns ratio was then set to $a = 4.47$. This limits the reverse voltage that the diode has to block to less than 200 V, which is a comfortable margin compared to its rating.

Finally, the coupled inductor windings were wound using as thin wire as possible (particularly for the primary winding), to fully fill the bobbin window and thus achieve the maximum possible primary inductance. The windings were arranged in a sandwich configuration using a standard “U” winding technique, to reduce proximity and leakage inductance effects [17].

The design parameters for the coupled inductor and values of the other major system components are listed in Table I, while the prototype converter (components loaded on PCB) is shown in Fig. 9.

B. Medium-Voltage Experiment

The experimental prototype was tested under full scale operating conditions with an MV ac supply to confirm the

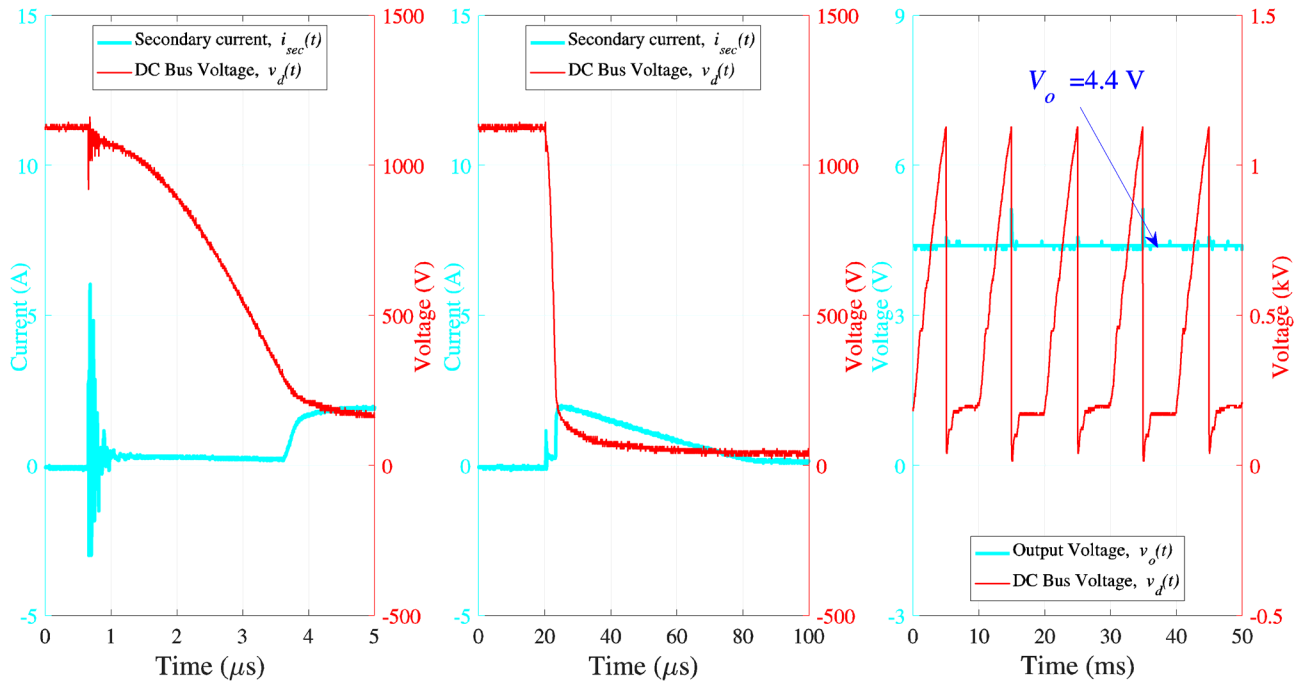


Fig. 11. Experimental results for 1024-V triggering voltage.

operation of the energy harvester under realistic operating conditions. However, the 12.7-kV line voltage was represented using the 4.5-kV (rms) ac supply available in the laboratory, feeding through a 100-pF HV coupling capacitor. This generated a maximum input current of $150 \mu\text{A}$, which is the same order of magnitude as for the full-line voltage system discussed in Section II. Hence, the proposed converter was working essentially at the designed maximum input triggering voltage and current levels (approximately 1 kV and about $150 \mu\text{A}$, respectively), so the study results matched what could be expected for a full field conditions. The parameters of the experimental setup are summarized in Table II.

Fig. 10 shows the experimental arrangement, which was found to introduce some additional capacitance C_{extra} to the dc bus. This capacitance was determined experimentally to be 660 pF, and adds to the parameter C_b . Such considerations are critical to evaluate a converter such as this, since the various conducted tests and the analysis shown in Fig. 8 have shown that the overall system is highly sensitive to any change in the effective bus capacitance. To identify the best possible power transfer conditions, different combinations of V_{b0} and C_b were then evaluated. V_{b0} was adjusted by setting a link on the PCB, as shown in Fig. 9, to choose between the four series strings of eight DIACs each. This allowed the response of the four triggering voltages of $V_{b0} = [292, 584, 860, 1140]$ V to be evaluated. Overall bus capacitances C_b of up to 1 nF (i.e., the sum of the actual C_b and C_{extra}) were then tested at each trigger voltage to determine the maximum possible power transfer that could be achieved.

From these tests, it was found that maximum power transfer was achieved with all four DIAC strings in series, (a triggering voltage of $V_{b0} = 1.14 \text{ kV}$), with a total effective bus capacitance of $C_b + C_{\text{extra}} = 1 \text{ nF}$. These conditions

TABLE III
THEORETICAL ENERGY TRANSFER

Parameter	Value	Description
E_d	713.4 μJ	Energy available in the DC bus
n	1	Number of pulses per half-grid cycle
P	71.3 mW	Power before losses
$E_{\text{loss,sw}}$	317 μJ	MOSFET losses
$E_{\text{loss,Dsec}}$	178.3 μJ	Secondary diode losses
P_o	21.7 mW	Actual power harvested

were then used for theoretical power transfer calculations based on the concepts presented in Section III. The results are shown in Table III, and predict a continuous output power of 21.7 mW. This represents a power transfer efficiency of 31%, with about 44% losses in the main MOSFET switch and 25% losses in the secondary diode.

Experimental waveforms for this condition are shown for two different time scales in Fig. 11 (left) and (center), for one energy transfer pulse. As can be seen in Fig. 11 (left), when the dc-bus voltage rises to 1.14 kV, the DIAC string triggers, and the dc-bus discharges in about $3 \mu\text{s}$ as predicted by the theoretical analysis. The secondary current i_{sec} can be seen for the flyback period in Fig. 11 (center), with its waveform showing the anticipated triangular discharge shape over a period of about $60 \mu\text{s}$, again in accordance with the theoretical analysis. Note that the high-frequency ring during the initial DIAC breakover period is primarily an artifact of common-mode voltage probe coupling, and illustrates the difficulty of making measurements for this type of application because the measurement probe loading effects are quite significant since measurement probes have nominal input impedances in the range of mega ohms (parasitic capacitances in the levels of

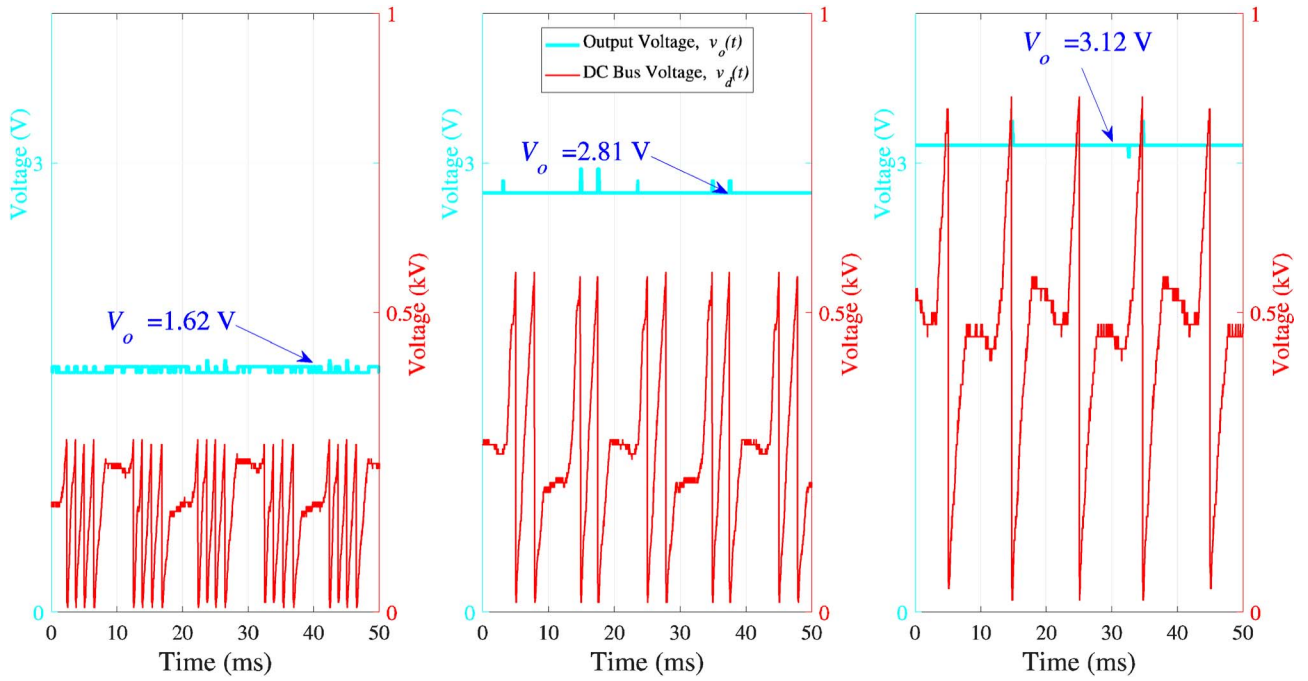


Fig. 12. Experimental results for triggering voltages of 288 V (left), 568 V (center), and 860 V (right).

picofarads), which are comparable with the capacitances of the EFEH divider. Hence, their presence influences the measured waveforms at various points of the circuit, and often also disturbs the system operation.

Fig. 11 (right) shows that the system achieves one energy transfer pulse for every 10 ms (half-grid cycle), and delivers an average output voltage of 4.4 V across the 820- Ω output load resistor. This represents a harvested output power of $P_o = V_o^2/R_o = 23.6$ mW, which matches very well with the theoretical expectations as presented in Table III. Note that in general and as predicted by (5), larger triggering voltages V_{bo} manage to harvest more power. However, they also produce larger losses, so that the best overall efficiency of the system that can be achieved remains at about 33%.

Additional results for triggering voltages of 288, 568, and 860 V are presented in Fig. 12, with the theoretical expectations for the harvested power using the theory of Section III are: 4 mW with $n = 4$, 10.3 mW with $n = 2$, and 12.2 mW with $n = 1$, respectively. The experimental power levels achieved for each triggering voltage are 3.2, 9.7, and 11.9 mW, respectively, as can be inferred from the output voltages on the 820- Ω load resistance presented in Fig. 12. These results match the experimental results quite closely, and hence validate further the theoretical analysis of the harvesting process.

VI. CONCLUSION

This paper presents a power electronic conversion strategy for electric-field energy harvesting from an MV feeder that does not require galvanic contact with the power line. The strategy uses the principle of flyback conversion in pulsed energy transfer mode. The converter is self-triggered so it does not require an additional power supply. The approach is able to

harvest 23.6 mW from a 12.7-kV power line. Detailed circuit analysis and experimental results are presented to confirm the theoretical analysis and physical viability of the concept.

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