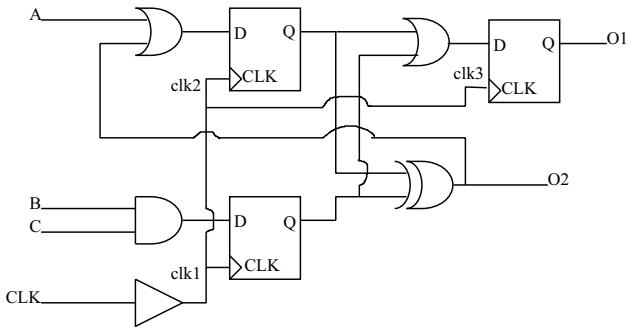
ECE428 Homework 3

1. The timing parameters of the components used in the following circuit are given as follows. Answer questions based on these data. **In your answer, you have to write down the equations that you use. You CANNOT just write a number as your solution.**

Propagation delay of buffer	$t_{buf} = 0.2ns$
Propagation delay of OR gate	$t_{OR} = 0.4ns$
Propagation delay of AND gate	$t_{AND} = 0.4ns$
Propagation delay of XOR gate	$t_{XOR} = 0.6ns$
DFF setup time	$t_{setup} = 0.5ns$
DFF hold time	$t_{hold} = 0.8ns$
DFF clock to Q delay	$t_{CLK \to Q} = 0.5ns$



1.1) Calculate the maximum clock frequency. (15)

1.2) Calculate the maximum external setup time. (15)

1.3) Calculate the maximum external hold time. (15)

1.4) Calculate the maximum clock to output delay. (15)

1.5) If the clock frequency is 500MHz and the propagation delay of the OR gate changes to 0.6ns, what type of timing violation will occur in the circuit? Why? (10)

1.6) If the propagation delay of the OR gate changes to 0.2ns, what type of timing violation will occur in the circuit? Why? (10)

1.7) Assume there exist clock skew due to interconnect delay. Clk1 is 0.1ns earlier than clk2. Clk2 is 0.1ns earlier than clk3. Considering clock skew, what type of timing violation will occur in the circuit? Why? (10)

1.8) How to fix the timing violation problem discussed in the previous question? After the problem is fixed, what's the maximum clock frequency of the new circuit? (**Hint: you need add an extra gate into the circuit.**) (10)