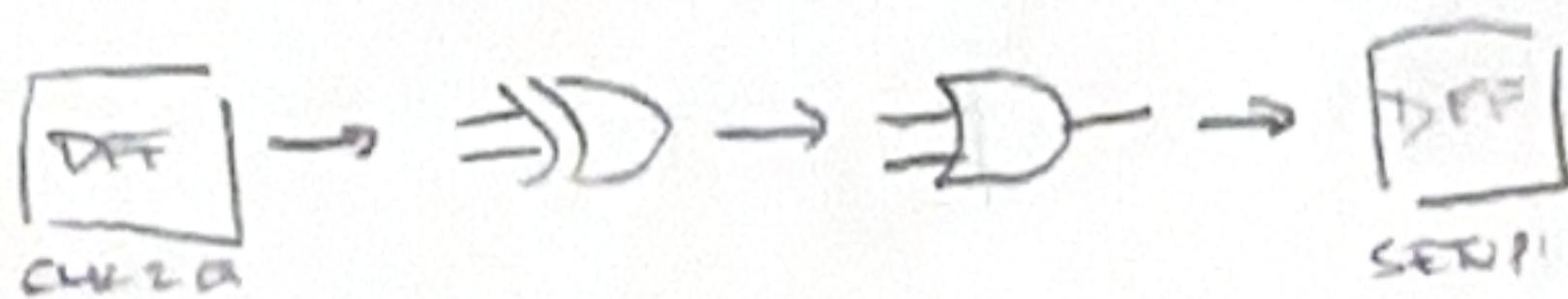


(1.1) MAX CLOCK FREQ.

WE NEED THE MAX REG-TO-REG DELAY.



$$\Rightarrow t_{max,reg} = t_{clk \rightarrow A} + t_{x02} + t_{o2} + t_{setup} \quad (1)$$

$$= (0.5 + 0.6 + 0.4 + 0.5) \text{ ns}$$

$$= 2 \text{ ns}$$

$$\text{So the CLK period } T_{clk} \geq 2 \text{ ns. } \Rightarrow f_{max} = \frac{1}{2 \text{ ns}} = \boxed{500 \text{ MHz}}$$

(1.2) MAXIMUM EXTERNAL SETUP TIME

NEED TO FIND THE LONGEST INPUT DATA PATH, MINUS CLOCK DELAY WHICH ADDS TIME BUFFER.

ALL  $A, B, C$  HAVE THE SAME PROPAGATION DELAY AND CLK DELAY.

$$\Rightarrow t_{ext,setup}^{(max)} = (t_{setup} + (t_{prop} - t_{buf})_{max}) - t_{clk} + t_{x02} + t_{o2} - t_{buf}$$

$$= (0.5 + 0.6 + 0.4 - 0.2) \text{ ns}$$

$$\boxed{t_{ext,setup}^{(max)} = 1.3 \text{ ns}}$$

$$t_{ext,setup} = t_{clk} + (t_{prop} - t_{buf})_{max}$$

(1.3) MAX EXTERNAL HOLD TIME

$$t_{H,ext} = t_H + (t_{clk} - t_{data})_{min} \text{ for same DFF}$$

$t_{clk}$  IS SAME FOR ALL  $\Rightarrow t_{buf} \rightarrow t_{clk} = t_{buf} = 0.2 \text{ ns}$

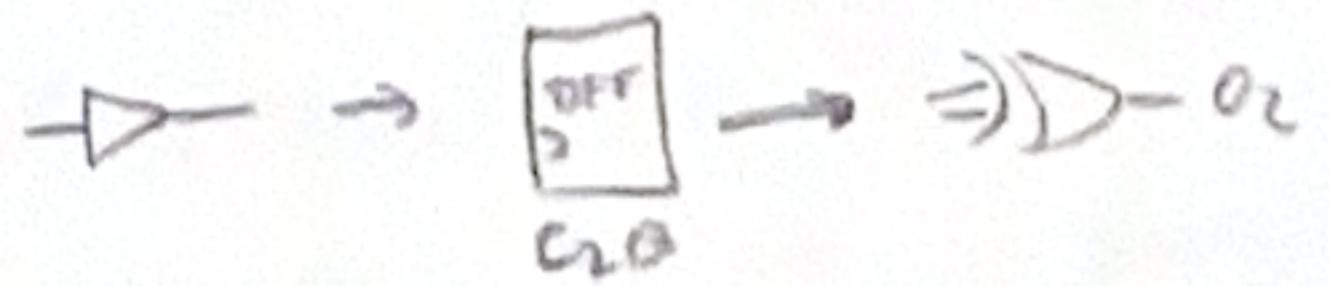
MIN  $t_{data}$  FOR ALL DFFs IS  $0.4 \text{ ns}$  FOR  $t_{o2}$  OR  $t_{x02} \Rightarrow t_{data} = 0.4 \text{ ns}$ .

$$\Rightarrow t_{ext,hold}^{(max)} = 0.8 \text{ ns} + (0.2 \text{ ns} - 0.4 \text{ ns})$$

$$= 0.8 \text{ ns} - 0.2 \text{ ns}$$

$$\boxed{t_{ext,hold}^{(max)} = 0.6 \text{ ns}}$$

(1.4) MAX CLK TO OUT DELAY



$$\Rightarrow t_{\text{CLK-OUT}}^{\text{(max)}} = (t_{\text{CK}} + t_{\text{C-Q}} + t_{\text{prop}})_{\text{max}} + t_{\text{BUF}} + t_{\text{C-Q}} + t_{\text{DQ}}$$
$$= 0.2 \text{ ns} + 0.5 \text{ ns} + 0.6 \text{ ns}$$
$$= 1.3 \text{ ns}$$

(1.5)  $f_{\text{CLK}} = 500 \text{ MHz}$ ,  $t_{\text{DQ}} = 0.6 \text{ ns}$ . WHAT TIMING VIOLATION OCCURS? WHY?

$$\Rightarrow f_{\text{CLK}}^{\text{max}} = \frac{1}{(0.5 + 0.6 + 0.6 + 0.5) \text{ ns}} \approx 455 \text{ MHz...}$$

SINCE THE CLOCK WILL BE RUNNING TOO FAST, THE CLK EDGE WILL ARRIVE TOO SOON AND THE DATA ~~WILL NOT BE READY~~ WE WILL EXPERIENCE SETUP TIME VIOLATIONS.

↑ text, set

(1.6)  $t_{\text{DQ}} = 0.2 \text{ ns}$ . WHAT TIMING VIOLATION WILL OCCUR? WHY?

$$f_{\text{CLK}}^{\text{max}} = \frac{1}{(0.5 + 0.6 + 0.2 + 0.5) \text{ ns}} = \frac{1}{1.8 \text{ ns}} = 555.5 \text{ MHz}$$

THE 500MHz CLOCK WILL BE SLOW AND CAUSE HOLD-TIME VIOLATIONS  
IF DATA IS PTD FOR THE SAME TIME AND THE SHOULD BE 555MHz  
CLK WILL RUN LATE EACH CYCLE.

(1.7) ASSUME  $\exists$  CLOCK SKEW DUE TO INTERCONNECT DELAY. CLK1 IS 0.1ns EARLIER THAN CLK2. CLK2 IS 0.1ns EARLIER THAN CLK3. WITH THIS CLOCK SKEW, WHAT TYPE OF TIMING VIOLATION WILL OCCUR? WHY?

\* FOR SETUP VIOLATIONS:  $t_{\text{CK-Q}} + t_{\text{pd, long}} + t_{\text{setup}} \leq T_{\text{clk}} + t_{\text{skew}}$  ] equations

\* I'M ASSUMING  
 $T_{\text{clk}} = 2 \text{ ns}$ , i.e.,  
 $f_{\text{max}} = 500 \text{ MHz}$

FOR HOLD VIOLATIONS:  $t_{\text{CK-Q}} + t_{\text{pd, short}} \geq t_{\text{hold}} + t_{\text{skew}}$

↓ CLK2 SKEW

0.5ns + (0.6ns + 0.4ns) + 0.5ns ≤ 2ns + 0.2ns

⇒ 2ns ≤ 2.2ns ∴ NO SETUP VIOLATIONS

████████ CLK3 SKEW...

0.5ns + (0.4ns) ≥ 0.8ns + (0.1ns + 0.1ns + 0.1ns)

⇒ 0.9ns ≥ 1.1ns ∴ HOLD-TIME VIOLATION

SINCE THE RISING EDGE OF CLK3 WILL ARRIVE TOO LATE!

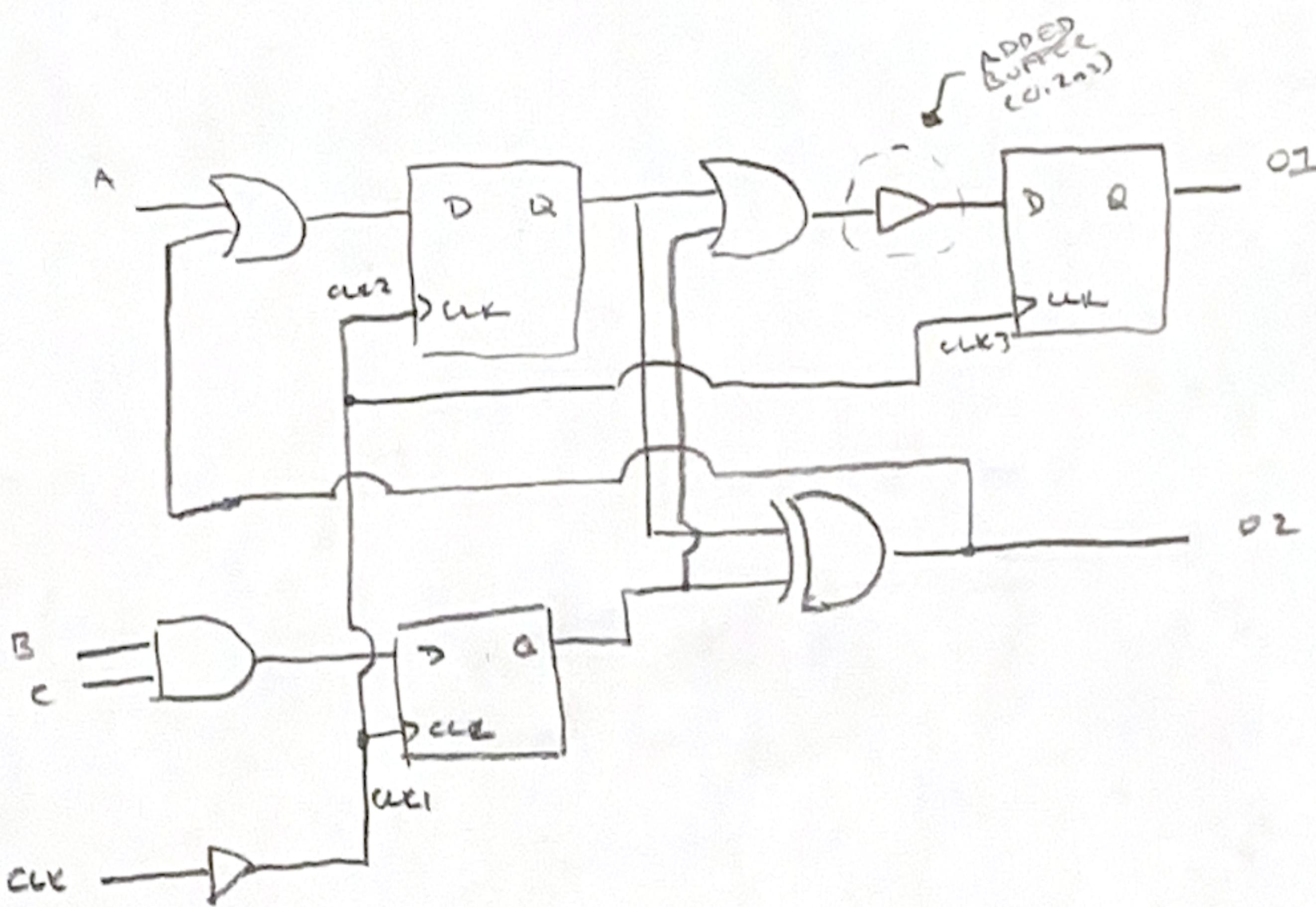
1.8 HOW DO YOU FIX THE VIOLATION IN 1.7? AFTER THE FIX, WHAT IS THE MAX FREQUENCY OF THE CLOCK?

THERE NEEDS TO BE A BUFFER ADDED BETWEEN THE OR GATE AND DFF DRIVING O1. s.t.:

$$0.5\text{ns} + (0.4\text{ns} + 0.2\text{ns}) \geq 0.8\text{ns} + (0.3\text{ns})$$

$\Rightarrow 1.1\text{ns} \geq 1.1\text{ns}$  is NO HOLD-VIOLATION.

MODIFIED CIRCUIT



NEW fmax

THE MAX REG-TO-REG PROPAGATION DELAY HAS INCREASED WITH THE ADDITION OF THE BUFFER.

$$\Rightarrow t_{max, r2} = t_{clock, a} + \overbrace{(t_{xor} + t_{or} + t_{buf})}^{t_{pd}} + t_{setup}$$

$$= 0.5\text{ns} + 0.6\text{ns} + 0.4\text{ns} + 0.2\text{ns} + 0.5\text{ns}$$

$$= 2.2\text{ns}$$

$$\Rightarrow f_{max} = \frac{1}{2.2\text{ns}} = 454.5 \text{MHz}$$