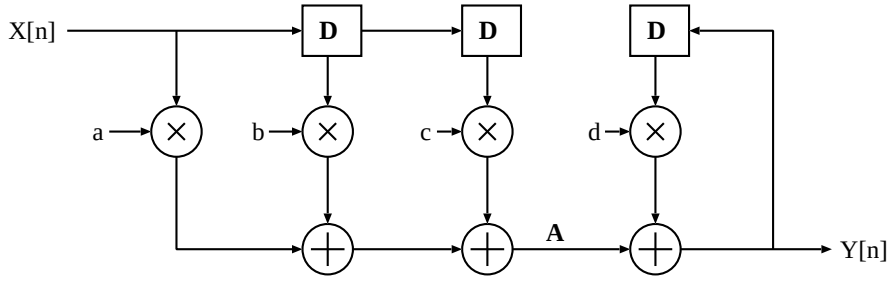
ECE428 Homework 6

1. Draw the block diagram to show how to implement filter function y[n]=$a_0 \cdot x[n] + a_1 \cdot x[n-1] + a_5 \cdot x[n-5]$. You implementation should be able to work with a clock frequency of $\frac{1}{t_{mult}}$, where t_{mult} is the multiplier delay. Assume the multiplier delay is much larger than adder delay and your circuit can have latency of multiple clock cycles. (40)

2. The following diagram shows a filter implementation. a, b, c, d are filter coefficients. The filter input $X[n]$ and filter coefficients are all 8-bit fixed-point two's complementary numbers. The delay of the multiplier and adder circuits are 25ns and 5ns, respectively. Answer the following questions based on this filter block diagram.



   2.1) Write down its output function. (10)

   2.2) Ignore the clock to Q delay and setup time associated with DFFs. Please identify the critical path in this filter implementation and calculate the delay on the critical path. Calculate the maximum clock frequency of this implementation. (10)

   2.3) Assume there is no truncation performed in computing signal A (refer to the diagram in the previous page). What's the width (in terms of numbers of bits) of the signal A. (10)

   2.4) Assume a look-up table (LUT) is used to implement the multiplier that performs $a \cdot X[n]$ in the given implementation. Determine the size of the look-up table that you should select. (10)

   2.5) If $a = 00111111$, give a more efficient implementation of the multiplier that computes $a \cdot X[n]$. You can use a 16-bit adder and an 8-bit XOR gate in your implementation. Draw the block diagram to show your implementation. (10)

   2.6) If filter coefficients b and c have the same value, how do you modify the filter circuit to save one multiplier. Your implementation has to maintain the clock frequency of 30MHz. Draw the block diagram of your implementation. (10)