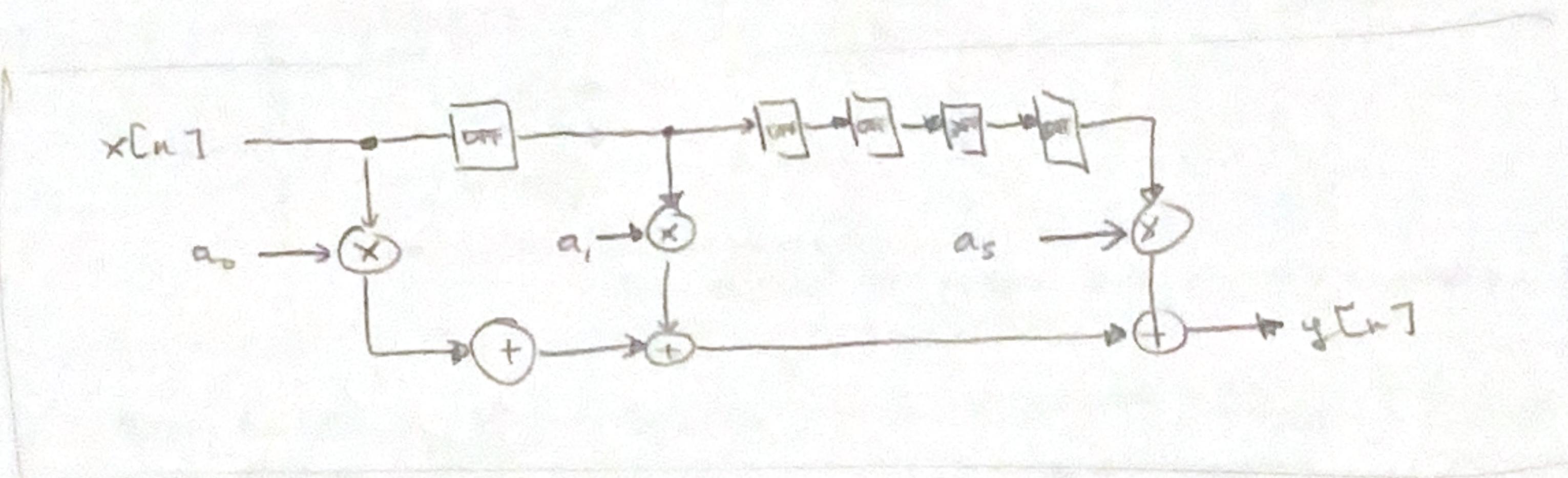


- ① DRAW THE BLOCK DIAGRAM FOR THE FILTER:

$$y[n] = a_0 x[n] + a_1 x[n-1] + a_2 x[n-2]$$

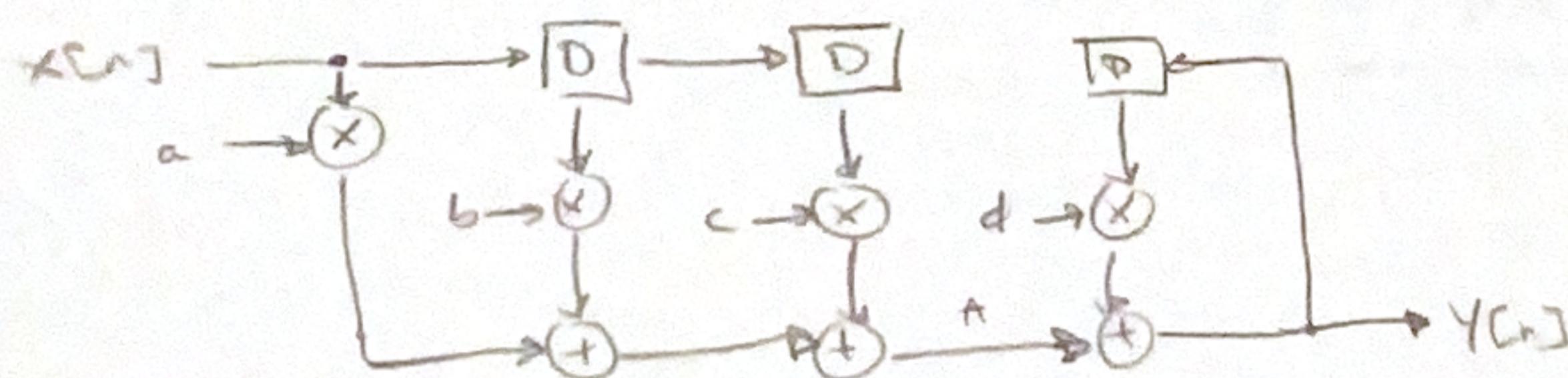
THE IMPLEMENTATION SHOULD OPERATE @  $f = 1/t_{\text{mult}}$  ( $t_{\text{mult}}$  IS MULTIPLIER DUTY).

\*~~ASSUME  $x[n]$  mult >> adder~~



IF  $t_{\text{mult}} \gg t_{\text{adder}} \rightsquigarrow \text{full} > \frac{1}{t_{\text{mult}}}$

- ② IIR FILTER:  $a, b, c, d \in \mathbb{R}$ .  $x[n]$  AND FILTER COEFFICIENTS ARE 8-BIT FIXED POINT 2's COMPLEMENTARY NUMBERS. THE DELAY OF THE MULTIPLIER AND ADDER CIRCUITS ARE 25ns AND 5ns, RESPECTIVELY.



- ②.1 ACTUAL FUNCTION

$$A = aX[n] + bX[n-1] + cX[n-2]$$

$$Y[n] = A + dY[n-1]$$

$$Y[n] = aX[n] + bX[n-1] + cX[n-2] + dY[n-1]$$

(2.2) IGNORING DELAY & SETUP OF THE DFFs. IDENTIFY THE CRITICAL PATH, THE DELAY OF THE PATH. CALCULATE  $f_{clk}$ .

OUT OF THE FIRST DFF  $\rightarrow$   $(\otimes) \rightarrow (+) \rightarrow (\oplus) \xrightarrow{A} (+) \rightarrow \text{out}$

$$\Rightarrow t_{delay} = t_{mult} + 3t_{add}$$

$$= 25\text{ns} + 3(5\text{ns})$$

$$= 25\text{ns} + 15\text{ns}$$

$$\boxed{\text{Delay} = 40\text{ns}}$$

$$\boxed{f_{clk} = \frac{1}{40\text{ns}} = 25\text{MHz}}$$

(2.3) ASSUMING NO TRUNCATION, WHAT IS THE WIDTH OF SIGNAL A?

$$\Rightarrow A = a \times x[n] + b \times x[n-1] + c \times x[n-2]$$

$\underbrace{a}_{8\text{bit} \times 8\text{bit}} \quad \underbrace{b}_{8\text{bit} \times 8\text{bit}} \quad \underbrace{c}_{1 \times 1}$   $\rightarrow 16\text{bit} + 16\text{bit} + 16\text{bit} \xrightarrow{\text{if overflow}} 17\text{-bit}$

AT WORST A IS 17-bits wide

(2.4) A LUT IS USED FOR  $a \times x[n]$ , DETERMINE LUT SIZE.

$$\Rightarrow 2^8 \times 2^8 = 2^{16} = \boxed{65,536}$$

$\underbrace{\quad}_{8\text{bit times}} \quad \underbrace{\quad}_{8\text{bit}}$

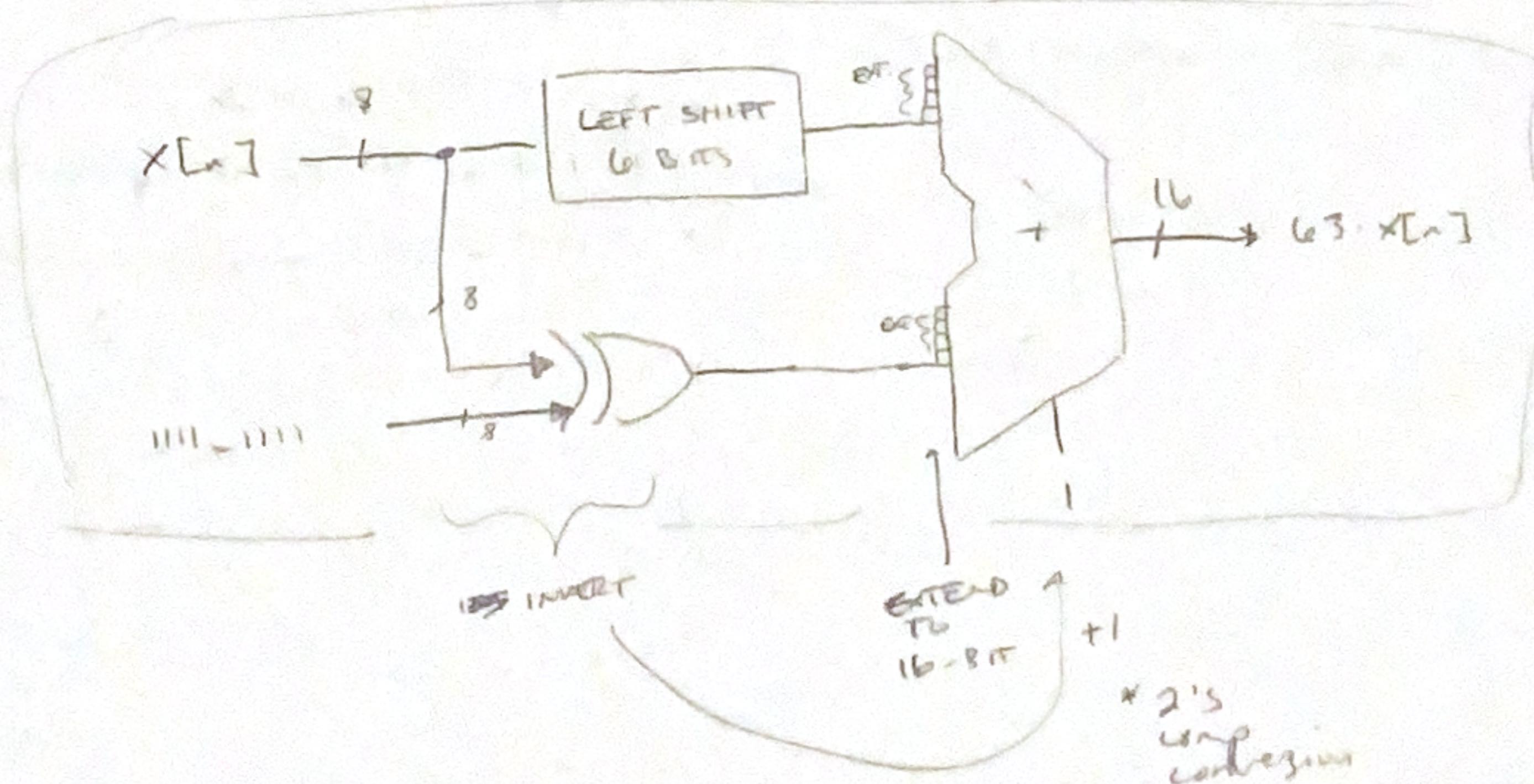
(2.5) IF  $a = 0011-1111$ , GIVE A MORE EFFICIENT MULTIPLIER IMPLEMENTATION. USE A 16-BIT ADDER AND 8-BIT XOR GATE. DRAW THE BLOCK DIAGRAM.

$$(0011-1111)_2 = (63)_10$$

$$\begin{aligned} \Rightarrow & 63 \cdot x[n] \\ = & (64-1)x[n] \\ = & 64x[n] - x[n] \\ = & 2^6 \cdot x[n] - x[n] \end{aligned}$$

SO LEFT SHIFT 6 BITS

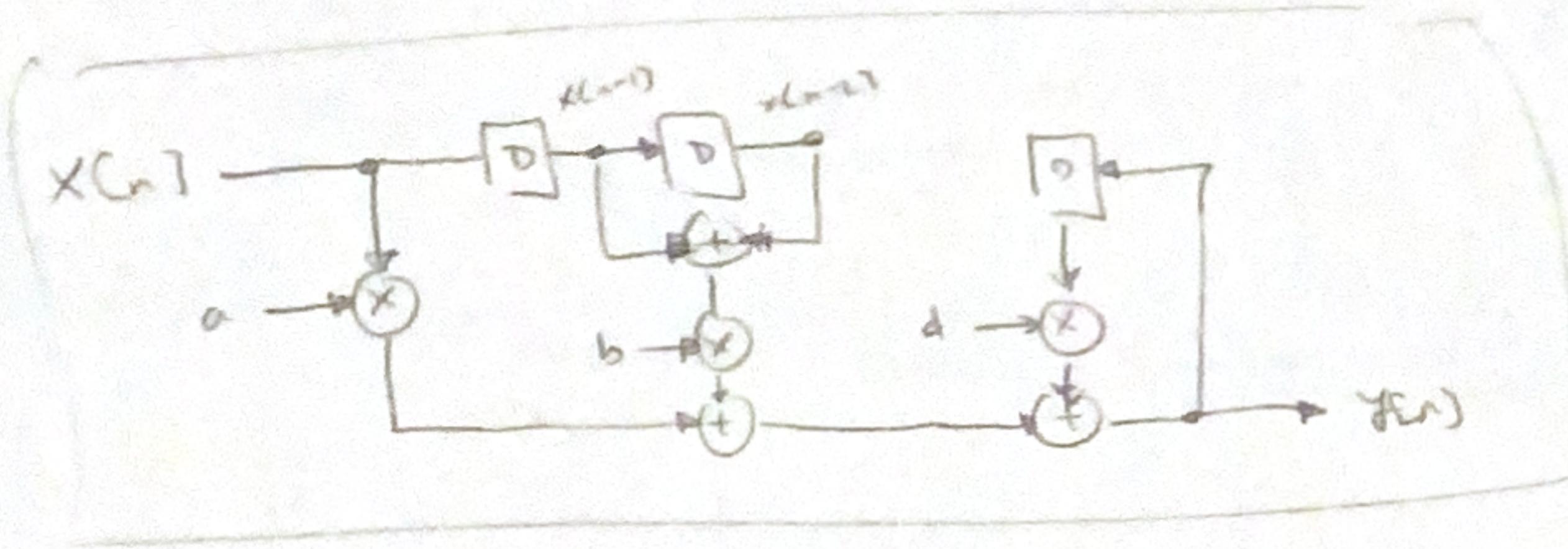
THEN SUBTRACT.



(2.6) If  $b=c$ , modify circuit to save a multiplier. full rate or 30 MHz?  
?

$$\begin{aligned} \rightarrow A &= a \times [n] + b \times [n-1] + c \times [n-2] \\ &= a \times [n] + b \times [n-1] + b \times [n-2] \\ &= a \times [n] + b(x[n-1] + x[n-2]) \end{aligned}$$

add these  
first



This maintains  $f_{full} = 25 \text{ MHz}$  which is consistent w/ 2.2.