ECE428 Lab 1 Instruction

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This lab assignment consists of three mandatory tasks and optional tasks and presentation for bonus points. These tasks are described below:

Task 1: Read the Tutorial_basys_vivado file, implement the counter circuit and write a testbench for simulation. Perform simulation at behavioral, post-synthesis functional, and post-implementation functional simulations and observe the differences of the simulated waveforms. You can download the Verilog code and design constraint file from D2L, but will have to write your own testbench code. This is to get familiar with the Vivado design flow. **In simulation, you can directly observe the count register value instead of SSG_D (7 segment LED driving signal) since it directly shows the current counter value. Alternatively, you can include a functional block that converts the SSG_D output from the circuit under test (CUT) to some values that easy to read (kind of opposite operation of the last always block in lab.v file).**

For this task, please include the obtained waveforms in different simulations and explain the differences among these waveforms and why. Successfully completing this task will earn 40 points.

Task 2: Design and simulate a circuit that can recognize a secret code. The function of the circuit is described below: (60)

- **a.** The secret code is entered by pushing the buttons shown below. Before entering your code, you need push the center button to reset the circuit. After resetting, one LED displays 0 to signal the circuit is ready for taking inputs.
- **b.** The secret code consists of the following sequence: 1) pushing the top button; 2) pushing the left button; 3) pushing the left button again; 4) pushing the right button.
- **c.** After the correct secret code is entered, the LED displays 9 to indicate the authentication is complete. If incorrect codes are entered, the LED should display E.
- **d.** Write testbench to validate your design via simulation. Like Task 1, you may use a convenient method to monitor the values to be displayed on the 7 segment LED.

Figure 1: Button and LEDs on the Basys 3 board

For this task, please include your FSM state diagram, you Verilog code and waveforms obtained from post-implementation functional simulation. The included waveforms should separately show two scenarios: 1) password is correctly typed and 2) wrong password is typed. In the waveform, mark when the circuit output indicates correct or incorrect password has been typed. Successfully completing this task will earn 60 points.

Task 3: Your circuit can include a timer function. After pushing the reset button (the center button), the user has 10 seconds to enter the code. If 10 seconds are passed without the correct code entered, the circuit will no longer take any input and the LED displays E. (40)

Since it is impractical to simulate the circuit operation for 10 seconds, you can change the 10 second time period to 30 clock cycles when you perform simulation.

Bonus for extra tasks and presentation (up to 50):

You can work on one or multiple of the following tasks. Successfully completing one of these bonus tasks **and presenting your design with a demo in class** will earn 20 points until reaching 50 points. For each completed task, your lab report should include its state transition diagram, Verilog code and adequate simulated waveforms (from post-implementation functional simulation) to demonstrate the required functionality.

1. You circuit can give users three chances to try. If the user cannot enter the correct code after three tries, the circuit will no longer take any input and the LED displays E.
2. You can use the switches at the bottom of board to change the secret code.
3. A switch or a push button often exhibits bouncing behavior when it is being switched or pushed. An illustration of the bouncing behavior is shown in Figure 2. Such bouncing behavior will cause your circuit malfunction from occasionally. Please add de-bounce circuits to address this problem. Also, the push down button signals are asynchronous inputs and may cause meta-stability problems. Please add synchronizer to your design.

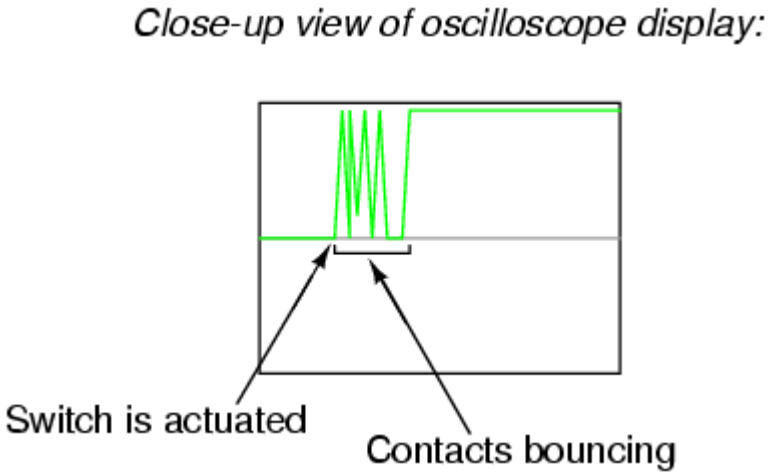

Figure 2: Switch bouncing behavior

4. You can add any addition function that make the circuit more interesting (need explain your idea and get approval from the instructor before starting your design).

The presentation may include the followings:

1) Explanation of your design
2) Explanation of the differences between behavioral, post-synthesis, and post-implementation simulation
3) Show the synthesized schematic
4) Show where the circuit is implemented on FPGA device
5) Show programmable logic blocks (CLB) and programmable interconnect resources
6) **Live demo at the end of the class**