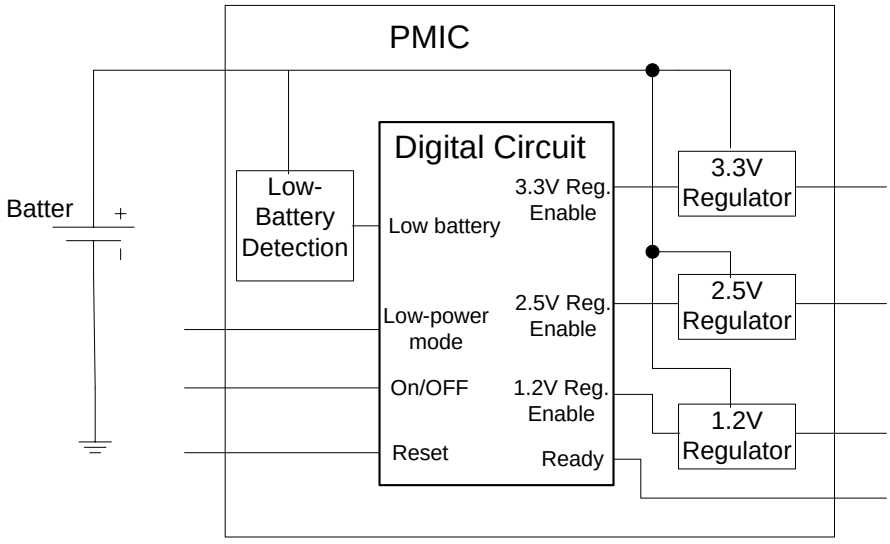
ECE428 Lab2 Instruction

Haibo Wang

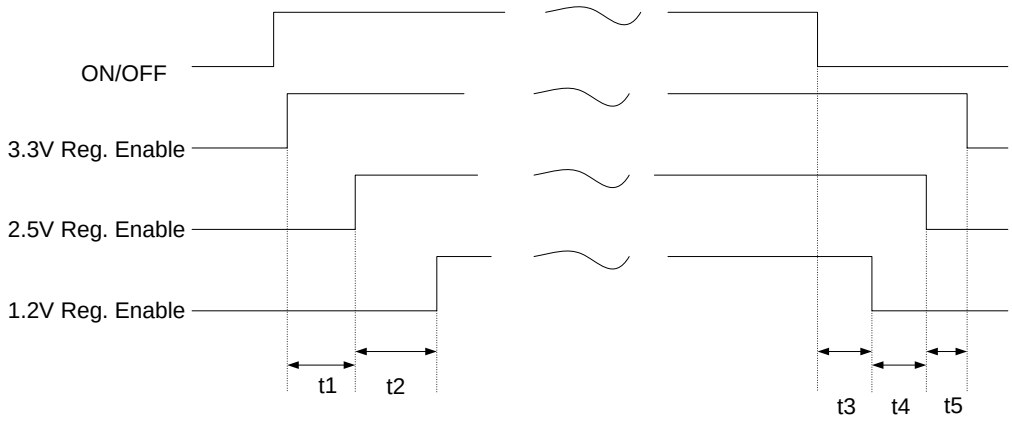
Power Management IC (PMIC) is one of the fast growing semiconductor sectors. You are a team member of a PMIC design group and your responsibility is to design the digital circuit of the following PMIC chip. The PMIC take power from a battery and generates three voltage outputs: 3.3V (for I/O circuits), 2.5V (for analog circuits), and 1.2V (for logic circuits). The digital circuit has four input signals and their functions are listed as follows:

1. Reset: it is used to reset the digital circuit after connecting the battery.
2. Low-battery detection: it turns logic 1 when the low battery detection circuit detects that battery is low. Then, the logic 1 value of the signal will trigger the PMIC circuit to shut off the output voltage according to the power-off sequence.
3. Low power mode: When the low power mode input is 1, it triggers the PMIC circuit to shut off the 3.3V and 2.5V outputs according to the timing described in the power-off sequence (except 1.2V output is not turned off).
4. ON/OFF: When the input is 1, PMIC turns on the three output voltage according to the power-up sequences. When the input keeps 0 for t_3 time period, PMIC turns off the output voltage according to the power-off sequences.



The digital circuit has four out puts and three of them are for enabling the voltage regulators. The fourth output Ready becomes 1 when the power up sequence is complete and it becomes 0 as soon as the power-off sequence starts.

The power-up and power-off sequences are illustrated in the figure below. The values of the timing parameters in the figure are: t_1=1s, t_2=1.5s, t_3=1s, t_4=0.5s, and t_5=0.5s. Note: when switching to low-power mode, immediately after low-power mode input becomes 1, the 2.5V output can be turned off and the 3.3V output is off after a delay of t_5.



Lab Tasks:

1. Discuss possible input combinations that are not covered by the above function descriptions and decide how your design responds to such inputs.
2. Implement the design. You can use schematic, HDL code and state diagram to enter your design.
3. Perform simulation to verify your design. Note: in simulation use the following time parameters: t_1=5, t_2=6, t_3=5, t_4=3, and t_5=3 (all the numbers are in terms of clock cycles) to reduce simulation time.
4. Download your design into FPGA board. Use the original timing parameter values. Use the clock signal on the prototype board (refer to the board manual for pin number and clock frequencies). Use the slide switches as the digital circuit inputs: reset, On/OFF, Low-battery, and Low-power mode. Connect output signals 3.3V_reg._enable, 2.5V_reg._enable, 1.2V_reg._enable, and Ready to LEDs (see Figure 16 on page 15 of the board manual for pin assignments). Demonstrate the operation of your circuit.

Lab report:

1) One report is needed for a group. The lab report should be printed. The report should discuss your design and lab activities. Meanwhile, it should be concise. The following materials are needed in your report:
    a. Discussion related to Lab task 1.
    b. FSM state diagram of your design
    c. A snapshot of the simulation waveform