SliVER: Slicing-based GPU Virtualization for Edge Resources

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EE 491: B. Tech Project I

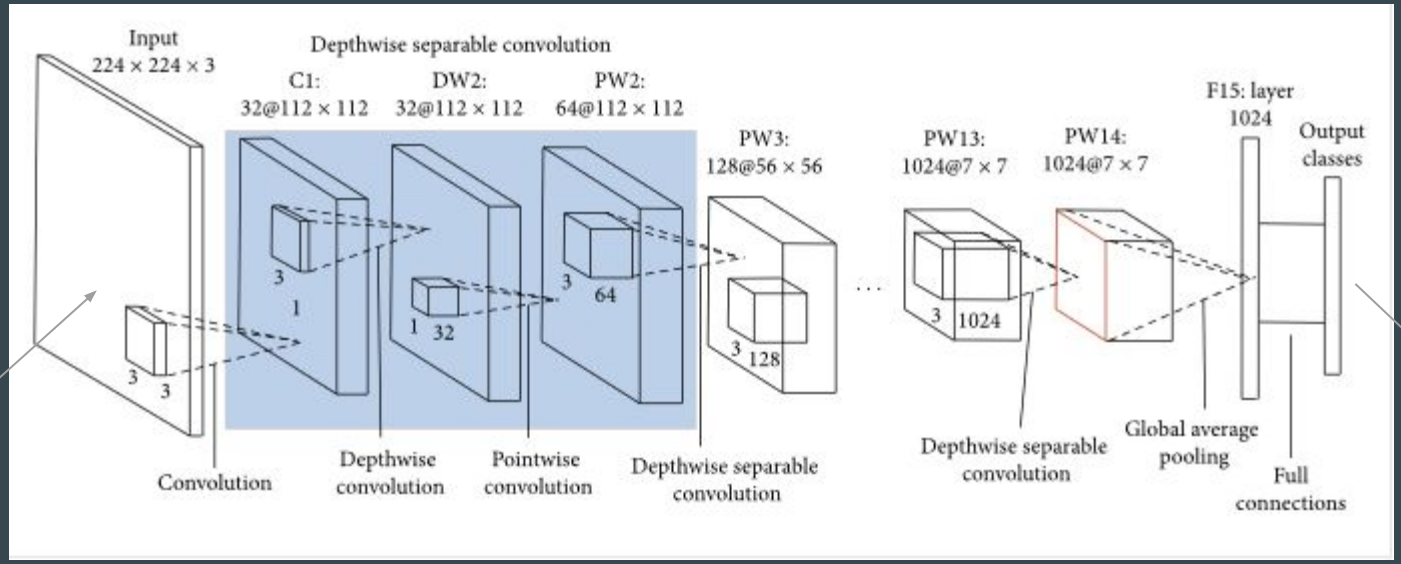
Aditya Sriram (200070004)

Why virtualize Edge GPUs?

- Rapid growth in Internet of Things (IoT)
- Keep compute unit close to sensors to minimize latency
- Edge GPUs can compete with server-grade ones
  - NVIDIA's AGX Orin can deliver similar performance to an RTX 3060 Ti workstation with ≤ 50W
- Applications
  - Image Processing
  - Surveillance
  - Extended Reality (XR)
  - Deep Learning (DL): inference and training
- Potential to run multiple applications on edge GPUs ⇒ need for efficient sharing
  - Contention for resources: registers, shared memory
  - Possible allocation schemes: proportional, priority, or deterministic; must be dynamic

MobileNet for Mobile Applications

Image



Label

Tensorflow's first mobile CV model

Image taken from https://wikidocs.net/165429

Requirements

- Focus on virtualization of resource-constrained, CUDA-enabled GPUs
- Enable efficient multiplexing of edge GPUs
- Spatial multiplexing
  - Requires driver-level modification
  - Made infeasible by lack of hardware support + proprietary IP
- Time multiplexing
  - Already present at level of CUDA contexts; inefficient
  - Existing solutions incompatible (discussed later)
- Process-level orchestration requires IPC, shared memory
- Attempt to solve the multithreaded problem rather than multiprocess one

Problem Statement

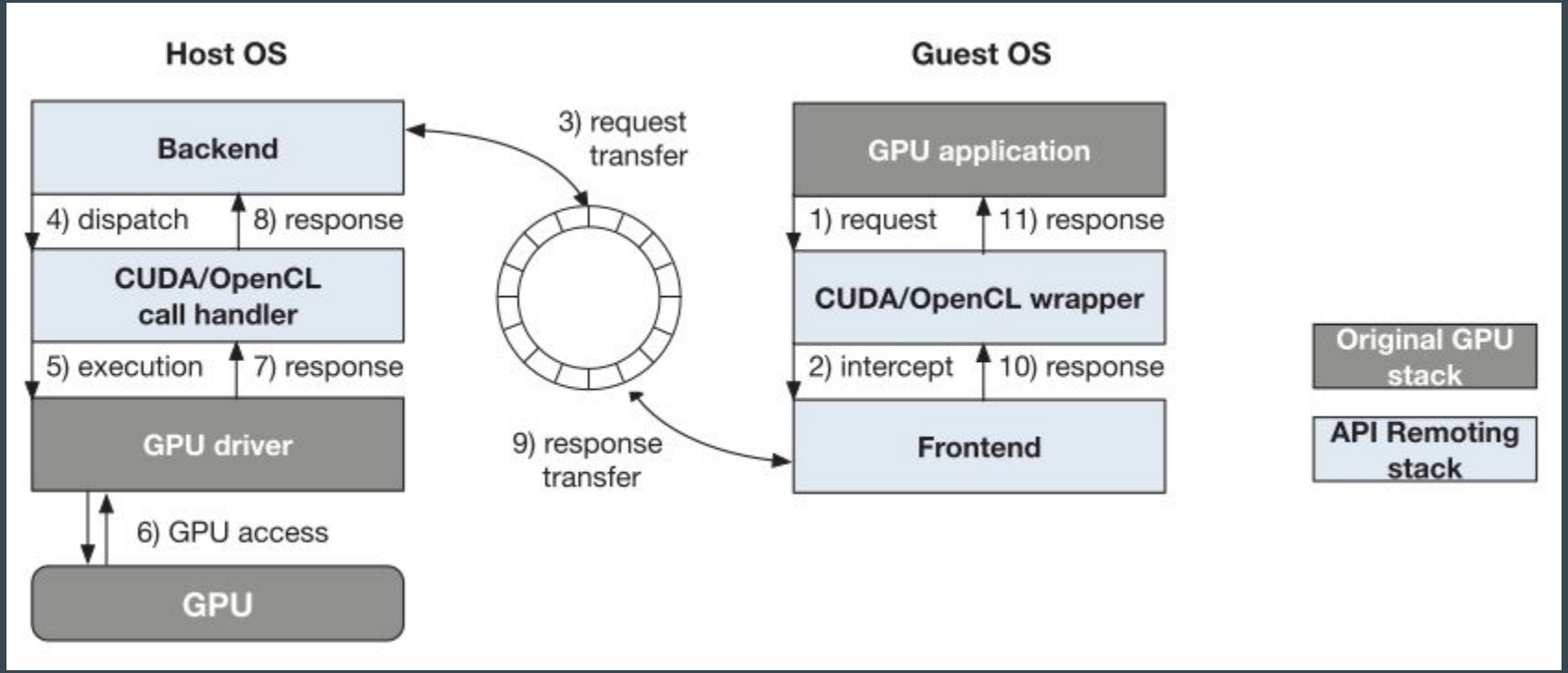
In the absence of hardware support, can we design a software-only virtualization solution for resource-constrained GPUs like the Jetson Nano to enable efficient time-sharing across multiple applications with CPU threads abstracting the applications?

Contributions

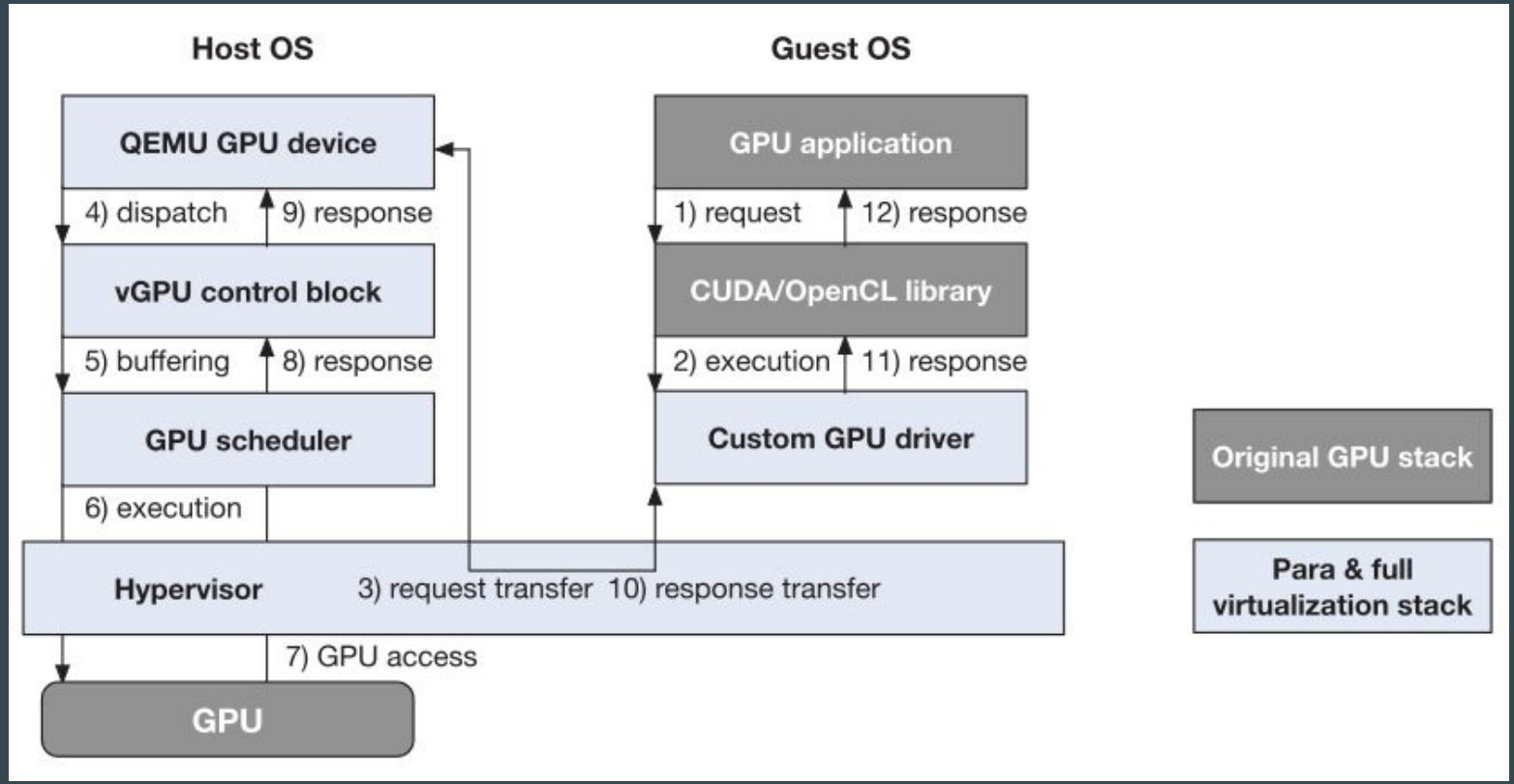
- Performance analysis of an existing software-based solution, *kernel slicing*
- Design of a middleware framework to demonstrate the potential of kernel slicing

GPU Virtualization

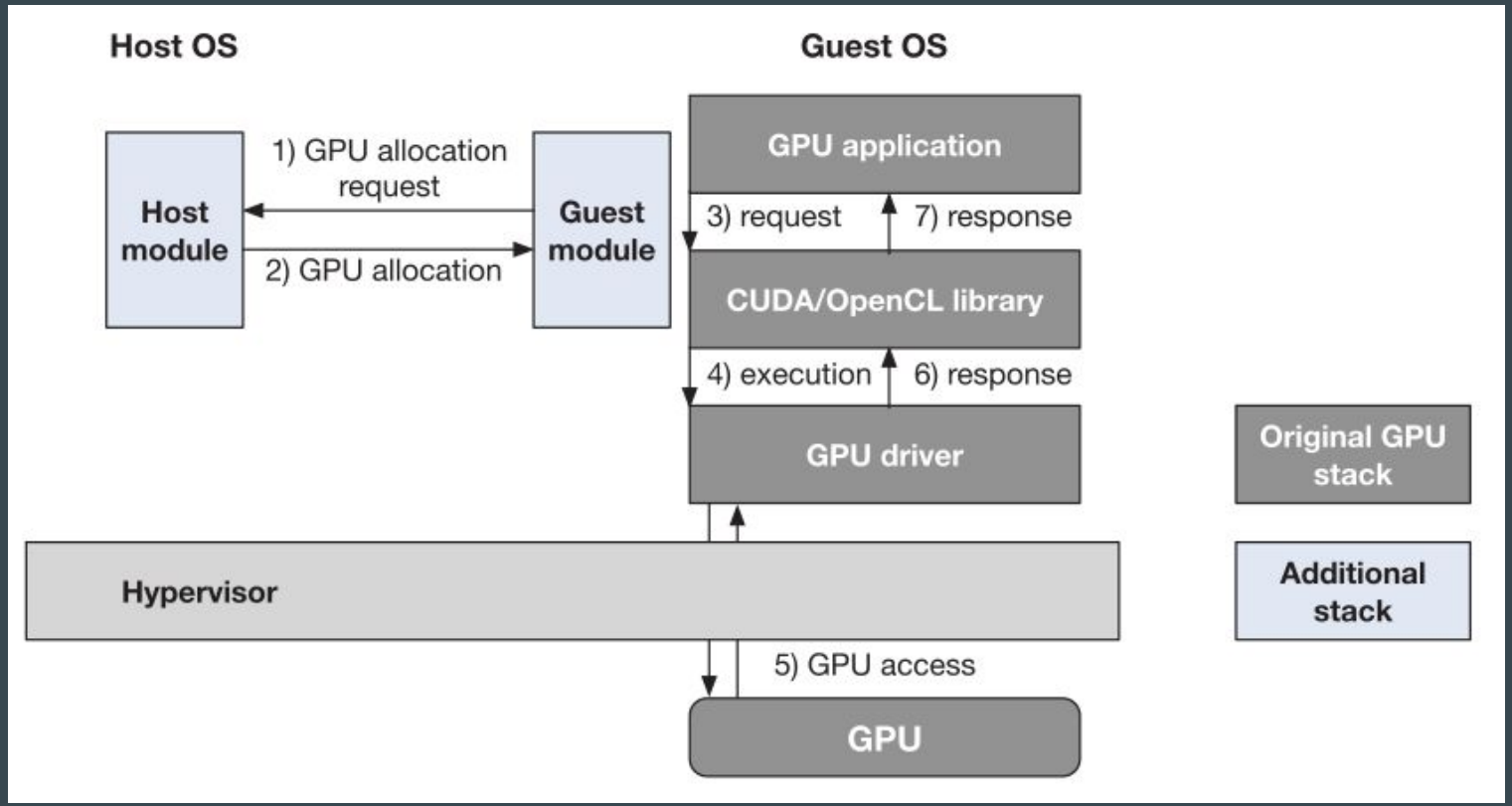
API Remoting



Full or Paravirtualization



Hardware-assisted Virtualization

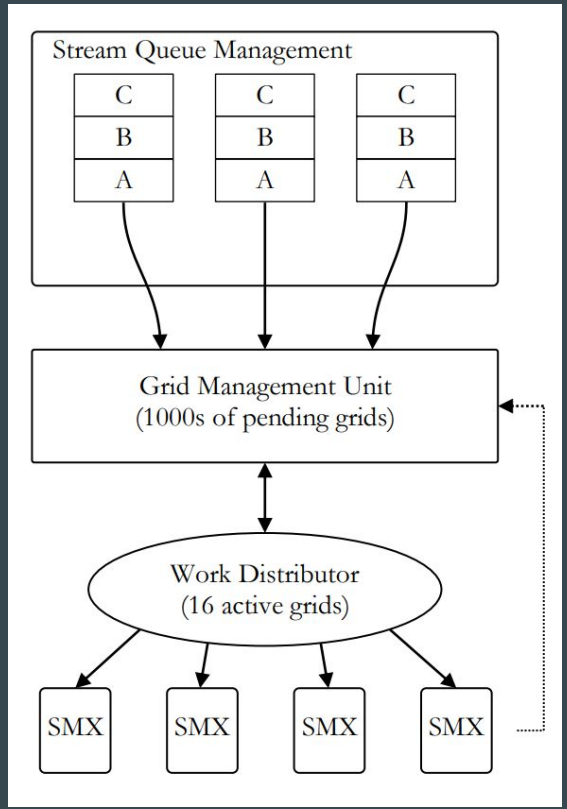


NVIDIA Virtualization Solutions

Hyper-Q

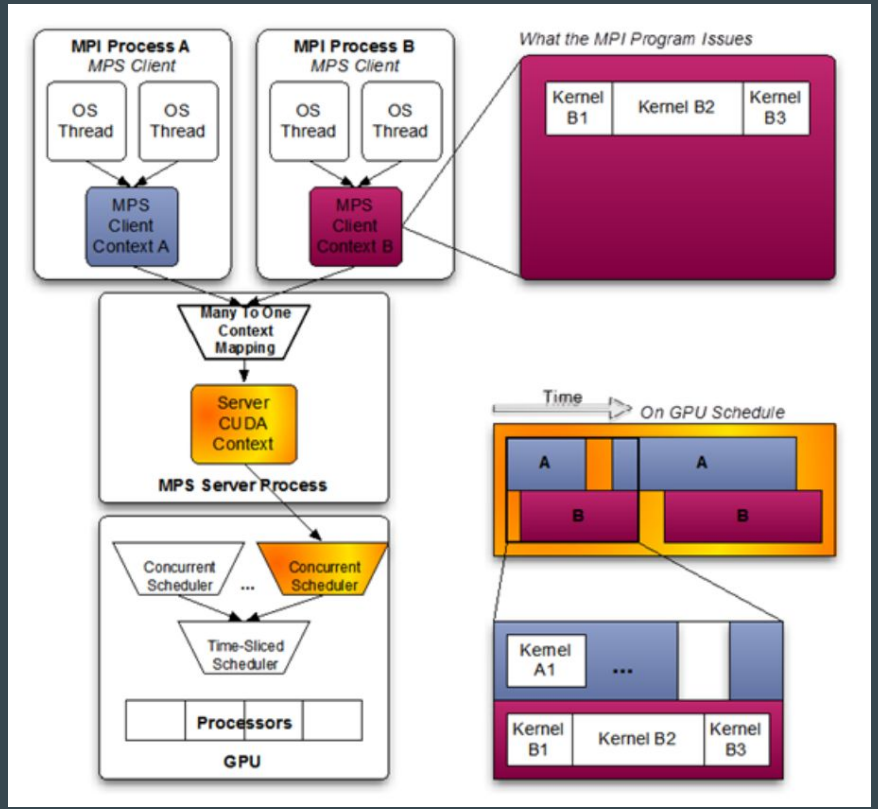
- Post-Kepler architectures
- Multiple work queues to eliminate and remove false dependencies in streams
- SM multiplexing (Jetson has single SM)

Expected time for serial execution	0.330s-0.640s
Expected time for fully concurrent execution	0.020s
Measured time	0.360s



Multi-Process Service (MPS)

- Alternative implementation of CUDA API
- Kernel scheduling across MPI processes
- Time-sliced
- Not supported on Tegra SoCs
- Current design similar to MPS

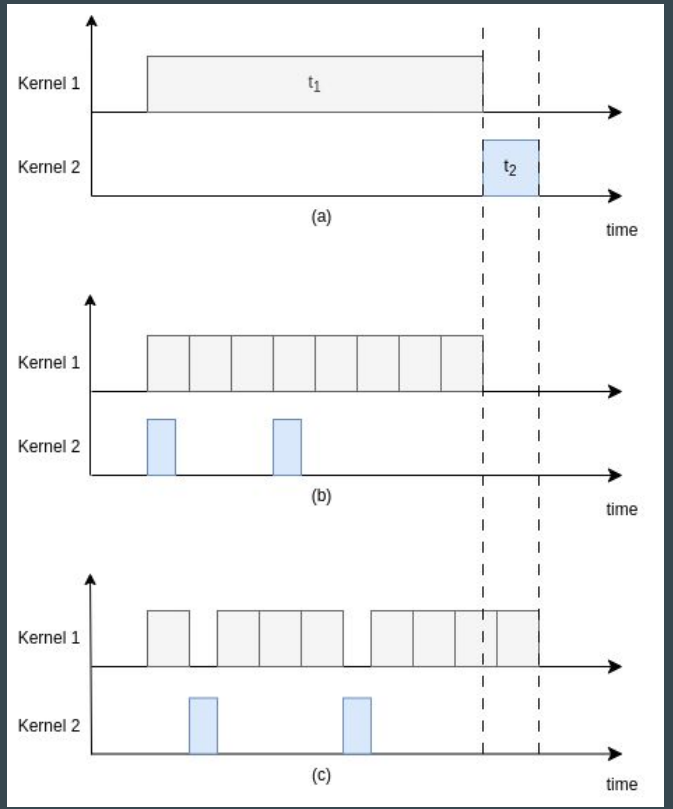


Our Contributions

Performance Analysis of Kernel Slicing

Kernel Slicing

- Requires developer assistance
- Break user kernel into “slices”
  - Slicing at granularity of thread blocks
- Enables efficient kernel preemption
- Exposes co-scheduling opportunities



Index Rectification

- Original block indices invalid
- Block Offset: additional argument to kernel
- Requires modification to original kernel

```
// kernel accepts an additional argument to index within set of slices
__global__ void matrixAdd(float *a, float *b, float *c, int width,
                          dim3 blockOffset)
{
    // correct indices using blockOffset
    int i = (blockIdx.x + blockOffset.x) * blockDim.x + threadIdx.x;
    int j = (blockIdx.y + blockOffset.y) * blockDim.y + threadIdx.y;
    if (i < width && j < width)
        c[i * width + j] = a[i * width + j] + b[i * width + j];
}

int main()
{
    ...
    dim3 sGridConf(4,1); // size of kernel slice
    dim3 blockOffset(0,0);
    while (blockOffset.x < gridConf.x && blockOffset.y < gridConf.y)
    {
        matrixAdd<<<sGridConf, blockConf>>>(a, b, c, width, blockOffset);
        blockOffset.x += sGridConf.x;
        while (blockoffset.x >= gridConf.x)
        {
            blockOffset.x -= gridConf.x;
            blockOffset.y += sGridConf.y;
        }
    }
```

Experiment

- Two kernels: SGEMM and MRI-Q from Parboil benchmark
- Measure total memory transfer+kernel execution time (in ms)
  - Exclude synchronous memory allocation times
  - Non-blocking CUDA events used
- Study variation in memory transfer+kernel execution time with slice size
- Round-robin scheduling used to decide kernel launch

Setup - I

- Both kernels launched on single thread
- CUDA streams used to exploit concurrency
- Avoid stalling CPU by using asynchronous operations
- Batched memory transfers
    - Do not overlap with kernel execution

Results

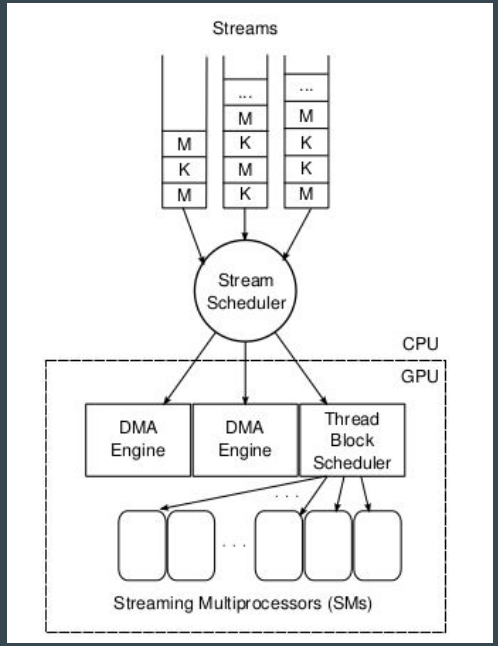
SGEMM \ MRI-Q	1024	512	256	128	64	32	16	8	4
(8,66)	294.0	293.8	294.1	293.7	293.3	294.6	297.8	294.8	294.1
(4,66)	294.5	294.8	294.0	293.8	293.3	294.7	297.5	294.7	293.9
(2,66)	297.5	293.6	294.1	293.7	293.2	294.3	297.9	294.6	294.4
(1,66)	298.9	297.9	293.2	292.8	292.4	293.7	296.8	294.2	293.6
(8,33)	295.4	294.8	293.8	294.0	293.2	294.7	297.6	295.3	294.4
(4,33)	297.1	293.7	293.9	292.9	293.1	294.7	297.6	294.5	294.1
(2,33)	296.9	297.3	293.1	292.9	292.7	293.6	296.7	294.3	292.9
(1,33)	298.4	298.0	296.8	291.4	290.8	291.9	295.3	292.8	292.2
(8,22)	297.2	293.7	293.4	293.4	292.8	294.7	297.6	294.6	294.1
(4,11)	298.0	297.3	296.1	292.2	291.7	292.8	295.6	293.2	292.8
(2,11)	298.0	298.3	296.3	294.5	289.8	290.6	293.4	291.5	291.0
(1,11)	299.0	298.1	297.3	295.6	292.3	286.6	289.7	289.9	287.7
(8,6)	297.9	296.7	296.1	292.1	291.8	293.0	296.0	294.2	293.1
(4,6)	297.6	296.9	295.9	294.4	289.8	290.8	294.2	292.2	291.7

Discussion

- Timings more sensitive to changes in MRI-Q slice size
- For fixed SGEMM slice size, timing decreases and then increases
  - Initial decrease due to opportunities for co-scheduling
  - Later increase due to overhead of launching more kernels
- Timing without kernel slicing: 294.0ms
- Timing with optimal slice size: 286.6ms

Setup - II

- Same as setup 1, BUT utilize concurrent kernel and copy execution mechanism



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(2,66)	293.6	293.7	293.3	289.8	289.7	290.6	295.5	293.6	294.6
(1,66)	294.9	294.9	293.5	292.0	288.7	289.6	294.5	293.1	293.1
(8,33)	293.8	293.8	290.2	289.9	289.4	290.9	296.1	293.9	295.0
(4,33)	294.1	293.2	293.5	289.8	289.3	290.3	295.5	293.9	294.7
(2,33)	295.1	294.1	293.7	292.2	288.7	289.8	294.0	293.4	292.5
(1,33)	295.9	295.4	294.3	293.1	290.9	288.0	293.0	292.3	292.0
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(4,6)	294.7	294.0	293.3	292.4	290.6	287.1	292.1	291.9	291.3

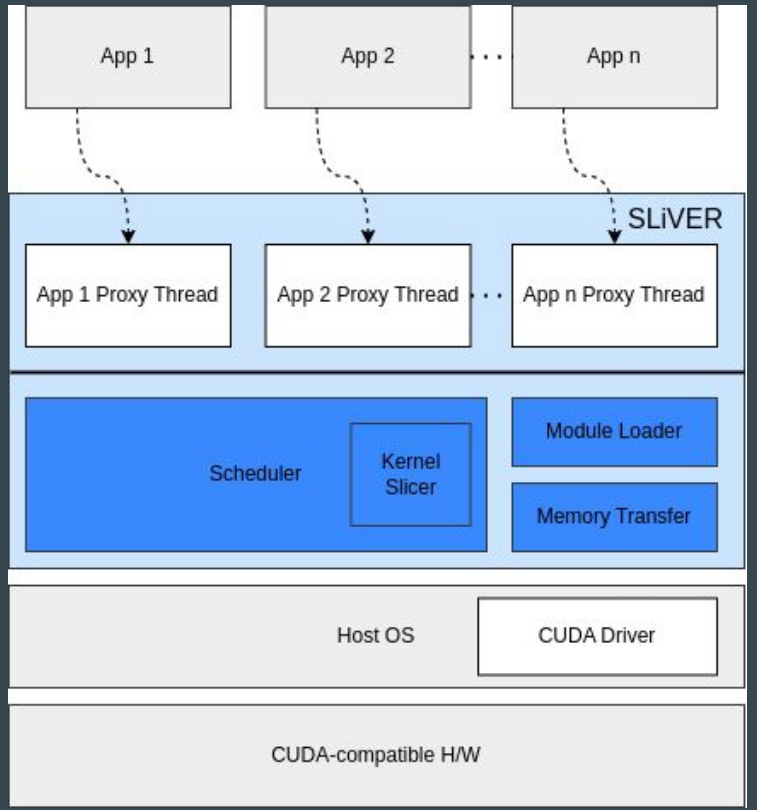
Discussion

- Overall reduction in times: memory latency hidden by kernel execution
- Timings more sensitive to changes in MRI-Q slice size
- For fixed SGEMM slice size, timing decreases and then increases
  - Initial decrease due to opportunities for co-scheduling
  - Later increase due to overhead of launching more kernels
- Timing without kernel slicing: 293.3ms
- Timing with optimal slice size: 287.0ms

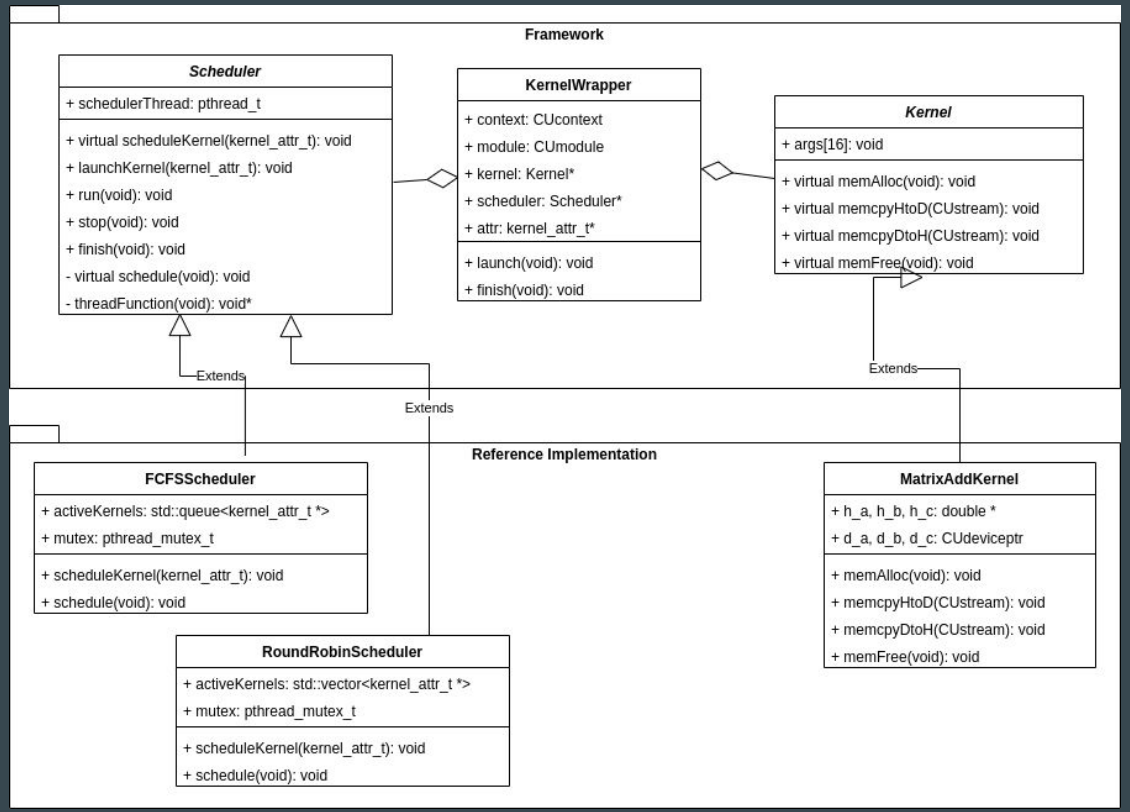
SliVER

Design

- Framework to demonstrate potential of kernel slicing
- Built using CUDA driver API
  - Context creation
  - Load module and get kernel
- Scheduler thread supports slicing
- Similar to MPS
  - Scheduler thread ≡ Daemon process



SliVER - Entity Diagram



SliVER - Kernel

- CUDA kernel abstracted as virtual class, Kernel in C++
- User implements:
  - Memory allocation (cuMemAlloc)
  - Asynchronous host-to-device memory transfer (cuMemcpyHtoD)
  - Asynchronous device-to-host memory transfer (cuMemcpyDtoH)
  - Memory free (cuMemFree)

MatrixAddKernel

```
void MatrixAddKernel::memAlloc()
{
    h_a = (double *)malloc(N * sizeof(double));
    h_b = (double *)malloc(N * sizeof(double));
    h_c = (double *)malloc(N * sizeof(double));

    cuMemAlloc(&d_a, N * sizeof(double));
    cuMemAlloc(&d_b, N * sizeof(double));
    cuMemAlloc(&d_c, N * sizeof(double));
}

void MatrixAddKernel::memcpyHtoD(const CUstream &stream)
{
    cuMemcpyHtoDAsync(d_a, h_a, N * sizeof(double), stream);
    cuMemcpyHtoDAsync(d_b, h_b, N * sizeof(double), stream);
}

void MatrixAddKernel::memcpyDtoH(const CUstream &stream)
{
    cuMemcpyDtoHAsync(h_c, d_c, N * sizeof(double), stream);
}

void MatrixAddKernel::memFree()
{
    cuMemFree(d_a);
    cuMemFree(d_b);
    cuMemFree(d_c);
}
```

SliVER - Kernel Module

- User must compile kernel into PTX
- Kernel name mangling must be disabled for ease of loading
- Module name and kernel name used by KernelWrapper class

MatrixAdd

```
extern "C" __global__ void matrixAdd(int blockOffsetX,
                                     int blockOffsetY,
                                     int blockOffsetZ,
                                     double *a,
                                     double *b,
                                     double *c)
{
    int tid = (blockIdx.x + blockOffsetX) * blockDim.x + threadIdx.x;
    if (tid < N)
    {
        c[tid] = a[tid] + b[tid];
    }
}
```

SliVER - KernelWrapper

- Interface between Kernel and Scheduler classes
- Responsibilities
  - Launch dedicated thread for application
  - Set current thread context
  - Load kernel from module
  - Execute “CUDA” calls defined in Kernel
  - “Launch” kernel
- Non-blocking: once kernel is “launched,” thread continues executing CPU-side code till kernel result required
- Current implementation has support for one kernel per application

KernelWrapper

```
void *KernelWrapper::threadFunction()
{
    // set CUDA context and load kernel

    // kernel launch setup
    kernel->memAlloc();
    kernel->memcpyHtoD(attr->stream);
    set_state(&(attr->kcb), MEMCPYHTOD);

    // scheduler intercepts kernel launch
    scheduler->scheduleKernel(this->attr);

    // application can continue executing

    // wait for scheduler to complete executing kernel
    pthread_mutex_lock(&(attr->kcb.kernel_lock));
    while (attr->kcb.state != MEMCPYDTOH)
    {
        pthread_cond_wait(&(attr->kcb.kernel_signal),
                          &(attr->kcb.kernel_lock));
    }
    pthread_mutex_unlock(&(attr->kcb.kernel_lock));

    // wrap up
    kernel->memcpyDtoH(attr->stream);
    kernel->memFree();
}
```

SliVER - Scheduler

- Implemented as a virtual class; different schedulers for different logic
- Responsibilities
  - Launch scheduler thread
  - Maintain set of active kernels
  - Choose kernel to schedule and launch on GPU
  - Return result of execution to corresponding application thread
- Synchronization between application and scheduler threads via mutex+conditional signals

FCFSScheduler

```
void FCFSScheduler::scheduleKernel(kernel_attr_t *kernel)
{
    // assign id to kernel and update state to LAUNCH

    // enqueue kernel
    pthread_mutex_lock(&mutex);
    activeKernels.push(kernel);
    pthread_mutex_unlock(&mutex);
}

// wrapper around launchKernel
void FCFSScheduler::schedule()
{
    if (activeKernels.size() == 0)
    { // nothing to do? yield the CPU
        usleep(1);
    }
    else
    {
        activeKernels.front()->kcb.slicesToLaunch = 2;
        launchKernel(activeKernels.front());
        if (activeKernels.front()->kcb.totalSlices == 0)
        { // all slices done? dequeue
            set_state(&(activeKernels.front()->kcb), MEMCPYDTOH, true);
            pthread_mutex_lock(&mutex);
            activeKernels.pop();
            pthread_mutex_unlock(&mutex);
        }
    }
}
```

Summary

- Discussion of existing virtualization solutions and incompatibility with edge GPUs
- Performance analysis of kernel slicing on co-scheduling SGEMM and MRI-Q kernels
- Generic multithreaded framework to demonstrate client orchestration with kernel slicing

Future Work

- Add support for launching multiple kernels from single application
- More benchmarking
  - Slicing tested only for SGEMM and MRI-Q kernels
  - Focus on representative Edge benchmarks
- Performance evaluation of SliVER
- Scheduling policies based on nature of kernel launched
  - Current support for FCFS, round-robin, and priority-based scheduling
- Tailored solution for edge GPUs
  - Investigate shared memory model
- Extension to multi-process GPU scheduling (similar to MPS)

References

- GPU Virtualization and Scheduling Methods: A Comprehensive Survey. Hong et. al
- Hyper-Q Example, Thomas Bradley
- Multi-Process Service, NVIDIA Corporation
- Improving GPGPU concurrency with elastic kernels, Pai et. al