# SliVER: Slicing-based GPU Virtualization for Edge Resources

## Bachelor's Thesis Project

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*by*

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# SliVER: Slicing-based GPU Virtualization for Edge Resources

**Aditya Sriram**

## Abstract

The IoT boom has resulted in edge GPUs becoming competitive for several applications typically performed in Cloud, including extended reality (XR) and deep learning (DL), and it has become necessary to virtualize them to fully utilize hardware in a shared setting. Kernel slicing is one such software mechanism requiring developer assistance that slices user kernels to offer more fine-grained scheduling opportunities to the GPU scheduler. We conduct a detailed study of the performance gains due to slicing and present the design of SliVER, a software middleware framework that utilizes kernel slicing to orchestrate GPU access across multiple client applications. Code for the project can be found at `https://github.com/aweditya/edge-gpu-virt`.

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# Chapter 1

# Introduction

Although graphics processing units (GPUs) were originally intended to accelerate computer graphics and image processing applications, they have become ubiquitous with the advent of machine learning and are being increasingly used for embarassingly parallel applications like neural network (NN) training+inference and cryptocurrency mining. NVIDIA dominates the discrete GPU market with a reported 87% market share at the end of the second fiscal quarter in 2023 and manufactures a broad spectrum of GPUs, ranging from resource-constrained devices like the NVIDIA Jetson Nano and Jetson AGX Orin to server-grade GPUs like the NVIDIA RTX 40 series. Due to their pervasiveness, most cloud vendors like IBM, Amazon Web Services (AWS), NVIDIA, and Google provide paid access to their physical GPU resources in the form of clusters. For example, it is estimated that training GPT-4, OpenAI's multimodal large language model (LLM) took around 25,000 NVIDIA A100 GPUs with a hardware cost of nearly $63 million with respect to today's equivalent hardware.

Clients access the provider's services through virtual machines (VMs) and typically several VMs share access to the common underlying physical resource. This is enabled through a technique called virtualization which separates a service from its physical delivery and is at the heart of cloud computing. One key advantage of virtualization is that it improves utilization of the underlying physical resource. Since GPUs are first-class resources in most data centres, the necessity to maximize GPU utilization has resulted in several virtualization solutions being developed for high-end GPUs. This has been accompanied by hardware changes intended to make more efficient virtualization possible resulting in a variety of hardware-based solutions like vGPUs, MiGs that provide spatial and temporal multiplexing and software-based approaches like gViM, vCUDA, and multi-process service (MPS) that provide efficient temporal multiplexing.

At the same time, rapid growth in Internet of Things (IoT) has shifted focus from cloud computing to computation on the "Edge," closer to data sensors. Edge devices are becoming more powerful while retaining their low power requirement. [5] provides for a case for systems research at the edge and the need for virtualizing resource-constrained GPUs.

## 1.1 Problem Description

Since edge GPUs lack the required hardware support to enable efficient virtualization, any solution must be purely software-based and motivates the need for a middleware. We aim to answer the following the question:

> In the absence of hardware support, how can a software-based virtualization solution be realized for resource-constrained GPUs like the Jetson Nano to enable efficient time-sharing across applications?

Any solution must orchestrate GPU access at the process level. Since processes do not share a common address space, shared memory and IPC mechanisms are required. Therefore, we modify the above goal:

> In the absence of hardware support, how can a software-based virtualization solution be realized for resource-constrained GPUs like the Jetson Nano to enable efficient time-sharing across applications with *CPU threads* abstracting the applications?

## 1.2 Contributions

Kernel slicing has been proposed as a software-based solution to enable efficient temporal multiplexing of GPUs across multiple applications. We explore the potential of developer-assisted kernel slicing to improve utilization of edge GPUs. This is accompanied by the design of a middleware that implements slicing to orchestrate access from multiple clients represented as threads. However, the solution can be further expanded to support clients in a multi-process setting. To summarise, we make the following contributions in this report,

1. The feasibility of existing GPU virtualization is discussed and we describe why they are inadequate for resource-constrained GPUs, with the Jetson Nano being used as a characteristic GPU.

2. The performance benefits of kernel slicing for co-scheduling kernels with different characteristics is studied. Two different schemes are implemented and benchmarked: multithreaded launches or For this purpose, the SGEMM [6] and MRI-Q [7] kernels are used from the Parboil benchmark [8]. We evaluate kernel slicing using memory transfer+kernel launch time as the metric.

3. A purely software-based approach for efficient multiplexing of edge GPUs based on kernel slicing is proposed. The design is presented for multiplexing at the thread (not process) level and is implemented as a `C++` library that exposes custom APIs an application must conform to.

# Chapter 2

# Background and Prior Work

## 2.1 CPU and GPU Architectures

While CPUs are designed to perform serial tasks, incurring the least possible latency, GPUs are optimized for throughput. This is evident from the difference in the number of cores (a core is the fundamental unit capable of executing programs) between a CPU and GPU.

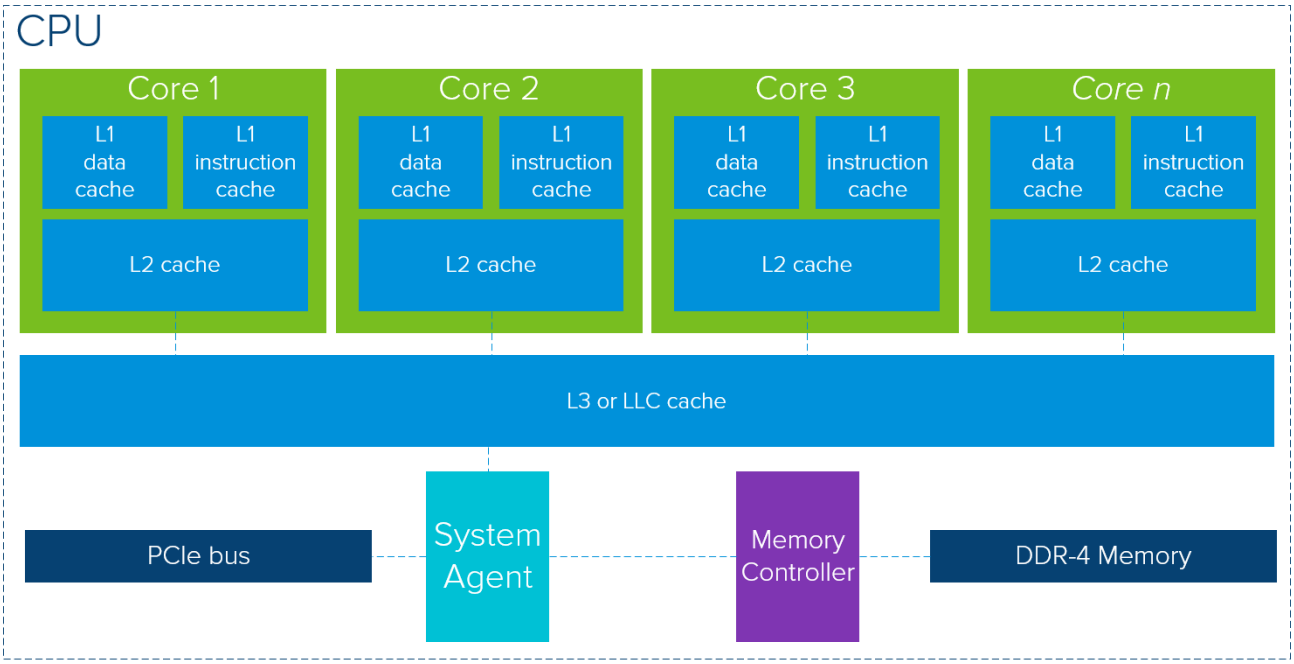


Figure 2.1: CPU architecture consisting of $n$ cores with separate L1 instruction and data caches, L2 cache, and L3 cache shared among all cores. Image taken from [1]

A CPU consists of multiple cores. A core has an execution unit or ALU along with a dedicated L1 data and instruction cache. Per-core L2 caches are used to support L1 caches. All cores share the last-layer or L3 cache (LLC). Multiple caches located at different distances from the execution unit constitute a memory hierarchy. Memory access time increases with distance to the cache. Technology advances increased the performance gap between CPUs and memory which resulted in memory operations becoming a performance bottleneck. The goal of the memory

hierarchy is to give an impression to the ALU that memory is both large and fast. If data is found in a certain level, it is fetched from the next level and hence, if data is not found in caches, it is fetched from global memory.

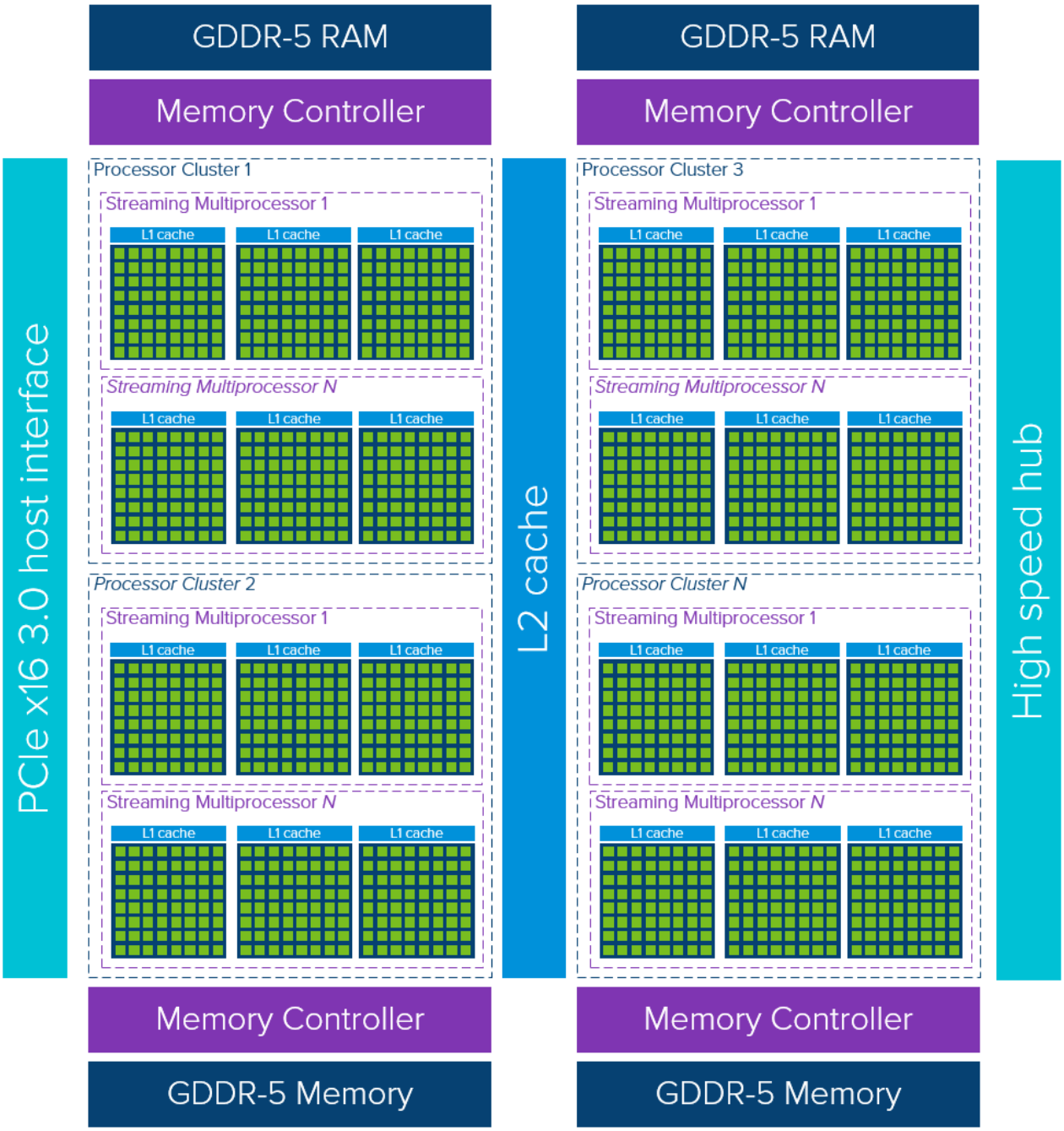


Figure 2.2: A single GPU device consisting of multiple processing clusters (PC), divided into streaming multiprocessors (SM). L1 caches are associated with each SM while the L2 cache is shared across SMs. Image taken from [1]

Compared to CPUs, GPUs have a far larger number of cores. A GPU device is divided into several processor clusters and each processor cluster is divided into streaming multiprocessors (SMs). Each SM consists of multiple cores sharing an L1 cache, while the L2 cache is shared among multiple SMs. Similar to CPUs, if data is not available in caches, it is fetched from

Graphics Double Data Rate 5 (GDDR-5) memory by the memory controller. Devoting more area to processing enables GPUs to hide memory access latency with computation. Hence, GPUs typically have smaller caches. The large number of cores makes GPUs ideal for parallel computation which is why GPUs are at the forefront of development in high-performance computing (HPC). Since applications consist of a mix of serial and parallel parts, systems are designed with both CPUs and GPUs to maximize performance where the GPU serves as a co-processor.

## 2.2 CUDA

A brief overview of CUDA is presented below. CUDA, earlier known as Compute Unified Device Architecture, is a proprietary, general purpose computing platform and programming model by NVIDIA, used to write programs that can take advantage of NVIDIA GPUs. By using CUDA's application programming interface (API), developers familiar with `C`, `C++`, and Fortran can write programs for graphics processing or general computation. CUDA became popular due to its gentle learning curve as compared to previous platforms like Direct3D and OpenGL which require a thorough understanding of the graphics processing pipeline.

### 2.2.1 Kernels

Kernels are functions written in C++ that are executed on the GPU in parallel threads. A kernel is defined using the `__global__` declaration specifier and the number of threads that will execute the kernel is specified using a chevron (`<<<...>>>`). Individual threads can be referred to inside the `C++` program through a unique thread identifier called `threadIdx`. `threadIdx` has three components which lets threads be identified using 1D, 2D, or 3D thread identifiers, representing 1D, 2D, or 3D thread blocks.
There is a limit to the number of threads in a thread block since thread blocks are executed on an SM and must share the memory of that core. However, one can split the total number of threads into thread blocks so that the product of number of threads per block and number of thread blocks equals the total number of threads. Just like threads, blocks are organized into 1D, 2D, or 3D grids. The number of threads per block and number of blocks can be specified inside `<<<...>>>` as `int` or `dim3`. For example, the following program creates a kernel to add two matrices. The kernel is launched with 256 threads arranged in a square block.

```
// matrix addition kernel; computes c = a + b
__global__ void matrixAdd(float *a, float *b, float *c)
{
    int i = blockIdx.x * blockDim.x + threadIdx.x;
    int j = blockIdx.y * blockDim.y + threadIdx.y;
    if (i < N && j < N)
        c[i * N + j] = a[i * N + j] + b[i * N + j];
}
```

```
int main()
{
    ...
    // kernel invocation
    dim3 blockConf(16, 16);
    dim3 gridConf(N / 16, N / 16);
    matrixAdd<<<gridConf, blockConf>>>(d_a, d_b, d_c);
    ...
    return 0;
}
```

Thread blocks must be capable of being executed independently (there should be no interdependencies). This lets blocks be scheduled on different SMs irrespective of their order. Since threads in the same thread block are scheduled on the same SM, they can access a common shared memory. Synchronization points can be introduced using `__syncthreads()`, which acts as a barrier at which all threads must wait before being allowed to proceed.

### 2.2.2 Memory Hierarchy

Memory hierarchy is a key abstraction in the CUDA API. CUDA threads can access data in different memory spaces. Each thread has private memory, which is accessible only to the thread. Each thread also has access to the shared memory associated with the corresponding thread block. Shared memory has the same lifetime as the thread block and can only be accessed by threads within the thread block. Finally, all thread blocks have access to global memory, which is shared between GPU kernels. CUDA also provides two additional read-only memory spaces accessible by all threads: constant and texture. Unlike shared memory, global, constant, and texture memory persist across kernel launches by the same application.

### 2.2.3 Heterogeneous Programming

Typically, applications are heterogeneous in nature. Some portions are serial (suitable for CPUs) and some are parallel (suitable for GPUs). The CUDA programming model makes the following assumptions:

- CUDA threads execute on a physically separate device as opposed to the host, which is running the C++ program.
- The host and device maintain their own memories called *host memory* and *device memory*. The CUDA runtime is responsible for managing device memory allocation/deallocation and data transfers between the host and device.

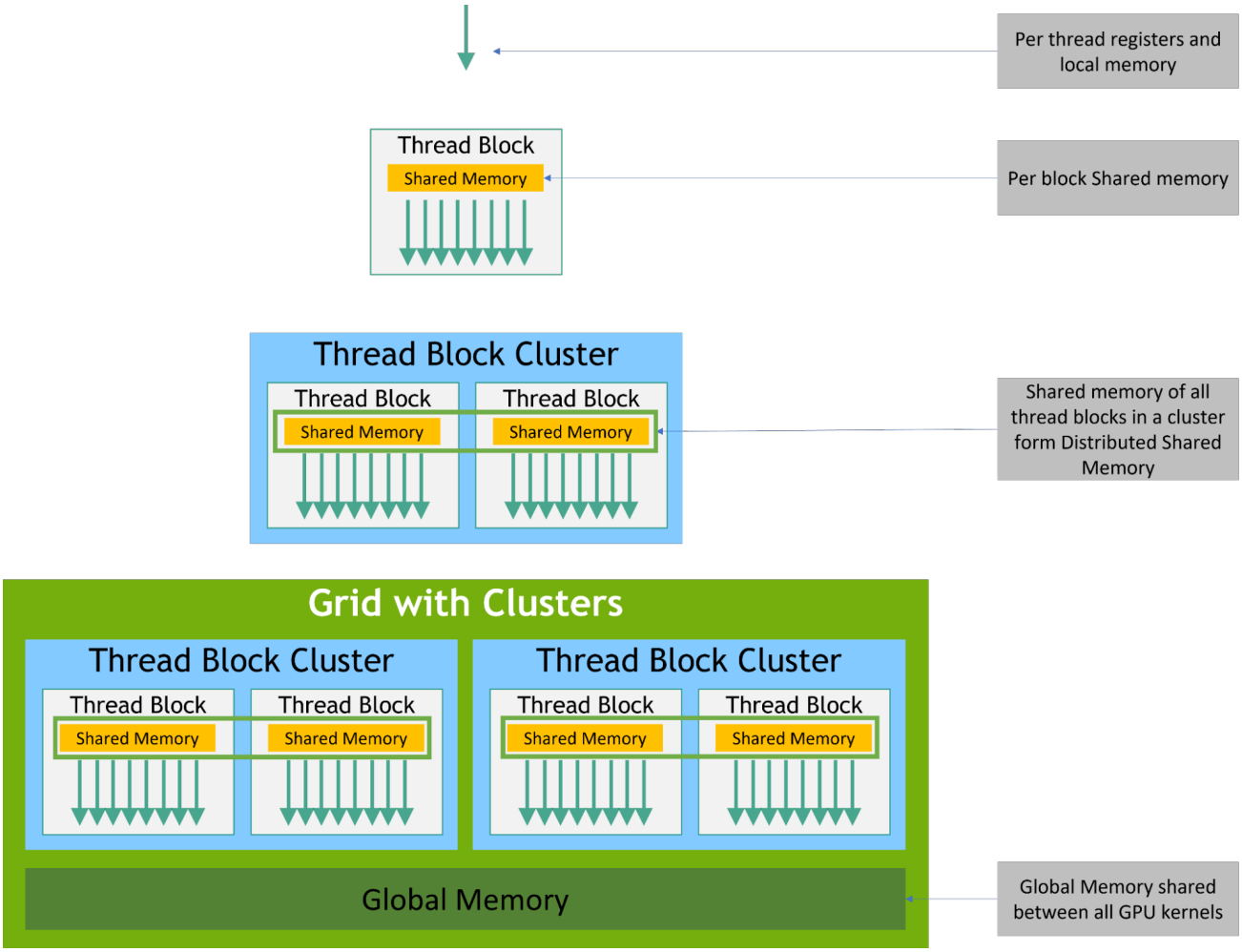


Figure 2.3: Thread and memory hierarchy in CUDA. Image taken from [2]

CUDA also provides unified memory called managed memory by exposing a common address space that is accessible to both, the host and device. This avoids data transfers between the host and device.

### 2.2.4 Programming Interface

The CUDA programming interface provides a set of language extensions to the `C++` library along with a runtime library. Code that uses the provided language extensions must be compiled with `nvcc`. The CUDA runtime library provides functions that execute on the host to launch compute kernels, allocate and deallocate device memory, and transfer data between the host and device. The runtime is built on top a low-level driver API. The CUDA driver API exposes *contexts,* which store the state of execution on the GPU.
`nvcc` is used to compile device code written in `C++` to the CUDA instruction set architecture (ISA) called, *PTX*. `nvcc` also modifies the host code, replacing kernel launches using `<<<...>>>` with the corresponding CUDA runtime function call to load and launch the compiled kernel. The transformed host code can be then fed through a `C++` compiler that outputs object code. Finally, the executing application invokes the PTX code at runtime which is then compiled by the GPU device driver to generate binary code. This is an example of *just-in-time compilation.*

### 2.2.5 Memory Management

As mentioned earlier, the CUDA runtime is responsible for managing device memory allocation/deallocation and data transfers between the host and device and provides several APIs to do so. Any CUDA program can be broken into the following stages,

1. Host memory allocation via `malloc()` and its variants while device memory can be allocated using `cudaMalloc()`
2. host-to-device memory transfer via `cudaMemcpy()` passing `cudaMemcpyHostToDevice` as an argument
3. Kernel launch using `<<<...>>>`
4. device-to-host memory transfer via `cudaMemcpy()` passing `cudaMemcpyDeviceToHost` as an argument
5. Host memory deallocation via `free()` and device memory deallocation via `cudaFree()`.

Returning to the matrix addition kernel example,

```
// matrix addition kernel; computes c = a + b
__global__ void matrixAdd(float *a, float *b, float *c);

int main()
```

```
{
    int N = ...;

    // host memory allocation
    float *h_a = (float *)malloc(N * sizeof(float));
    float *h_b = (float *)malloc(N * sizeof(float));
    float *h_c = (float *)malloc(N * sizeof(float));

    // device memory allocation
    float *d_a, *d_b, *d_c;
    cudaMalloc((void **)&d_a, N * sizeof(float));
    cudaMalloc((void **)&d_b, N * sizeof(float));
    cudaMalloc((void **)&d_c, N * sizeof(float));

    // host-to-device memory copy
    cudaMemcpy(d_a, h_a, N * sizeof(float), cudaMemcpyHostToDevice);
    cudaMemcpy(d_b, h_b, N * sizeof(float), cudaMemcpyHostToDevice);

    // kernel invocation
    dim3 blockConf(16, 16);
    dim3 gridConf(N / 16, N / 16);
    matrixAdd<<<gridConf, blockConf>>>(d_a, d_b, d_c);

    // device-to-host memory copy
    cudaMemcpy(h_c, d_c, N * sizeof(float), cudaMemcpyDeviceToHost);

    // free host memory
    free(h_a);
    free(h_b);
    free(h_c);

    // free device memory
    cudaFree(d_a);
    cudaFree(d_b);
    cudaFree(d_c);
    return 0;
}
```

### 2.2.6 Asynchronous Concurrent Execution

By default, memory operations include allocation/deallocation and host-to-device and device-to-host transfers are synchronous and blocking (an exception to this rule is when the memory block size is 64kB or less, in which case data transfers are asynchronous). On the other hand, kernel launches are asynchronous and program control is immediately returned to the host. CUDA exposes concurrent execution through *streams* and offers alternative data transfer APIs to take advantage of stream concurrency.

A stream is a sequence of commands that are guaranteed to execute in-order. However, operations in different streams are not synchronized and may be executed concurrently. Streams can be created and destroyed using the `cudaStreamCreate()` and `cudaStreamDestroy()` APIs that accept an argument of type `cudaStream_t`. The stream object can be passed to `<<<...>>>` to launch a kernel on the specified stream. CUDA also exposes the `cudaMemcpyAsync()` API for asynchronous data transfers between the host and device that accepts a stream argument. In the absence of any stream argument, operations are performed on the *default stream.* The default stream posseses the property of *implicit synchronization,* which means operations on the default stream will not execute until all previous CUDA activity has finished.

### 2.2.7 Hardware Implementation

NVIDIA GPUs consist of multiple streaming multiprocessors (SMs). When a compute kernel is launched, the thread blocks are allocated to available SMs in a round-robin fashion. Threads of a thread block are executed entirely on an SM and depending on resources available (number of registers, memory), it is possible for multiple thread blocks to execute on an SM.

SMs follow the *single-instruction, multiple-thread* (SIMT) architecture. Thread blocks are first partitioned into groups of 32 threads, called a *warp.* This partitioning is static: the first 32 threads starting from thread ID 0 go into the first warp and so on. Warps start executing at the same program address but have their own program counter, registers, and call stack (the program counter, register states, and call stack is collectively known as the execution context) and are free to execute independently. However, maximum efficiency is achieved when all threads in a warp agree on their execution path and do not diverge.

The state for each thread in a warp is stored on the device during execution for the entire lifetime of the warp. This implies that switching execution contexts has no cost. At instruction issue time, the warp scheduler selects warps that are ready to execute their next instruction and schedules them.

### 2.2.8 CUDA Driver API

Salient features of the CUDA driver API are discussed in brief since the simulator design presented later uses features offered by the same. The driver API is implemented in the CUDA dynamic library. Objects available in the driver API include:

1. `CUdevice` which is a handle for a CUDA-enabled device,
2. `CUcontext` which is equivalent to a CPU process,
3. `CUmodule` which is equivalent to a dynamic library,
4. `CUfunction` which is a handle for a CUDA kernel,
5. `CUstream` which is a handle for a CUDA stream.

The driver API is initialized by calling `cuInit()` before any function in the driver API is called. After this, a CUDA context must be created using `cuCtxCreate()` and passing a reference to a `cuDevice` object. If the driver API is used from multiple CPU threads, the context created must be made current by calling `cuCtxSetCurrent()`. For example, the function below is a convenient wrapper to get information about the first CUDA device in a multi-GPU environment and create a context for the same device. *Note that CUDA creates separate contexts for each process running on the CPU and GPU access is time multiplexed across contexts.*

```
void initCuda()
{
    int deviceCount = 0;
    cuInit(0);
    int major = 0, minor = 0;

    // get number of devices
    cuDeviceGetCount(&deviceCount);

    // get first CUDA device
    cuDeviceGet(&device, 0);
    char name[100];
    cuDeviceGetName(name, 100, device);

    // get compute capabilities and the devicename
    cuDeviceComputeCapability(&major, &minor, device);

    // create context for first device
    cuCtxCreate(&context, 0, device);
}
```

All driver objects like modules, streams are referenced with respect the current context. Once a module has been loaded, kernel handles can be retrieved through the following,

```
CUmodule module;
std::string moduleFile = "matrixAdd.ptx";
```

```
std::string kernelName = "matrixAdd";

// set current context in CPU thread
cuCtxSetCurrent(context);
 // load module given as PTX file
cuModuleLoad(&module, moduleFile.c_str());
// get handle to matrixAdd kernel
cuModuleGetFunction(&(attr->function), module, kernelName.c_str());
```

## 2.3 Virtualization and VMMs

Virtualization is the technology behind cloud computing that lets multiple "virtual computers" share the underlying physical resources of a computer. The virtual computers are commonly known as virtual machines (VMs) and run their own operating system (OS). The main goal of virtualization is to improve hardware utilization.

VMs can be thought of as "software-defined" computers that emulate hardware. However, VMs do not directly access the underlying hardware but through a software layer called the virtual machine monitor (VMM) or hypervisor. There are two types of hypervisors: type-1 or bare-metal, and type-2 hypervisors. In type-1 hypervisors, the hypervisor runs directly on the underlying hardware while in type-2 hypervisors, the hypervisor runs as a process on the host.

Just like the OS must be able to efficiently context switch between processes, a VMM must be able to efficiently perform "machine switches." VMs must be able to run instructions in privileged (the guest OS) mode and unprivileged mode while the VMM retains control over hardware (the VMM is running in privileged mode) [9]. Whenever a userspace process inside the VM attempts to perform some privileged operation like a system call, the CPU traps to the VMM which redirects control to the guest OS trap handler. Return from trap operations are trapped by the VMM which transfers control back to the userspace process. Additionally, any privileged operations by the guest OS would be trapped to the VMM. The guest OS is oblivious to the fact that it is being virtualized. However, this method does not work directly because modern CPU architectures were not designed to be virtualizable (did not natively support this kind of direct execution). For example, the x86 architecture consisted of *sensitive instructions* which were capable of modifying hardware state in both privileged and unprivileged mode. The standard example of this is the `POPF` instruction which is used to pop CPU flags off the stack. In privileged mode, executing `POPF` would overwrite the interrupt flag but this was disallowed in unprivileged mode and such a trap-and-emulate mechanism would be faulty.

Several techniques to virtualizable non-virtualizable ISAs have been proposed. In *paravirtualization,* nonvirtualizable portions of the ISA are replaced with virtualizable equivalents. The guest OS knows it is being virtualized and invokes *hypercalls* which are executed by the VMM. The Xen hypervisor is based on this design. Although applications can run inside the VM

without modification, the guest OS must be modified. An alternative to paravirtualization is *full virtualization,* where the guest OS runs unmodified and sensitive instructions are trapped to the hypervisor. This happens on the fly at a binary level. However full virtualization incurs an overhead compared to paravirtualization. The VMWare workstation is based on this design. The addition of hardware support also made more efficient virtualization possible.
Memory virtualization was traditionally implemented using *shadow paging,* where the VMM maintains a shadow of the VM's page table. Translation from guest virtual address (GVA) to guest physical address (GPA) is avoided by directly storing the GVA to host physical address (HPA) mapping the shadow table when the VM is running. With the addition of hardware support, it became possible to store *extended page tables* (EPTs) where the hardware memory management unit (MMU) has access to two pointers: one for the guest OS's page table and one for the host OS's page table. Whenever a GVA had to be translated, the MMU traversed both page tables to get the corresponding HPA.
I/O virtualization [10] can either be implemented using *emulation* or *device passthrough*. In emulation, an I/O request made by an application inside a VM is first handled by the guest OS's I/O stack. The guest device driver issues an I/O request to a virtual device which is intercepted by the hypervisor. The hypervisor then schedules the request on the physical device by a device driver with access to the hardware, managed by the hypervisor (or running as a separate control VM). On completion, the physical device issues an interrupt handled by the hypervisor. The hypervisor determines the source of the I/O request and issues a virtual interrupt to the virtual device of the corresponding VM. Hence, emulation is achieved using a frontend emulated device exposed to the VM, and a backend device part of the hypervisor. In device passthrough, a single I/O device is partitioned into multiple slices and each slice is assigned to a single VM. Single Root I/O Virtualization (SR-IOV) is an example of device passthrough for PCIe devices. One challenge of device passthrough is for devices support direct memory access (DMA). When the guest device driver provides a DMA buffer, it is using GPAs which are not the same as HPAs and completely wrong. To overcome this problem, devices with SR-IOV are modified to be aware of virtualization and have an I/O memory management unit (IOMMU). The IOMMU knows about host page tables and translates invalid GPAs to valid HPAs that can be passed to the device.

## 2.4 VirtIO

virtio [11] provides a common interface for emulated devices in a paravirtualized hypervisor. The Linux kernel contains several hypervisor implementations including Xen [12], KVM [13], and lguest [14] that have their own format for device drivers. virtio provides standardization to enable code reuse; the frontend drivers in the guest VM are independent of the specific hypervisor while the backend drivers need not be common as long as they expose a common frontend. A virtio device is registered using a transport-specific method—peripheral component interconnect (PCI), memory-mapped I/O (MMIO), or channel-command word (CCW)—and contains a device status field, feature bits, notifications, device configuration space, and virtqueues. The file

configuration operations associated with the guest driver can be used to read/write feature bits, read/write the configuration space, read/write the device status bits, and perform a reset.
The guest driver must perform a certain sequence of steps to initialize a virtio device. The *device status word* indicates which all initialization steps have been completed. The device lists all its supported features and during initialization, the driver reads this list and must indicate the list of features it supports. For example, feature bit 0 of a network device indicates that it supports checksumming of packets [15]. There are three types of *notifications*:

1. Configuration change notifications which are initiated by the device to indicate a change in the device configuration space described below.

2. Available buffer notifications which are initiated by the driver to indicate that a buffer may have become available on the virtqueue specified in the notification.

3. Used buffer notifications which are initiated by the device to indicate that a buffer may have been used on the virtqueue specified in the notification.

The implementation of notifications is transport-dependent and usually interrupt-based. virtio devices also have a reset operation to reset the device during initialization and cleanup. The mechanism used to initiate a device reset is transport-specific. The *device configuration space* contains device-specific information and is used for static or initialization-time parameters.
virtio abstracts the I/O mechanism through one or more *virtqueues* which is a queue of guest buffers consumed by the virtual device (block devices have a single virtqueue, while network devices and two virtqueues, for receiving and transmitting respectively). One of the configuration operations is `find_vq,` which returns a virtqueue, given the virtio device structure, `struct virtio_device`. The guest driver can issue a request to the device by adding an available buffer to the virtqueue, and optionally signalling the device with an available buffer notification. The device executes the request and when complete, adds a used buffer to the virtqueue, signalling the driver with a used buffer notification. It is not necessary for a device to execute requests in the order they were issued.
The virtqueue transport mechanism is implemented as a ring buffer which is discussed in brief. The *split virtqueue format* separates a virtqueue into three areas, where each part is writeable by the driver or device, but not both: descriptor area, driver area, and device area. The *descriptor table,* stored in the descriptor area, contains an array of guest addressed buffers (GPAs are used for addressing purposes). The *available ring,* stored in the driver area, contains guest buffers offered to the device for consumption. The available ring is only written to by the driver. The *used ring,* stored in the device area, contains buffers processed by the device.

## 2.5 GPU Virtualization

Typically, GPU virtualization fall under the following categories: API remoting, para and full virtualization, and hardware-assisted virtualization and in the following detail, these approaches

are discussed in brief.

### 2.5.1 API Remoting

Virtualizing GPUs at the driver level is difficult because vendors do not expose source code details to the public. API remoting virtualizes GPUs at a higher level by providing a wrapper API identical to the original library. GPU calls are intercepted by the wrapper before control reaches the emulated GPU device driver in the VM. The wrapper library transfers control to the host OS, which executes the API call on behalf of the guest. Only the result of execution is returned back to the application through the wrapper library. The frontend and backend communicate through a *shared ring*. The frontend driver encapsulates requests into a message which is sent to the backend driver through shared memory. The backend driver extracts the API request from the message and executes the requested operation through the GPU driver. The result of execution is transferred to the frontend in the opposite direction.

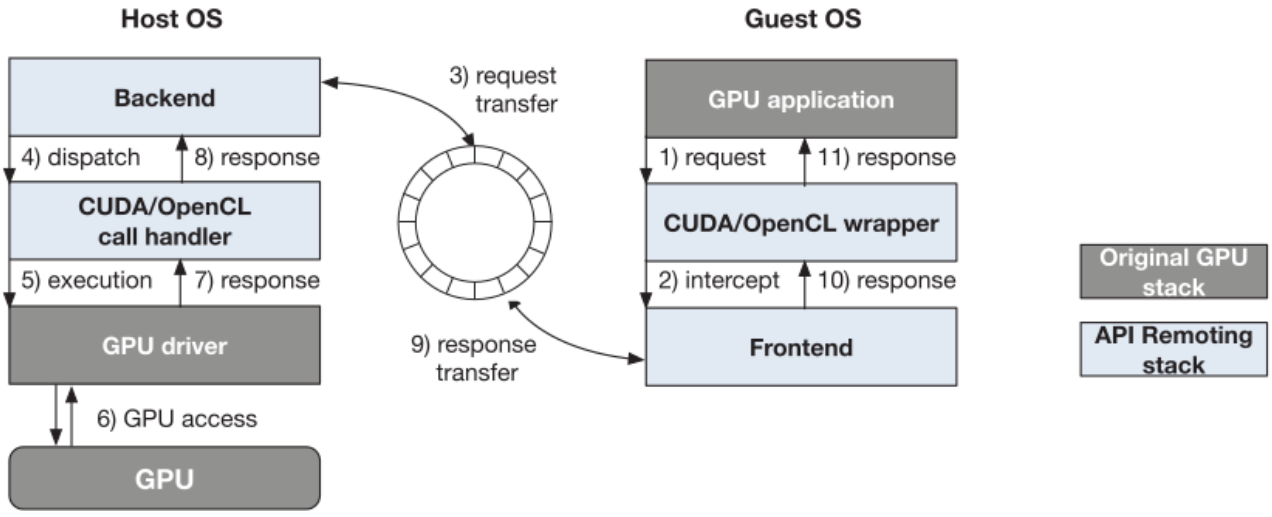


Figure 2.4: API remoting. Image taken from [3]

GViM [16] implemented virtualization at the CUDA API level for the Xen hypervisor. The GPU frontend is implemented in every VM while the backend is implemented in the management domain, dom0 for Xen. To avoid making unnecessary copies between the frontend and backend (which is expensive for HPC applications where memory might span several pages), shared memory provided by Xenstore [12] is used. A one-copy solution is also presented that avoids guest user to kernel copy by directly allocating memory in the frontend driver, which is shared with the backend driver through Xenstore.
vCUDA [17] implemented virtualization at the CUDA API level for KVM [13] based on a client-server model consisting of the vCUDA library in the guest OS, virtual GPU in the guest OS, and vGPU stubs in the server running as an application in the host OS. The vCUDA library is a wrapper around the original CUDA API that intercepts and redirects calls to the host. vGPUs presented to the guest OS are abstractions of the actual hardware and provide virtual GPU

contexts to each application. vCUDA stubs receive requests, create execution contexts, launch requests on the physical GPU, and return the result back to the guest OS. vGPU and vCUDA stubs are periodically synchronized. A high efficiency RPC virtualization tool is developed based on shared memory in VMMs. vCUDA supports two execution modes: TRANSMISSION mode which is compatible with XML-RPC and SHARE mode based on VMRPC [18]. In TRANSMISSION mode, transfers use TCP/IP while in SHARE mode, they use a shared memory zone between the guest OS and host OS.

### 2.5.2 Para and Full Virtualization

Although API remoting has little virtualization overhead, the frequent addition of new APIs and modification of old ones makes updating the wrapper library challenging. In para and full virtualization, GPUs are virtualized at the driver level. The guest OS runs a custom GPU device driver and GPU requests coming from the guest driver are transferred to the host OS through shared memory in the hypervisor. The host device driver schedules requests from VMs and returns results back to the guest driver. This approach does not require modification to GPU libraries but due to its dependence on custom drivers might not be compatible with future microarchitectures.

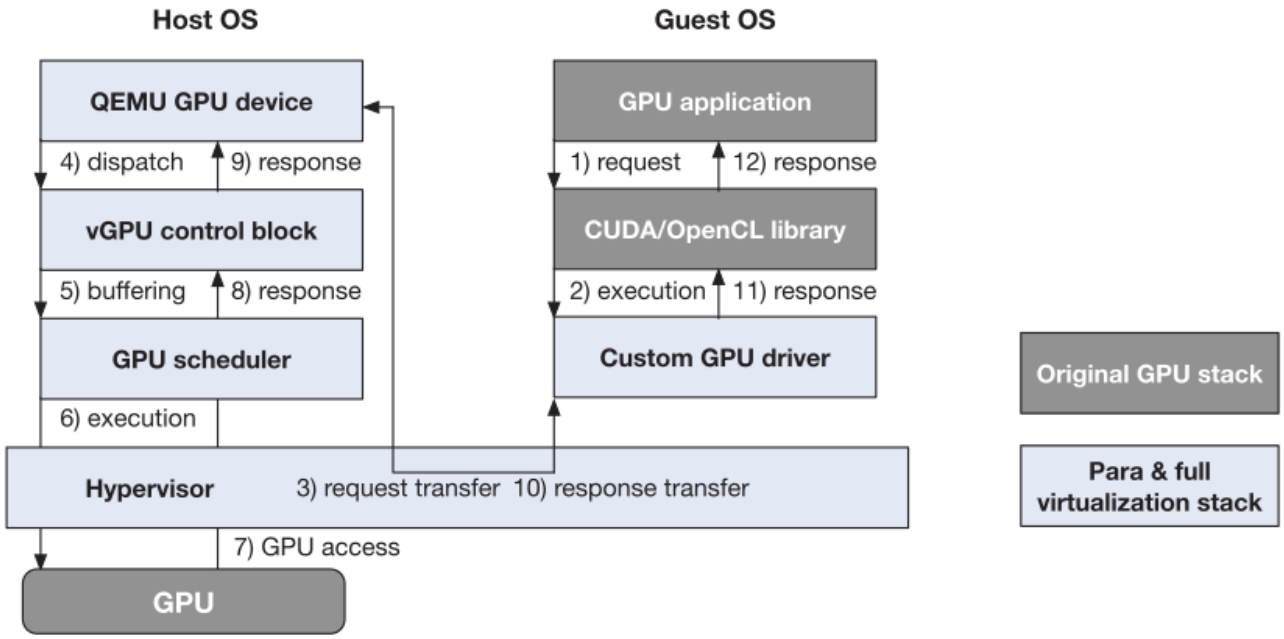


Figure 2.5: Full or paravirtualization. Image taken from [3]

Reference [19] introduced a KVM-based parvirtualization hypervisor solution for AMD's Heterogeneous System Architecture (HSA). A HSA-compliant system combines CPU and GPU on the same silicon die to reduce communication overhead. The CPU and GPU share a virtual address space which makes memory virtualization simple since a table translating guest virtual address to physical addresses is sufficient. It also eliminates host-to-device memory copies. To

construct the GVA-to-HPA mapping, shadow page tables (SPTs) are used which are available to the IOMMU as well. Device DMA is not possible in HSA because all devices can access the entire memory space which would require pinned memory. This requires I/O page faulting and is handled by the *Peripheral Page Service Request* (PPR). When I/O devices attempt to access memory, the IOMMU performs a permission check and address translation. If the device does not have sufficient permission or the page is not in memory, the IOMMU writes the faulty GVA to the PPR's log and issues a PPR interrupt to the CPU. The hypervisor notifies the guest OS with information about the faulty GVA and the guest OS updates its page table. Meanwhile, the hypervisor also updates it SPT on the PPR interrupt. HSA allows the CPU and GPU to share userspace buffers to store GPU commands. This is virtualized by directly passing the address of the shared buffer to the GPU from the guest.
gVirt [20] implemented a full virtualization solution for Intel on-chip GPUs for the Xen hypervisor. The following abstraction is used for Intel GPUs: the render engine in the GPU fetches commands from the *command buffer* for acceleration and the display engine fetches pixel data from the *frame buffer* and sends them to external displays. The command and frame buffers are treated as performance-critical resources so VMs can directly access them through their native graphics drivers. Graphics memory is partitioned by the gVirt mediator for this purpose. Privileged resources like the *page table entries* (PTEs) which carry GPU page tables and *I/O registers* including memory-mapped I/O registers, port registers are protected by trap-and-emulation by the gVirt mediator. This technique is called *mediated passthrough.*

### 2.5.3 Hardware-assisted Virtualization

With hardware-assisted virtualization, each VM is given direct access to the GPU through hardware extension features. API and driver modification is not required. DMA channels and interrupts are directly mapped to the guest OS, bypassing the hypervisor and this method achieves near-native performance. NVIDIA GRID [21], targetted for cloud-sharing environments, implemented a new IOMMU that can directly map GVA to the physical address of the GPU. GPUs supporting GRID include NVIDIA Tesla M6, and M60 [3].

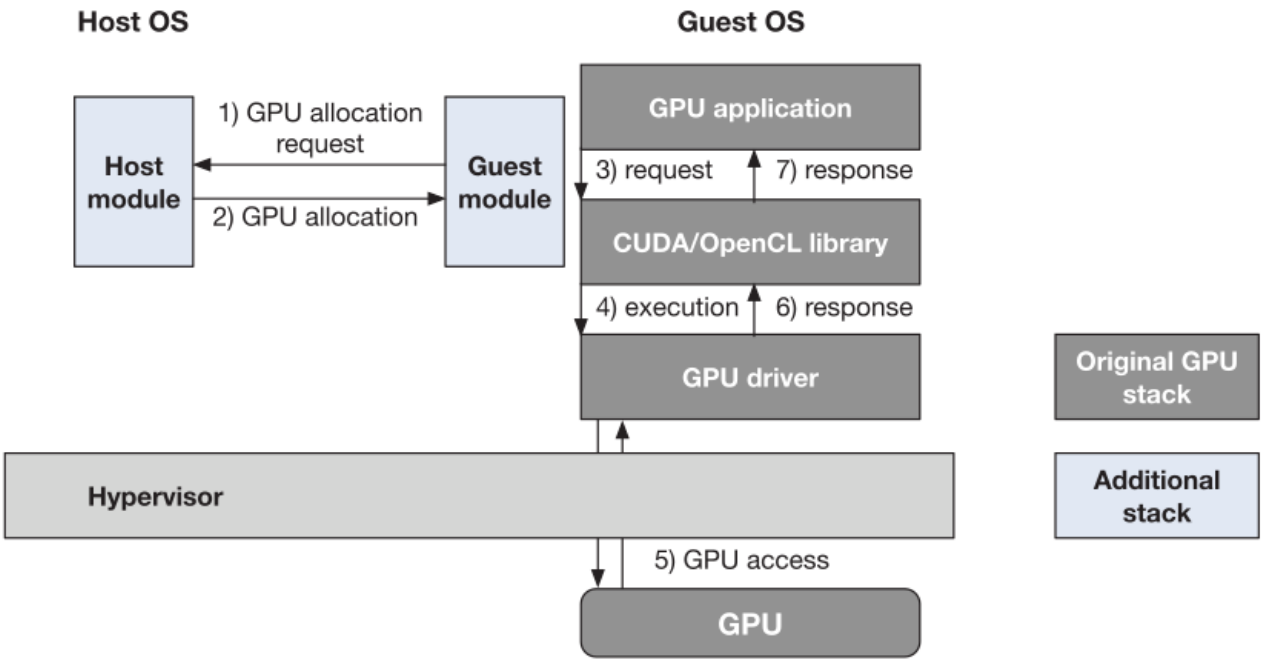


Figure 2.6: Hardware-assistend virtualization. Image taken from [3]

# Chapter 3

# SliVER

In this section, we present the design of our multithreaded middleware, *slicing-based GPU Virtualization of Edge Resources* (SliVER). The *NVIDIA Jetson Nano* was used as a representative resource-constrained GPU. For comparison, experiments were also run on a *NVIDIA GeForce GTX 1650 Ti with Max-Q Design,* a mid-range graphics card for laptops. By default, the Jetson Nano supports dynamic voltage and frequency scaling (DVFS) due to which there is a large variation in execution times. All timings were reported by disabling DVFS writing `0` to the `enable_3d_scaling` file in `/sys/devices/57000000.gpu` [22].

## 3.1 Compute Capabilities

NVIDIA defines the *compute capability (CC)* of a device as a version number that indicates the set of hardware features supported by the GPU architecture; this information is used by the CUDA runtime. The compute capability consists of a major and minor number. Major number is used to identify the core architecture; devices with the same major number share their core architecture. Minor numbers correspond to revisions to the core architecture.

| Compute Capability (CC) | Core Architecture |
|---|---|
| 9 | Hopper |
| 8 | Ampere |
| 7.5 | Turing |
| 7 | Volta |
| 6 | Pascal |
| 5 | Maxwell |
| 3 | Kepler |

Table 3.1: List of compute capabilities and their corresponding architecture

For example, the Jetson Nano has a CC of 5.3, and the GeForce GTX 1650 Ti with Max-Q Design has a CC of 7.5. [23] provides a list of CUDA-enabled GPUs and their compute capabilities however, this information can also be found using the `deviceQuery` utility available in CUDA samples [24]. Results of running `deviceQuery` on both GPUs are given below in table

3.2,

| Device Properties | Jetson Nano | GeForce GTX 1650 Ti with Max-Q Design |
|---|---|---|
| Multiprocessors | 1 | 16 |
| Cores | 128 | 2048 |
| GPU Max Clock Rate (MHz) | 992 | 1200 |
| Memory Clock Rate (MHz) | 13 | 5001 |
| Memory Bus Width (bits) | 64 | 128 |
| Total amount of constant memory (bytes) | 65536 | 65536 |
| Total amount of shared memory per block (bytes) | 49152 | 49152 |
| Total registers available per block | 32768 | 65536 |
| Warp size | 32 | 32 |
| Maximum number of threads per multiprocessor | 2048 | 1024 |
| Maximum number of threads per block | 1024 | 1024 |
| Number of copy engines for concurrent copy and kernel execution | 1 | 3 |

Table 3.2: `deviceQuery` output

## 3.2 Hyper-Q and MPS

Since the Jetson Nano has a CC of 5.3, it can potentially support *Hyper-Q* [25]. Without Hyper-Q, kernels submitted in different streams are merged into a single pipeline to the work distributor which introduces false dependencies between kernels in different streams. This required a careful construction of the kernel launch order to maximize performance. The Kepler architecture introduced multiple work queues managed by a grid management unit that allowed multiple kernels to be executed concurrently without introducing false dependencies. However, the work distributor distributes work among the available *SMs.* Since the Jetson Nano has a single SM, it cannot take advantage of Hyper-Q. This is confirmed by the `simpleHyperQ` utility available in [24]. The timings obtained on running the utility are reported below.

| Expected time for serial execution | 0.330s-0.640s |
|---|---|
| Expected time for fully concurrent execution | 0.020s |
| Measured time | 0.360s |

Table 3.3: Execution times to check for Hyper-Q technology

Hyper-Q is used in NVIDIA's Multi-Process Service (MPS) [26], an alternative implementation of the CUDA API for concurrent kernel scheduling across multiple MPI [27] processes, increasing GPU utilization. The GPU scheduler does not support concurrent execution of kernels from different applications; each application is given a time slice to access the GPU and submit jobs.

The MPS design allows multiple applications to transparently share the GPU via a server daemon process and bypasses the time sliced scheduling limit. However, MPS is not supported on Tegra system-on-chips (SoCs) which is used by on the Jetson Nano.
Since existing software solutions do not cater to edge GPUs like the Jetson Nano, the feasibility of driver-level virtualization is examined next. This is promising because although spatial multiplexing is not possible at the SM-level, it may be possible at the core level; for reference, the Jetson Nano has 128 cores in its single SM. In 2022, NVIDIA open sourced their GPU drivers [28], starting with the R515 driver. However, these drivers are compatible with NVIDIA core architectures starting from Turing, and do not support the Jetson Nano which has its own drivers that come pre-installed with the NVIDIA JetPack toolkit [29]. Therefore, driver-level modifications are not possible.

## 3.3 Kernel Slicing

The absence of hardware and software support for virtualization on the Jetson Nano leads to the examination of solutions that require developer intervention. One such method is *kernel slicing* [30] which breaks a user kernel into small pieces and co-schedules slices from different kernels. Kernel slicing can be performed at granularity of threads (warps) or thread blocks. Since different warps within the same thread block might have data dependencies (through shared memory), slicing is typically done at the thread block level. Kernel slicing can potentially improve GPU utilization by offering fine-grained scheduling opportunities to the GPU kernel; a smaller application arriving after a larger application does not need to wait for the larger application to finish execution which can be preempted after executing a fraction of all its thread blocks. 3.1 illustrates the potential performance benefits due to kernel slicing on a GPU with a simple SM. Due to kernel slicing, the original block indices are not valid and *index rectification* must be performed. Index rectification is illustrated for a matrix addition kernel in the a for a slice size of $4 \times 1$. [30] implemented index rectification without any user intervention; PTX code is directly used to modify the kernel for slicing support. For simplicity, we give the responsibility of kernel slicing to the user who must add an additional argument to support indexing into the slice set. Slices are launched in a loop with `blockOffset` updated every time a slice is launched. To evaluate the performance of kernel slicing, we use the SGEMM [6] and MRI-Q [7] kernels, part of the Parboil benchmark [8]. One kernel of each type—SGEMM and MRI-Q—was launched for varying slice size configurations (keeping the number of threads constant) and total execution time was measured using CUDA events.

### 3.3.1 Multithreading Performance

To evaluate the performance of kernel slicing in a multithreaded environment, all CUDA operations (kernel launches and their associated memory operations) were performed in a dedicated stream, on a dedicated CPU thread. Four applications were launched: two SGEMM and two

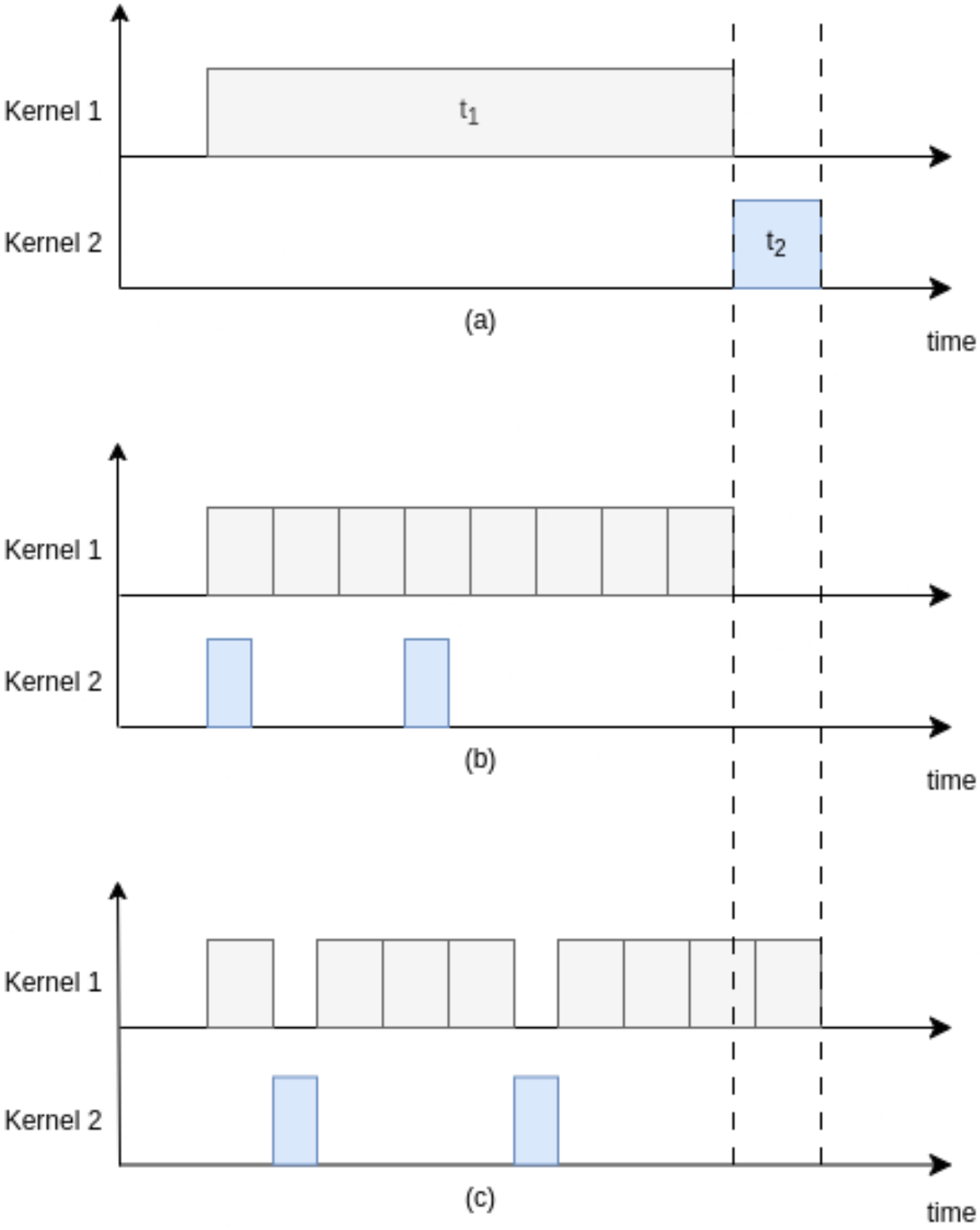


Figure 3.1: Gains due to kernel slicing. In (a), the sequential execution of kernels on the GPU creates a bottleneck, with kernel 2 waiting for kernel 1 to finish. Pre-Pascal architectures lack the ability to evict a GPU kernel mid-instruction, and even if available, the associated state-saving overhead is impractical [4]. Co-scheduling is infeasible when the GPU lacks the necessary resources. (b) shows how kernel slicing can enable co-scheduling and reduce overall execution time with carefully choosing slice sizes. Even if co-scheduling might not be possible, (c) illustrates how kernel slicing supports efficient preemption, eliminating the need to save/restore state.

MRI-Q, concurrently and the total execution time for different slice size configurations, run on the GeForce GTX 1650 Ti with Max-Q Design, is given below.

| SGEMM \ MRI-Q | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 |
|---|---|---|---|---|---|---|---|---|---|
| (8,66) | 52.83 | 51.38 | 52.31 | 53.99 | 53.87 | 57.38 | 72.46 | 107.1 | 161.8 |
| (4,66) | 50.46 | 53.39 | 52.41 | 52.50 | 55.93 | 56.42 | 75.00 | 113.6 | 156.6 |
| (2,66) | 52.28 | 52.67 | 55.61 | 55.59 | 55.68 | 56.51 | 73.59 | 109.5 | 139.7 |
| (1,66) | 53.94 | 52.25 | 53.79 | 52.57 | 55.33 | 58.94 | 72.77 | 101.1 | 141.7 |
| (8,33) | 54.49 | 54.26 | 55.82 | 55.26 | 56.46 | 59.69 | 77.48 | 126.2 | 140.2 |
| (4,33) | 55.88 | 51.49 | 56.04 | 53.86 | 54.17 | 59.72 | 74.37 | 110.5 | 160.1 |
| (2,33) | 53.69 | 53.82 | 54.10 | 56.11 | 53.36 | 56.35 | 73.65 | 98.4 | 127.3 |
| (1,33) | 54.47 | 56.39 | 55.39 | 53.99 | 56.97 | 58.53 | 79.08 | 97.1 | 148.9 |
| (8,22) | 50.83 | 53.87 | 54.26 | 55.71 | 56.16 | 57.65 | 75.38 | 107.4 | 140.1 |
| (2,11) | 53.75 | 54.22 | 55.64 | 56.33 | 55.46 | 57.97 | 75.17 | 112.8 | 151.6 |
| (1,11) | 58.90 | 55.90 | 57.85 | 60.99 | 59.91 | 63.60 | 74.83 | 91.6 | 139.9 |

Table 3.4: Total execution time (in ms) for different slice size configurations in a multithreaded setting with OS thread scheduling for four kernels, two SGEMM and two MRI-Q instances

To establish a baseline, execution times were also measured for CUDA operations on a single thread, with and without streams. With a single CPU thread launching all CUDA operations on a single stream, the total execution time was 64.23ms. With a single CPU thread launching CUDA operations for each kernel on dedicated streams, the total execution time was 63.79ms. The top left entry in table 3.4 with SGEMM sliced grid size, $(8, 66)$ and MRI-Q sliced grid size, 1024 reports execution time without slicing. Timings were reported after running the application 5 times and averaging. A separate scheduler to determine the kernel order launch was not used and we relied on the OS' thread scheduling logic. No significant performance improvement was observed due to kernel slicing. However, the performance degrades significantly with smaller slice sizes because of the additional overhead incurred due to launching a large number of kernels. Due to the non-deterministic nature of multithreaded applications, it is difficult to achieve differentiated GPU provisioning in this manner without using synchronization primitives. To avoid using synchronization primitives, we make the design choice of launching kernels from a single CPU thread. The kernel launch order may be determined by a scheduler, and support for implementing custom scheduling logic in the middleware is described later.

### 3.3.2 Single-threaded Performance

We also studied the effects of kernel slicing where all CUDA operations are performed on a single thread. To isolate the effects the kernel slicing, only the memory transfer and kernel launch times are measured (memory allocation times are ignored). All host-to-device memory transfers for different kernels are batched together and executed before the kernel launch event loop. A round-robin scheduler is used to launch slices of each kernel in an alternating fashion following which the device-to-host memory transfers are completed. Execution times for different slice

size configurations, run on the Jetson Nano, are given below.

| SGEMM \ MRI-Q | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 |
|---|---|---|---|---|---|---|---|---|---|
| (8,66) | 294.0 | 293.8 | 294.1 | 293.7 | 293.3 | 294.6 | 297.8 | 294.8 | 294.1 |
| (4,66) | 294.5 | 294.8 | 294.0 | 293.8 | 293.3 | 294.7 | 297.5 | 294.7 | 293.9 |
| (2,66) | 297.5 | 293.6 | 294.1 | 293.7 | 293.2 | 294.3 | 297.9 | 294.6 | 294.4 |
| (1,66) | 298.9 | 297.9 | 293.2 | 292.8 | 292.4 | 293.7 | 296.8 | 294.2 | 293.6 |
| (8,33) | 295.4 | 294.8 | 293.8 | 294.0 | 293.2 | 294.7 | 297.6 | 295.3 | 294.4 |
| (4,33) | 297.1 | 293.7 | 293.9 | 292.9 | 293.1 | 294.7 | 297.6 | 294.5 | 294.1 |
| (2,33) | 296.9 | 297.3 | 293.1 | 292.9 | 292.7 | 293.6 | 296.7 | 294.3 | 292.9 |
| (1,33) | 298.4 | 298.0 | 296.8 | 291.4 | 290.8 | 291.9 | 295.3 | 292.8 | 292.2 |
| (8,22) | 297.2 | 293.7 | 293.4 | 293.4 | 292.8 | 294.7 | 297.6 | 294.6 | 294.1 |
| (4,11) | 298.0 | 297.3 | 296.1 | 292.2 | 291.7 | 292.8 | 295.6 | 293.2 | 292.8 |
| (2,11) | 298.0 | 298.3 | 296.3 | 294.5 | 289.8 | 290.6 | 293.4 | 291.5 | 291.0 |
| (1,11) | 299.0 | 298.1 | 297.3 | 295.6 | 292.3 | 286.6 | 289.7 | 289.9 | 287.7 |
| (8,6) | 297.9 | 296.7 | 296.1 | 292.1 | 291.8 | 293.0 | 296.0 | 294.2 | 293.1 |
| (4,6) | 297.6 | 296.9 | 295.9 | 294.4 | 289.8 | 290.8 | 294.2 | 292.2 | 291.7 |

Table 3.5: Memory transfer+kernel slicing time (in ms) for different slice size configurations in a single thread setting with batched memory transfers and round-robin kernel launch scheduling for two kernels, one SGEMM and one MRI-Q instance

With a sliced size of 32 for MRI-Q and $(1, 11)$ for SGEMM (highlighted in table 3.5), kernel slicing shows a 3% improvement in performance. The memory transfer+kernel slicing times can be improved further by utilizing the GPU's concurrent copy and kernel execution mechanism. The scheduling loop can be modified to execute memory transfers in a round-robin fashion, instead of scheduling them completely before and after the kernel slice launches. With a sliced size of 32 for MRI-Q and $(2, 11)$ for SGEMM (highlighted in table 3.6), kernel slicing shows a 2% improvement in performance, which is lower than before. However, in general, the memory transfer+kernel slicing execution times reduced.
For the optimal slice size derived empirically above, we also measured the memory transfer+kernel slicing time with varying number of slices launched in each round-robin iteration.

## 3.4 Middleware Design

Now, we present the design of a multithreaded middleware, which simulates client orchestration at the thread level. API remoting is used; we present a set of custom API wrappers around CUDA operations that client applications can use within their code to interface with the kernel scheduler. The CUDA driver API is used instead of the CUDA runtime API although the simulator can easily be extended to work for the more familiar runtime API. The kernel scheduler runs as a separate CPU thread—similar to a daemon process—providing clients with indirect access to the underlying GPU. Each component of simulator is described in detail below.

| SGEMM \ MRI-Q | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 |
|---|---|---|---|---|---|---|---|---|---|
| (8,66) | 293.3 | 293.6 | 290.3 | 290.1 | 289.5 | 290.7 | 295.4 | 294.3 | 295.9 |
| (4,66) | 294.1 | 293.2 | 290.0 | 290.0 | 289.5 | 290.4 | 295.4 | 294.0 | 294.9 |
| (2,66) | 293.6 | 293.7 | 293.3 | 289.8 | 289.7 | 290.6 | 295.5 | 293.6 | 294.6 |
| (1,66) | 294.9 | 294.9 | 293.5 | 292.0 | 288.7 | 289.6 | 294.5 | 293.1 | 293.1 |
| (8,33) | 293.8 | 293.8 | 290.2 | 289.9 | 289.4 | 290.9 | 296.1 | 293.9 | 295.0 |
| (4,33) | 294.1 | 293.2 | 293.5 | 289.8 | 289.3 | 290.3 | 295.5 | 293.9 | 294.7 |
| (2,33) | 295.1 | 294.1 | 293.7 | 292.2 | 288.7 | 289.8 | 294.0 | 293.4 | 292.5 |
| (1,33) | 295.9 | 295.4 | 294.3 | 293.1 | 290.9 | 288.0 | 293.0 | 292.3 | 292.0 |
| (8,22) | 293.6 | 293.5 | 293.9 | 289.5 | 289.7 | 290.4 | 295.3 | 293.9 | 295.5 |
| (4,11) | 294.4 | 294.0 | 293.2 | 292.3 | 288.3 | 289.1 | 294.3 | 293.0 | 292.6 |
| (2,11) | 294.9 | 294.8 | 293.6 | 292.8 | 291.0 | 287.0 | 291.7 | 291.1 | 290.6 |
| (1,11) | 296.1 | 295.4 | 294.6 | 293.5 | 291.9 | 289.6 | 288.1 | 289.3 | 287.5 |
| (8,6) | 294.5 | 294.3 | 293.2 | 292.3 | 288.3 | 289.5 | 294.4 | 293.3 | 292.2 |
| (4,6) | 294.7 | 294.0 | 293.3 | 292.4 | 290.6 | 287.1 | 292.1 | 291.9 | 291.3 |

Table 3.6: Memory transfer+kernel slicing time (in ms) for different slice size configurations in a single thread setting with round-robin CUDA operations scheduling for two kernels, one SGEMM and one MRI-Q instance

| SGEMM \ MRI-Q | 1 | 2 | 4 | 8 | 16 | 32 |
|---|---|---|---|---|---|---|
| 1 | 286.6 | 291.7 | 293.1 | 293.7 | 293.8 | 293.9 |
| 2 | 287.0 | 286.8 | 291.2 | 292.6 | 292.8 | 292.8 |
| 4 | 291.3 | 287.0 | 287.3 | 290.7 | 291.0 | 291.1 |
| 8 | 292.2 | 287.3 | 287.2 | 290.1 | 290.6 | 290.5 |
| 16 | 292.5 | 286.9 | 287.0 | 287.1 | 290.1 | 290.0 |
| 24 | 293.0 | 286.8 | 286.8 | 287.2 | 290.4 | 290.4 |

Table 3.7: Memory transfer+kernel slicing time (in ms) for different number of slices launched in a single thread setting with round-robin CUDA operations scheduling for two kernels, one SGEMM and one MRI-Q instance

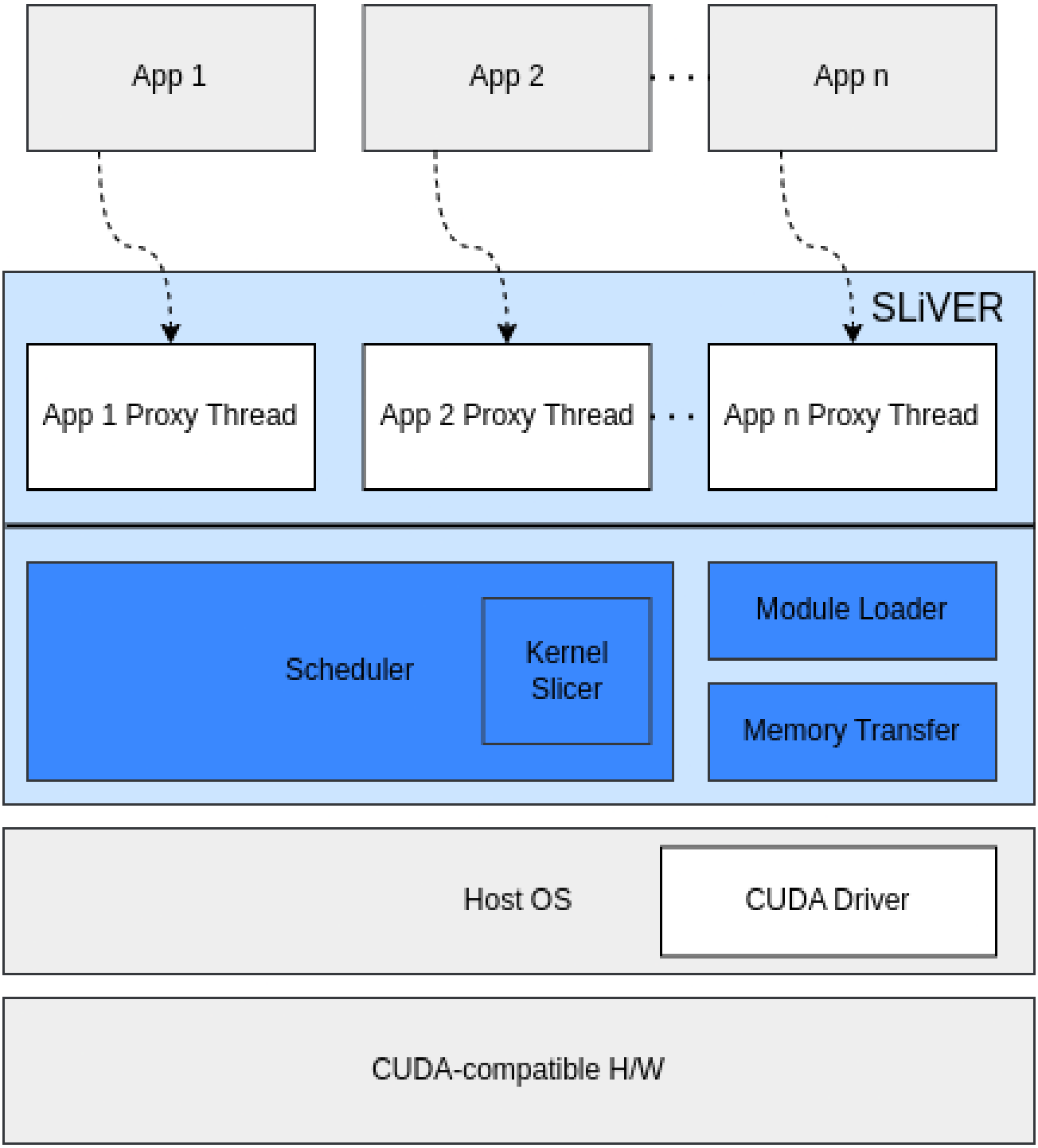


Figure 3.2: Logical design of SliVER. Applications are abstracted as threads that make CUDA calls using the driver API. The core logic of SliVER includes: a module loader to load kernels at runtime, memory transfer APIs, and a scheduler implementing kernel slicing. Any attempt to launch a kernel in the application is intercepted by the scheduler, which schedules the launch, and returns the result back to the thread proxy.

### 3.4.1 Kernel

Each CUDA kernel is represented as a virtual class, `Kernel`. `Kernel` has a single member, `void *args[16]` to store arguments passed to the kernel. The first three arguments are in the array are reserved for block offsets to support kernel slicing. The user is expected to derive from `Kernel` and populate the following pure virtual functions,

- `void memAlloc()`: All host and device memory allocations must performed inside this function.
- `void memcpyHtoD(const CUstream &stream)`: host-to-device memory transfers must be performed inside this function. A `CUstream` object is provided because the user is expected to use asynchronous APIs like `cuMemcpyAsyncHtoD` to take advantage of concurrent kernel execution capabilities in the GPU.
- `void memcpyDtoH(const CUstream &stream)`: device-to-host memory transfers must be performed inside this function. A `CUstream` object is provided because the user is expected to use asynchronous APIs like `cuMemcpyAsyncDtoH` to take advantage of concurrent kernel execution capabilities in the GPU.
- `void memFree()`: All host and device memory free operations must be performed inside this function.

The user is also expected to implement a function, `getKernelConfig` that returns the thread and block configurations of the kernel. The appendix contains an illustration of the same using the matrix addition kernel.

### 3.4.2 Kernel Wrapper

The class, `KernelWrapper` provides the interface between `Kernel` and the scheduler class, `Scheduler`. Each `Kernel` object has a corresponding `KernelWrapper` object. `KernelWrapper` is multi-threaded; the application thread is launched inside the `void launch()` function. The user is expected to compile his/her kernel into PTX code, which is used to load the kernel inside `launch()`.

```
class KernelWrapper
{
public:
    KernelWrapper(Scheduler *scheduler,
                  CUcontext &context,
                  const std::string &moduleFile,
                  const std::string &kernelName,
                  kernel_attr_t *attr,
                  Kernel *kernel) : scheduler(scheduler),
```

```
                                context(context),
                                moduleFile(moduleFile),
                                kernelName(kernelName),
                                attr(attr),
                                kernel(kernel)
    {
        // populate block offset

        // initialize kernel control block
    }

    void launch()
    {
        pthread_create(&thread, NULL, threadFunction, this);
    }

    void finish()
    {
        pthread_join(thread, NULL);
        kernel_control_block_destroy(&(attr->kcb));
    }

private:
    CUcontext context;
    pthread_t thread;
    std::string moduleFile;
    std::string kernelName;
    CUmodule module;

    kernel_attr_t *attr;

    Kernel *kernel;
    Scheduler *scheduler;

    void *threadFunction()
    {
        // set CUDA context and load kernel

        // kernel launch setup
        kernel->memAlloc();
```

```
        kernel->memcpyHtoD(attr->stream);
        set_state(&(attr->kcb), MEMCPYHTOD);

        // scheduler intercepts kernel launch
        scheduler->scheduleKernel(this->attr);

        // application can continue executing

        // wait for scheduler to complete executing kernel
        pthread_mutex_lock(&(attr->kcb.kernel_lock));
        while (attr->kcb.state != MEMCPYDTOH)
        {
            pthread_cond_wait(&(attr->kcb.kernel_signal),
                              &(attr->kcb.kernel_lock));
        }
        pthread_mutex_unlock(&(attr->kcb.kernel_lock));

        // wrap up
        kernel->memcpyDtoH(attr->stream);
        kernel->memFree();
    }

    static void *threadFunction(void *args)
    {
        KernelWrapper *kernelWrapper = static_cast<KernelWrapper *>(args);
        return kernelWrapper->threadFunction();
    }
};
```

The `KernelWrapper` constructor is passed a pointer to the **Scheduler** object, a CUDA context for executing the kernel, the path to the kernel module (as a PTX), and the name of the kernel. `threadFunction()` has been *thunked* to allow `pthread` to launch the function through a static function. Since the kernel name must be used while calling `cuModuleGetFunction()` in `threadFunction`, we recommend prepending `extern "C"` to the function prototype to avoid name mangling in `C++`. The sequence of steps followed to execute the CUDA kernel remains identical: memory allocation, host-to-device memory transfer, kernel launch, device-to-host memory transfer, and memory freeing, except memory operations are done in the application thread while the kernel launch happens in the scheduler thread. Execution on the application thread is non-blocking and can continue until the kernel finishes executing.

### 3.4.3 Kernel Attributes and Control Block

The `kernel_control_block` structure stores configuration information necessary for implementing kernel slicing. It also stores the state of the user application during execution; the application can be in one of four states: `INIT`, `MEMCPYHTOD`, `LAUNCH`, and `MEMCPYDTOH` stored in an enum, `kstate`. `kernel_control_block_t` also includes `pthread` primitives like `pthread_mutex_t` and `pthread_cond_t` for synchronization between the application and scheduler thread and to update attributes in a thread-safe manner.

The `kernel_attr` structure is a wrapper for kernel configuration used by the `Scheduler` object to launch kernels. `Scheduler` also assigns a unique identifier to `KernelWrapper` which is stored in `kernel_attr->id`. `kernel_attr` also includes a `CUfunction` object containing the kernel to be executed along with the `CUstream` it must be executed in. A niceness value is also included which can be used for priority scheduling.

```
typedef struct kernel_attr
{
    unsigned int id;
    CUfunction function;

    unsigned int gridDimX;
    unsigned int gridDimY;
    unsigned int gridDimZ;

    unsigned int blockDimX;
    unsigned int blockDimY;
    unsigned int blockDimZ;

    unsigned int sGridDimX;
    unsigned int sGridDimY;
    unsigned int sGridDimZ;

    unsigned int blockOffsetX = 0;
    unsigned int blockOffsetY = 0;
    unsigned int blockOffsetZ = 0;

    unsigned int sharedMemBytes;
    CUstream stream;
    void **kernelParams;

    kernel_control_block_t kcb;
```

```
    unsigned int niceness = 0;
} kernel_attr_t;
```

### 3.4.4 Scheduler

The core scheduling logic of the simulator is implemented in a virtual class called `Scheduler`. Developers must derive from `Scheduler` and override certain virtual member functions depending on the scheduling logic to be tested. `Scheduler` exposes a common API to launch kernels irrespective of the scheduling logic and only requires a pointer to the `kernel_attr` structure. Member functions of the class are described below in brief.

- `virtual void scheduleKernel(kernel_attr_t *)`: The function must be implemented by the derived class depending on the scheduling logic. Every scheduler maintains a list of kernels to-be launched in a data structure. This method must handle insertions into the list of active kernels in a thread-safe manner.
- `void launchKernel(kernel_attr_t *)`: One of the active kernels is selected according to some scheduling decision and launched on the GPU through this method depending on the number of slices defined. This method also performs index rectification for the kernel and updates the corresponding `kernel_attr` structure.
- `void run()`: The `Scheduler` object runs in a dedicated CPU thread and `run()` launches this thread. Similar to the `Kernel` class, `threadFunction()` is thunked.

Foe example, the implementation of a first-come first-serve scheduler is given in the appendix.

# Chapter 4

# Conclusion and Future Work

We discussed existing GPU virtualization solutions in the context of high-end GPUs and explained why they cannot be extended to resource-constrained GPUs due to their lack of hardware support. We demonstrated the potential of kernel slicing to improve memory transfer+kernel launch times on the co-scheduling of SGEMM and MRI-Q kernels in the Parboil benchmark. We presented the design of a software middleware framework, SliVER that successfully time multiplexes multiple clients abstracted as threads.

Although we were able to show improvements due to kernel slicing, more extensive benchmarking is necessary to study the slice size-execution time trade-off in detail. The design of SliVER requires benchmarking as well, especially the overhead introduced due to the middleware. In this work, the kernel launch decision does not take into consideration the nature of kernels being scheduled and the possibility of application-specific schedulers must be investigated. Additionally, we have presented the design of a generic middleware that does not take advantage of some characteristic features of edge GPUs including a shared address space. Finally, the design of SliVER can potentially be extended to solve the original problem of efficiently time-multiplexing multiple client processes by bypassing the inherent time sharing across different CUDA contexts.

# Chapter 5

# Appendix

## 5.1 Index Rectification

```
// kernel accepts an additional argument to index within set of slices
__global__ void matrixAdd(float *a, float *b, float *c, int width,
                          dim3 blockOffset)
{
    // correct indices using blockOffset
    int i = (blockIdx.x + blockOffset.x) * blockDim.x + threadIdx.x;
    int j = (blockIdx.y + blockOffset.y) * blockDim.y + threadIdx.y;
    if (i < width && j < width)
        c[i * width + j] = a[i * width + j] + b[i * width + j];
}

int main()
{
    ...
    dim3 sGridConf(4,1); // size of kernel slice
    dim3 blockOffset(0,0);
    while (blockOffset.x < gridConf.x && blockOffset.y < gridConf.y)
    {
        matrixAdd<<<sGridConf, blockConf>>>(a, b, c, width, blockOffset);
        blockOffset.x += sGridConf.x;
        while (blockoffset.x >= gridConf.x)
        {
            blockOffset.x -= gridConf.x;
            blockOffset.y += sGridConf.y;
        }
    }
```

```
    ...
}
```

## 5.2 SliVER Entity Relation

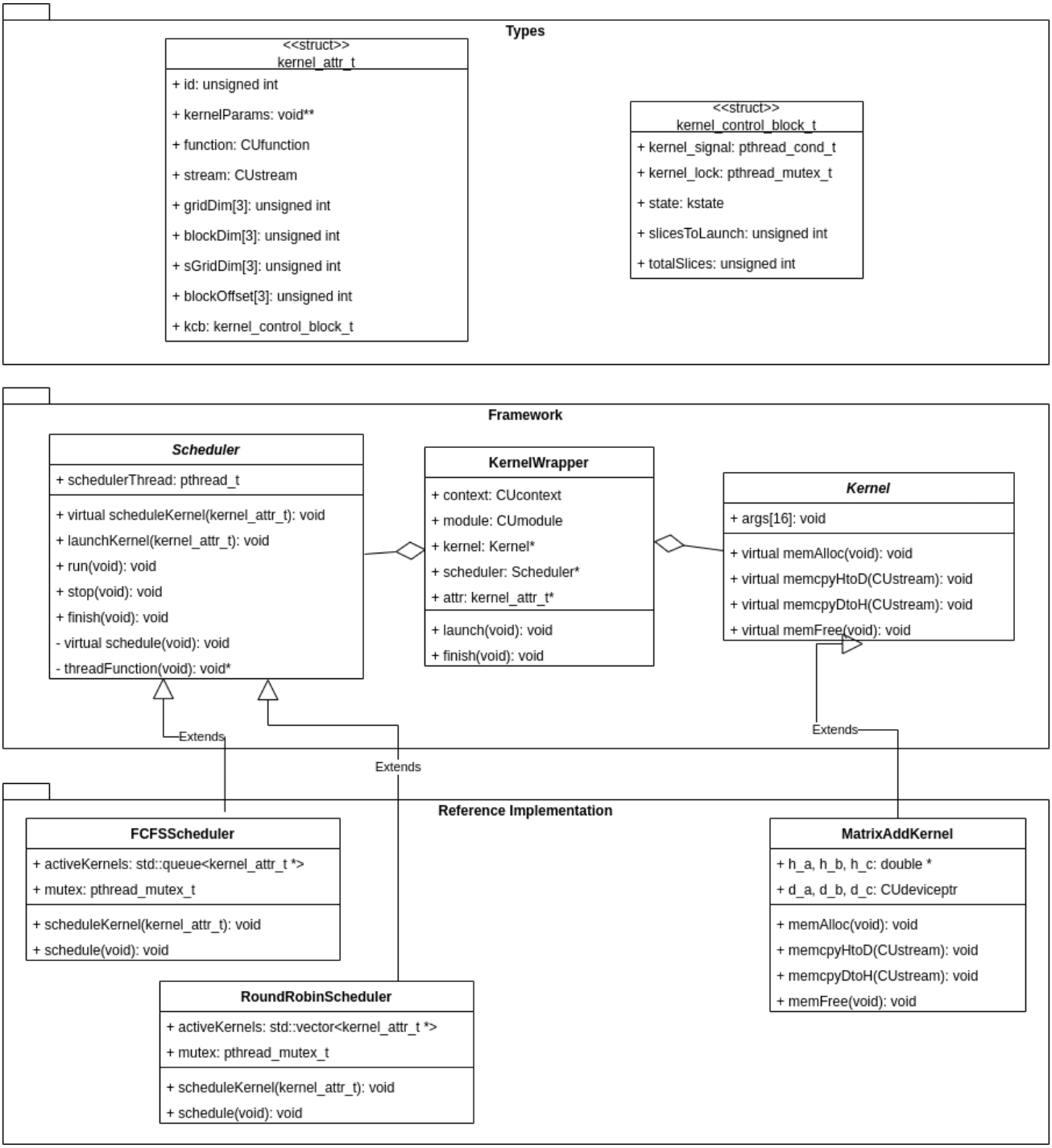


Figure 5.1: Entity Relation for SliVER

## 5.3 Matrix Addition Kernel

```
class MatrixAddKernel : public Kernel
{
public:
    void memAlloc();
    void memcpyHtoD(const CUstream &stream);
    void memcpyDtoH(const CUstream &stream);
    void memFree();

    void getKernelConfig(unsigned int &gridDimX,
                         unsigned int &gridDimY,
                         unsigned int &gridDimZ,
                         unsigned int &blockDimX,
                         unsigned int &blockDimY,
                         unsigned int &blockDimZ)
    {
        gridDimX = N;
        gridDimY = 1;
        gridDimZ = 1;

        blockDimX = 1;
        blockDimY = 1;
        blockDimZ = 1;
    }

private:
    double *h_a, *h_b, *h_c;
    CUdeviceptr d_a, d_b, d_c;
};

void MatrixAddKernel::memAlloc()
{
    // host memory allocation
    h_a = (double *)malloc(N * sizeof(double));
    h_b = (double *)malloc(N * sizeof(double));
    h_c = (double *)malloc(N * sizeof(double));

    // device memory allocation
    cuMemAlloc(&d_a, N * sizeof(double));
```

```
    cuMemAlloc(&d_b, N * sizeof(double));
    cuMemAlloc(&d_c, N * sizeof(double));

    // arguments to kernel
    args[3] = &d_a;
    args[4] = &d_b;
    args[5] = &d_c;
}

void MatrixAddKernel::memcpyHtoD(const CUstream &stream)
{
    // copy h_a and h_b to device
    cuMemcpyHtoDAsync(d_a, h_a, N * sizeof(double), stream);
    cuMemcpyHtoDAsync(d_b, h_b, N * sizeof(double), stream);
}

void MatrixAddKernel::memcpyDtoH(const CUstream &stream)
{
    // copy d_c to host
    cuMemcpyDtoHAsync(h_c, d_c, N * sizeof(double), stream);
}

void MatrixAddKernel::memFree()
{
    // free device memory
    cuMemFree(d_a);
    cuMemFree(d_b);
    cuMemFree(d_c);

    // free host memory
    free(h_a);
    free(h_b);
    free(h_c);
}
```

## 5.4 First-Come First-Serve Scheduler

```
class FCFSScheduler : public Scheduler
{
```

```
public:
    FCFSScheduler() { pthread_mutex_init(&mutex, NULL); }
    ~FCFSScheduler() { pthread_mutex_destroy(&mutex); }

    void scheduleKernel(kernel_attr_t *kernel);

private:
    std::queue<kernel_attr_t *> activeKernels;
    pthread_mutex_t mutex;

    void schedule();
};

void FCFSScheduler::scheduleKernel(kernel_attr_t *kernel)
{
    // assign id to kernel and update state to LAUNCH

    // enqueue kernel
    pthread_mutex_lock(&mutex);
    activeKernels.push(kernel);
    pthread_mutex_unlock(&mutex);
}

// wrapper around launchKernel
void FCFSScheduler::schedule()
{
    if (activeKernels.size() == 0)
    { // nothing to do? yield the CPU
        usleep(1);
    }
    else
    {
        activeKernels.front()->kcb.slicesToLaunch = 2;
        launchKernel(activeKernels.front());
        if (activeKernels.front()->kcb.totalSlices == 0)
        { // all slices done? dequeue
            set_state(&(activeKernels.front()->kcb), MEMCPYDTOH, true);
            pthread_mutex_lock(&mutex);
            activeKernels.pop();
            pthread_mutex_unlock(&mutex);
```

```
            }
        }
    }
```

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