**Part 1: Knowledge Base (5 points)**

1. List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions.

- **Multiple streams**: to replicate the initial portions of the pipeline and allow the pipeline to fetch both instructions, making use of two streams.  
  
- **Prefetch branch target**: When a conditional branch is recognized, the target of the branch is prefetched, in addition to the instruction following the branch. This target is then saved until the branch instruction is executed. If the branch is taken, the target has already been prefetched.  
  
- **Loop buffer**: A loop buffer is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions, in sequence.  
  
- **Branch prediction**: A prediction is made whether a conditional branch will be taken when executed, and subsequent instructions are fetched accordingly.  
  
- **Delayed branch**: It is possible to improve pipeline performance by automatically rearranging instructions within a program, so that branch instructions occur later than actually desired.

1. What are some typical characteristics of a RISC instruction set architecture?

* One instruction per cycle. Register-to-register operations. Simple addressing modes. Simple instruction formats.

1. Briefly define the following terms:

• True data dependency Can fetch and decode second instruction in parallel with first but can NOT execute second instruction until first is finished.

• Procedural dependency Can not execute instructions after a branch in parallel with instructions before a branch.  
• Resource conflicts Two or more instructions waiting for the same resource.  
• Output dependency Write after write (WAW).

• Antidependency Write after Read (WAR).

1. What is the purpose of an instruction window?

* Allows out-of-order issue to separate the decoding and execution stages.

**Part 2: Multiple Choice (5 points)**

1. \_\_\_\_\_\_\_\_\_\_ are bits set by the processor hardware as the result of operations.

A. MIPS B. Condition codes

C. Stacks D. PSWs

1. The \_\_\_\_\_\_\_\_\_ contains the address of an instruction to be fetched.

A. instruction register B. memory address register

C. memory buffer register D. program counter

1. The \_\_\_\_\_\_\_\_ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

1. \_\_\_\_\_\_\_\_\_ is a pipeline hazard.

A. Control B. Resource

C. Data D. All of the above

1. A \_\_\_\_\_\_\_\_ hazard occurs when there is a conflict in the access of an operand location.

A. resource B. data

C. structural D. control

1. A \_\_\_\_\_\_\_\_\_ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the *n* most recently fetched instructions in sequence.

A. loop buffer B. delayed branch

C. multiple stream D. branch prediction

1. The \_\_\_\_\_\_\_\_\_ is a small cache memory associated with the instruction fetch stage of the pipeline.

A. dynamic branch B. loop table

C. branch history table D. flag

1. The ARM architecture supports \_\_\_\_\_\_\_ execution modes.

A. 2 B. 8

C. 11 D. 7

1. \_\_\_\_\_\_\_\_\_ determines the control and pipeline organization.

A. Calculation B. Execution sequencing

C. Operations performed D. Operands used

1. \_\_\_\_\_\_\_\_\_ is the fastest available storage device.

A. Main memory B. Cache

C. Register storage D. HLL

1. A \_\_\_\_\_\_\_\_ instruction can be used to account for data and branch delays.

A. SUB B. NOOP

C. JUMP D. all of the above

1. A tactic similar to the delayed branch is the \_\_\_\_\_\_\_\_\_, which can be used on LOAD instructions.

A. delayed load B. delayed program

C. delayed slot D. delayed register

1. The MIPS R4000 uses \_\_\_\_\_\_\_\_ bits for all internal and external data paths and for addresses, registers, and the ALU.

A. 16 B. 32

C. 64 D. 128

1. All MIPS R series processor instructions are encoded in a single \_\_\_\_\_\_ word format.

A. 4-bit B. 8-bit

C. 16-bit D. 32-bit

1. A \_\_\_\_\_\_\_\_\_ architecture is one that makes use of more, and more fine-grained pipeline stages.

A. parallel B. superpipelined

C. superscalar D. hybrid

1. The R4000 can have as many as \_\_\_\_\_\_\_ instructions in the pipeline at the same time.

A. 8 B. 10

C. 5 D. 3

1. The superscalar approach can be used on \_\_\_\_\_\_ architecture.

A. RISC B. CISC

C. neither RISC nor CISC D. both RISC and CISC

1. The essence of the \_\_\_\_\_\_\_\_ approach is the ability to execute instructions independently and concurrently in different pipelines.

A. scalar B. branch

C. superscalar D. flow dependency

1. Which of the following is a fundamental limitation to parallelism with which the system must cope?

A. procedural dependency B. resource conflicts

C. antidependency D. all of the above

1. The situation where the second instruction needs data produced by the first instruction to execute is referred to as\_\_\_\_\_\_\_

A. true data dependency B. output dependency

C. procedural dependency D. antidependency

1. The instructions following a branch have a \_\_\_\_\_\_\_\_\_ on the branch and cannot be executed until the branch is executed.

A. resource dependency B. procedural dependency

C. output dependency D. true data dependency

1. \_\_\_\_\_\_\_\_ refers to the process of initiating instruction execution in the processor’s functional units.

A. Instruction issue B. In-order issue

C. Out-of-order issue D. Procedural issue

1. Instead of the first instruction producing a value that the second instruction uses, with \_\_\_\_\_\_\_\_\_\_\_ the second instruction destroys a value that the first instruction uses.

A. in-order issue B. resource conflict

C. antidependency D. out-of-order completion

1. \_\_\_\_\_\_\_\_\_\_ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.

A. Flow dependency B. Instruction-level parallelism

C. Machine parallelism D. Instruction issue

1. \_\_\_\_\_\_\_\_\_ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.

A. Machine parallelism B. Instruction-level parallelism

C. Output dependency D. Procedural dependency

1. Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?

A. duplication of resources B. out-of-order issue

C. renaming D. all of the above

1. SMPs, clusters, and NUMA systems fit into the \_\_\_\_\_\_\_\_ category of computer systems.

A. SISD B. MIMD

C. SIMD D. MISD

1. A \_\_\_\_\_\_\_\_\_ problem arises when multiple copies of the same data can exist in different caches simultaneously, and if processors are allowed to update their own copies freely, an inconsistent view of memory can result.

A. cache coherence B. cluster

C. failover D. failback

1. A \_\_\_\_\_\_\_\_\_\_ is an instance of a program running on a computer.

A. process B. process switch

C. thread D. thread switch

1. A \_\_\_\_\_\_\_\_ is a dispatchable unit of work within a process that includes a processor context and its own data area for a stack.

A. process B. process switch

C. thread D. thread switch