Final Project: The Register File

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ELECTRICAL & COMPUTER ENGINEERING

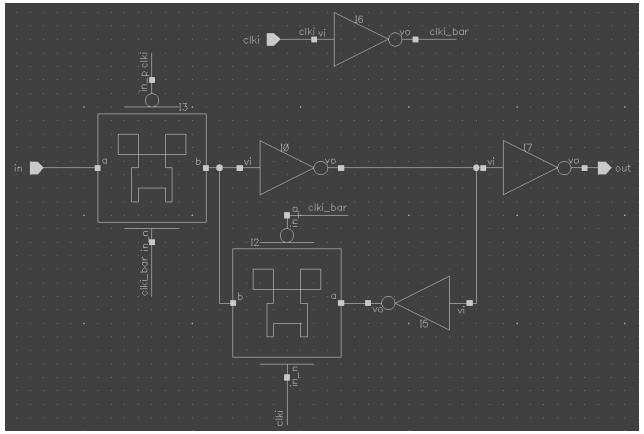
Work Distribution

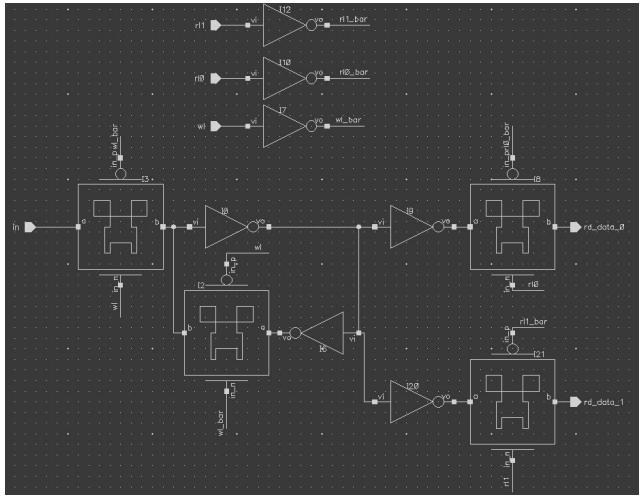
- **Denil**:
  - Write and Read decoder (2 variants) schematic and layout
  - Routing from decoder to master and slave latches
  - Top level layout with latched write decoder (scrapped)
- **Oliver**:
  - Write and Read decoder (2 variants) schematic and layout
  - Standard cell layout (AND2, NOR4, etc)
  - RF schematic
  - Latched Write decoder layout (scrapped)
- **Matthew**:
  - Slave latch redesign
  - Top-level layout
  - Some of vector testing for logical verification

Design Considerations

Three main components: decoder, bit cell array, read select

- **Decoder**:
  - **Build 4x13 decoder in one**
  - Build 2x4 decoder and scale up
- **Bit cell array**:
  - Use 16x13 DFFs
  - **Use 16x13 slave latches and 16x1 master latches at the top**
  - Use a new SRAM design
- **Read select**:
  - Use 13:1 muxes for each bit
  - **Use a tri-state inverter to disconnect un-read cells**



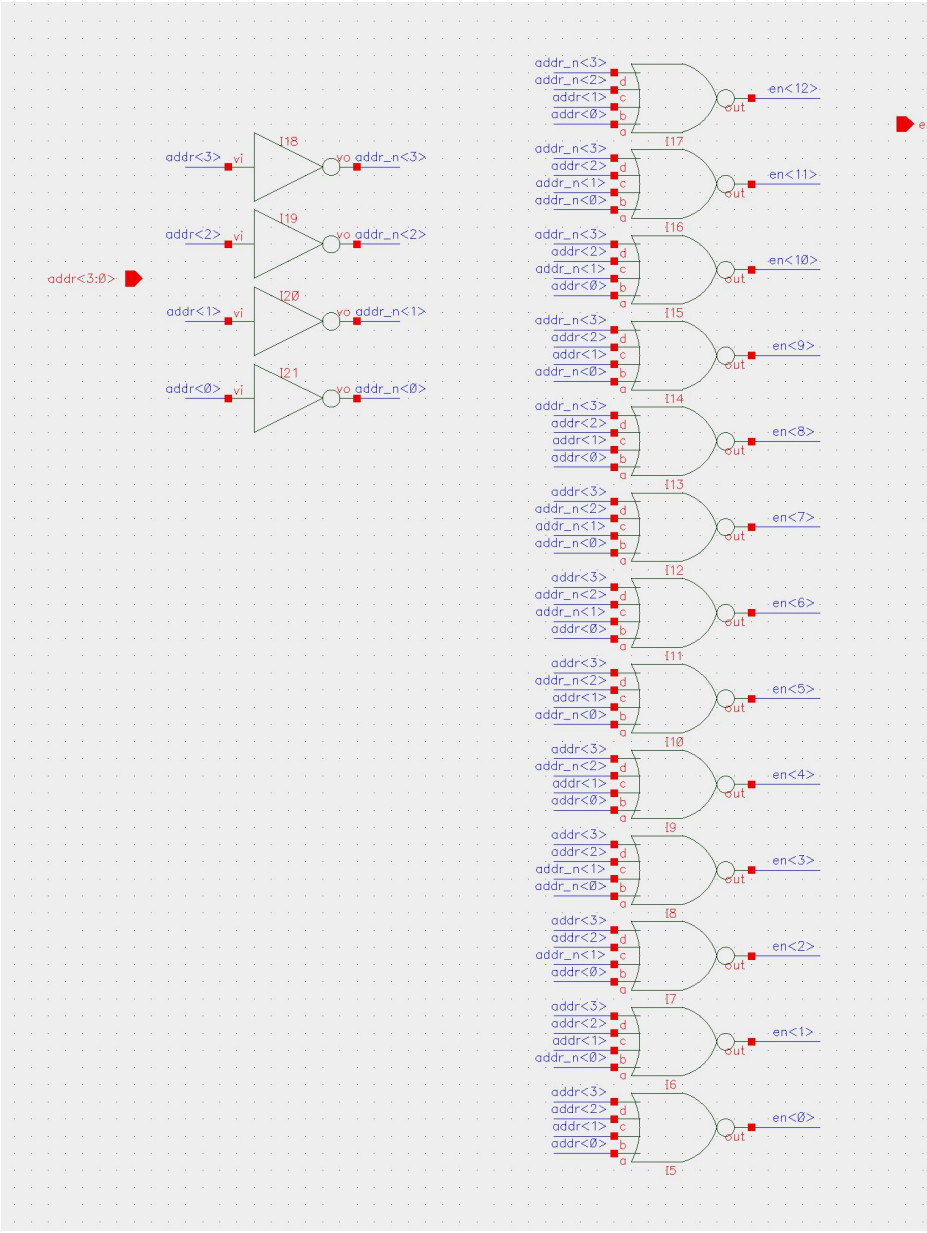


Key Architecture Details

- **Decoder**: built a 4x13 decoder in one
  - Used three decoders total (one for read_1, one for read_2, one for write)
  - The write decoder has AND gates attached to the output to AND the decoder enable signal with clk AND wr_en
- **Bit cell array**: used 16x13 slave latches with 16x1 master latches
  - More efficient (in energy and area) than full DFFs
- **Read select**: modified slave latch to include tri-state inverters
  - More efficient (in energy and area) than full muxes
  - Output is “shorted” in schematic, but by definition of the regfile’s function, only one cell can drive each output line at a time
  - Required redesign of slave latch but allowed for more compact design

Schematic - Decoder

- Bubble method enables using less inverters
- NOR4 is made of two NOR2s and one AND
- Write decoder built off read decoder
- Added AND gates for the write enable signal within the schematic to reduce LVS
- Created clock tree due to large fanout
- Write is synchronous (shown in later slides)



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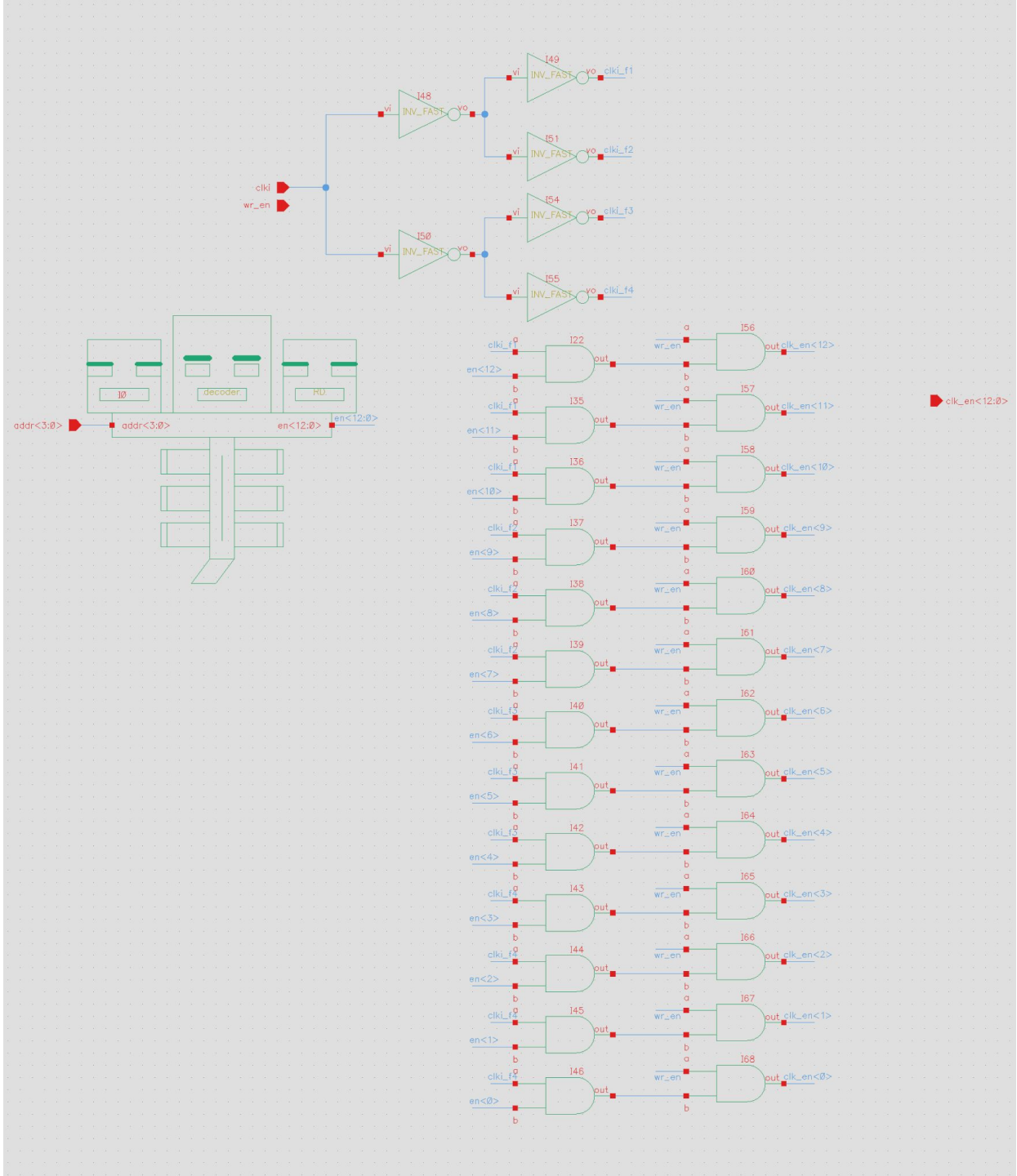
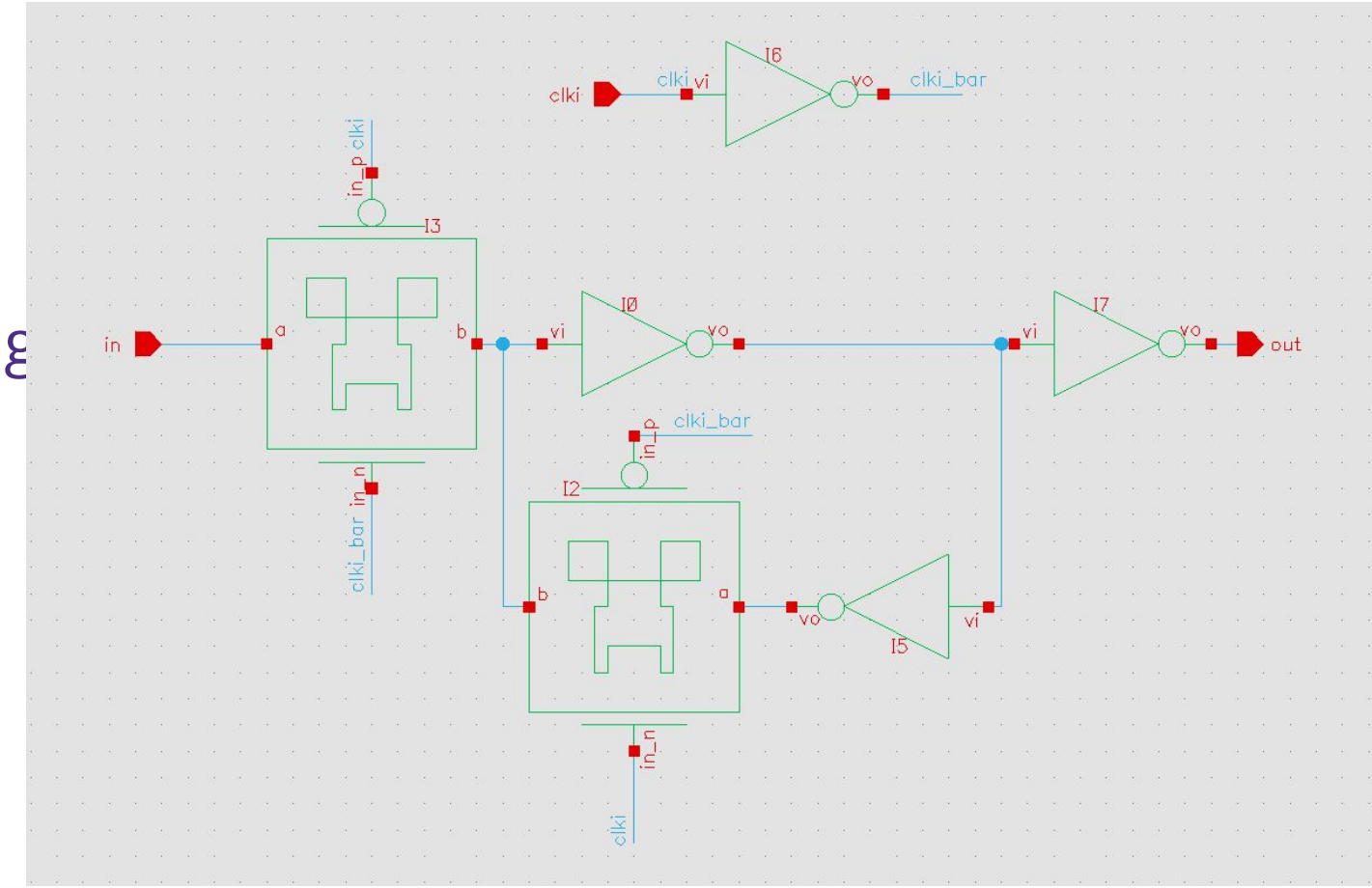
Write Decoder



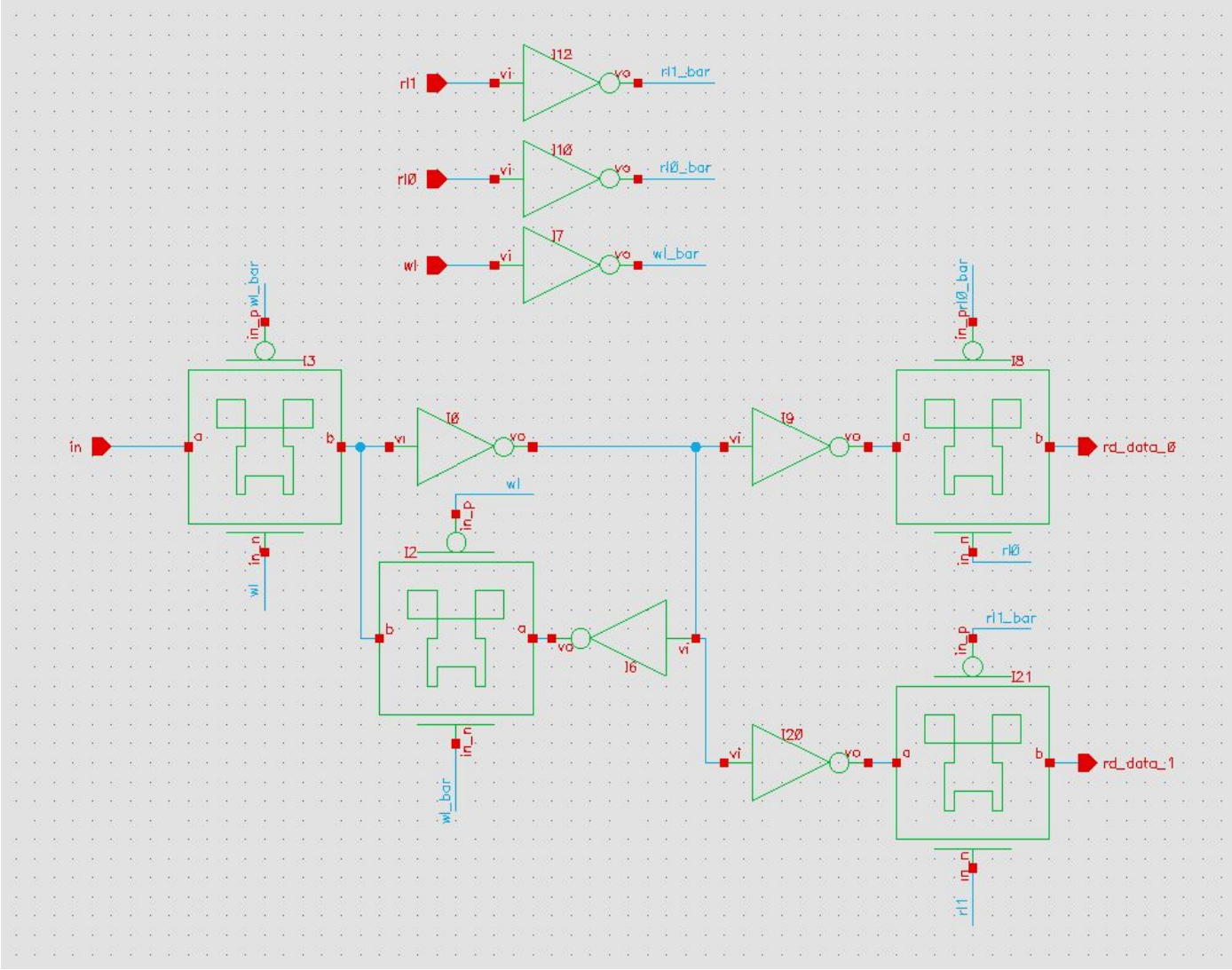
Schematic - Master Latch

- Reused from DFAR and replaced NAND/NOR with INV due to no reset
- Added inverter before the output to maintain polarity of signal going into slave latches

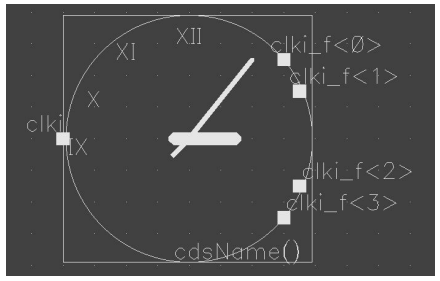


Schematic - Slave Latch

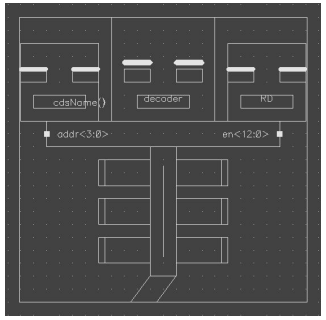
- Only when wl (write decoder, clk, and wren) is high does the memory update
- INV+TGATE on every output functions like a mux, to select only one line to read from (for each rd_data_0, rd_data_1)

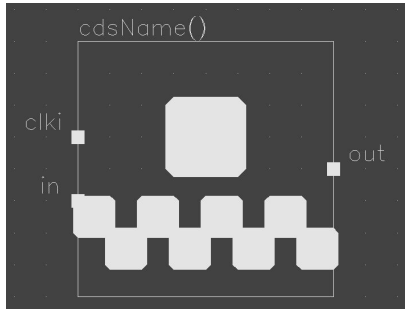


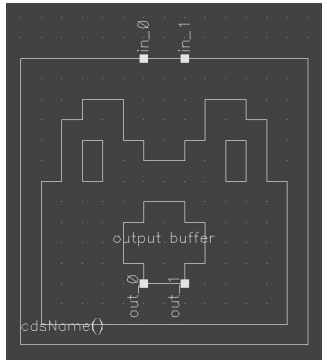
And now… the complete schematic

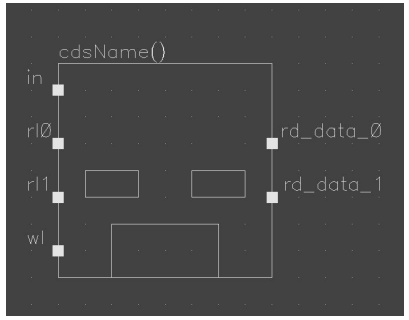


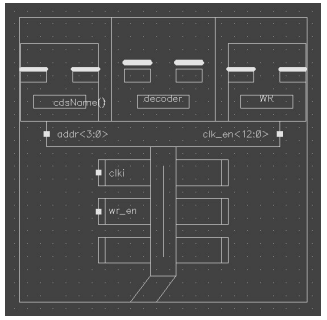
Please hold your applause until the end, no matter how impressed you are.









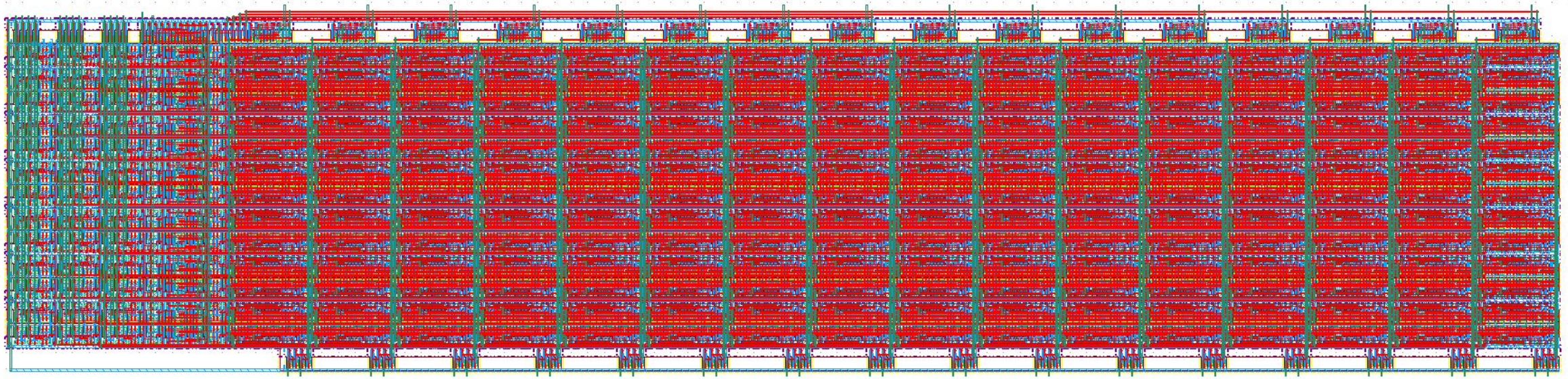


Schematic - Register File

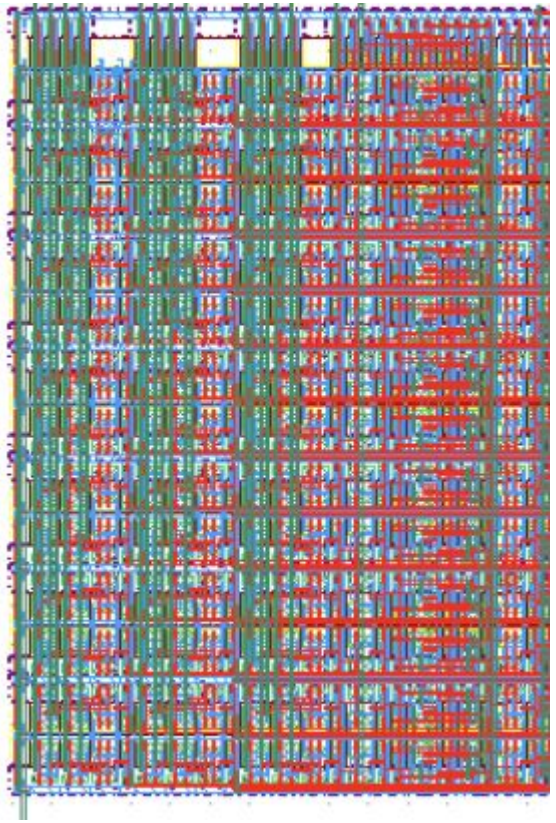
Layout

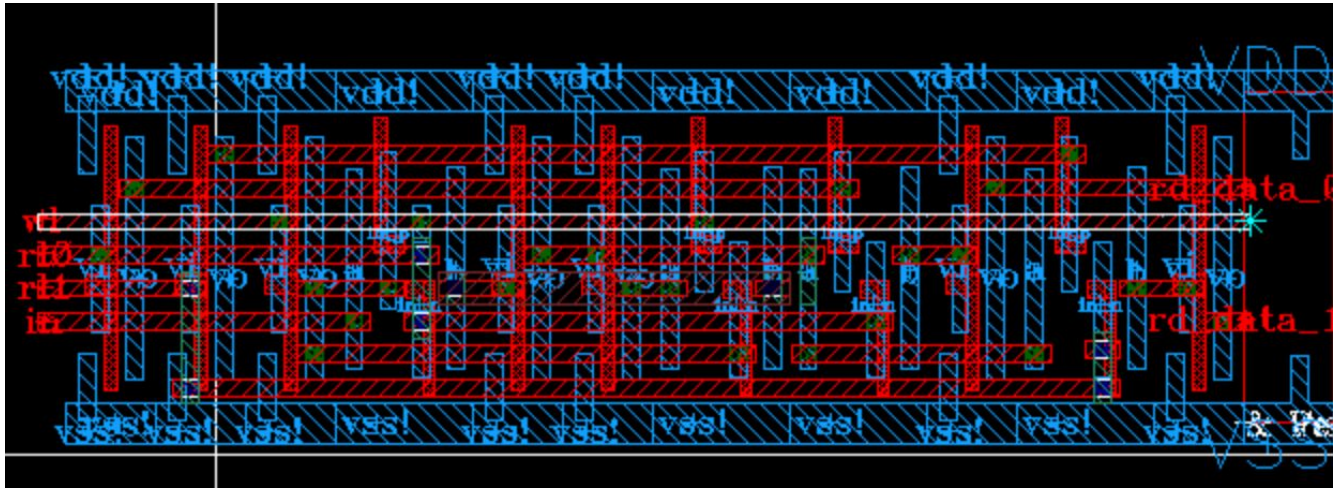
- Minimise usage of metals above metal 3
- Made decoder wires compact in the middle so that enable signals could be routed in VDD and VSS
- Ensured that cells were only 1.4 micrometers pitch to align with write decoder
- Designed slave latch to be used efficiently so that connecting adjacent slaves would be easier for routing

Layout



Layout





Design Specifications

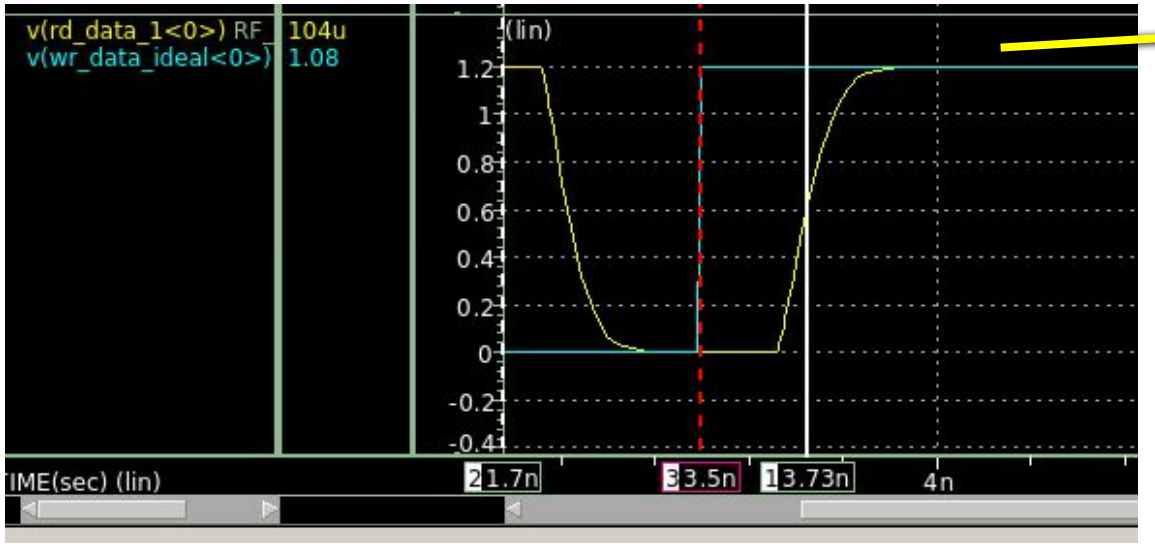
Schematic:

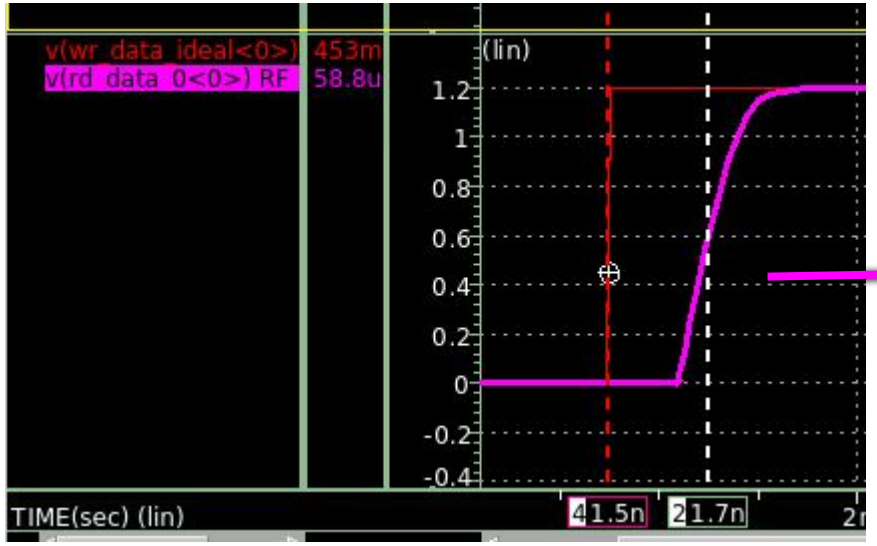
- Energy per read/write:
  Read: 1.29e-12
  Write: 8.33e-12

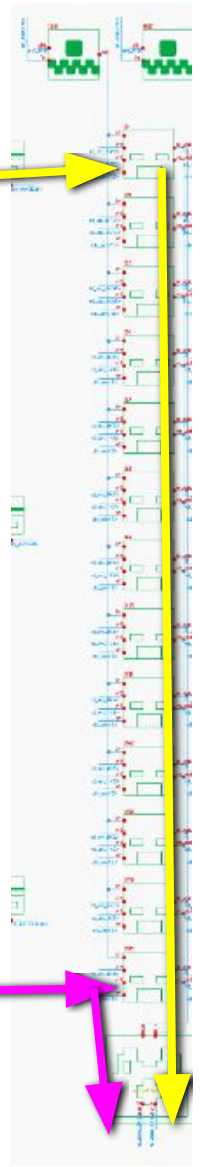
Layout:

- Energy per read/write:
  Read: 2.63e-12
  Write: 1.05e-11

Time Analysis: time to see data update
at read port top/bottom different addresses
(longest paths through write decoder)





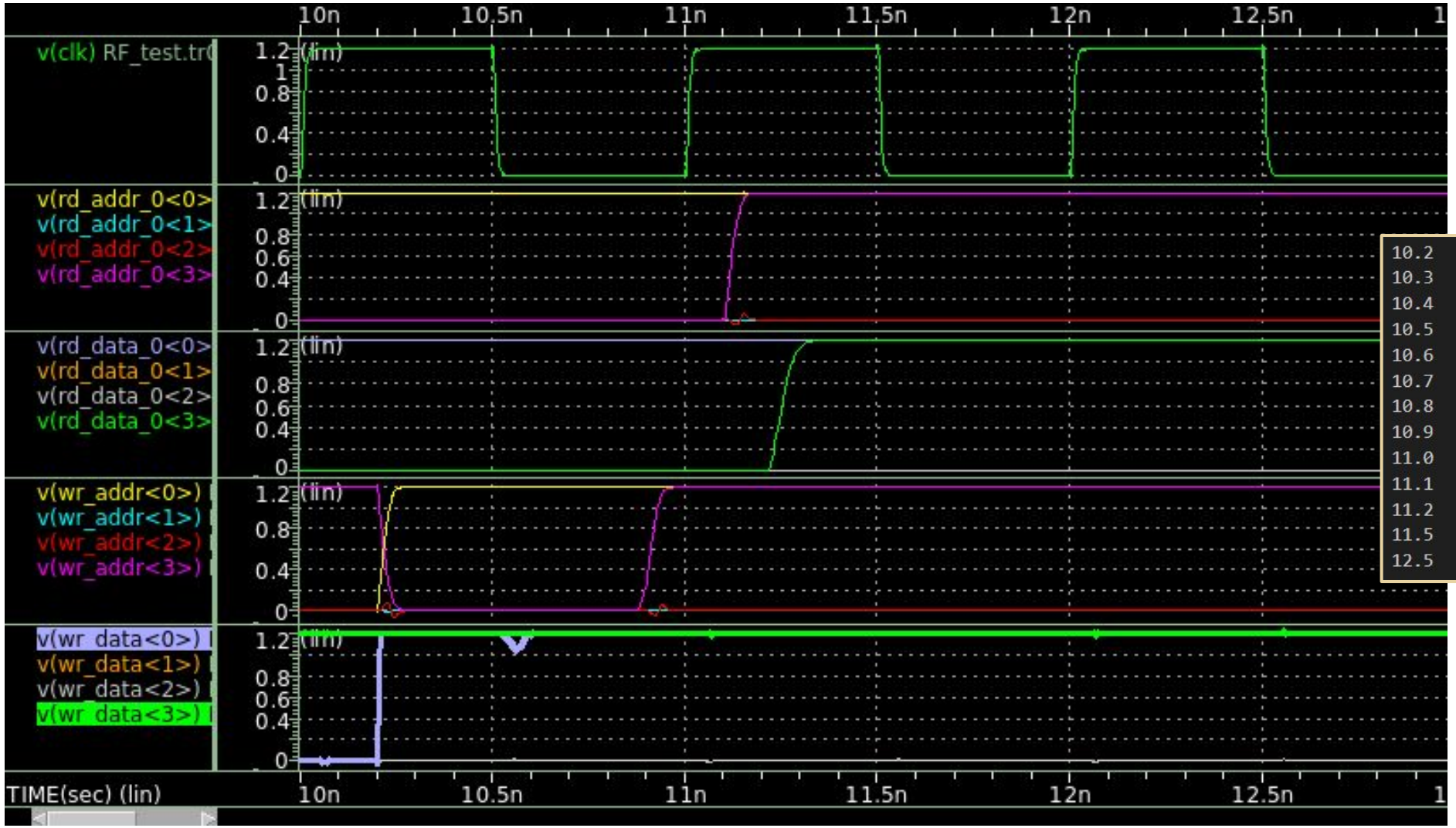


Waveform - Sync Write

Waveform- Sync Write

0.0	x x	x x	xxxx xxxx xxxx
0.5	1 0	1 1	0000 xxxx xxxx
1.5	1 1	1 1	0001 xxxx xxxx
2.5	1 2	1 1	0002 0001 0001
3.5	1 3	1 1	0003 0001 0001
4.5	1 4	1 1	0004 0001 0001

Waveform- Sync Write



10.2	1 1	1 1	0009	0001 xxxx
10.3	1 1	1 1	0009	0001 xxxx
10.4	1 1	1 1	0009	0001 xxxx
10.5	1 1	1 1	0009	0001 xxxx
10.6	1 1	1 1	0009	0001 xxxx
10.7	1 1	1 1	0009	0001 xxxx
10.8	1 1	1 1	0009	0001 xxxx
10.9	1 9	1 1	0009	0001 xxxx
11.0	1 9	1 1	0009	0001 xxxx
11.1	1 9	9 9	0009	0001 xxxx
11.2	1 9	9 9	0009	0001 xxxx
11.5	1 9	9 9	0009	0009 xxxx
12.5	1 9	9 9	0009	0009 xxxx

Waveform- Overall Read/Write

0.0	x	x	x	x	xxxx	xxxx	xxxx
1.5	1	0	0	0	0001	xxxx	xxxx
2.5	1	1	1	1	1111	0001	0001
3.5	1	2	2	2	2222	1111	1111
4.5	1	3	3	3	3333	2222	2222
5.5	1	4	4	4	4444	3333	3333
6.5	1	5	5	5	5555	4444	4444
7.5	1	6	6	6	6666	5555	5555
8.5	1	7	7	7	7777	6666	6666
9.5	1	8	8	8	8888	7777	7777
10.5	1	9	9	9	9999	8888	8888
11.5	1	A	A	A	AAAA	9999	9999
12.5	1	B	B	B	BBBB	AAAA	AAAA
13.5	1	C	C	C	CCCC	BBBB	BBBB
14.5	1	C	C	C	CCCC	CCCC	CCCC

Waveform- Read

1.5	1	0	0	0	0001	xxxx	xxxx
2.5	1	1	1	1	1111	0001	0001
3.5	1	2	2	2	2222	1111	1111
4.5	1	3	3	3	3333	2222	2222
5.5	1	4	4	4	4444	3333	3333
6.5	1	5	5	5	5555	4444	4444

Design Challenges

- Routing the signals in the slave latch was difficult since there were three enable signals (read 1, read 2, write)
- Tried to maintain only using metals 1-3 to avoid power dissipation
- The output of the decoders needed to be routed in the VDD and VSS regions and reconnected to the slave latches
- Read output was initially inverted, because we modified the slave latch output but did not add an offsetting inverter to the master latch

2-Minute Q&A