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MEng Hons Phase One Project Report HSP 2386

Prototype Design of a System on Chip for Visible Light Communication

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Original Mission Statement

MEng Project Mission Statement

Prototype Design of a System on Chip for Visible Light Communication

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Background

My project will be done with the PASTA project [1] in the University of Edinburgh School of Informatics. The PASTA project initially began as a research-project, addressing topics within compiler synthesis and microprocessor architecture, and through its research it has developed a family of customisable embedded processors, the EnCore family.

A developing technology within communication engineering is Optical Wireless, or Visible Light Communication. [2] This is being worked on by Professor Haas et al. within the school of Engineering at the University of Edinburgh.

One of the goals of the PASTA project is to build a custom system on chip, comprising of the EnCore processor, that will enable it to communicate with other devices that facilitate Optical Wireless Communication. My project will be to design the hardware that converts, buffers and scales the signals between the processor and the optical input and output.

Aims

The EnCore processors are able to communicate with external devices using the standard on-chip AXI protocol. The signal received from and sent to the optical input and output must therefore be converted to and from the AXI protocol. The hardware required to do this will be described in Verilog, and will initially be synthesised on a FPGA which will have the EnCore processor running on it. My project will be to design the AXI-converters which will

allow the processor to communicate with the outside world through optical wireless, with a possible scope for extension being to also create an AXI-converter allowing the processor to transmit and receive data over a network.

In order to do this there are a number of interim tasks I will have to carry out.

- Become familiar with the AXI protocol and how it is used as well as the Analogue To Digital, and Digital to Analogue converters that will be used to convert the optical signals.
- Gain an understanding of the need to buffer and up-sample or down-sample the optical signals.
- Program the AXI converters themselves.
- Attempt to optimise the hardware with regards to speed, die-area required, power consumed, etc.

The supervisor and student are satisfied that this project is suitable for performance and assessment in accordance with the guidelines of the course documentation.

Christian Leonard Quale	Björn Franke

Abstract

Visible Light Communication is a technology that has the potential to revolutionise the way in which data is transferred wirelessly. The PASTA group is a research-group carrying out research on methods which have the potential to revolutionise the way in which processors are customised. The work I will be carrying out for my thesis is with the aim of helping to fuse these two areas, creating an AXI converter in order to facilitate Visible Light Communication on PASTA's System on Chip. This report makes up Phase 1 of my thesis. A societal chapter is included, and it is concluded that the deployment of Visible Light Communication would have a positive societal impact. An introduction and history of Visible Light Communication and the PASTA project is given for context, as well as discussion on the practical work I will be carrying out, and what goals I aim to reach by the end.

I declare that this thesis is my original work except where stated.

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Christian Leonard Quale

Table of Contents

List of Acronyms

ADC	Analog to Digital Converter
AMC	Analog Monitoring and Control Circuit
DAC	Digital to Analog Converter
FSM	Finite State Machine
IEEE	Institute of Electrical and Electronics Engineers
LED	Light Emitting Diode
lm/W	Lumen per Watt
OFDM	Orthogonal Frequency-Division Multiplexing
QoS	Quality of Service
RAM	Random Access Memory
SNR	Signal to Noise Ratio
UOFDM	Unipolar Orthogonal Frequency-Division Multiplexing
VLC	Visible Light Communication
VLCC	Visible Light Communication Consortium
WLAN	Wireless Local Area Network

Chapter 1

Introduction

This is the report for Phase 1 of my thesis. Here I discuss what impact the research relating to my project could have on society as a whole, summarise the current state of the relevant research, and present some preliminary work. This chapter introduces the rest of the report.

1.1 Introduction

The work carried out in my thesis will revolve around the design of a Verilog module which is to be used for a very specific purpose. It will be a step on the way to realising a multi-processor System on Chip (SoC) that will be able to to send and receive data using Visible Light Communication (VLC).

This Phase 1 report serves three main purposes. The reader should get an overview of the potential impact the widespread use of Visible Light Communication could have on society. An important consideration when planning to carry out any significant Engineering task is to assess the effect it will have on society as a whole. Any potential downsides will have to be weighed up against the advantages, and an engineer should be confident that the work they are about to carry out will not have a net adverse effect on society.

Fortunately, in terms of the work I will be carrying out for my thesis, the societal case is an easy one to make. As the use of mobile data traffic is projected to increase dramatically over the next few years, and as public wireless internet hotspots become more common, urban environments will begin to experience that these signals, all being transmitted simultaneously on the radio frequency band, interfere with each other. In a society which is becoming increasingly reliant on being constantly connected to the internet, it is of importance that the growth in infrastructure surrounding wireless data transmission is allowed to be developed

without limitations imposed by a lack of available bandwidth. The first part of this report presents the reasoning behind this, and also touches upon the environmental impact that will be a general result of a widespread deployment of LEDs replacing traditional light bulbs. With this my aim is to provide the reader with a context to which they can relate the rest of the report, demonstrating the societal purpose of the work I carry out.

Secondly, the report will give the reader a brief overview of the research that has been, and is being carried out in the fields to which my thesis will relate. The provided information will be sufficient to give the reader some familiarity with the academic background on which my thesis is being based. The PASTA group, which carries out research in the field of efficient design of customised processors, will be introduced. In its future work the group aims to look into a multi-processor System on Chip, and as part of this, compatibility with sending and receiving data through visible light will be explored. A short discussion of the tools and resources I shall be using is also included.

Thirdly the preliminary work relating to my dissertation will be presented. This should give the reader a preview of the nature of work that will be carried out for the main part of my thesis. Further, this outlines the environment in which the work will be carried out as well as describing how I will be approaching the next phase.

The ultimate aim of this report is for the reader to be given an introduction to my future work. After reading this report it should be clear what I am doing, why I am doing it, and how I am planning to do it.

Chapter 2

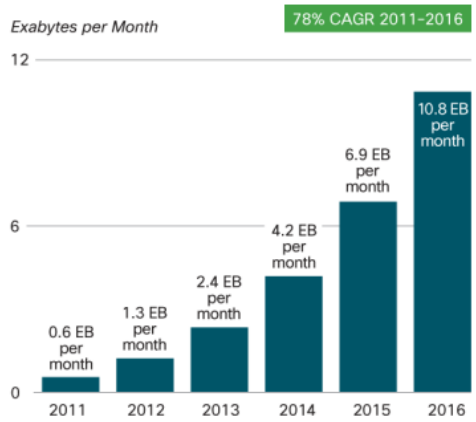
Societal Chapter

For academic work to be justifiable, it should set out to solve or investigate a problem. In some cases the problem approached is purely academic, in other cases it may be of a more practical nature. In the case of this project, I am working on facilitating the use of Optical Wireless Communication, or, Visible Light Communication. At present this technology may by some be seen as a solution looking for a problem, or research which is purely of academic interest. In reality, however, Visible Light Communication is the solution to a problem which is more imminent than most people realise. The further development of the technology, and of devices that support the technology, would be of real benefit to society. This chapter will explain why.

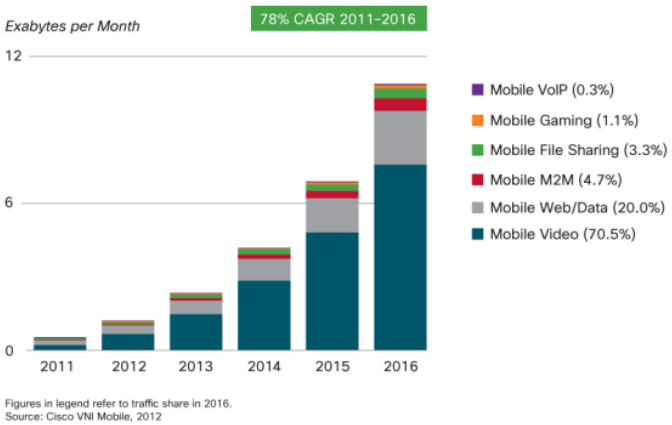
2.1 An introduction to Visible Light Communication

For this chapter, that concerns societal benefits of the development of Visible Light Communication (VLC), a brief introduction to the technology is provided. Further information on the background of the technology, and additional technical details, are given in section 3.1.

The essence of VLC is transmitting data through Light Emitting Diodes, or LEDs, using the visible light spectrum. One of the properties of LEDs is that they respond very quickly to changes in current. This enables LEDs to toggle between intensity-levels, or turn on or off, very rapidly. Through encoding data in ways which can be represented by the intensity-levels of the LED, a photo diode can pick up the changes in intensity, and convert the light back to data. LED lighting is becoming very fashionable, and as a result great strides are being made in the development of the technology behind them. As LED technology matures, and prices drop, Visible Light Communication continues to become a more viable option for the



(a) Figure 1 from the Cisco Global Mobile Data Traffic Forecast Update [4], showing the predicted amount of Exabytes transferred per month for years 2011 through 2016.



(b) Figure 6 from the Cisco Global Mobile Data Traffic Forecast Update [4], showing the predicted distribution of mobile data-traffic over different applications.

Figure 2.1: Figures as published in the White Paper, *Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2011-2016*.

transmission of data over short distances. Different modulation-techniques can be used for encoding the actual data, but the basic concept consists of having a circuit that modulates the intensity of the light emitted by the LEDs based on a digital or analogue input. This light is then picked up by a sensor that converts it back to usable data. The technology already works with existing low-cost LEDs, and all that is required to turn these into hot-spots is circuitry that can vary the intensity of the light, along with the electronics needed for encoding and decoding. This technology is already functional, and even back in 2009, speeds of up to 230 MB/s were reached using a low-cost white LED and a cheap PIN diode [3].

2.2 What Problems Could VLC Solve?

When it comes to mobile handsets, the popularity of so-called smartphones is growing. The term *smartphone* as we know it today has its origins as a marketing-term used to describe mobile phones that close the gap between phones and computers, and allow the user to perform tasks on their phones which previously could generally only be performed with the aid of a computer. Initially one of the main smartphone selling-points was the ability to send and receive emails from a mobile phone. As the technology has matured, web-browsing on mobile handsets has become widespread, and the use of applications on smartphones has proved to be popular enough to spawn a whole new market based entirely around smartphone applications, or “apps”. The popularisation of email, web-browsing and mobile applications

has led to an increase in demand on the mobile network operators to be able to provide quick and reliable access to the internet through their existing infrastructure. Worldwide only 12% of the handsets currently in use are smartphones, however, these 12% make up 82% of all data traffic transmitted and received through mobile handsets [4]. Smartphones are becoming cheaper, and they will continue to eat into the market-share of the traditional mobile handsets. As a result, the global demand for mobile data traffic capacity will increase significantly. In the UK the situation is more immediate, as a large number of internet users already use their phones as a gateway to the internet. According to the office of national statistics, 45% of internet users in the UK also used a mobile phone to connect to the internet in 2011 [5]. As these numbers continue growing, there is no doubt the amount of data transmitted will also grow along with them.

According to projections made by Cisco, as shown in figure 2.1a, overall mobile data traffic in 2012 will be 1.3×10^{18} bytes, or 1.3 Exabytes. By 2016, Cisco projects that this number will have grown to 10.8 Exabytes. This is an explosive rate of growth, and will place a significant strain on the current infrastructure. The capacity of the existing mobile data infrastructure will struggle to keep up with the additional demand that will be created as an inevitable result of this growth.

The radio frequency spectrum is currently used by Wi-Fi, 3G, Bluetooth, and a range of other methods of transferring information. The frequencies available in this spectrum are limited, ranging from 3 KHz to 300 GHz, and are strictly regulated. In the UK, Ofcom is the body regulating the use of the radio frequency spectrum. Figure 2.2 shows the allocations in the UK as of 2007, and the radio frequency spectrum has only become more crowded since then [6]. As more devices start using frequencies that lie close to or even on top of each other, these devices will start interfering. As the spectrum continues to becomes more crowded, interference between devices will become more common, and more noticeable.

In the short term, this problem can be circumvented by inventing smarter modulation-techniques or coming up with systems for handling more devices connecting to a single-access point. In the longer term, however, the underlying problem will not go away. The Cisco-projections indicate a future where the amount of data transferred wirelessly will not only increase, but increase at a very rapid rate. On top of this comes the increase in demand for wireless access-points, and the growing expectation of being able to access the internet from "anywhere" with a quality of service that is sufficient to stream even bandwidth-intensive media. As this demand grows, lack of available frequencies will become a problem too significant to ignore.

Back in 2003, Park et. al. showed how interference between Wi-Fi networks and everyday items could drastically slow down the speed of the wireless internet, in some cases even block it [8]. In 2005 Sikora and Groza concluded that *"There clearly is a coexistence issue in the*

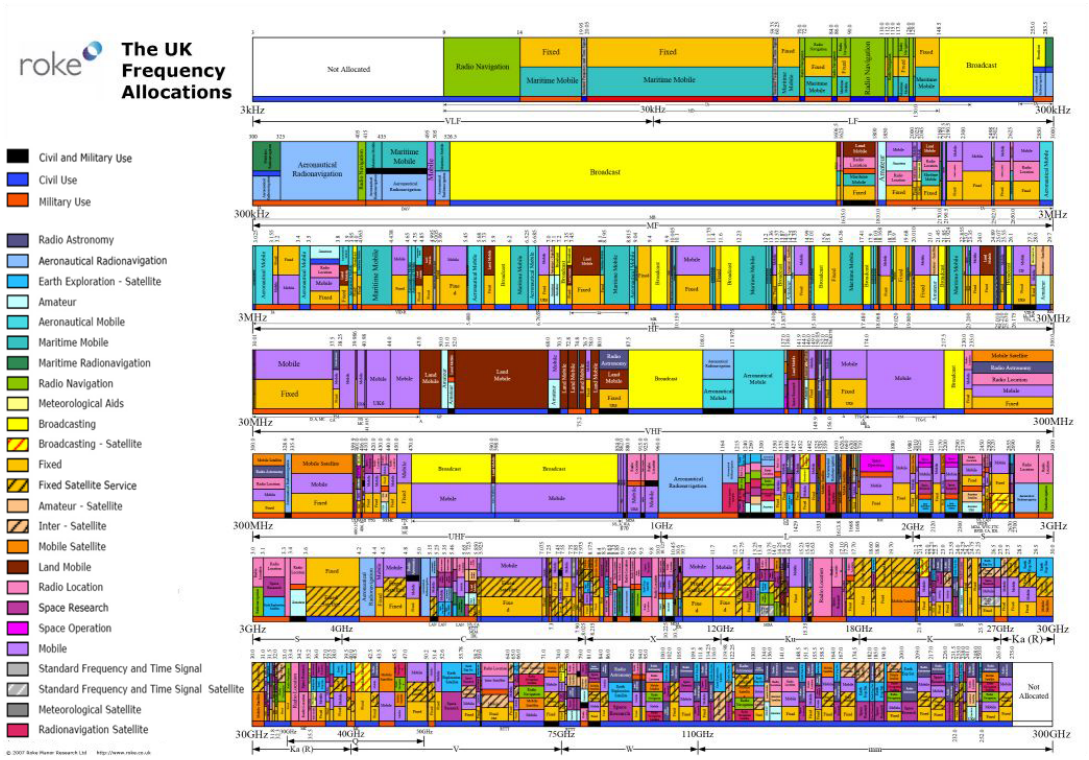


Figure 2.2: Ofcom UK frequency allocation-table, as of 2007. Chart from Roke Manor Research Ltd. [7] based on data from Ofcom [6]. Chart has been altered to magnify legends.

2.4 GHz band" [9].

Another issue which will continue to become more of a problem are the demands on the quality of service of mobile data transfer. According to the projections by Cisco, [Figure 2.1b], more than 70% of mobile data transfer by 2016 will be mobile video. Visible Light Communication sets out to provide the QoS that would be required. This is another one of the reasons why it has the potential to be the future of short-range wireless data transfer.

Another, more general, issue faced by society as a whole is that of finding ways to minimise our environmental footprint. In *Present Status of Energy Saving Technologies and Future Prospect in White LED Lighting* from 2007 [10], Tsunemasa Taguchi presents some estimates of how much energy could be saved by migrating from regular light bulbs to white LEDs. Taguchi makes the assumption that old fashioned light bulbs are replaced by LEDs with an efficiency of 120 lumen per watt (lm/W). Though the average efficiency of LEDs on sale in the US in 2009 was only around 46 lm/W [11], there are commercially available LED light-bulbs which achieve an efficiency as high as 150 lm/W [12]. As LEDs are becoming more efficient quite quickly, the assumption made by Taguchi of 120 lm/W can be said to be reasonable. According to the calculations made by Taguchi, if 10% of the lighting used in Japan were to be replaced by LEDs, this could save almost 2.6 billion kWh of energy every

Figure 2.3: A rendering of the visible light spectrum, with the top y-axis showing wavelength in nanometres. Image created, and released to the public domain, by David Eccles under the Wikimedia user name of *Gringer* [13].

year. In environmental terms this is, according to the paper, equivalent to 630 million litres of crude oil. In financial terms it would save about 50.5 million Yen, or over £409,000.[1] The same paper also makes the claim that up to 10.4 tonnes of carbon dioxide emissions a year could be eliminated simply by switching standard 200W street lamps with LEDs of equivalent brightness that have a capacity of 50W [10]. If VLC catches on, and can be integrated into the lighting infrastructure of buildings and public places, this could potentially create an additional incentive to accelerate deployment of LED illumination, and have a positive impact in terms of the energy efficiency of illumination.

2.3 Solving the Problems

Visible Light Communication, through the ways in which it differs from traditional communication technology, can go far in contributing to solve the foreseen problems with regard to wireless data transmission capacity. Its ability to utilise the vast light frequency spectrum, as well as the fact that it does not interfere with radio frequencies at all, makes it an attractive prospect.

2.3.1 Solving the Problem of the Crowded Spectrum

Visible light has a wavelength of between 380nm and 750nm, and occupies the frequencies of 380 to 750 THz. This is a band of 370 THz, which is larger than the radio frequency spectrum by a factor of about 1000, the RF spectrum being about 300 GHz wide. As there is a lot more bandwidth available to VLC, there could be a much larger gap in frequency between signals used by different devices, making interference between devices on adjacent frequencies less of a problem. VLC can, of course, not be a substitute for all radio frequency transmissions, but has the potential to be used for a number of applications. For instance, Wireless Local Area Networks (WLAN) are extremely widespread, and have become the norm in homes,

[1] Using the conversion rate as of the 14th of July, 2012.

workplaces, and public places. 77% of households had an internet connection in 2011, almost all of which were a broadband connection. In addition to this, 13% of internet users also used public wireless hotspots [5].

In many of these cases there will be wireless transmitters within the line of sight of where users are located while using them. In certain use cases one could question the efficiency of this. If the scenario involves someone using a device out in the open, and the data could be transmitted using line of sight, why should one "pollute" the air with radio waves if this could be avoided? Most places with a WLAN presence also have lighting. If this lighting were to be provided by LED bulbs of equivalent brightness, it would then be viable to transmit data using Visible Light Communication instead. In homes the entire lighting circuit could be coupled up to enable internet using VLC. This would give better overall signal strength than current WLAN technology, and also open for a range of new possibilities. For instance, devices within the home could be made VLC compatible, and would be able to communicate with the home network over VLC.

The popularity of publicly available wireless hotspots is growing quickly. Just between 2010 and 2011 the number of people using wireless hotspots in Great Britain almost doubled, going from 2.6 million to 4.9 million [5]. As availability of public WLAN increases, this is a trend that will continue. In metropolitan areas, VLC could also be used to provide mobile data-access. Access points could be set up in street-lamps, or other public lighting, and compatible devices would be able to use these access points instead of having to transmit data over radio frequencies.

If VLC could be used in locations where many users are currently using radio frequency based wireless data transmission, this could contribute to solving a number of problems caused by devices interfering with each other.

2.3.2 Solving Quality of Service Requirements

The projections by Cisco predict that over 70% of mobile data transfer in 2016 will be video, as shown in figure 2.1b. Streaming of video brings forth a set of quality-of-service requirements that differ from those of normal data transfer. As a higher quality is preferable, the bandwidth requirements when streaming video is likely to be much larger than the requirements for regular web-browsing. Retransmission of lost or damaged packets is also undesirable, as the video may have passed the point of the packet in question once it has been retransmitted. Therefore a type of forward error correction would be desirable over a system which relies on retransmission. The amount of forward error correction that can be done is dependent on the bandwidth available for data transfer. The degree to which forward error correction is needed also depends on the Signal to Noise Ratio (SNR) of the environment.

Generally, however, the typical scenario under which VLC operates is shown to have a very high SNR [14], an observation which, along with the bandwidth available, supports the notion of VLC being well suited for transmitting delivery-critical signals.

Thanks to the abundance of bandwidth available in the visible light spectrum compared to that in the radio frequency spectrum, VLC may also transfer data at higher speeds, and speeds as high as 513 Mbit/s have already been achieved for blue-chip LEDs [15]. As development and research in the area continues, the technology and modulation-techniques will mature, and speeds this high will become the norm rather than being speeds achieved in a controlled lab environment.

Using H.264 encoding [16], a high definition television channel requires a bandwidth of about 8 Mb/s and a standard definition channel takes up around 2.3 Mb/s [17, p.33], making VLC not only a suitable technology for streaming video from the internet, but also a potential way to stream high definition television live to compatible television sets.

2.4 Conclusion

Visible Light Communication could be very beneficial to society. The viability of the technology has been proven, and it continues to improve. However, for VLC to continue to gain traction it must move from the laboratory into the commercial realm. What I aim to do in the process of working on my thesis is to develop a prototype that shows what an interface between an actual device and visible light communication could look like, as well as to investigate how efficient such an interface could be made. If this project can demonstrate that a relatively moderate amount of hardware resources can facilitate high-speed data transfer to a system as a whole using VLC, then this could be a springboard for further investigation into how existing devices such as mobile phones, computers, and televisions could start utilising VLC. This is a crucial step in preparing the ground for commercially viable data transfer over VLC, which again is important in terms of creating a financial incentive to develop the technology further. Once the technology becomes widespread, the community as a whole will reap the benefits in the form of quicker, more reliable data transfer, less interference between devices, and potentially the environmental benefits that might be brought on by the knock-on effects from the added incentive to switch to LED lighting.

Chapter 3

The Current State of Research

My project is linked with two areas in which research is being done. The open research in the field of Visible Light Communication, and the research undertaken by the PASTA group. Some background about these fields is relevant in order to put my work into a context. For the benefit of the reader, this chapter therefore presents some brief background on Visible Light Communication and on the PASTA-project. The chapter also contains some information on the tools I will take in use for my project.

3.1 Visible Light Communication

The work I will undertake for my thesis will be a step in the process of enabling the use of Visible Light Communication (VLC). This section introduces the technology behind VLC, and some history relating to its development.

3.1.1 Brief History of Visible Light Communication

The idea of relaying information using light has been around for a while. An early proof of concept that uses visible light to convey information is the photophone, invented [18] and patented [19] by Alexander Graham Bell and his assistant, Charles Sumner Tainter, in 1880.

Another early example of visible light communication is transmission of data through free space using lasers. This method of data transfer was deployed commercially, and according to a US Army report had a typical throughput of 1 Gb/s at ranges of 500 metres [20]. However, the report also points out that the operation of such a system is very dependant on conditions, and that certain conditions can prevent the system from working at all. Also, the

implementation was reported to be expensive, with the typical price of one two-way link in the range of 5,000 US Dollars.

While transmitting information through visible light has not been widely done, transmitting information using close-to-visible radiation has been very common. Just about every home has had a remote control for controlling a television, stereo, or other electronic device. This has been done mostly using infrared radiation. Infrared transmission has also been used for transferring data to and from mobile devices. In 1993 the Infrared Data Association was set up by a coalition of companies looking to use infrared technology to transmit data [21]. The implementation of infrared technology in mobile devices was successful, and became a popular way of transmitting nuggets of data such as contact information and small data files on mobile devices until Bluetooth gained traction. Infrared was intended, and used, for short distance, line-of-sight transmission of data, and was eventually replaced due to Bluetooth's higher speeds and better range.

As discussed in Chapter 2, the radio frequency bands on which Bluetooth operates, are starting to become crowded. It has therefore been desirable to look into ways of transmitting data that do not make use of radio frequencies. With the recent progress in the development of LEDs, and their properties allowing them to be switched on and off rapidly, data transmission using visible light has now become a viable option.

The development and research in the field of VLC progressed rapidly over the past decade. VLC has many appealing qualities for short-range communication links, such as a very large amount of bandwidth which is not regulated or licenced. In November 2003 the Visible Light Communication Consortium (VLCC) was set up, forming an alliance between *"major companies in Japan"* [22]. The VLCC consists of four committees aiming to research, develop, standardise, plan, and advertise the technology behind Visible Light Communication. As a result of, and based on, the work of the VLCC, the Japan Electronics and Information Technology Industries Association has created two standards relating to Visible Light Communication, JEITA CP-1221 [23] and CP-1222 [24]. In January 2009 a VLC-orientated task group, IEEE 802.15.7, was set up by the IEEE [25], and in September 2011 they published their first standard, *"Short-Range Wireless Optical Communication Using Visible Light"* [26]. The scope of this standard, according to itself, is to *"[Define] a PHY and MAC layer for short-range optical wireless communications using visible light in optically transparent media."* Shortly afterwards, in October 2011, the more specialised Li-Fi Consortium was set up [27]. The Li-Fi Consortium has aims more specific to the transfer of data using VLC, including promoting the technology and coordinating standardisation groups.

3.1.2 Current Proofs of Concept and Challenges

There are two main types of white LEDs, which create the light in different ways, Trichromatic and Blue-chip LEDs. Trichromatic LEDs consist of red, green and blue lights which together produce white light. Blue-chip LEDs are based on purely blue LEDs which are then combined with phosphor of various colours, making the resulting light white. However, while both these methods are used to create white light, which is suitable for lighting up rooms, both have disadvantages as far as VLC is concerned. Trichromatic LEDs, requiring the circuitry to provide three separate lights at once, are more complex to produce. The differing attenuation of the three lights also causes some instability in the colour temperature that is provided by the light. Blue-chip LEDs, having to excite phosphor in the process of lighting up, incur much higher delays when changing the intensity of the light, apparently making blue-chip LEDs less suitable for the purpose of VLC. However, this problem can be eliminated by fitting optical filters on the receivers, causing them to ignore the components of the light that wasn't emitted by the blue LED. The downside to this approach is that only a part of the available visible light spectrum can be used, limiting the available bandwidth.

There are also a range of other, more obvious, potential problems when it comes to Visible Light Communication. Light from sources other than the transmitters, such as daylight, could in some cases lead to a washing out of the signal. Multipath effects will also occur, as light will easily bounce off walls and objects in a room. When modulation-techniques which rely heavily on timing are used, these excessive multipath signals could interfere with the quality of the signal.

One of the more recent milestones is Vučić et. al. demonstrating a VLC link achieving 513 Mbit/s [15]. This paper points to two main limitations in previous experiments, intrinsic noise in receivers and underutilised available bandwidth from the sender, and overcomes these. It also uses a number of other tricks, among them quadrature amplitude modulation in a modified version of Orthogonal Frequency Division Multiplexing (OFDM).

As VLC is still an emerging technology, a lot of research is being put into the basics of data transmission, such as modulation techniques. It has been argued that the traditional disadvantages of using OFDM when transmitting data over radio frequencies will not come into play when transmitting data using visible light [28]. New ways of using OFDM, like Unipolar Orthogonal Frequency Division Multiplexing (UOFDM), have been proposed as a way of specialising this scheme for Visible Light Communication [29].

In the meantime, there are other important unsolved problems relating to VLC which must be overcome before it can be deployed widely. Some of these are discussed in *Indoor Optical Wireless Communication: Potential and State-of-the-Art* by Elgala, Mesleh and Haas [2]. One barrier which could prove to be a problem, especially with regards to OFDM, is

the non-linearity of LEDs. LEDs have a well-defined minimum brightness for light they can emit, and they should not be used above their highest operating current, effectively specifying a maximum amount of emitted light. This is a challenge that can be overcome in different ways, for instance by using OFDM in new, more application-specific, ways such as UOFDM mentioned in the previous paragraph.

Another barrier is the difficulties encountered in realising an uplink. A range of potential solutions to this problem are currently being researched. One solution could be time-division duplexing, with data transmission alternating between uplink and downlink. Another proposed, and to an extent proven, solution involves the use of infrared transmission for the uplink, while the downlink is delivered by visible light. However, this defeats the purpose of transmitting data using only VLC.

In summary, Visible Light Communication is very much a technology still in development. It is being well funded, and as it starts generating greater commercial interest, the research going into it will continue to the point where it could very possibly be the future de-facto standard used for short-range wireless communication.

3.2 PASTA and The EnCore Processor

The PASTA[1] project [1] started up in September of 2006, funded by a research grant from the Engineering and Physical Sciences Research Council. The stated goal of the PASTA project is to enable *"rapid, automated creation of high-performance energy-efficient, application-specific processors"* [30]. The PASTA project has since evolved into the PASTA 2 project, and the area of research has shifted towards the development of a Multi-Processor System on Chip.

3.2.1 What the PASTA Group Does

The project has aimed to innovate within certain fields, the primary ones being automated processor customisation, automated exploration of many design options, applying statistical methods to allow for dynamic optimisation and the co-design of the processor and the compiler.

For a single processor, a designer could come up with many different configurations. These would have different properties, making some more suited to certain tasks than others. The development of processors for mobile devices includes extensive customisation aimed to make embedded processors suited for mobile-specific applications. With the growth in popularity of mobile devices, one metric that has become especially crucial is low power

[1] **P**rocessor **A**utomated **S**ynthesis by i**T**erative **A**nalysis

consumption. Processors that have been heavily customised with regard to a metric which is important in certain applications will, naturally, outperform a generic processor when it is judged by that metric. Therefore, mobile devices tend to run on processors which have been synthesised and laid out with low power consumption in mind.

Currently, this customisation is done manually, to a large extent. Designers will spend days, sometimes weeks, testing and simulating different designs. As transistors become smaller, and designs become even more complex, this customisation is becoming increasingly time-consuming, leading to higer costs. In addition, with a larger number of transistors in a system, the work done by low-level synthesis tools will have a much higher impact on the performance of a system as a whole. In the creation of customised processors it is therefore important that even the lowest level of synthesis is done with thought to the desired final result.

PASTA is working on developing tools, methods, and algorithms that facilitate and improve this customisation process. Rather than manually testing each design, the project has developed methods that use statistical machine learning to quickly iterate over many more potential designs than it would be feasible for a human to do. Through statistical modelling, the tools can quickly come up with a design that would be suitable for a certain application.

Commercial interest has been given to two products in particular that have thus far been created by the PASTA group. One is the simulator created for use in the project which is able to simulate instruction sets extremely quickly, executing operations more quickly than they would be executed on silicon. It provides cycle-accurate simulation, and has proved so successful that it has been licenced, and is now commercially available under the name of ArcSim. The other is the EnCore processor, which was developed to facilitate the research done by the PASTA group. The performance of the taped out EnCore test-chips has proved to be extremely high, better than many similar processors on the market. EnCore has therefore also generated a lot of interest, and has been licenced for commercial use.

3.2.2 The EnCore Processor

EnCore was created as a way of being able to implement and test the results of PASTA's work, and to provide a proof of concept [30]. It is based on the ARCompact instruction set architecture, which, as the name suggests, aims to be compact as well as being easily extendible. The processor is implemented as configurable Verilog IP libraries, and has various configurable options, including pipeline depth, instruction sets, and cache-settings. Two chips have so far been produced in silicon by PASTA, first the 130nm EnCore Calton, and later the 90nm EnCore Castle. These have shown themselves to be able to operate at very high speeds, with excellent power efficiency.

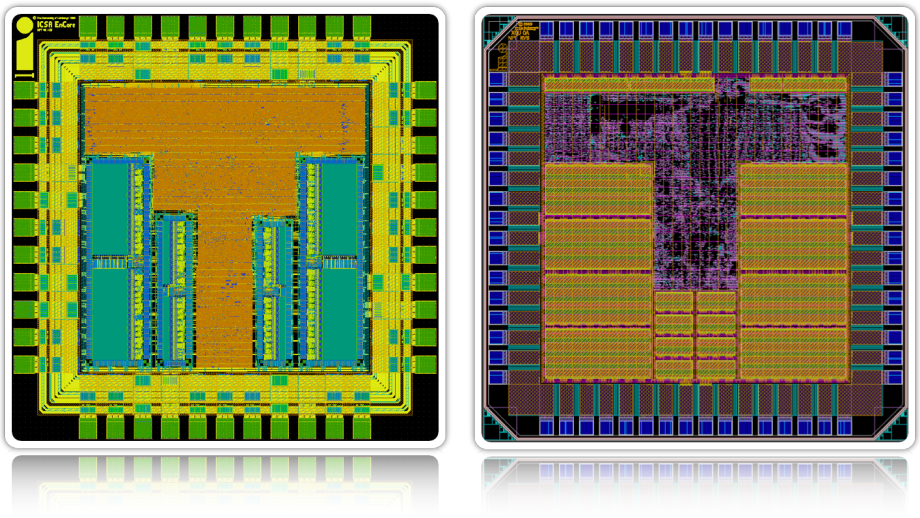


Figure 3.1: The two EnCore processors which have been put into research silicon so far, the 130nm EnCore Calton (left) and the 90nm EnCore Castle (right). Pictures from the PASTA project website [1].

3.2.3 The Future of PASTA

PASTA is continuing research in a number of fields. However, most relevant to my project is the further work on the EnCore processor.

Currently PASTA is researching the multi-core domain, trying to maximise performance with thought to die-area and power consumption [31]. One of the main commercial applications of the research carried out by the PASTA group will be facilitating the optimising of processors, making them suitable for quick, low-power use in mobile devices. The main focus of the current processor related research is a multi-processor system on chip, and optimising the way in which the system works as a whole. PASTA is therefore now working closely with Harald Haas and the rest of the team in the Edinburgh University School of Engineering that works on Visible Light Communication. VLC aims to transmit data quickly through the medium of light, and for the technology to be viable in hand-held devices, it is important to have chips that are fast enough to utilise VLC efficiently, and that will have a low power consumption.

3.3 Tools and Resources

This section presents background information on relevant software tools and standards that I intend to use for my project.

3.3.1 Verilog

Verilog is a hardware description language, and exists in form of a standard issued by the IEEE Computer Society [32]. According to the standard, the creation of Verilog was mostly influenced by HILO-2, a language developed by Brunel University for the British Ministry of Defence. HILO-2 was originally used for simulation, testing and analysis of electronic systems at a gate level. Verilog itself was originally developed by Cadence Design Systems who released it into the public domain in 1990. After further efforts to promote the language, an IEEE-working group was set up, and in December 2005 the first IEEE-standard on Verilog, IEEE Std 1364-1995 [33] was released. A further version, containing a number of updates and improvements, IEEE Std 1364-2001 [34], was released prior to the current version, IEEE Std 1364-2005 [32].

As a hardware description language, the purpose of Verilog is to allow for the description of a complex system through code. The Engineer writes this code, allowing them to specify the function of wires, registers and transitions at a high level. This is then interpreted by a compiler that maps the design out in the form of gates, and later in transistors. This process allows a designer to easily and quickly create very large and complex designs which would have been impossible to realise "by hand" on a gate level. For the compilation and synthesising of the Verilog-code written for this project I will use the Xilinx 12 ISE compiler.

3.3.2 ModelSim

ModelSim 6.4c is the simulator used by the PASTA group to simulate the EnCore processor, and is also the simulator I will be using to simulate and debug my Verilog code. ModelSim is owned and sold by Mentor Graphics, and is regarded as one of the three industry leaders for simulation of Verilog-code. It is able to simulate Verilog-code very quickly, and has a wide range of features making it a very useful tool for testing and debugging systems.

3.3.3 The AMBA AXI Protocol

The practical work in my project will to a large extent be to describe a Verilog-module that defines an AXI Interface for sending and receiving data through the EnCore processor using Visible Light Communication. The following is a brief introduction to what the AXI protocol is, and why it is used. More details on how I will be using the AXI protocol can be found in chapter 4.

Any system on chip will have a number of components that are all expected to work seamlessly with each other. These components will probably have been created by a range of different manufacturers. Therefore it is important that all the components on the system

conform to a standard specification for interconnecting, so the components will be able to work together in the system as a whole.

One of the most popular standards, and the one used by the PASTA project for the En-Core processor, is the AMBA AXI[2] protocol [35]. The AXI protocol is *"targeted at high-performance, high-frequency system designs"* and is a high-speed submicron interconnect. It is an open standard, and describes rules and procedures that components should conform to when passing data to the address and data buses. In practice, the AXI protocol is a burst-based way of reading and writing data between a component and a memory location. It is based on components acting as masters and/or slaves where a master instructs the slave either to accept data from it, or return data from a given address back to it. Unless a component is natively AXI-compatible, it is normal to use AXI modules as a translator between the component and the rest of the system.

3.3.4 AMC7823, Analog Monitoring and Control Circuit

The AMC7823 is described as an *"Analog Monitoring and Control Circuit"*, and features, among other things, an 8-channel, 12-bit Analog to Digital Converter (ADC) as well as eight 12-bit Digital to Analog Converters (DAC).

An Analog to Digital converter works by taking an analog input and sampling the level of the input at a given frequency. Each sample taken of the signal gives a digital representation of the state of the input at a given time. By combining these observations one can get a close-to-perfect digital representation of the original signal. The two main properties to note with regard to an ADC is its resolution, and the frequency at which it takes samples. The resolution dictates how many different levels of the analog input can be observed by the ADC. An ADC with a higher resolution will be able to distinguish between more subtle differences in the levels of the input-signal. The AMC7823 has a maximum ADC resolution of 12 bits, allowing it to distinguish between 2^{12}, or 4096 different levels of input. The sampling-frequency is decided by the system. In theory, the higher the frequency a signal is sampled at, the more accurate the digital representation of the signal will be. In practice it is sufficient to sample at twice the frequency of the highest frequency present in the signal, as stated by the NyquistShannon theorem.

A DAC does the opposite, namely converting a digital data representation into an analog signal. It does this by holding a voltage, and at a given frequency this voltage is adjusted to correspond to the data which is passed to the DAC, creating an analog signal corresponding to the data input.

[2] **A**dvanced **M**icrocontroller **B**us **A**rchitecture, **A**dvanced e**X**tensible **I**nterface

Chapter 4

Initial Practical Work

My work so far has been mainly to familiarise myself with the tools I will be using during the next stages of my project. During this process, I have done some preliminary tasks in creating a design model on which I can base my future work. This chapter reports on my work so far, including an outline of the observations made and problems I have encountered in the process.

4.1 Overview of My Task

As a part of the further work on the PASTA group's System on Chip (SoC), it should be made capable of receiving and transmitting data through VLC. This is done through Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC) respectively. The component that will be used for this is an AMC7823 [36], an Analog Monitoring and Control Circuit (AMC), containing both ADCs and DACs. When used with the EnCore processor the format and way in which data is presented needs to be compatible with the rest of the system. The EnCore system runs using the AXI protocol as an on-chip bus, however, the AMC provides and accepts data according to its own specification. An AXI-compliant module will therefore be needed to act as a gateway between the AMC and the rest of the system, interpreting and forwarding data produced by the ADC to the rest of the system, as well as passing data from the system back to the DAC. The core of my dissertation work will therefore be to create an AXI converter between the EnCore system as a whole, and an AMC7823 Analog Monitoring and Control Circuit (AMC). Figure 4.1 illustrates the part my module will play in this system. I will develop this module using the Hardware Description Language, Verilog.

My first activity will be to create a basic Verilog module that can act as translator between

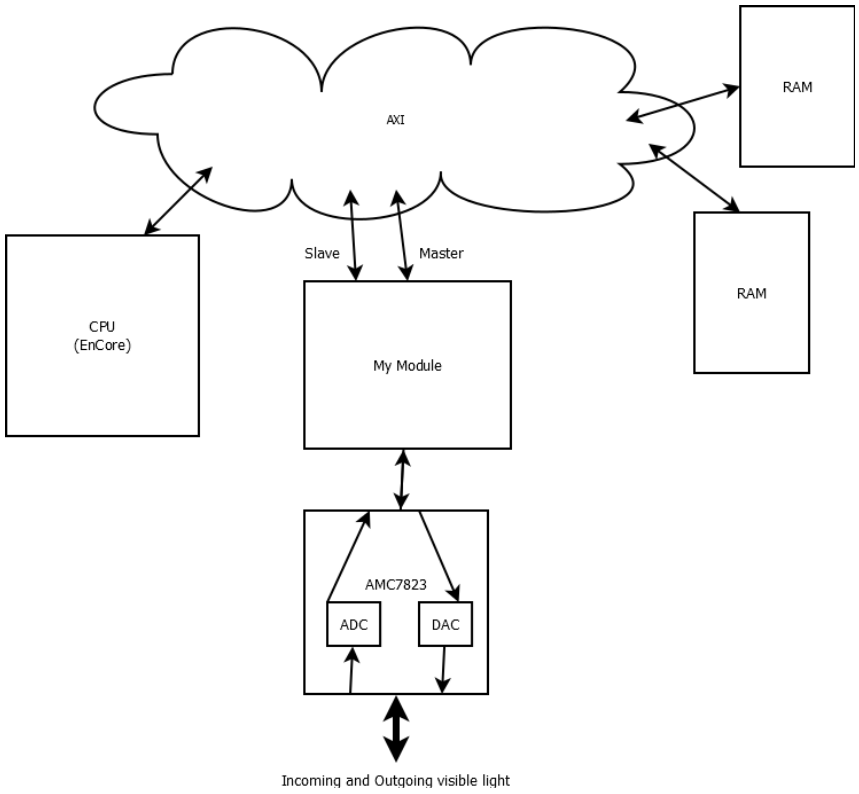


Figure 4.1: An overview of how my module will be working with the rest of the system.

the converters and the SoC. This work, which has started, describes a module that will read certain data from memory and pass it to the converter in a format that the converter can interpret, as well as taking any input from the converter and placing it in memory as data. Here I need to make sure the module conforms to the AXI standard, and also perform simulations, to make sure it fulfils the specification with regards to functionality.

After making a basic functioning module, my efforts will turn to making the module work in the context in which it is to be used. The ultimate purpose of the module is to send and receive data through visible light, a technology which is expected to achieve high data transfer speeds. This carries with it some specialised requirements. My module should be able to receive data very quickly, possibly quicker than the rest of the system will be able to accept. Therefore there might be a need for an amount of buffering in the module itself. I will also have to consider what should be done with data that is arriving too quickly to be handled by the receiving system due to speed-limitations, potentially having to find the best way of dropping packets which the system isn't ready to receive. As my work progresses, trade-offs might have to be made between the rate at which data can be received, and the hardware resources required to realise the module. Depending on observations made at that

stage of my work, focus may move from describing hardware to being more directed towards experiments and simulations in order to investigate these trade-offs.

4.2 Practical Work

Following is a review of my practical work so far. This consists of justification of the objectives I aimed to achieve and the approach I took to reach them, as well as the problems I encountered and how I solved them.

4.2.1 Gaining Familiarity with AXI

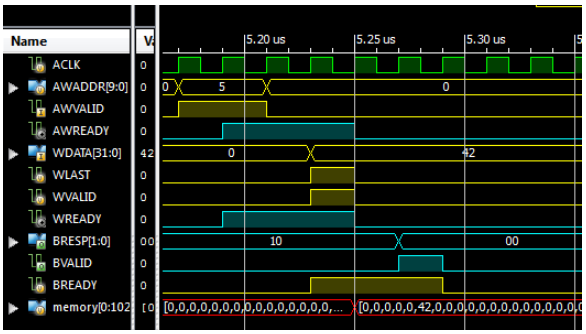
The first step was to familiarise myself with the standards, tools and components I will work with. As the work will revolve around the AXI protocol [35], of which an overview is given in section 3.3.3, I started by getting familiar with the standard, what it does, and how it is supposed to work. To practise my understanding of the specification, and familiarise myself with what signals AXI requires and how they are set, I made two simple Verilog-modules designed to act as an AXI master and an AXI slave. The slave acted as memory, and the master acted as a general component wanting to write data to, and read data from the memory. I then made a simple simulation using Verilog which wrote data to the memory, subsequently reading it back out.

Figure 4.2a shows the signals, along with their assertions and de-assertions, when writing the decimal number 42 to memory-address 5 of the memory in the slave. Figure 4.2b shows the simulation of the master reading data back from the same memory-address, transferring it to an output-wire for use by an imaginary component requiring that data. The state of the signals in figure 4.2 mirrors the example signals shown in the AXI standard for write burst and read burst examples [35].

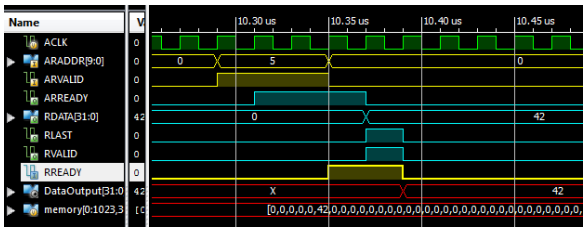
This part of the work was carried out using the Xilinx ISE Design Suite 13.4, due to my prior familiarity with the tool. The only reason for using the Xilinx Suite was to satisfy myself that I had a grasp of how AXI worked. It was not used for other tasks, thus no further description of this software is given in this report.

4.2.2 Working Environment

The next step was to familiarise myself with the environment I would be working in, and the tools I would be using. The EnCore code base is version controlled through an SVN repository. My initial plan was to use my personal laptop for the project, and I set up a Windows SVN client and downloaded the code base. However, after consulting with the



(a) Simulation showing signals when writing data to memory.



(b) Simulation showing signals when reading data from memory.

Figure 4.2: Simulations of simple AXI-signals. Signals from the master-module are marked in yellow, while signals from the slave-module are marked in cyan.

PASTA group, I discovered that gaining access to the tools required on my laptop would be highly impractical, mainly due to the way access to the necessary software licences was set up. After further consultation I concluded that the most practical way of working on the EnCore code would be to use SSH to log directly into the machine where the EnCore framework is set up, i.e. the *'pasta2'* machine on the informatics network. A user account was set up for me on that machine, as well as a checkout of the SVN repository. This turned out to be a very practical way to work, as I can easily log in remotely from my laptop using PuTTY. In addition I can work from any machine in the Informatics Forum, and in the Appleton Tower computer labs.

Editing code

The code I write is contained in a .vpp file which is picked up by the processor and converted to a standard .v Verilog file at compile-time. This enables certain parameters, like the number of bits in data-packets, to be set at compile-time, avoiding the need to change the code if such settings were to change globally. This .vpp file is saved along with the rest of the code-base. I use Vim over SSH to edit this code, and I can do so from any computer with an internet connection.

Compilation

Once the coding environment was set up, I was shown how to compile any Verilog code that I had written. The EnCore compilation process is highly automated, and details on how it works and what it does are rather complex and beyond the scope of this report. I therefore limit the description to an outline of how I am able to interact with it.

The Make-procedure is configured with the help of various parameters from a .sdsc-file

which specifies a range of settings, among them the size of the RAM, and what boot-loader and test file should be loaded onto the system. This is also the file which defines what modules should be included in the system, and what roles they should have in the AXI-setup. For the purposes of my module, I used this file to point to the .vpp file I created, as well as define it as both an AXI master and a slave. A base-address of the component is also specified in the .sdsc file.

The build process works from within a build directory, separate from the actual code base. From this directory a series of commands can be run to automatically compile all the code in the EnCore System on Chip. The make-file can be run with different parameters. The parameter I have used so far is the one allowing me to simulate my code, "make sim". This automatically compiles the code, sets up ModelSim, and opens it. The make-process will alert me to any Verilog errors it finds, making this the stage at which basic coding mistakes such as syntax errors and misdeclarations are found.

Testing

I was given a test harness that allows me to write tests in C for running on the design. Once the test has been written in C, it is compiled to a memory image. The C code for testing is quite basic, with instructions for writing data to a given address. This can be used to test my module by writing data to the address specified in the .sdsc-file as being the address of my module. The .sdsc-file is also where I configure what memory image to use for testing. The specified file will then run on the system after it has been compiled, and the results can be observed in the simulator.

Simulation

I use ModelSim, discussed in section 3.3.2, to simulate my code. Figure 4.3 shows the simulation environment I work with. As previously mentioned, the make-file automates the process of setting up and opening ModelSim. This can also be done over SSH, and by using X-window forwarding I am able to run the user interface of the simulator remotely from any Linux system. I've also been able to use the simulator from my personal laptop, using X-Window software for Windows called *X-Deep/32*.

4.2.3 Preliminary Goals

Four separate goals were defined for the practical work during the first stage of my project:

1. Write a simple AXI module in Verilog which can act as both a Master and a Slave in the EnCore system.

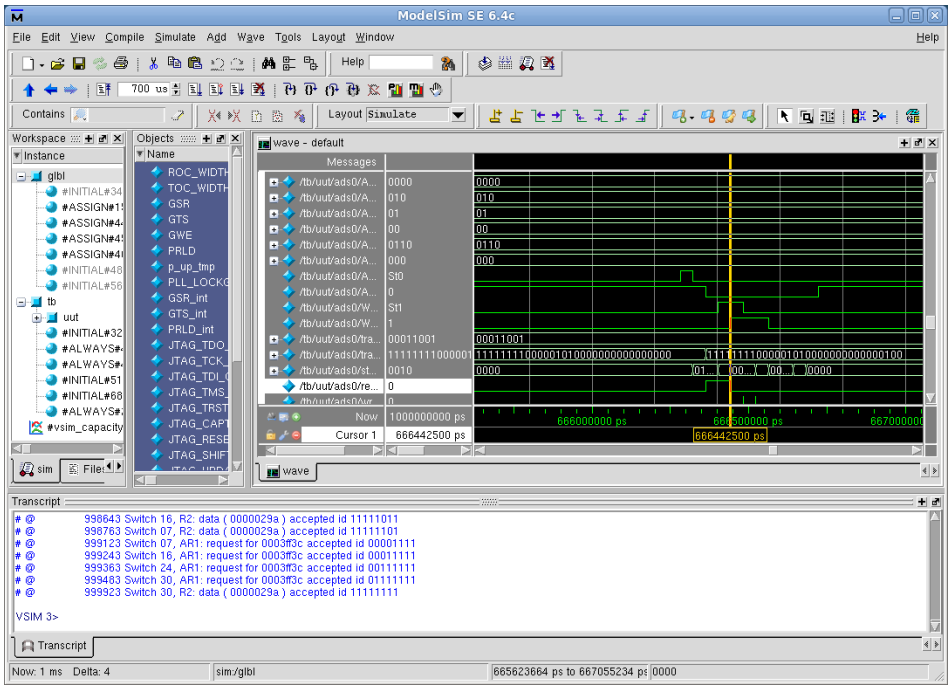


Figure 4.3: Screenshot of ModelSim, my simulation environment.

2. Enable the AXI module to receive settings from the CPU, through creating registers that can be configured by incoming data.

3. Write a valid test program for my module using C.

4. Make the module read data from a configurable address and output this data to a wire which will eventually be connected to a component.

The first three goals lead up to the final goal, which constitutes a key element of what my module ultimately should achieve. In the rest of this section I describe how these goals were approached, and the work I carried out to meet them.

Writing a simple AXI module

The first challenge was simply writing some code that would compile along with the rest of the system without any errors. Despite having become somewhat familiar with the wires used for the AXI protocol, the way they were denoted in the EnCore processor code was different. Two sets of every signal gets declared, suffixed by _M or _S depending upon whether it belongs to the Master or Slave part of the module. The main problem encountered turned out to be a mistake I had made in the .sdsc file while setting up the module. Once this was corrected the module compiled, and I was able to see it working in ModelSim by declaring a signal to be high.

Defining registers in the module and writing a test

One requirement for the final version of the module is that it should be configurable by the program code. The module will be reading data from certain memory locations, and the address of these locations needs to be set by the rest of the system. Implementing this capability was my first attempt at actually using AXI in practice. The required data would be addressed to the component using the AXI protocol, and my module had to assert the correct signals at the right times to appear as a working AXI-compatible module to the rest of the system.

This functionality was implemented by using a Finite State Machine (FSM). The state machine will wait in a *WAIT*-state, setting the AWREADY-signal high, informing the rest of the system that the module is ready to receive data. Once the module detects incoming data, it will save the ID and address of the incoming bursts to registers, and then go through the steps required to accept it. Depending on the address to which the data is sent, the module writes the data to one of two internal registers, before returning an "ok" signal, signifying that the transfer has been completed successfully.

This had to be tested by writing some straightforward C-code that wrote a value to one of the registers. Based on sample tests that were provided I was quickly able to develop a test that would write data to a memory address. In this case that address was the base-address of my module, as specified in the .sdsc file.

Making the module work properly turned out to be more of a challenge. The design of the state machine went smoothly, but problems were encountered with regard to following the AXI specification exactly. In addition to the signals I had used when familiarising myself with the protocol, described in section 4.2.1, there turned out to be additional signals that had to be asserted for the module to work. Once these were dealt with, the module functioned as expected.

With the working module in place it could be observed and verified through the simulator that its functions were carried out. This is shown in Figure 4.4.

Reading data from memory

Once I was able to configure a setting in the module, the next step consisted of enabling a memory address to be set as a parameter in the module, read the data from this address in memory, and return that data.

To achieve this I had to make my module act as a master, and treat the memory-space as a slave. For this a second FSM was triggered to execute once a memory address had been given to read from. The FSM then went through the steps for requesting data from the memory, using the AXI protocol. Writing a test for this function added a layer of complexity to my

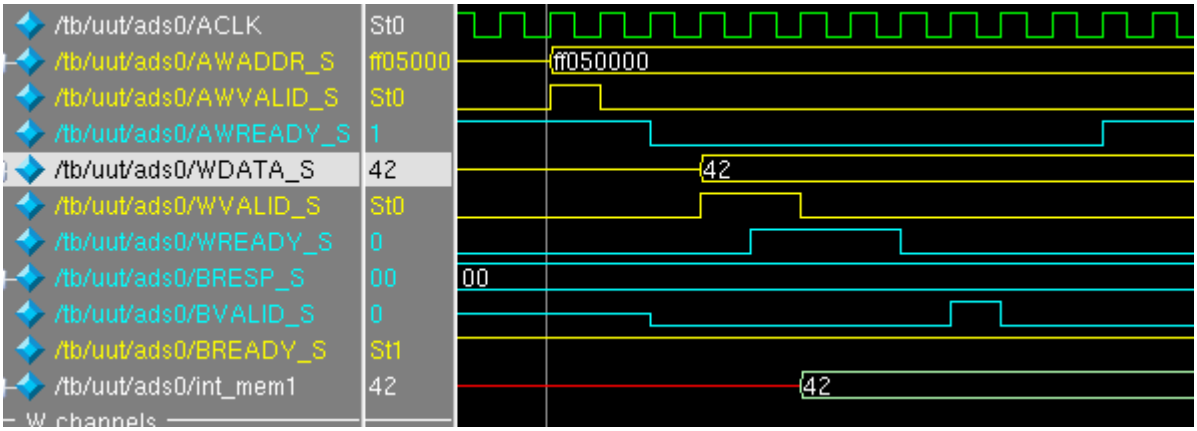


Figure 4.4: The simulation, in ModelSim, of a value being written to my module. Master-signals, which were provided by the system and not controlled by my module in this case, are in yellow. Slave-signals, the ones controlled by my module, are in cyan. The bottom signal is the internal memory of my module.

previous test, as the location of memory blocks is set dynamically at the time of synthesis, with the result that they would not always have the same base-address. Having consulted the PASTA-group on this issue, I was explained how memory is declared, and was able to declare my own memory partition in the test-code. I could then pass the location of this memory to the module by using a pointer, representing the location as a data value.

There were further bugs that had to be fixed, also as a result of my not having been careful enough in making sure I had all the required signals assigned. As part of the AXI protocol, the slave and the master have to go through a handshake-procedure, acknowledging that a transaction has been carried out successfully. I had not properly set the wires required to carry this out. This particular mistake caused me some additional problems when debugging, as my tests initially only carried out one burst before halting. Once I tested with multiple read or write bursts the error became apparent. My module had not properly concluded the previous transaction, and the system was still waiting for a confirmation of the initial burst having been completed. The problem turned out to be a mistake in the way the ID-tag of the transaction was handled, and once this was fixed the module worked as expected, as shown in Figure 4.5.

4.3 Results

As I have mostly carried out preliminary work there are few results or findings to be presented so far, however, there is one observation worth mentioning. Through using the AXI protocol to read data from memory I got an indication of the delay in the system, i.e., how long it

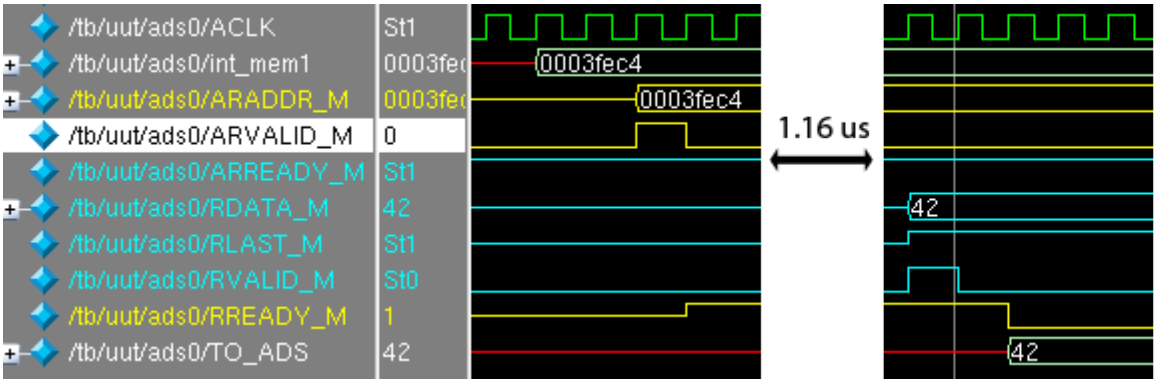


Figure 4.5: This simulation shows the module using the memory-address it has received from the system, stored in int_mem1, to read from that memory address. Master signals in yellow, slave signals in cyan. My module acts as the master and therefore controls the yellow signals in this case. TO_ADS at the bottom of the figure is the data sent out to the output which will eventually be hooked up to the DAC. Note that 1.16µs worth of simulation-time is cut out of the image to save space. This is due to the delay from when the read-signal was issued until the memory responded.

took from a request was issued until it was fulfilled. The observed delay in the simulation, as can be seen in Figure 4.5, is slightly more than 1.16µs. The exact time taken from the clock-edge where the signal indicating the module is ready-to-read is asserted, until the clock-edge where the data is present on the data-bus, is 31 clock cycles. The exact time taken by these cycles will depend on the speed at which the system is run. Currently I don't have enough of a context to be aware of how this will affect my future work. Still, it serves as a possibly important reminder that my module will have to be designed with delays in mind.

4.4 Summary

So far my work has focused on making a start on the module that I will be working on for the rest of my project. Through this period I have learnt to use the tools that will be at my disposal and have become familiar with the kind of Verilog-code that I will be writing more of. Up to this point I have only dealt with single packets of data in every burst. This I will have to change as I progress, as my module has to be able to deal with multiple packets of data. Though I have read its data sheet, I also have yet to explore the practical interaction with the component I will be working with. However, I have succeeded in reaching the goals that I had hoped to achieve at this point, and believe that I have established a good position for further work on my project.

Also, I have thus far not spent much time focusing on the efficiency of my code. As the work progresses, efficiency will become very important, and much of my focus will shift to making my module work as efficiently as possible.

Chapter 5

Conclusion

This report has presented the background around the work I will be doing for my thesis, as well as some preliminary work I have carried out so far. It has been argued that Visible Light Communication is an emerging technology that could prove to play an important part in the future of short range wireless data transfer. The radio frequency band is currently being used by practically all standards for transferring data wirelessly. It would be viable to replace some of these wireless links by new technology that utilises Visible Light Communication. VLC has advantages over the current de-facto standard, Wi-Fi, in terms of both licencing-freedom and throughput. This report has discussed why the widespread deployment of VLC could be beneficial to society, and how it is becoming a viable option given the current state of the art in LED technology, as well as within the field of VLC itself. The report has also given a general overview of the research that has been carried out so far in the field of Visible Light Communication, as well as outlining the research which has been done on processor customisation by the PASTA group.

This is the backdrop of the work I will be carrying out for my thesis, and working on this report has given me an introduction, not only to the theory, but also to the practical aspects of creating an AXI module in Verilog. Already I have been able to make a start on what I will be doing as I get further into the process. I have spent this time getting basic code working, getting familiar with the debugging environment I will be working with, as well as getting a good grip of the basic AXI signal protocols. With these issues now having been dealt with, I should be able to spend most of my remaining time on making my module as good as it can be, focusing my efforts on the more substantive work that will lead to an efficient module in terms of space and time.

Having investigated the background material, I am eager to get started with the proper work on my thesis. This overview of the background has made me realise how the thesis work can fit into a bigger picture, how and why the research into fast, more energy-efficient processors is important, and how linking this research up to VLC is a natural step to take. I

look forward to starting the work on the main part of my thesis, and hope that I will be able to play a small part in the future work on the EnCore processor to make it work with Visible Light Communication.

Acknowledgements

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I would also like to thank my family for their help in proofreading, and providing feedback on this report.

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