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NFV網路加速技術介紹

工研院資通所人工智慧運算平台組

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講者介紹

李育緯 Ray

現任：

工研院資通所人工智慧運算平台組技術經理
(前資料中心架構與雲端應用組)

專案經歷：

- NFV效能實驗室技術推廣
- 5G NFVI平台研發與5G專網系統整合
- 混合式軟體定義網路系統研發
- 國產Cloud OS資料中心網路系統研發





Outline

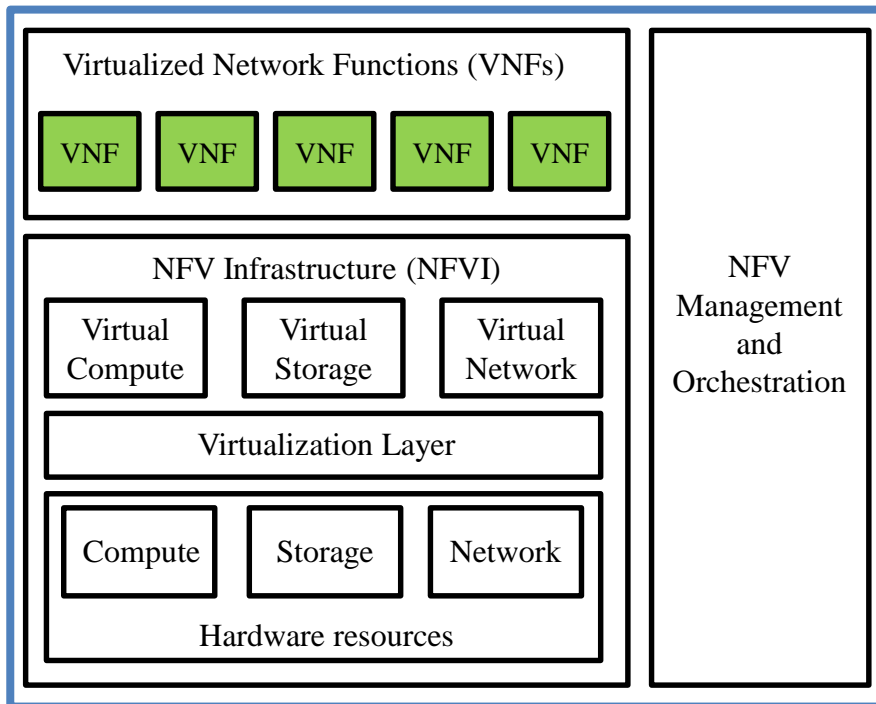
■ NFV Performance Lab介紹

- NFVI效能測試與優化技術
- SDWAN效能測試與優化技術
- Service Function Chain效能測試與優化技術

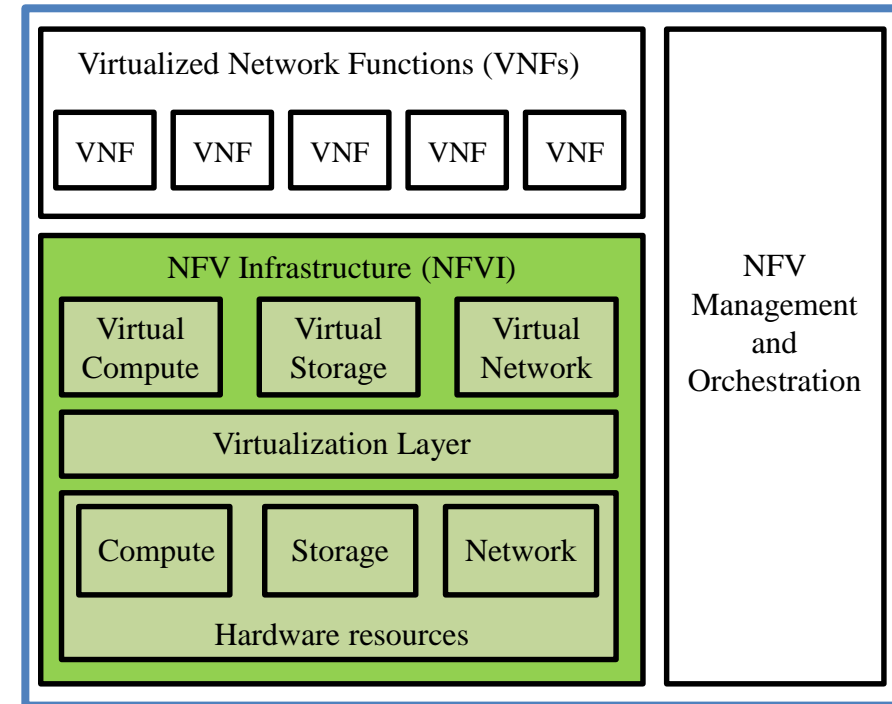
NFV Performance Lab

- Intel and ITRI build the NFV performance lab cooperatively
- Goal: NFV performance characterization
- NFVI characterization requires some “VNF”
- VNF characterization requires some NFV infrastructure

VNF Characterization focus



NFVI Characterization focus

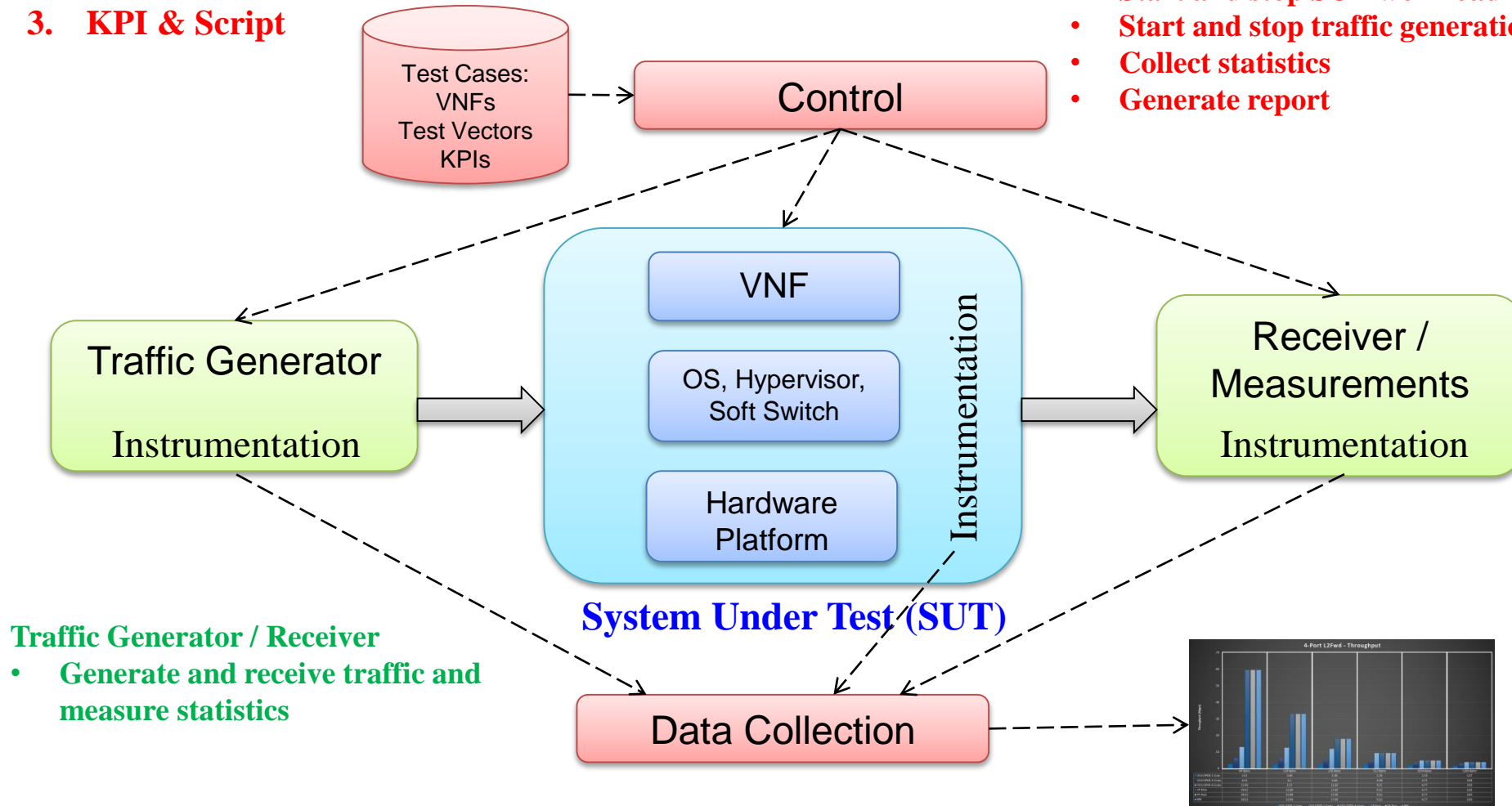


VNF and NFV Infrastructure Characterization

1. System Under Test (SUT)
2. Traffic Generator
3. KPI & Script

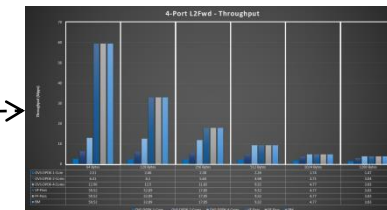
Control and Data Collection

- Test cases measurement
- Start and stop SUT workload
- Start and stop traffic generation
- Collect statistics
- Generate report



Traffic Generator / Receiver

- Generate and receive traffic and measure statistics



Throughput

Forwarding Rate at Maximum Offered Load (FROML, RFC 2889)

- Generate at line rate, and measure forwarded packets
- Easy to run, fast
- Measure high load behavior (overload?)
- Might represent a completely different number than maximum forwarding rate



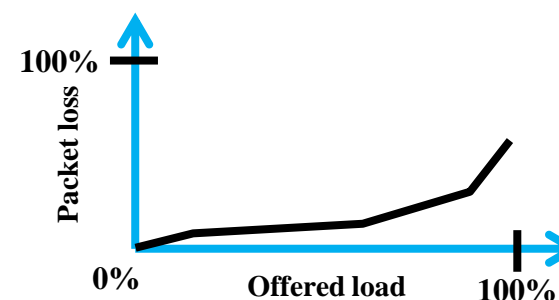
Maximum Forwarding Rate (MFR, RFC 2544)

- Start generating at 100% line rate and binary search for higher rate without packet loss
- Quite fast
- Might be very sensitive to spurious packet loss



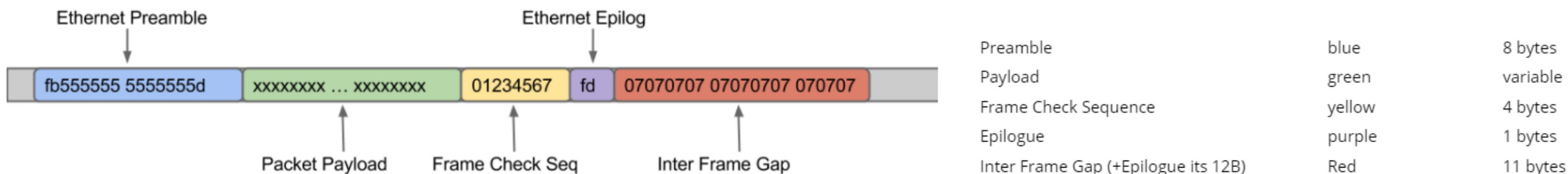
Measure packet loss for any rate, starting from 0.1% to 100% of line rate

- Slow
- Better picture of the performance
- Will highlight spurious packet loss



何謂10G Bit Line Rate

- 在NFV的領域，因為使用CPU來執行虛擬化網路功能(Router、Switch、Firewall等)，在討論NFV的效能時，我們要了解所謂的10G Bit究竟有多少封包要處理。
- 通常我們以64 Bytes的封包大小來估算應該要處理的封包數量
 - 64 Bytes封包包含60 Bytes的Payload與4 Bytes的Frame Check Sequence，再加上L1的20 Bytes的Overhead，封包大小總共是84 Bytes。
 - ☞ $10 \times 10^9 / 84 \times 8 = 14.88 \times 10^6$ (14.88百萬個封包)，每秒要處理14.88百萬個封包，相當於1個封包只有67ns的時間可以處理
 - ☞ DDR4的Memory Access Latency約15ns
- 若封包大小是1500 Bytes的話，又會如何呢？
 - 1500 Bytes封包，加上L1 20Bytes的Overhead，封包大小總共是1520 Bytes
 - ☞ $10 \times 10^9 / 1520 \times 8 = 822,368$ (82萬個封包)，每秒要處理82萬個封包，相當於1個封包有1216ns的時間可以處理。



Source: <https://fmad.io/blog-what-is-10g-line-rate.html>

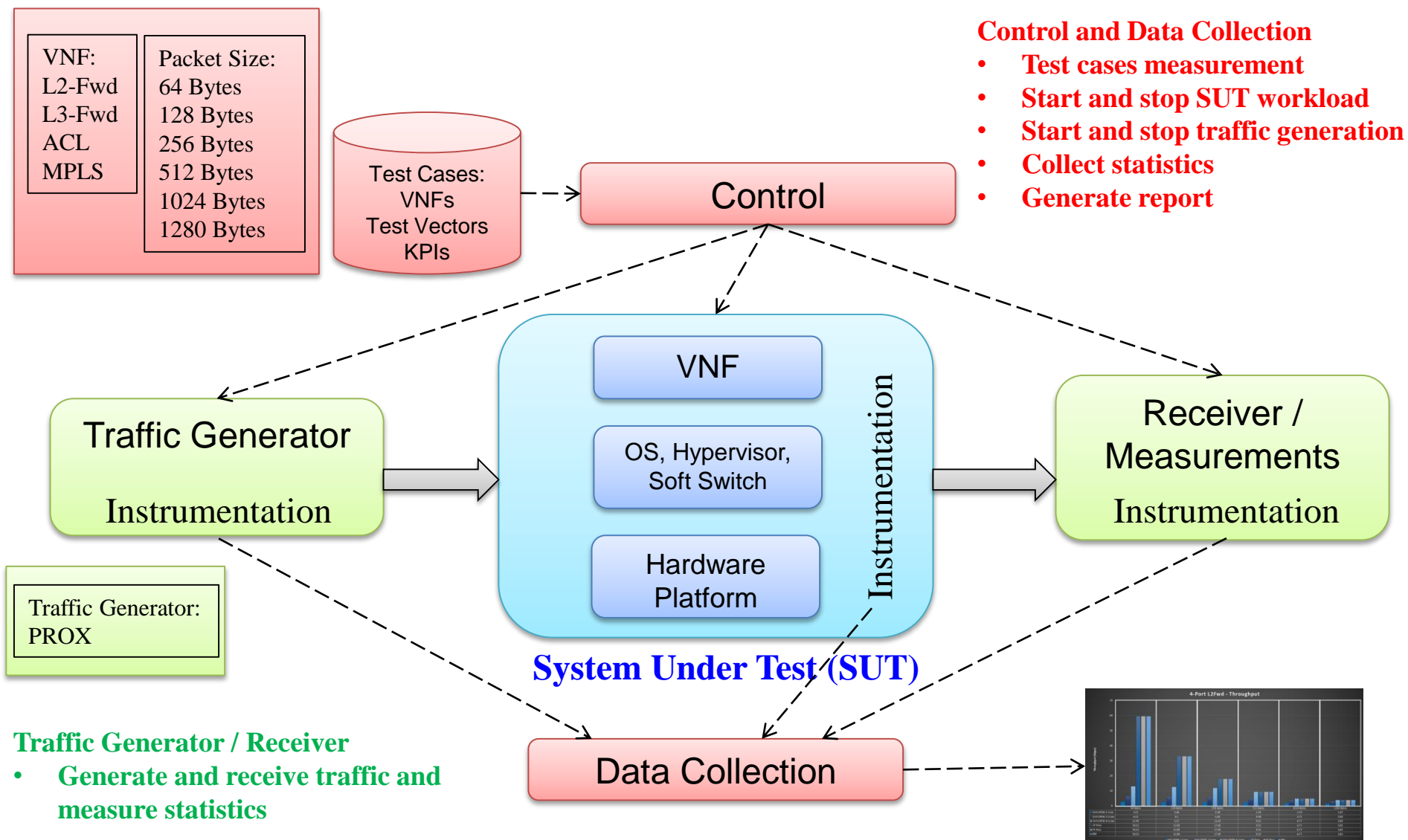


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Intel Xeon Processor E5-2695 v4 NFVI Performance Report

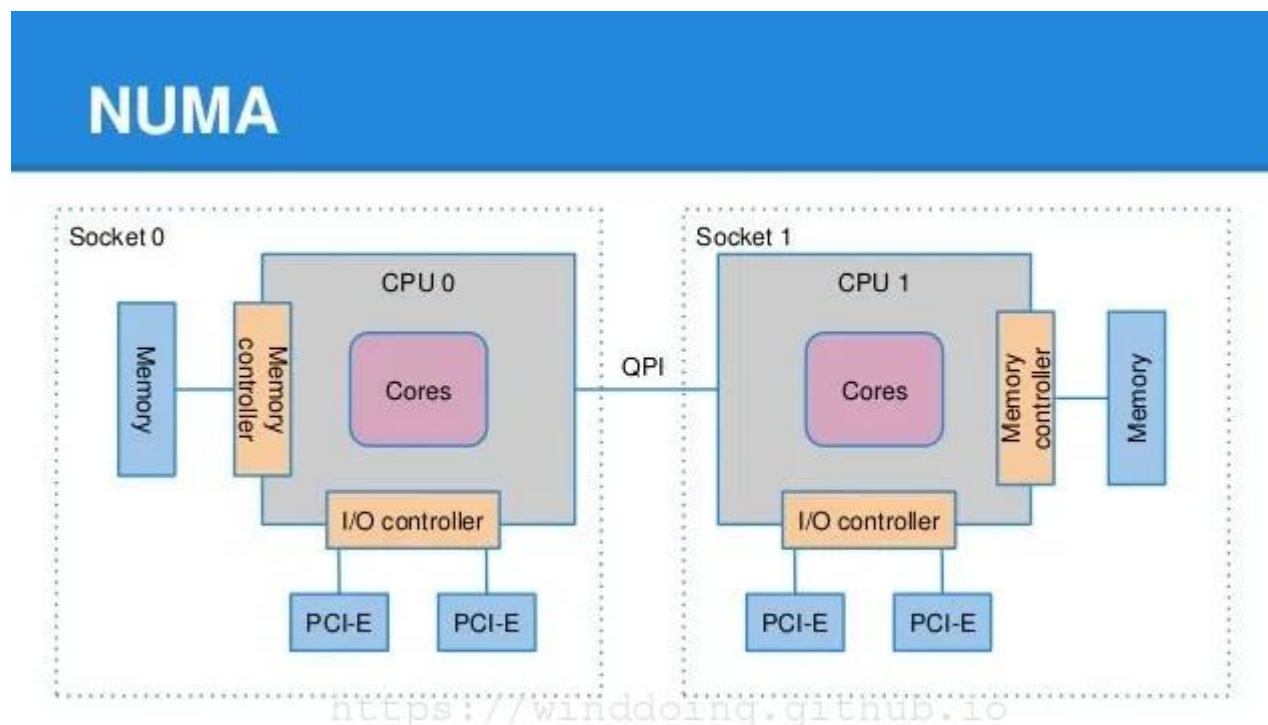
Produced by ITRI Performance Lab

NFVI Characterization



NUMA概念解說

- **Non-uniform memory access (NUMA)**系統是指一個主機板上有多個CPU，各CPU有各自的記憶體與IO控制器，CPU之間透過QPI介面可存取遠端的記憶體與IO設備，但CPU存取本地記憶體與IO設備的延遲與頻寬會優於存取遠端的記憶體與IO設備。

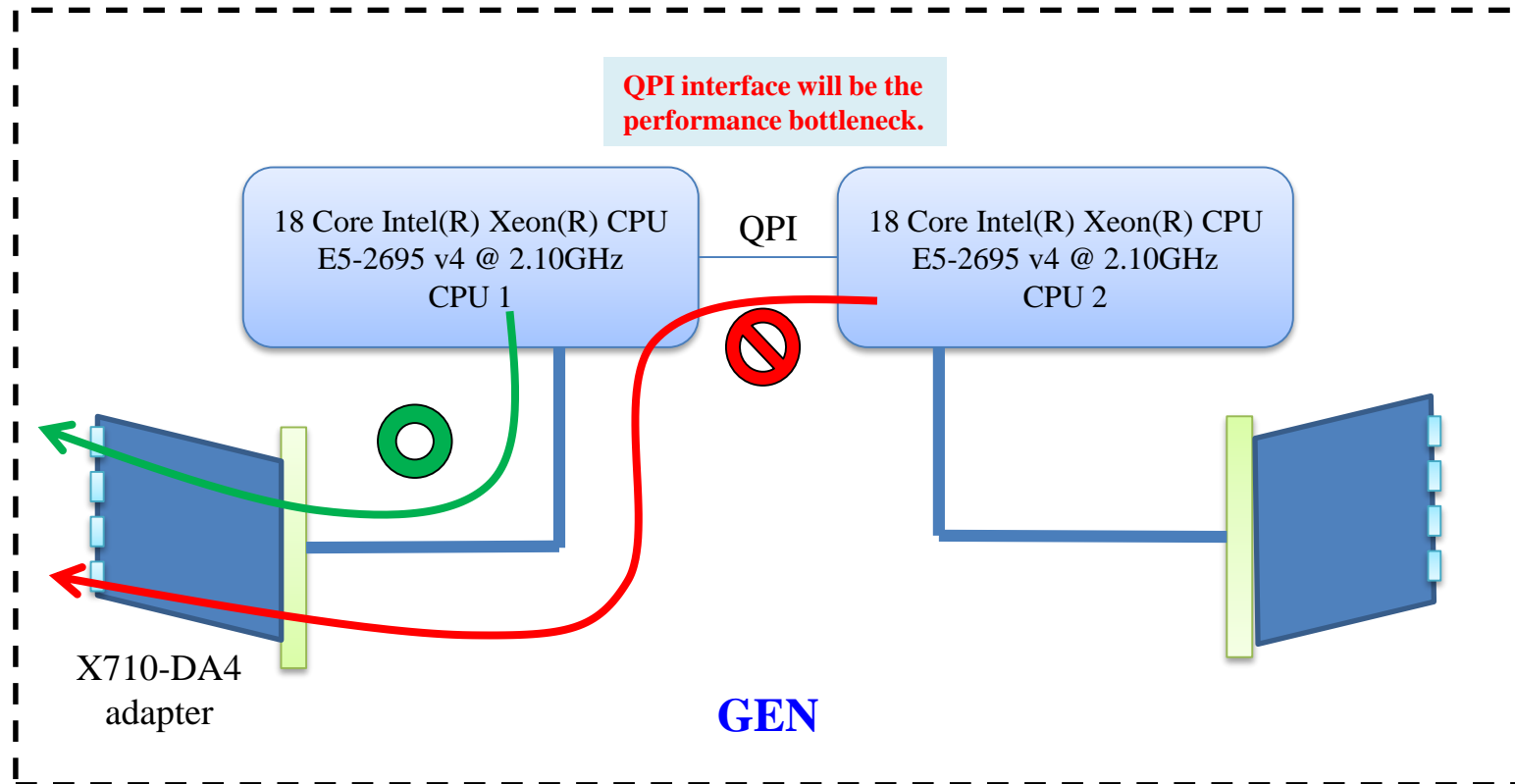


Source: <https://winddoing.github.io/post/13d4e2a6.html>

The Mapping Between CPU and NIC

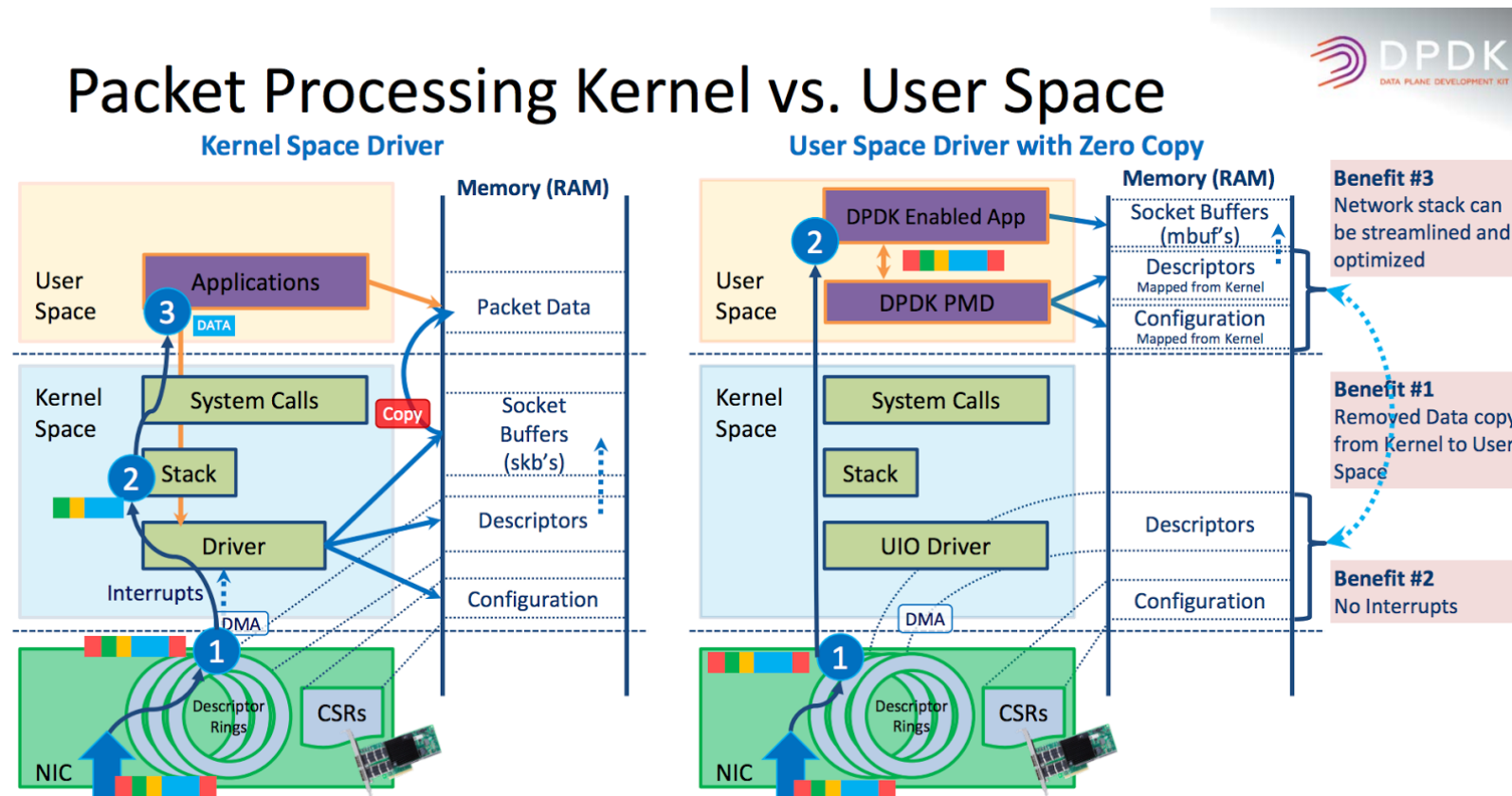
- The CPU core and NIC for packet generator should be in the same CPU socket, or the QPI interface will be the performance bottleneck.

- 10GbE line rate (64bytes packet) = $10.00\text{e}9 \text{ bits} / (8 \text{ bits} * (64 + 20)\text{bytes}) = 14.88\text{e}6 \text{ packets}$.
- CPU and NIC in **same socket**, 10G port could generate **14.88 Mpps**.
- CPU and NIC in **different socket**, 10G port only could generate **10 Mpps**.



DPDK介紹

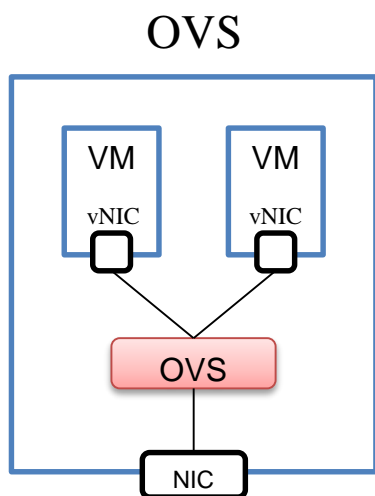
- DPDK (Data Plane Development Kit)是由Intel提供的開發工具集，不同於Linux系統以通用性設計為目的，而是專注於網路應用中數據封包的高性能處理。



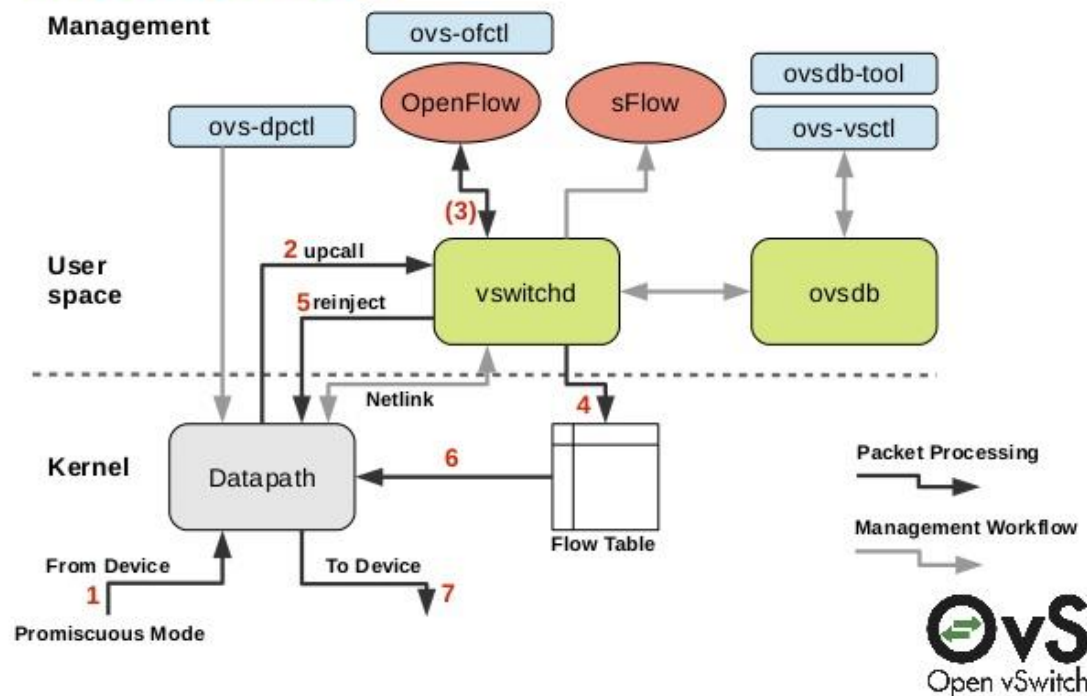
Source: <https://www.slideshare.net/MichelleHolley1/dpdk-1805-inflection-point>

OVS介紹

- Open vSwitch(OVS)是開源的虛擬交換器，支援VLAN/VxLAN/NVGRE等網路隔離功能，也支援QoS、sFLOW與OpenFlow協定。

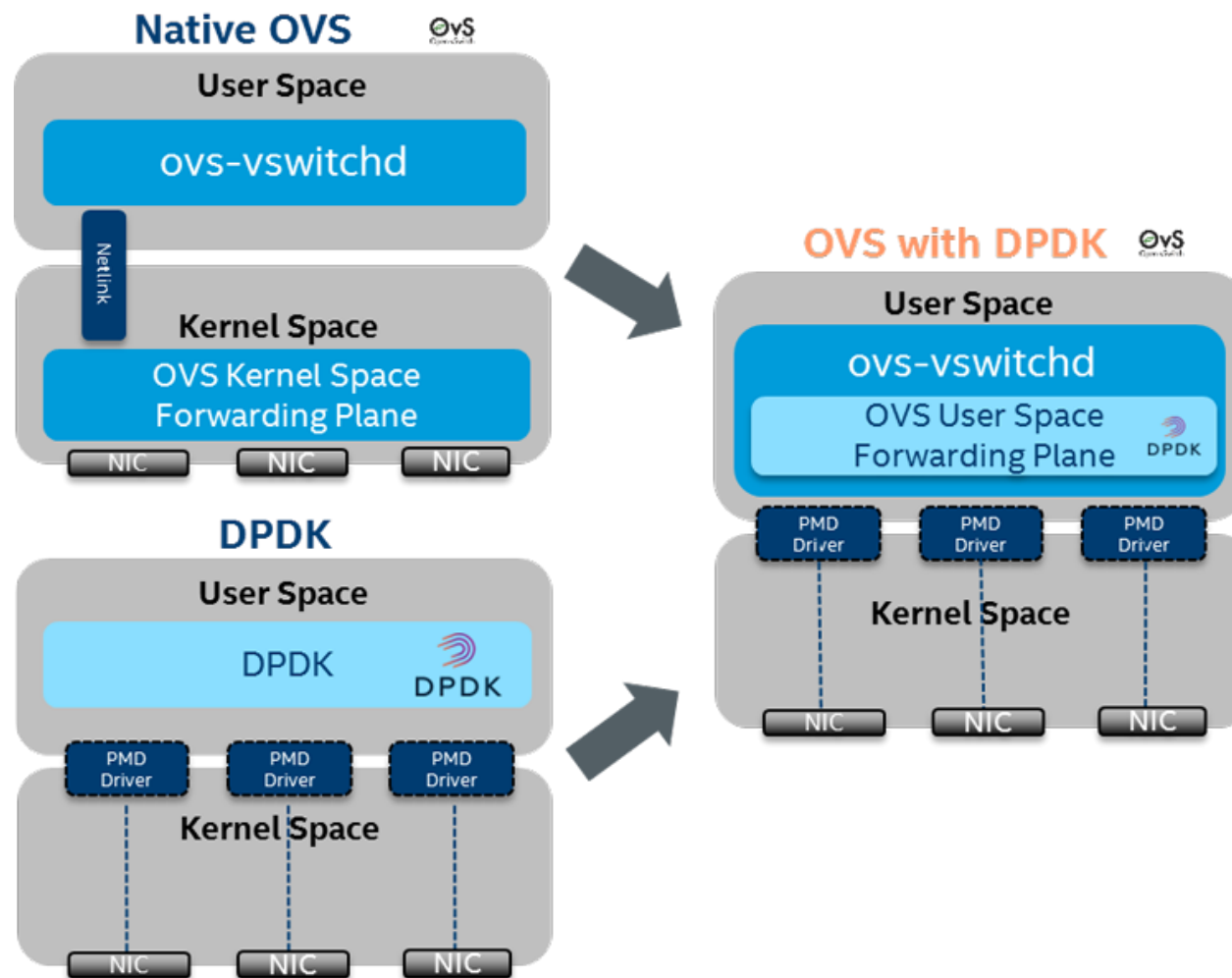


Architecture



Source: <https://hustcat.github.io/an-introduction-to-ovs-architecture/>

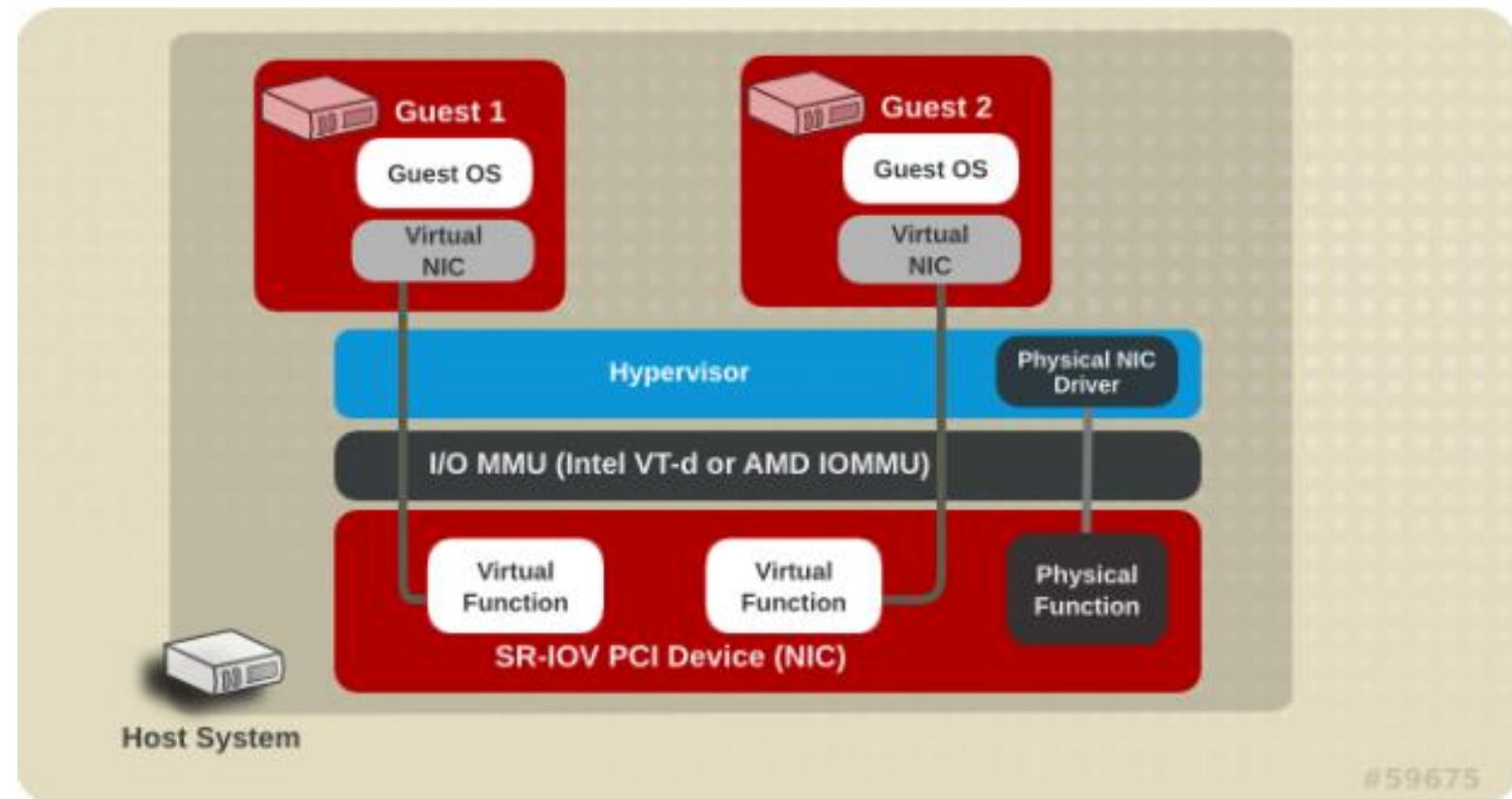
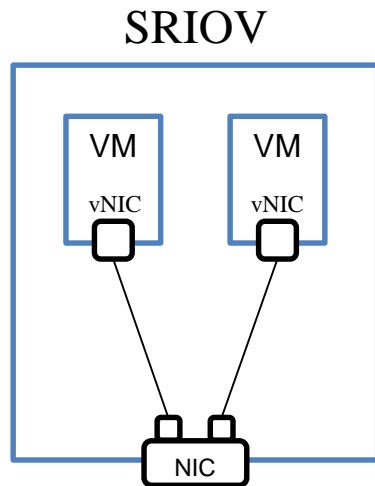
OVS + DPDK



Source: <https://sites.google.com/a/cnsr.cycu.edu.tw/da-shu-bi-ji/openvswitch/dpdk-ovs>

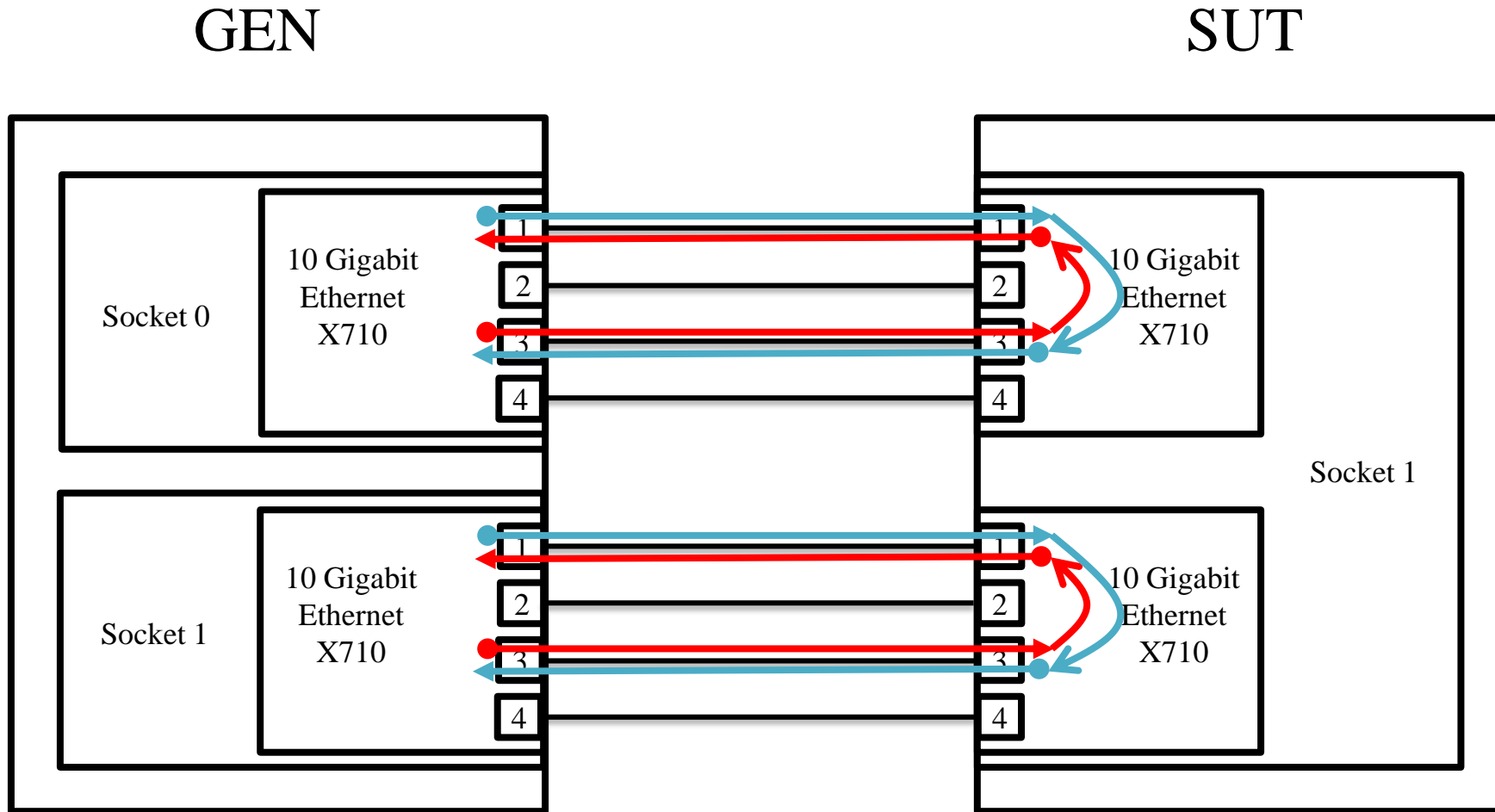
SRIOV網卡

- **Single Root I/O Virtualization (SR-IOV)**。SR-IOV為PCI-SIG標準，允許PCIe的I/O裝置以多個實體與虛擬裝置呈現。



Source: https://access.redhat.com/documentation/en-us/red_hat_enterprise_linux/6/html/virtualization_host_configuration_and_guest_installation_guide/chap-virtualization_host_configuration_and_guest_installation_guide-sr_iov

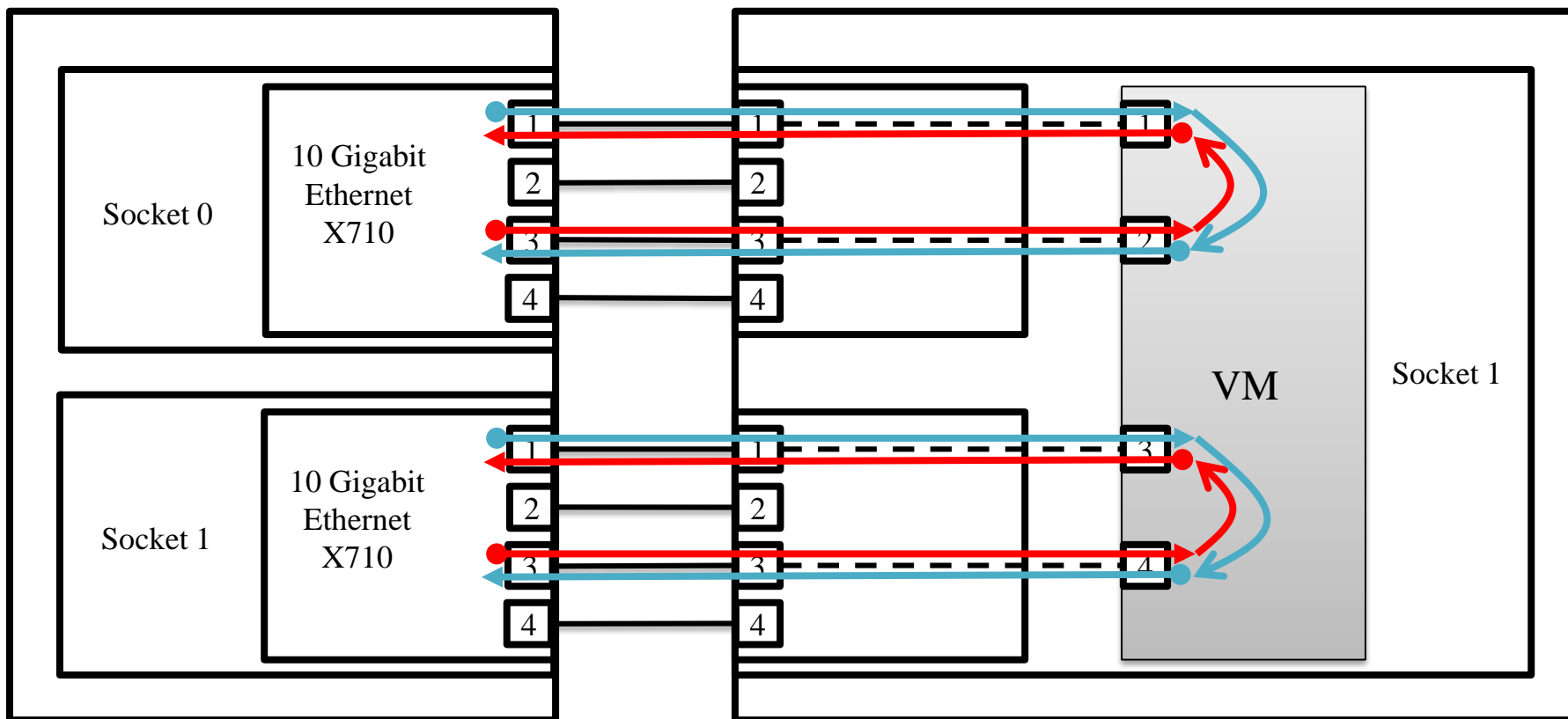
Baremetal Architecture



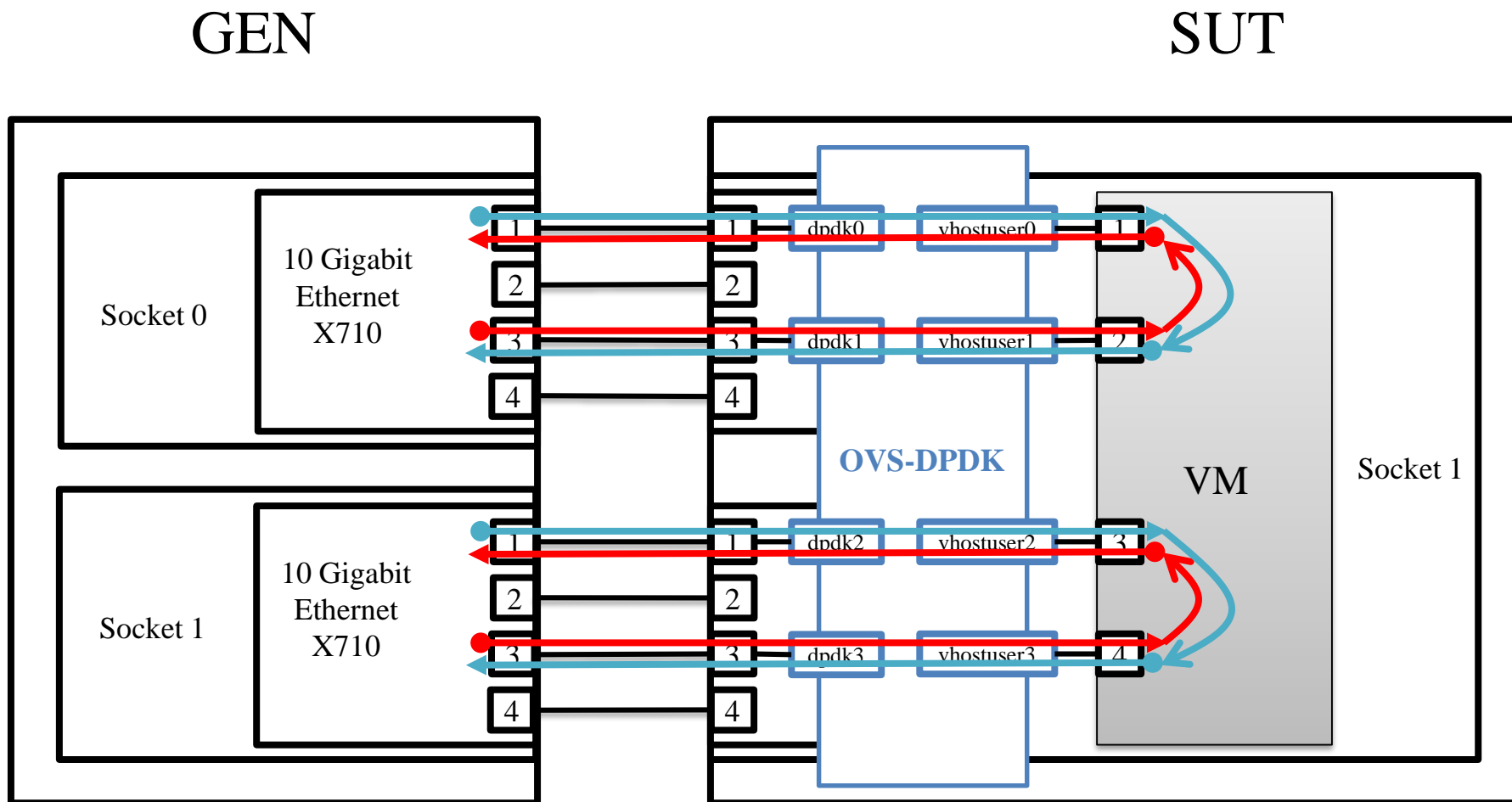
SRIOV Passthrough Architecture

GEN

SUT



OVS-DPDK Architecture

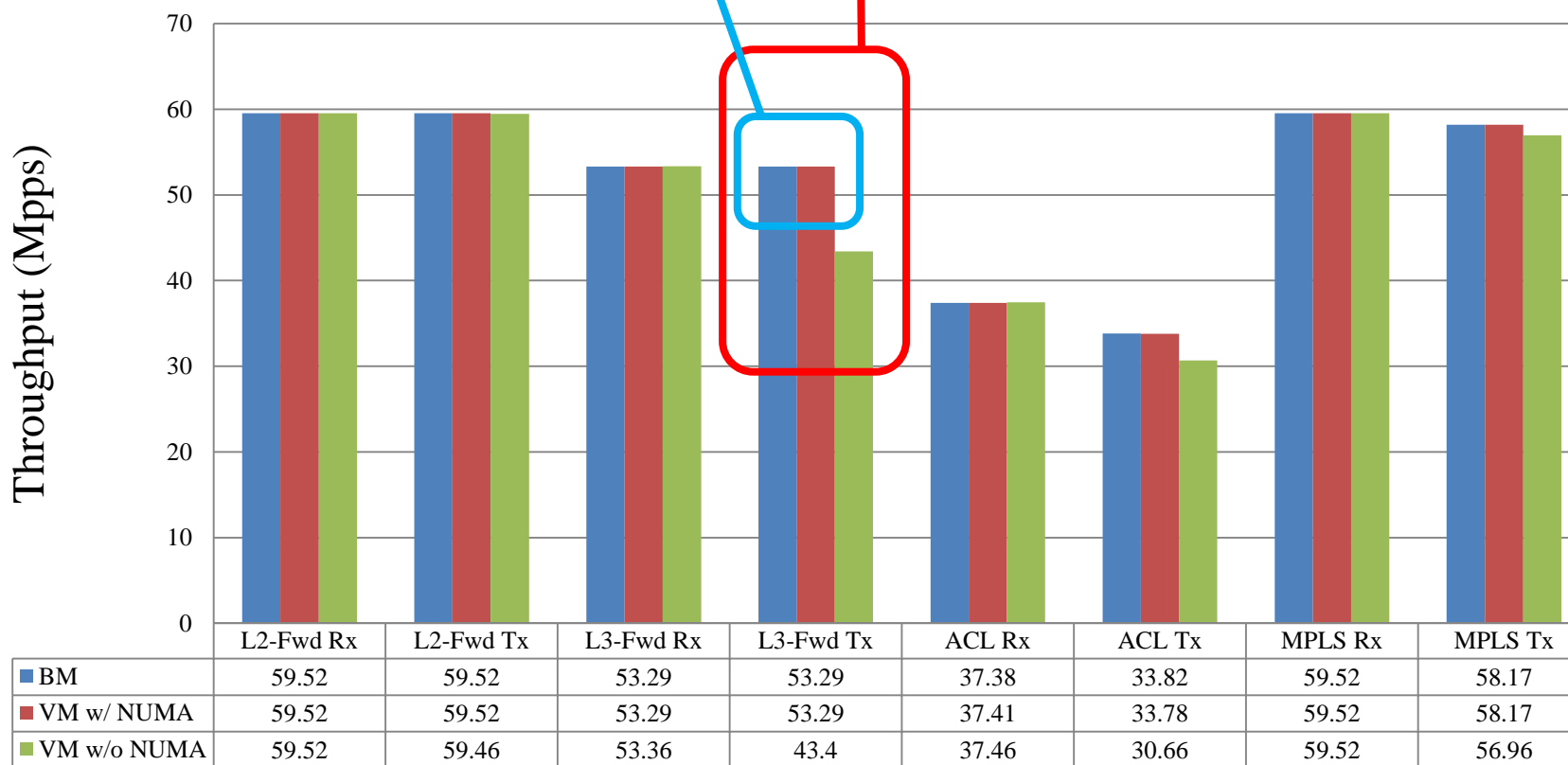


Baremetal vs SRIOV Performance Result

VM performance with NUMA-aware configuration is similar to Baremetal performance.

VM without NUMA-aware configuration may decrease 10 – 20% performance.

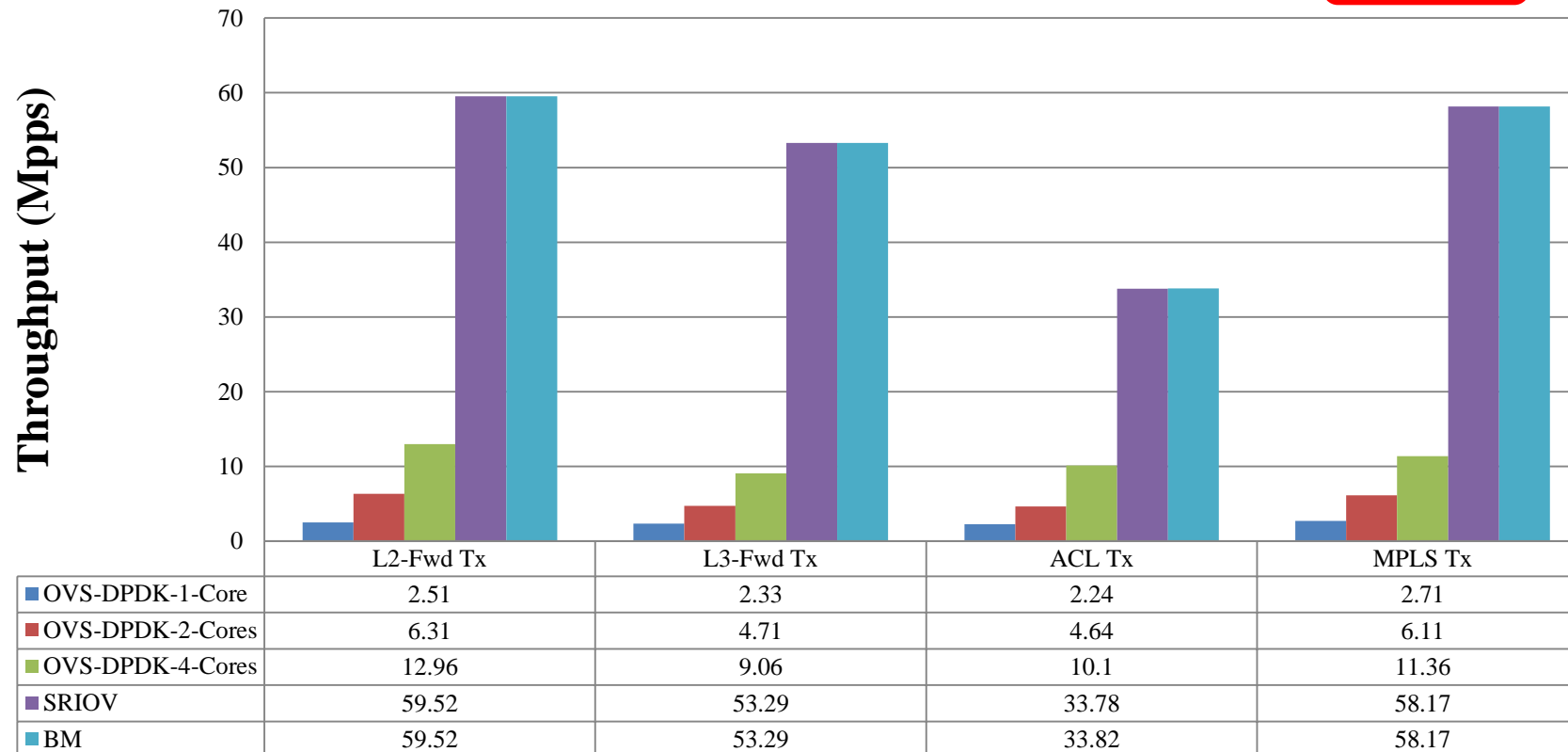
Baremetal vs SRIOV 4 Port - Throughput (64Bytes)



Baremetal vs SRIOV vs OVS-DPDK Performance Result

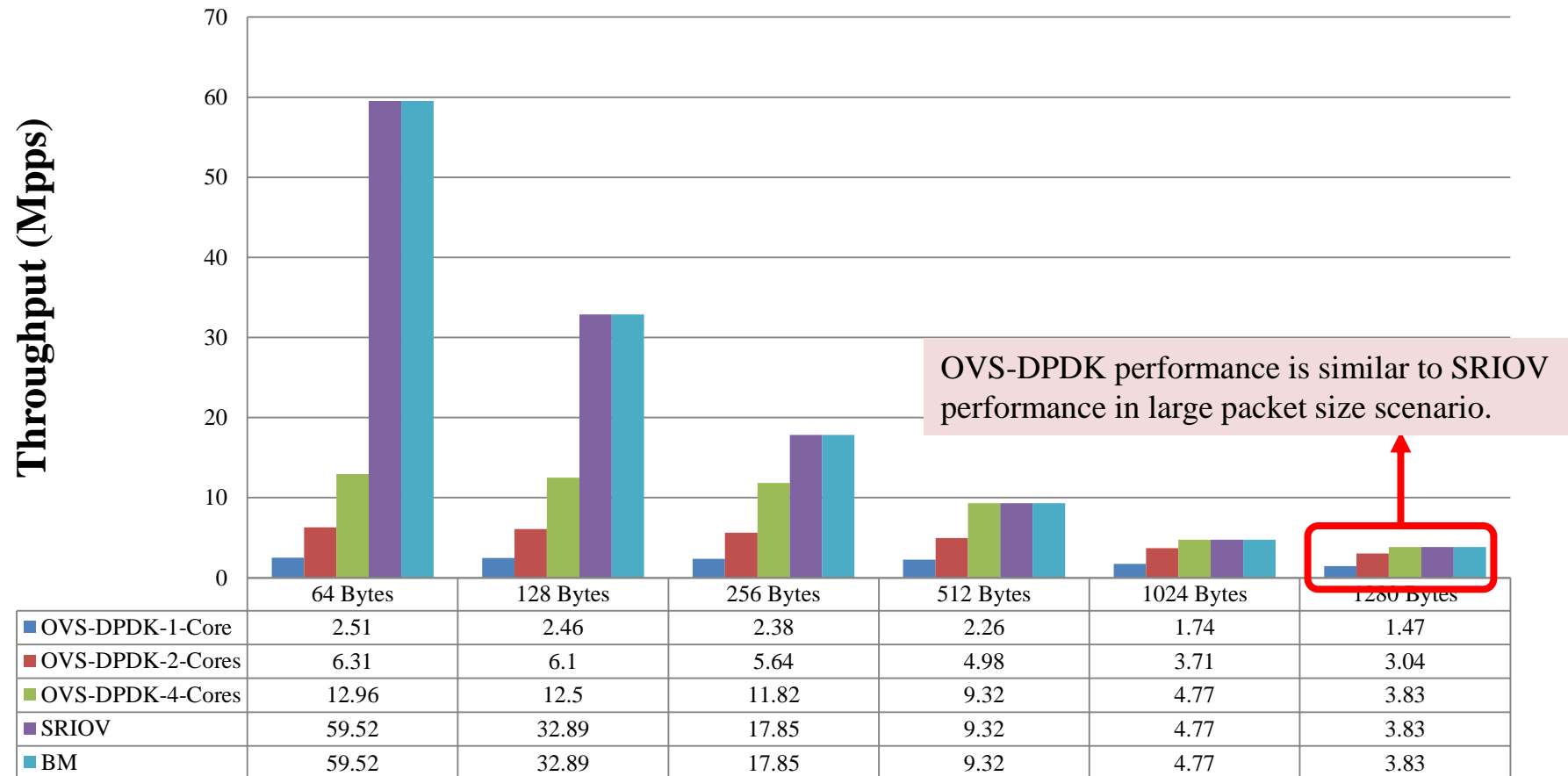
SRIOV could get better performance than OVS-DPDK in small packet size scenario.

OVS-DPDK vs SRIOV vs Baremetal 4 Port - Throughput (64Bytes)



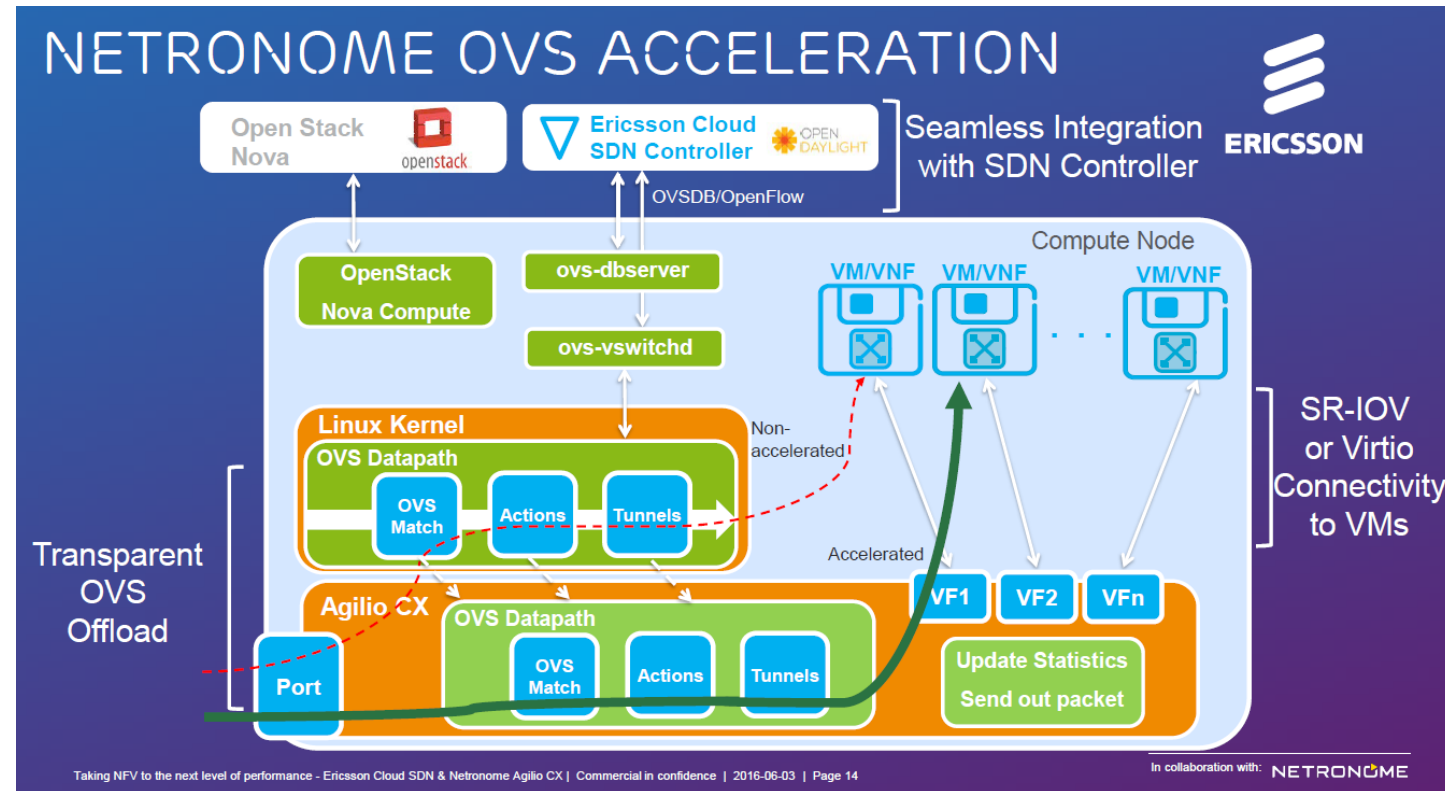
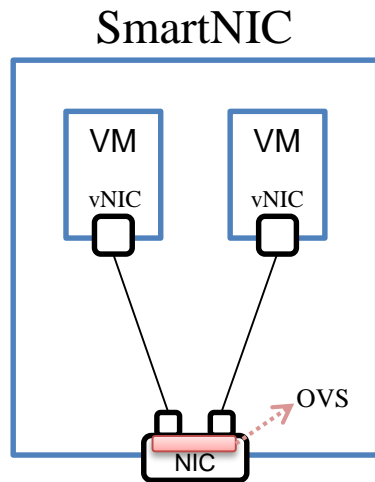
Baremetal vs SRIOV vs OVS-DPDK Performance Result

OVS-DPDK vs SRIOV vs Baremetal 4 Port - Throughput (L2-Fwd)



SmartNIC

- **Netronome SmartNIC**將OVS的功能做到硬體網卡中，可增加網路傳輸效能，並減少CPU資源的損耗。

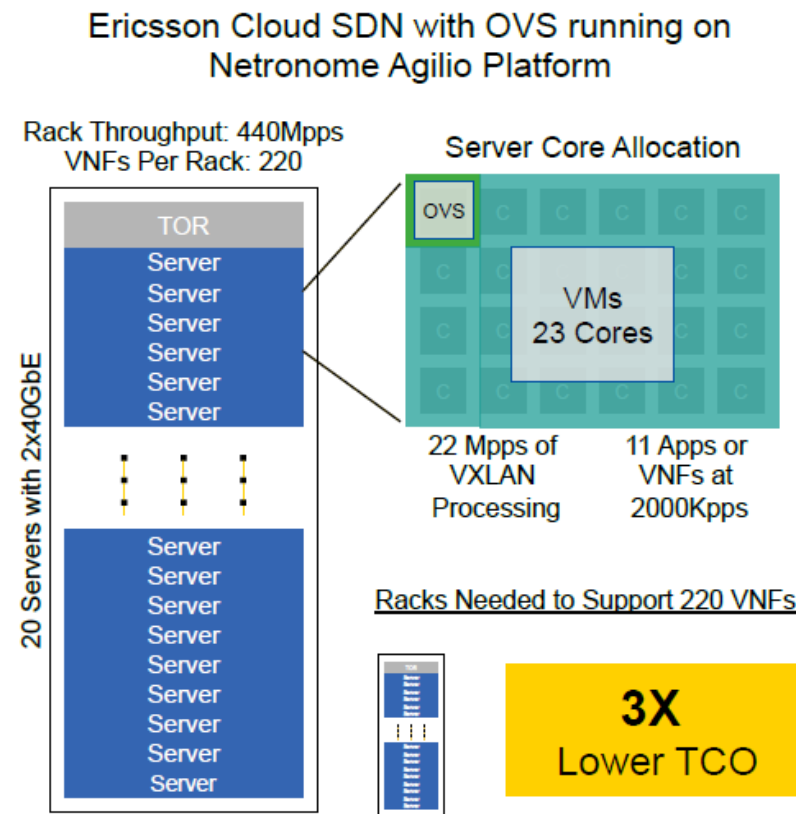
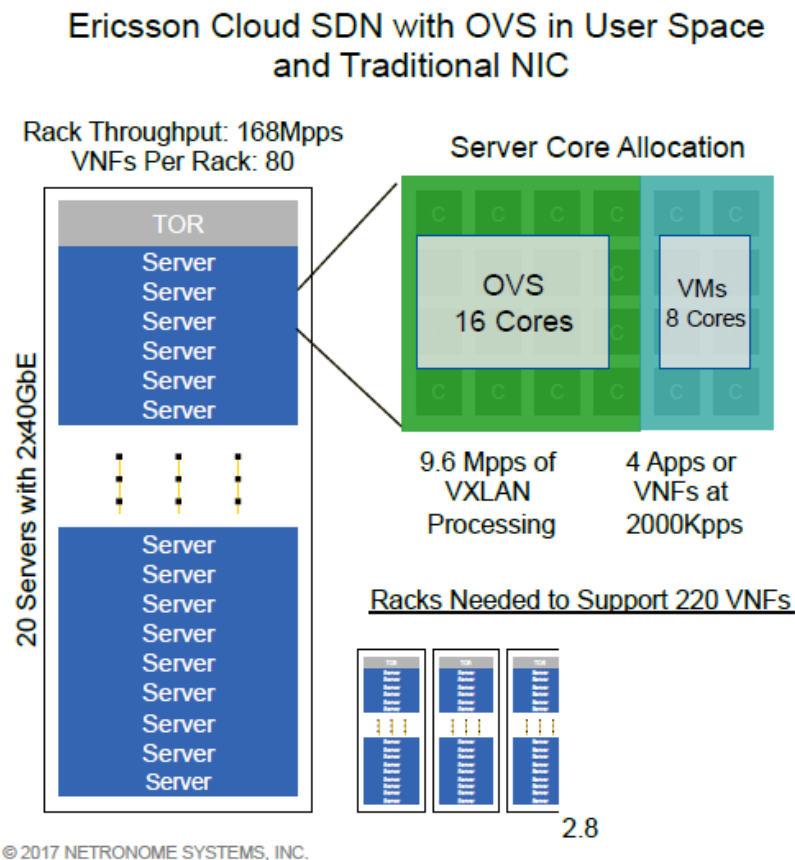


Source: <https://www.slideshare.net/Netronome/ericsson-cloud-sdn-netronome-agilio-cx-taking-nfv-to-the-next-level-of-performance>

Ericsson Cloud SDN & Netronome Agilio CX

NFV Use Case: 2,000Kpps per VNF or Application

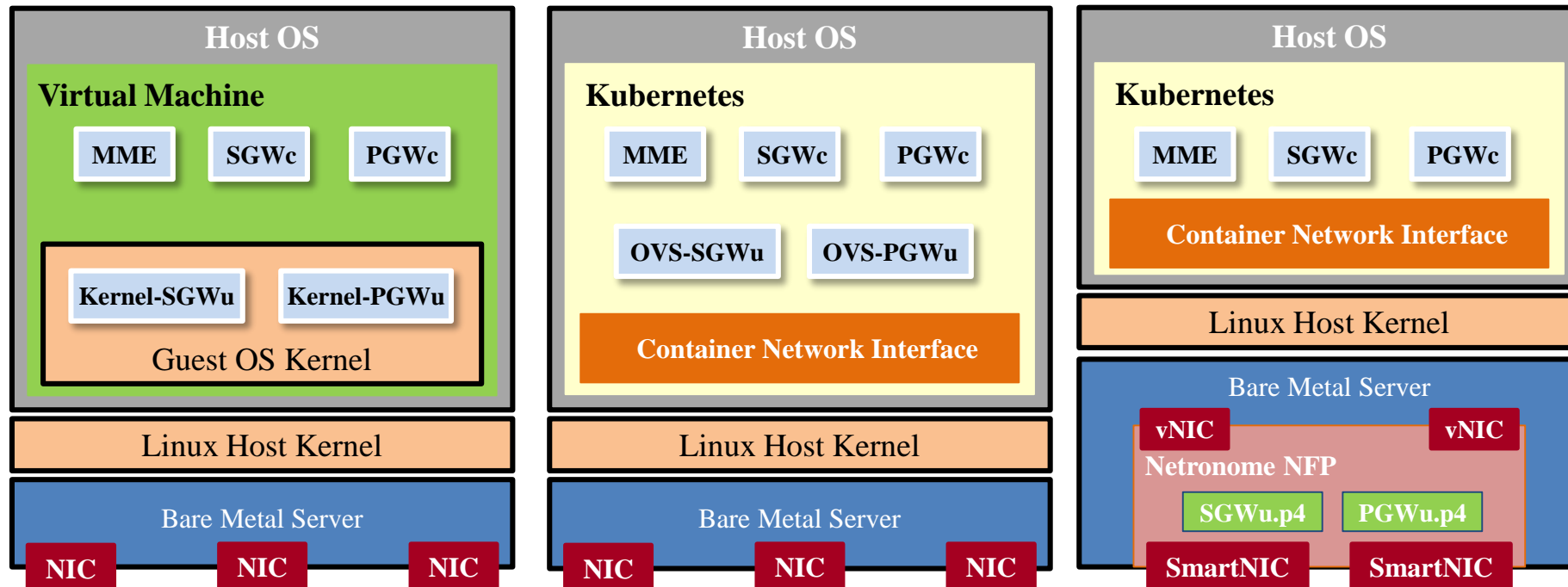
NETRONOME



Source: <https://www.slideshare.net/Netronome/ericsson-cloud-sdn-netronome-agilio-cx-taking-nfv-to-the-next-level-of-performance>

III vEPC Data Plane Enhancement

- 工研院協助資策會團隊優化vEPC的網路效能，並整合到NFVI平台。
- 三階段Data Plane效能優化：
 - Kernel-based GTPU data plane, throughput is about 800Mbps.
 - DPDK-based GTPU data plane, throughput is about 4Gbps.
 - SmartNIC-based GTPU data plane, throughput is about 9Gbps.
- 現今III 5GC的網路效能可達 25Gbps – 40Gbps



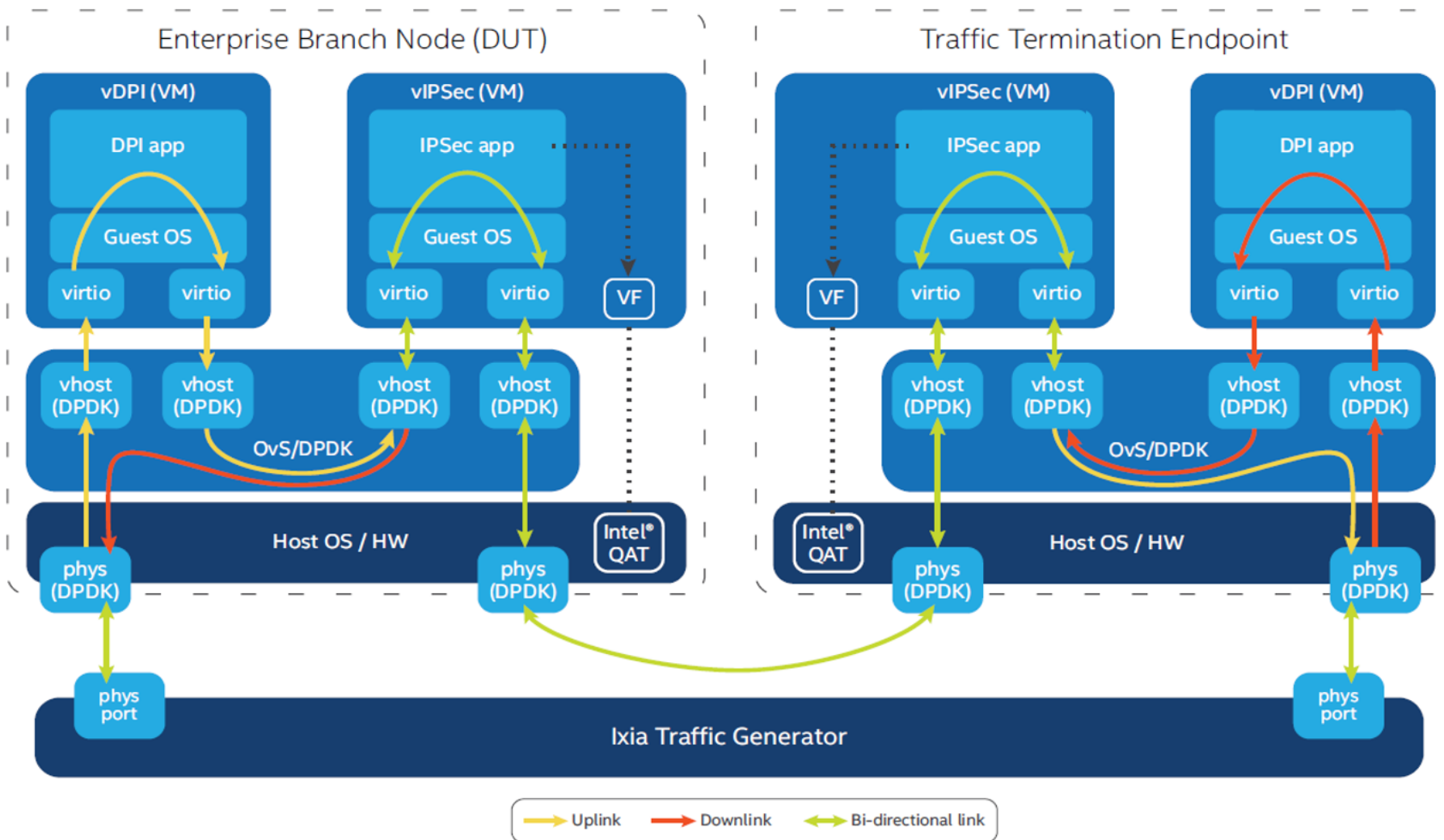


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Intel Atom Processor C3758 SDWAN Performance Report

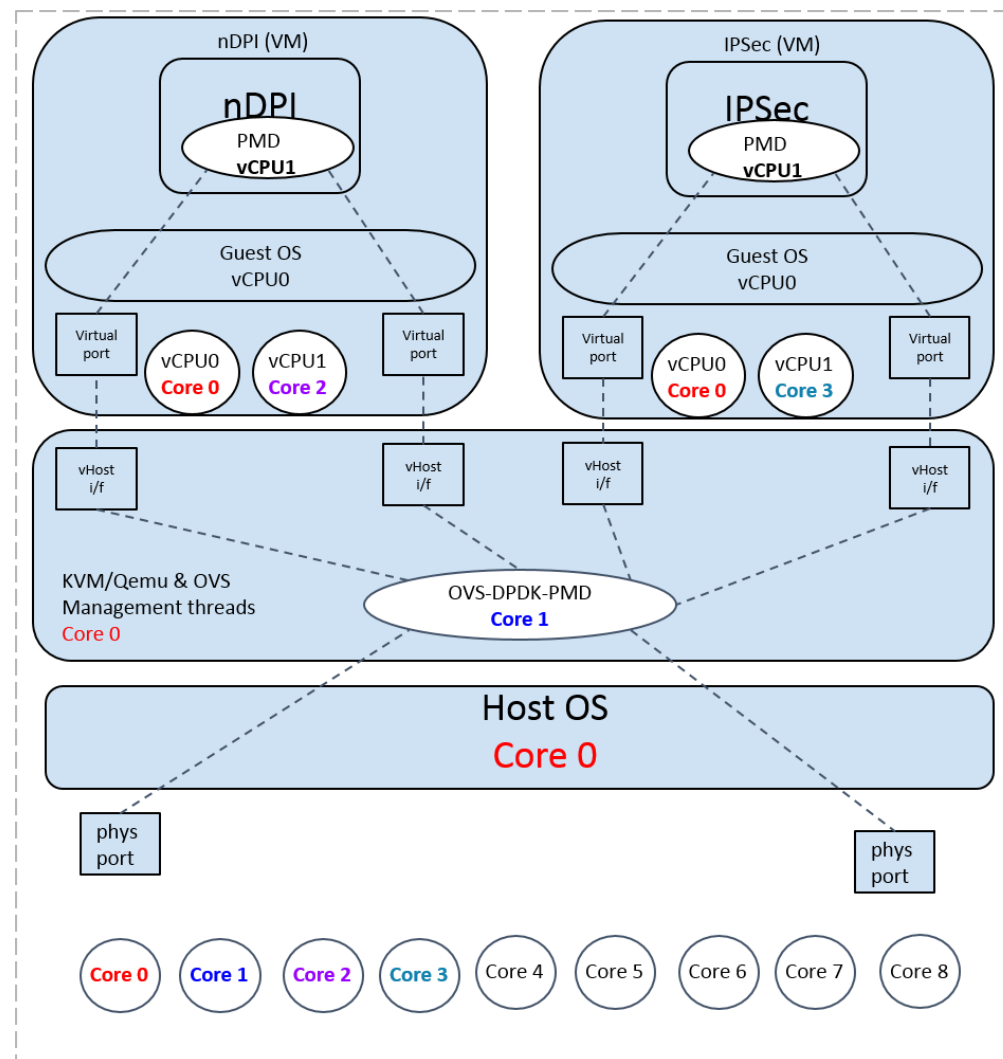
Produced by ITRI Performance Lab

SDWAN Topology



CPU Core Assignment – 4 Cores, 1 PMD Thread

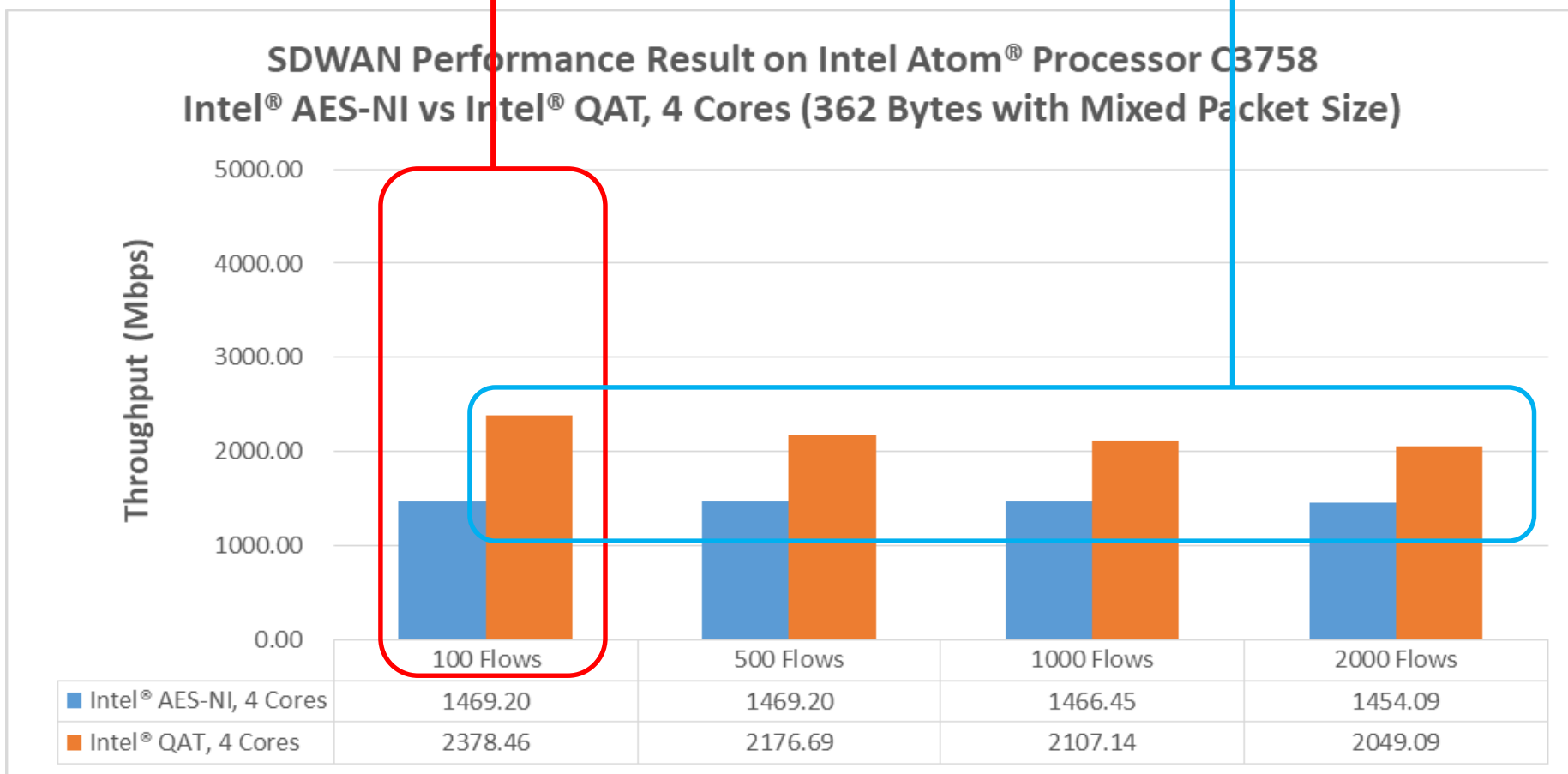
4-Core Configuration	
Host OS	Core 0
Hypervisor (KVM/Qemu)	Core 0
OVS Mgmt Threads	Core 0
OVS DPDK PMD	Core 1
DPI VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 2 (VM vCPU 1)
IPsec VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 3 (VM vCPU 1)



SDWAN Performance on 4 Cores Environment

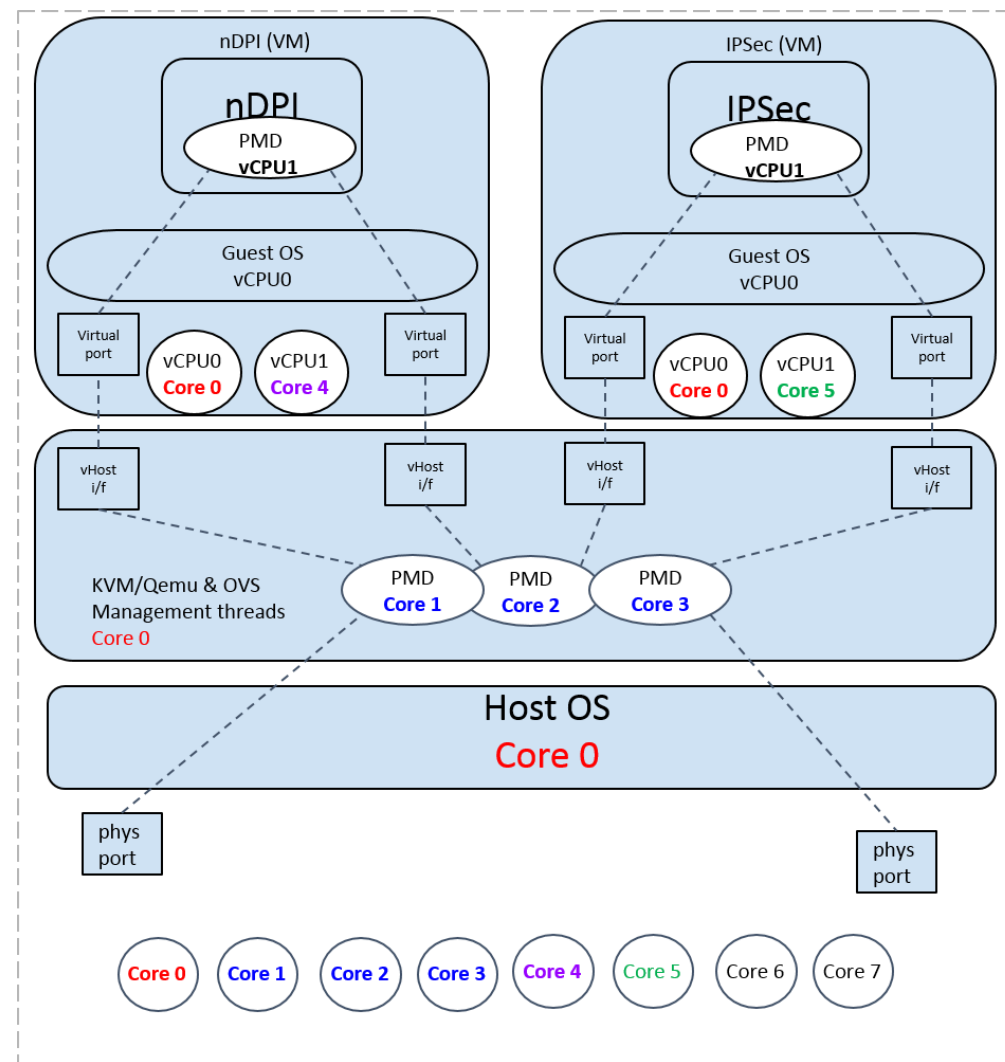
Use QAT accelerator can improve IPsec performance

QAT performance will be decrease when flow number is increase, OVS is the performance bottleneck.



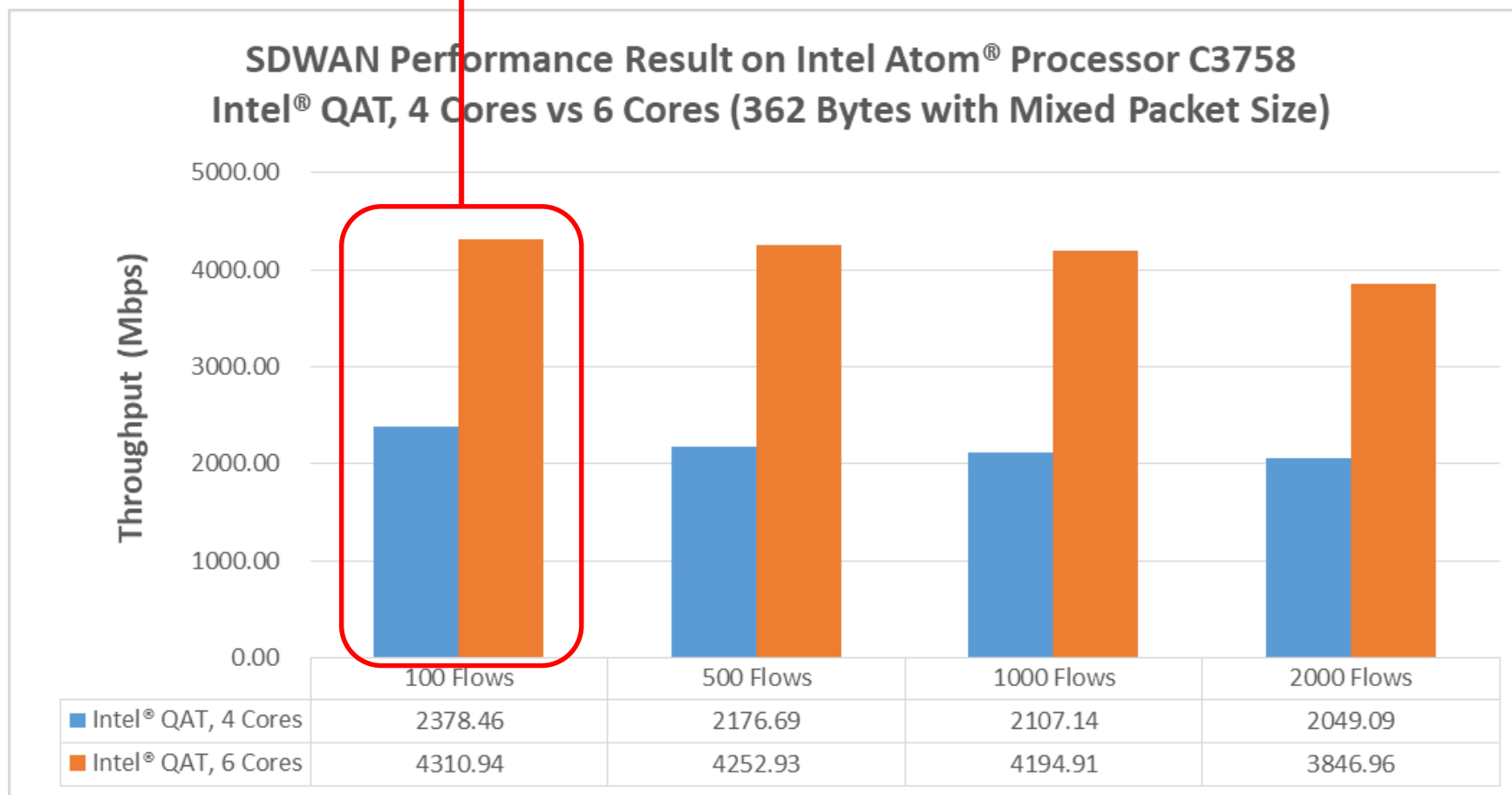
CPU Core Assignment – 6 Cores, 3 PMD Thread

6-Core Configuration	
Host OS	Core 0
Hypervisor (KVM/Qemu)	Core 0
OVS Mgmt Threads	Core 0
OVS DPDK PMD	Core 1 Core 2 Core 3
DPI VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 4 (VM vCPU 1)
IPsec VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 5 (VM vCPU 1)



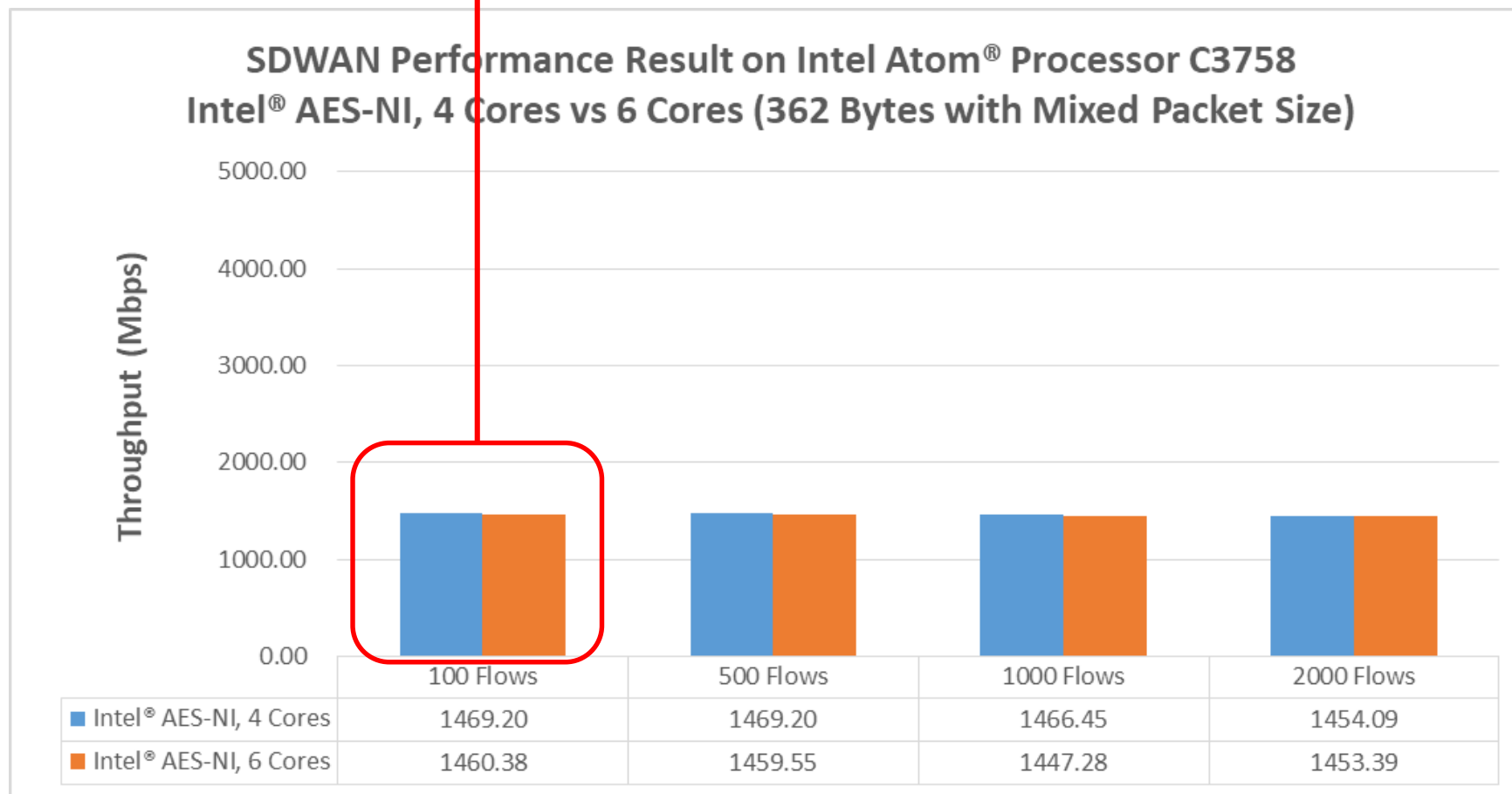
SDWAN Performance of QAT Scenario

QAT performance will be increase when we allocate more CPU core to OVS.



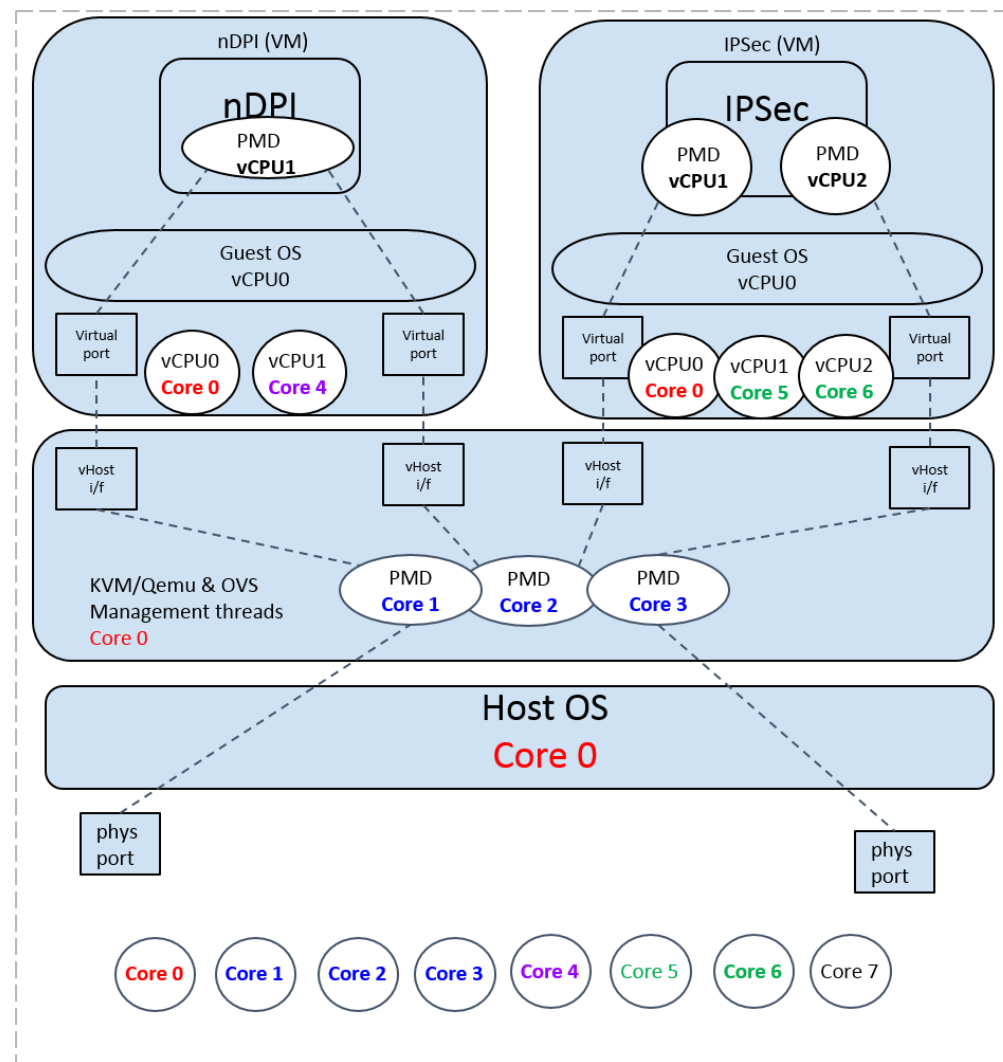
SDWAN Performance on 6 Core Environment

The performance of IPsec without QAT is almost the same with 4 core scenario, bottleneck is IPsec itself.



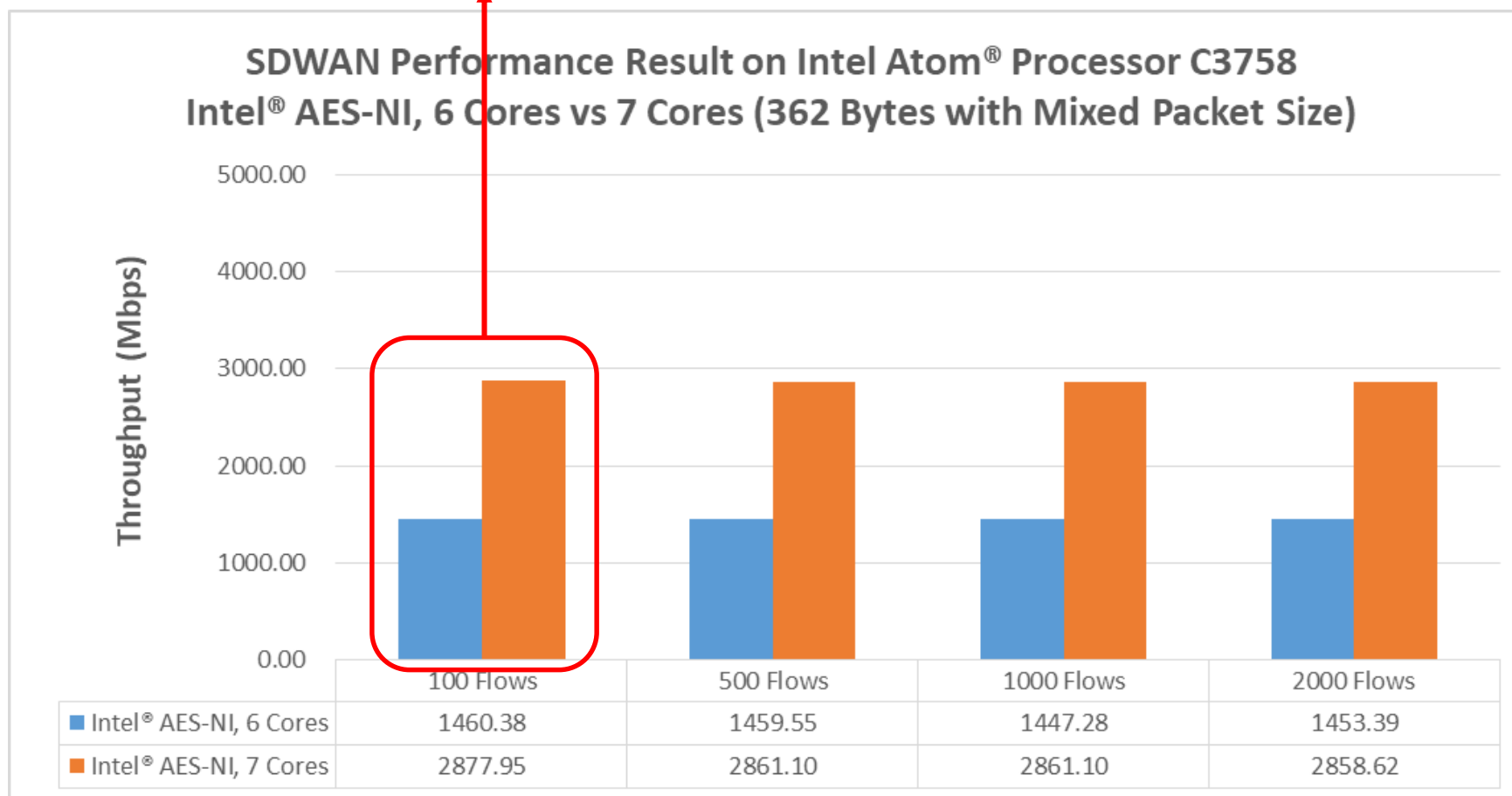
CPU Core Assignment – 7 Cores, 3 PMD Thread

7-Core Configuration	
Host OS	Core 0
Hypervisor (KVM/Qemu)	Core 0
OVS Mgmt Threads	Core 0
OVS DPDK PMD	Core 1 Core 2 Core 3
DPI VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 4 (VM vCPU 1)
IPsec VNF (vCPU threads)	Core 0 (VM vCPU 0), Core 5 (VM vCPU 1), Core 6 (VM vCPU 2)



SDWAN Performance of AES-NI Scenario

The performance of IPsec AES-NI will be increase when we allocate more CPU core to IPsec VNF.





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Intel Xeon Processor E5-2695 v4 Performance Report: 2-8 VMs Service Chain with SR-IOV, OVS-DPDK, VPP and SPP

Produced by ITRI Performance Lab

NTT's Presentation on DPDK Summit



The slide features a dark purple background. In the top right corner is the DPDK logo, which consists of a stylized orange and purple graphic followed by the text 'DPDK' in large white letters and 'DATA PLANE DEVELOPMENT KIT' in smaller orange letters below it. The main title 'Implementation and Testing of Soft Patch Panel' is written in large white font in the center. Below the title, the names 'Yasufumi Ogawa (NTT)' and 'Tetsuro Nakamura (NTT)' are listed in white, followed by 'DPDK Summit - San Jose – 2017'. In the bottom right corner, there is a photograph of a modern building with a prominent blue dome and orange walls, surrounded by palm trees and other greenery.

DPDK
DATA PLANE DEVELOPMENT KIT

Implementation and Testing of Soft Patch Panel

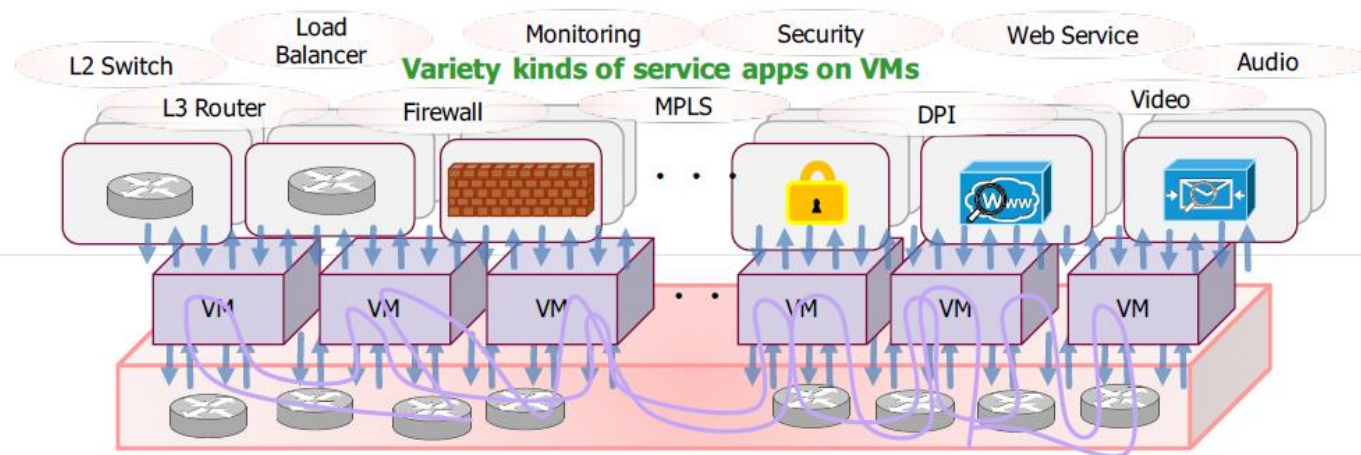
Yasufumi Ogawa (NTT)
Tetsuro Nakamura (NTT)
DPDK Summit - San Jose – 2017

VM Chaining Scenario

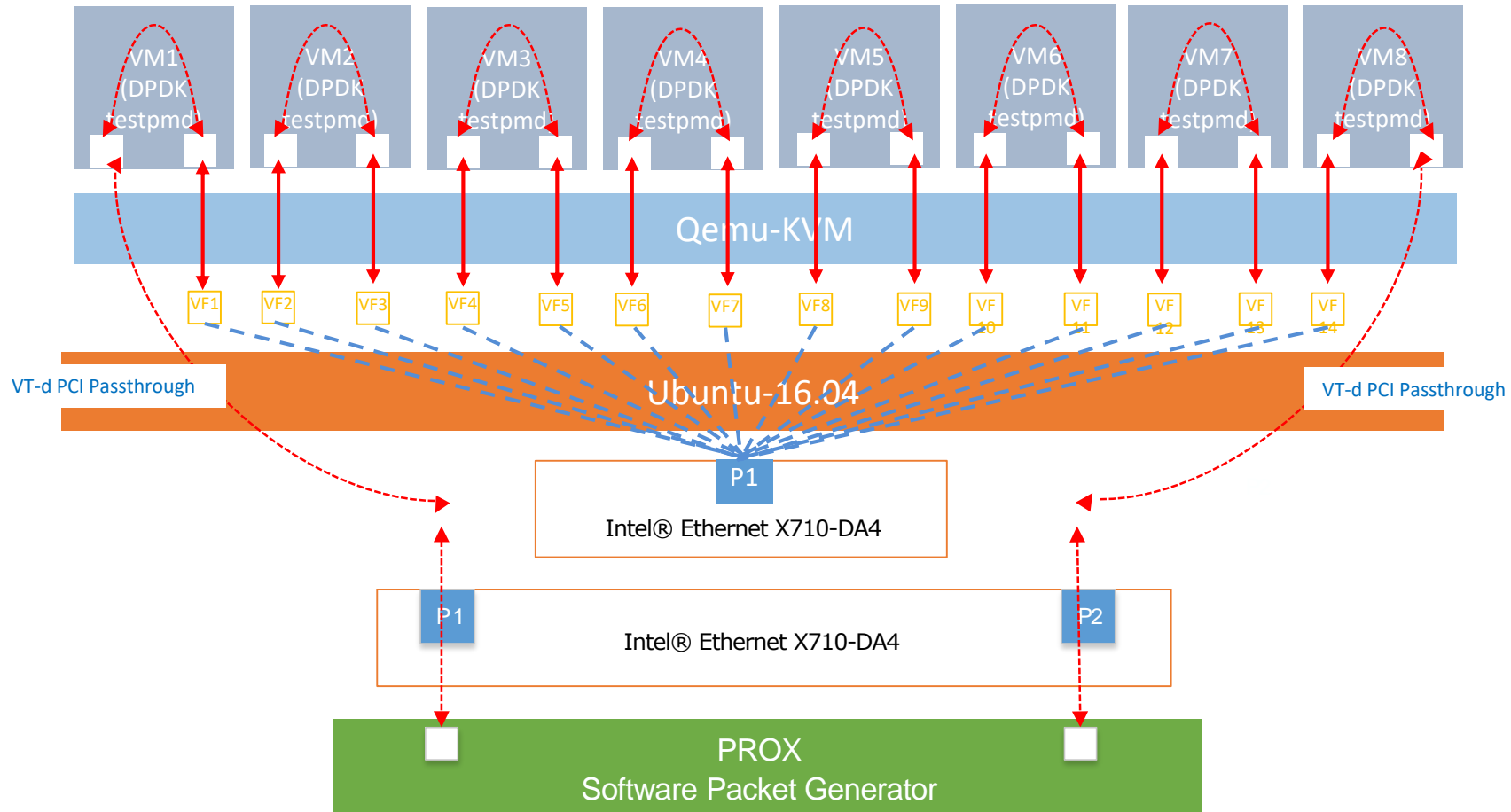
Motivation



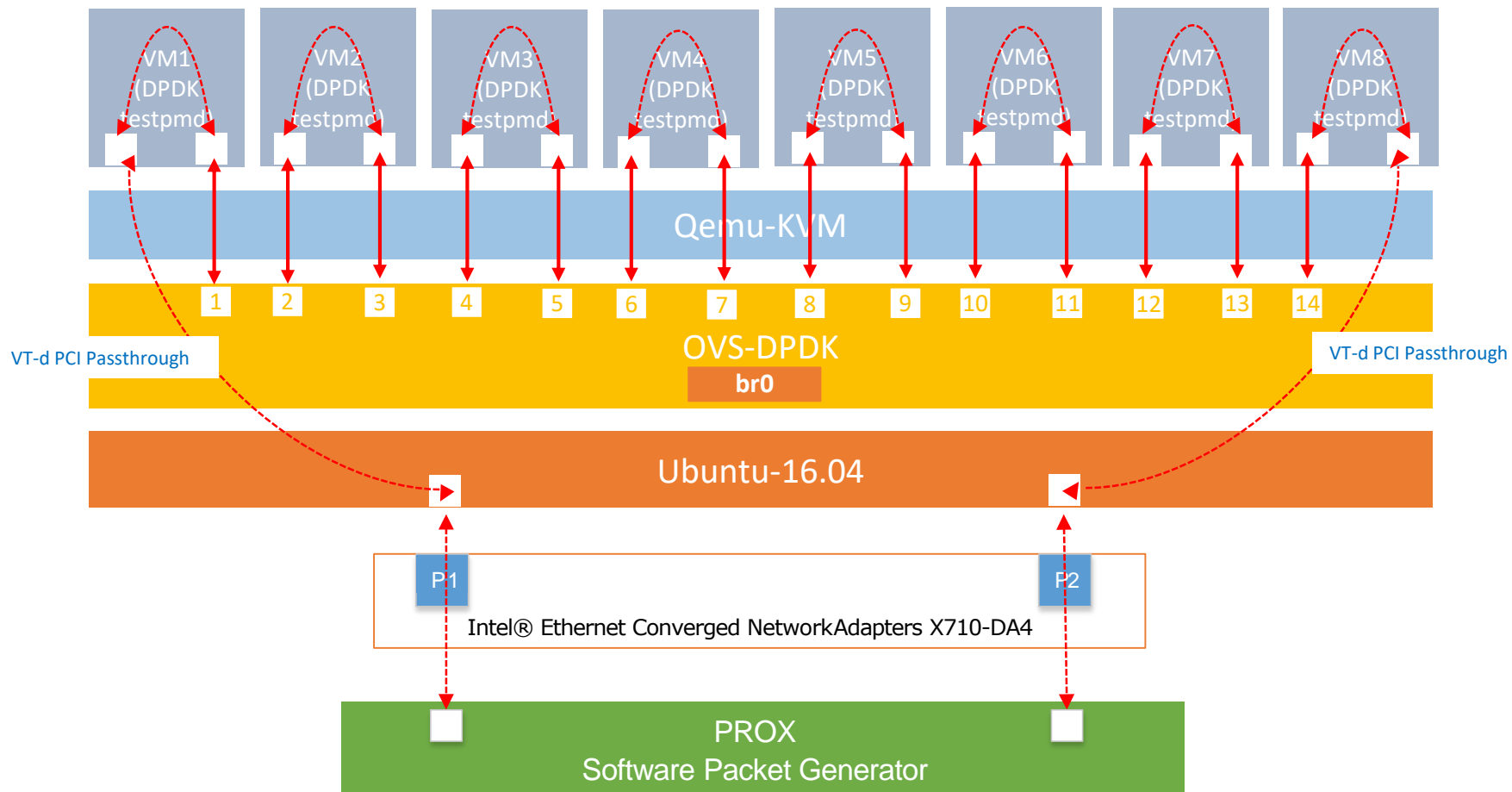
- ▶ Large-scale cloud for telecom services
- ▶ Service Function Chaining for virtual network appliances
- ▶ Flexibility, Maintainability and High-Performance



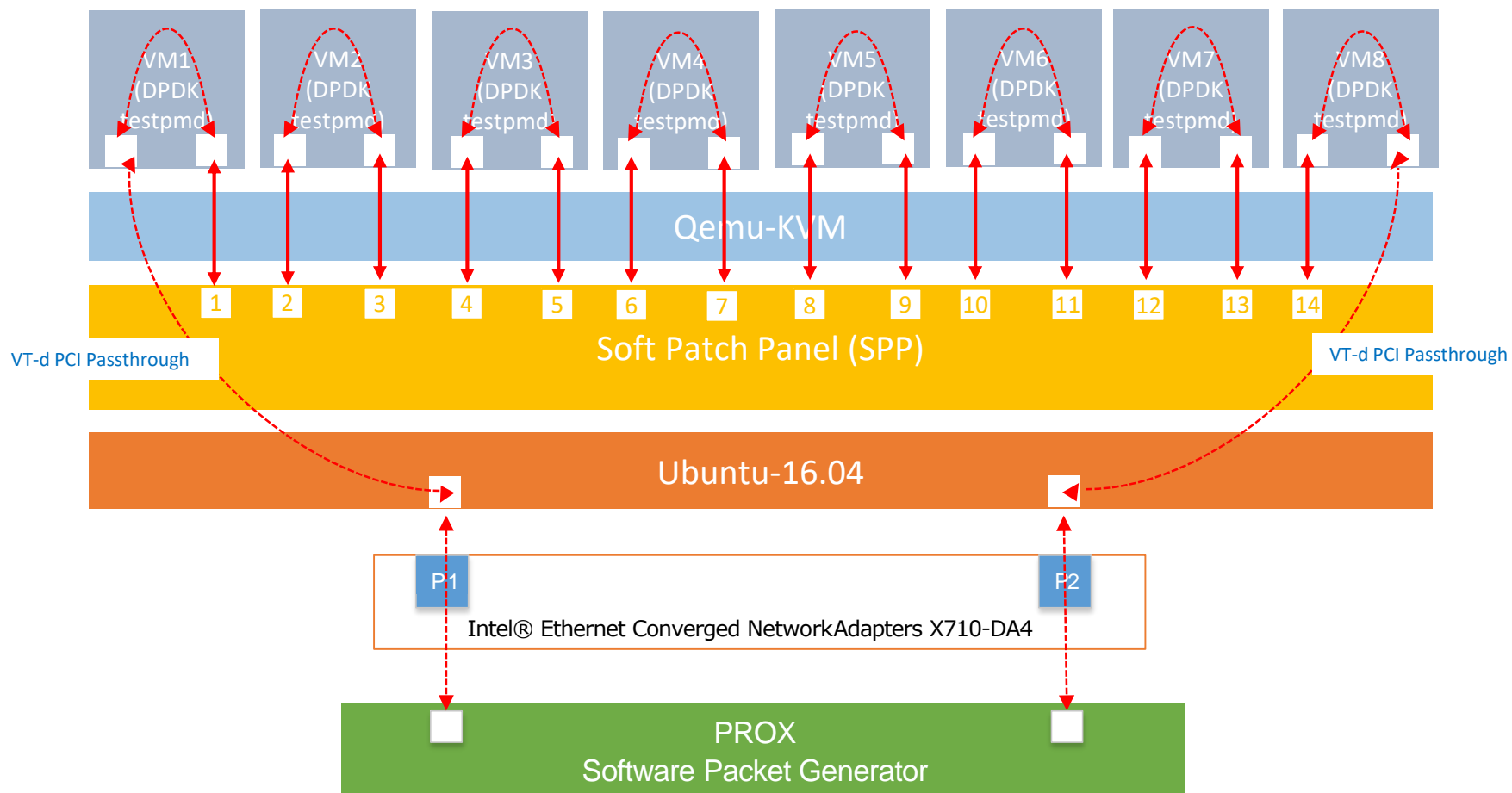
8 VMs Service Chain Test Setup Diagram (SRIOV)



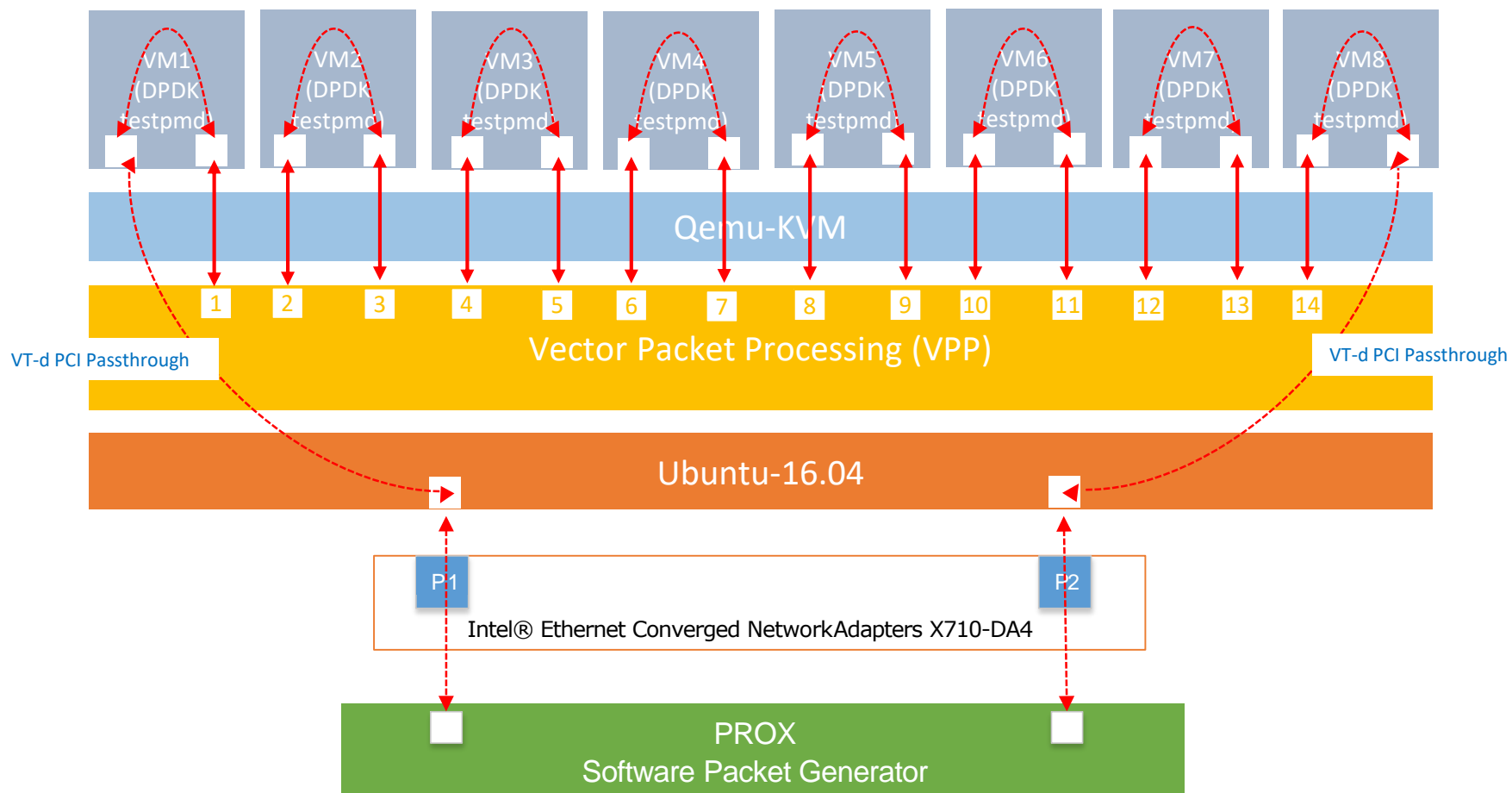
8 VMs Service Chain Test Setup Diagram (OVS-DPDK)



8 VMs Service Chain Test Setup Diagram (SPP)



8 VMs Service Chain Test Setup Diagram (VPP)





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Performance Result : Summary

2 to 8 VMs Service Chain Performance
64 Byte, 10K Flow
(Bi-Direction, total 20G)

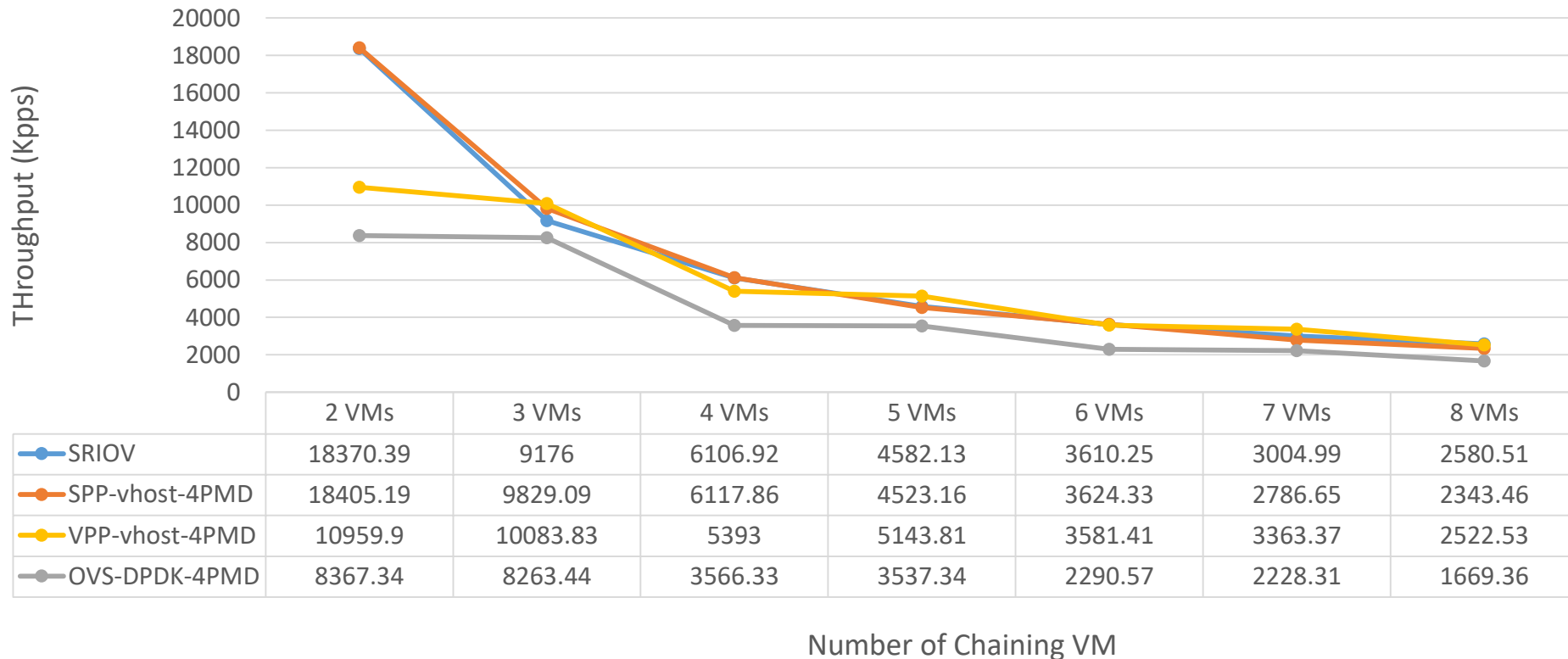
Binary-Search Pktgen



2 to 8 VMs Service Chain Performance: 64 Bytes, 10K Flow, Bi-Direction, Packet per second

SRIOV's performance is not good in VM chaining scenario,
the bottleneck is NIC's limitation.

Phy-VM-Phy Core Scalability Performance running 10K Flows on
Intel® Xeon® Processor E5-2695 v4
Multiple VM Service Chain (64Byte, 10K Flow, Bi-direction)





Performance Result : OVS-DPDK

2 to 8 VMs Service Chain Performance
64 Byte, OVS-DPDK, 4 PMD
with Different number of Flow
(Single Direction 10G / Bi-Direction 20G)

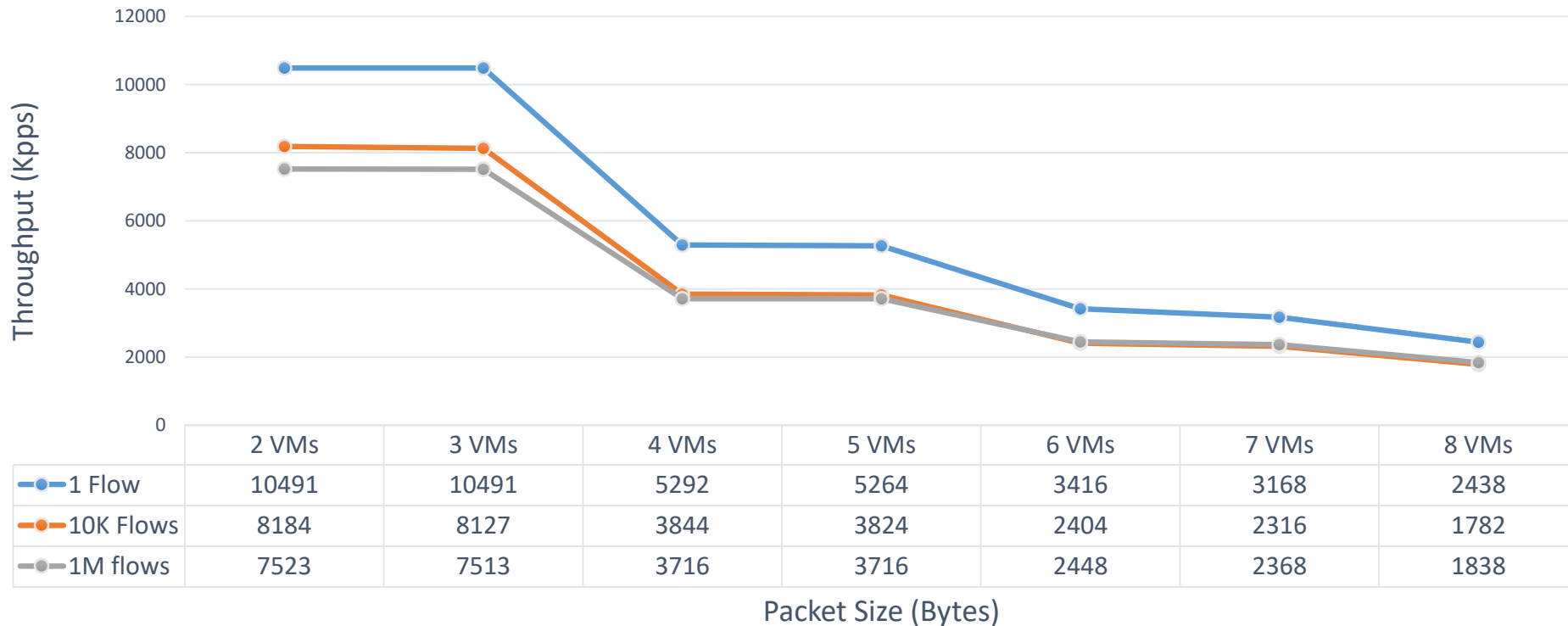
Full-Speed Pktgen



2 to 8 VMs Service Chain Performance: 64 Bytes, OVS-DPDK, 4 PMD, Single Direction

OVS performance will be effected by flow number, it may cause 20% performance decrease.

Phy-VM-Phy Core Scalability Performance running Different Flows on
Intel® Xeon® Processor E5-2695 v4
Multiple VM Service Chain (64 Bytes, OVS-DPDK, 4 PMD, Bi-direction)



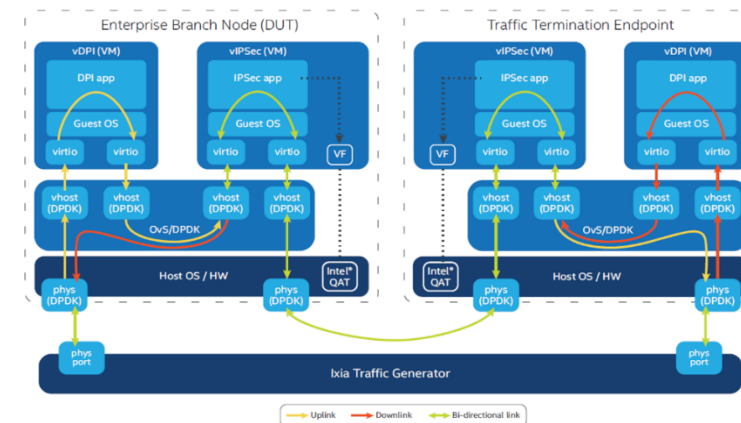
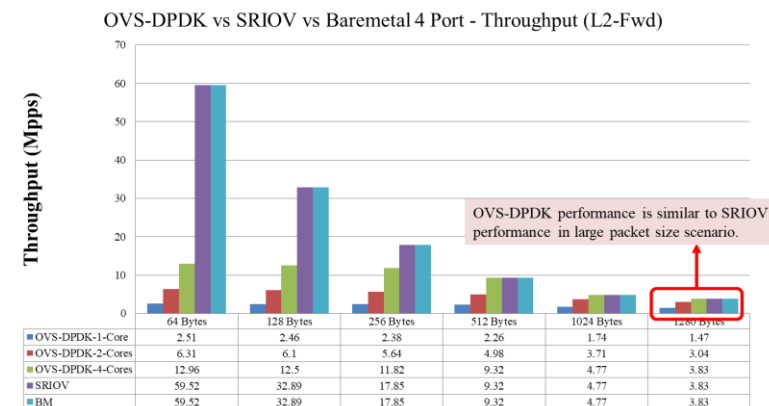
NFV Performance Lab

Features

- VM/Container Performance Tuning
 - CPU Pining
 - NUMA configuration
 - BIOS configuration
- Data Plane Acceleration
 - SRIOV, SmartNIC
 - Enable DPDK (OVS-DPDK, VPP, SPP)
 - QAT, Intel AES-NI
- Scenario / Use Cases
 - NFVI / VNF performance characterization
 - SDWAN scenario (uCPE, DPI, IPSEC)
 - VM Chaining with different data plane

Contribution

- Help ODM/OEM vendors build their own NFV performance lab, enhance their NFV performance optimization and testing skills.
- Help hardware and software vendors optimize their NFV product performance and publish performance white papers.
- Help operators evaluate and analysis performance bottleneck on specific NFV scenarios.



總結

- 影響NFV網路效能的因素眾多，也涵蓋多個領域，包含加速卡、系統架構、資源配置、軟體效能等，在本課程中，主要進行NFV效能實驗室執行過程的經驗分享，也介紹如何透過標準化的測試流程，來比較不同網路加速方案的效能差異。
- 使用正確的網路架構與加速方案來實現網路功能的虛擬化，並滿足商用上的效能需求只是第一步，如何做好虛擬化網路功能的管理與維運才是NFV長期且重要的課題。
- 本課程是根據講師在工研院執行NFV效能實驗室的經驗分享，後續如果有任何問題需要討論或交流，可與講師聯絡，聯絡資訊如下：
 - 工研院資通所技術經理 李育緯
 - Email: rayinlee@itri.org.tw