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Signal integrity research of high-speed interconnection systems based on scattering parameters

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As an important characteristic of a signal transmission network, scattering parameters can accurately reflect the signal transmission situation. By establishing a circuit model based on scattering parameters for the signal path unit, studying the signal attenuation and reflection curves of components including transmission lines, transmission media, vias, high-speed connectors, and transceiver termination devices, a circuit simulation model completely based on scattering parameters is proposed. This model can be parametrically adjusted according to the requirements of actual circuit implementation, and accurately reflect the high-speed signal transmission quality of the final circuit. This circuit simulation model is applied to the high-speed 5G small base station system. The transceiver performance of the modular circuit model completely based on scattering parameters and the scattering parameter model extracted based on board-level implementation is compared. The results show that the modular circuit completely based on scattering parameters can accurately match the channel communication indicators of board-level implementation.

Keywords Scattering parameters, Characteristics of transmission lines, Signal integrity, Eye diagram, Insertion loss

With the development of technologies such as artificial intelligence, high-performance computing, cloud computing, and ultra-high-speed networks, massive amounts of computing and transmission data have created an urgent demand for high-speed data transmission systems. The high-speed serializer/deserializer (serdes) technology has broken through 224 Gb/s, and high-speed data processing units such as Central Processing Unit (CPU), Graphics Processing Unit (GPU), and Data Processing Unit (DPU) are interconnected through serdes technology to form high-speed interconnection systems. The signal transmission quality of the interconnection systems has become crucial[1]. In recent years, both at home and abroad, the research on high-speed signal integrity has remained hot, mainly focusing on areas such as transmission line theory, high-speed signal simulation tools, high-speed signal measurement and testing equipment and their corresponding technologies, high-speed connector technology, and high-speed signal equalization algorithms[2].

The high-speed interconnection system encompasses complete end-to-end transmission module units, including Power Distribution Network(PDN), high-speed signal transceiver units (chip Serdes interfaces), transmission channels (print circuit boards, cables), transmission lines (strip-lines, micro-strip lines), and high-speed connectors (backplane interconnections). Each module unit will directly affect the transmission quality of high-speed signals. The line characteristics of the entire high-speed interconnection system from the source end to the terminal can be characterized by scattering parameters (S-parameters)[3]. S-parameters describe the frequency domain characteristics of the transmission channel, from which most of the useful information for signal integrity analysis can be obtained. Studying S-parameter modeling and simulation can predict the signal transmission problems of the complete system in the early stage of system design and can also evaluate system performance during the entire implementation process of the scheme. It is one of the effective means to ensure the transmission quality of high-speed signals.

In recent years, with the technological development and wide application of high-speed signals, significant progress has also been made in the research and application of S-parameters[4]. Mainly based on the theoretical model research of S-parameters, new ideas have been constantly introduced to adapt to more complex circuit structures and higher frequency requirements. New algorithms have been studied in microwave devices and antenna arrays to establish accurate S-parameter models to meet the needs of emerging technological fields[5,6]. In addition, combined with advanced technologies such as artificial intelligence and machine learning, S-parameter

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data are learned and analyzed to quickly and accurately predict circuit performance, etc[7–9]. Moreover, the S-parameter modeling methods have been continuously innovated, and the de-embedding technology has been used for circuit design and testing[10–12]. Breakthroughs have also been made in the development of domestic software and tools, and there are S-parameter analysis and testing tools with independent intellectual property rights to meet the domestic industry's demand for S-parameter analysis[13,14]. In addition, in the field of technology application, in circuit design, including radio frequency circuits, integrated circuit technology, and high-speed digital interconnection systems, by using S-parameter modeling and continuous optimization, the performance and quality of products can be effectively controlled in key fields such as domestic aerospace and national defense, so as to achieve good economic and social benefits[15].

This article mainly focuses on S-parameters as a key technical means in high-speed interconnection systems. It uses circuit simulation tools to analyze the signal integrity problems in the implementation process of high-performance high-speed interconnection systems. Combined with the key factors affecting the frequency domain characteristics of transmission channels, the transmission performance of the entire interconnection system is optimized. Through circuit modeling, the characteristics such as the transmission line effect of high-speed signals, via models, and layer stack parameters are analyzed and optimized. Compared with Print Circuit Board (PCB) design, this model has a very high degree of matching. Therefore, this model has high credibility and can be used for modeling the complete high-speed interconnection system to evaluate the quality of the transmission system in advance. Currently, there are relatively few studies on the credibility of S-parameter-based modeling and simulation for high-speed interconnection systems, and there are even no comparison results. Through researching the decisive factors that affect the signal integrity of high-speed systems, this paper improves and optimizes the quality of signal transmission and further demonstrates the accuracy of the simulation model. This key technology is applied to the Serdes interconnection system of the 5G small base station platform to ensure the quality of high-speed signal transmission, thus expecting to improve the performance and quality of the platform. This simulation platform can directly reflect the signal quality problems of the high-speed interconnection system without implementing the circuit and physical layout and routing, so that the circuit results to be achieved by the future structure of the interconnection system can be predicted in advance.

Research on S-parameters of Serdes differential signals

With the development of high-speed Serdes technology, the single-channel rate has been able to reach 64G-128 Gbit/s. By adopting the differential signal transmission technology, high-speed data transmission over longer distances can be achieved. Combined with the Pulse Amplitude Modulation 4-level (PAM-4) code pattern of more advanced coding and modulation technologies, a higher data rate is obtained in exchange for an extremely low signal amplitude, enabling more data to be transmitted under the same bandwidth conditions. Meanwhile, the signal integrity problems caused by the increase in signal transmission distance and the decrease in voltage amplitude have become more and more serious. At the beginning of system design, for high-speed differential Serdes interconnection systems, including the schemes for interconnections between chips and for backplane interconnections, the signal transmission quality can be evaluated through S-parameter circuit modeling to demonstrate the feasibility of the interconnection schemes. During the system implementation process, that is, during the process of completing circuit design and PCB layout and routing, the circuit parameters can also be extracted by using Electronic Design Automation (EDA) software such as Keysight ADS, a simulation model can be established, the system performance can be evaluated, and optimization measures can be proposed to improve the signal integrity problems of the system.

Another equivalent description of the differential signal is the differential pair, also known as the mixed-mode S-parameter[16,17]. The signal types are differential signals and common-mode signals. The conversion relationship between the mixed-mode S-parameter and the single-ended S-parameter is shown in Table 1. Among them, the S-parameter of two-port network is shown in Fig. 1, the expression is shown in Eq. (1)[18].

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1} = \frac{V_{reflected\ at\ Port1}}{V_{towards\ Port1}}\Big| a_2 = 0 \quad S_{12} = \frac{b_1}{a_2} = \frac{V_{out\ at\ Port1}}{V_{towards\ Port2}}\Big| a_1 = 0 \\ S_{21} &= \frac{b_2}{a_1} = \frac{V_{out\ at\ Port2}}{V_{towards\ Port1}}\Big| a_2 = 0 \quad S_{22} = \frac{b_2}{a_2} = \frac{V_{reflected\ at\ Port2}}{V_{towards\ Port2}}\Big| a_1 = 0 \end{aligned} \tag{1}$$

S_{11} represents the reflection coefficient of port 1, that is, when a signal is input from port 1, the ratio of the amplitude of the signal reflected back at port 1 to the amplitude of the input signal. S_{21} represents the forward transmission coefficient, that is, when a signal is input from port 1, the ratio of the amplitude of the signal transmitted to port 2 to the amplitude of the input signal; similarly, S_{12} is the reverse transmission coefficient, which reflects the situation when a signal is input from port 2 and transmitted to port 1, and S_{22} is the reflection coefficient of port 2. S_{DD} is used to represent the input and output of differential signals, S_{CC} is used to represent the input and output of common-mode signals, S_{CD} is used to represent the input of differential signals and the output of common-mode signals, and S_{DC} is used to represent the input of common-mode signals and the output of differential signals. The mixed-mode S-parameter describes the interaction between differential and common-mode signals at the ports of two differential pairs. S_{DD11} and S_{DD22} represent the return loss of the differential pair, and S_{DD12} represents the insertion loss of the differential pair. S_{DD12} is the most important S-parameter element, and it shows a decreasing trend as the frequency increases. The main reasons are conductor and dielectric losses. In addition, factors such as signal passing through layers and the impedance discontinuity of vias can cause fluctuations in S_{DD12}.

According to the transmission line theory, the insertion loss (IL) of a signal is defined as the logarithmic form of the ratio of the input power to the output power, that is, $\mathrm{IL} = -20\log|\mathrm{S}_{21}|$, and it is usually expressed in decibels (dB). It can be seen that S_{21} or $\mathrm{S}_{\mathrm{DD21}}$ is directly related to the insertion loss[19]. For a two-port

Diff–Diff		**Common–Diff**	
$S_{DD11} = 0.5[S_{11} - S_{13} - S_{31} + S_{33}]$	$S_{DD12} = 0.5[S_{12} - S_{14} - S_{32} + S_{34}]$	$S_{DC11} = 0.5[S_{11} + S_{13} - S_{31} - S_{33}]$	$S_{DC12} = 0.5[S_{12} + S_{14} - S_{32} - S_{34}]$
$S_{DD21} = 0.5[S_{21} - S_{23} - S_{41} + S_{43}]$	$S_{DD22} = 0.5[S_{22} - S_{24} - S_{42} + S_{44}]$	$S_{DC21} = 0.5[S_{21} + S_{23} - S_{41} - S_{43}]$	$S_{DC22} = 0.5[S_{22} + S_{24} - S_{42} - S_{44}]$
Diff–Common		**Common–Common**	
$S_{CD11} = 0.5[S_{11} - S_{13} + S_{31} - S_{33}]$	$S_{CD12} = 0.5[S_{12} - S_{14} + S_{32} - S_{34}]$	$S_{CC11} = 0.5[S_{11} + S_{13} + S_{31} + S_{33}]$	$S_{CC12} = 0.5[S_{12} + S_{14} + S_{32} + S_{34}]$
$S_{CD21} = 0.5[S_{21} - S_{23} + S_{41} - S_{43}]$	$S_{CD22} = 0.5[S_{22} - S_{24} + S_{42} - S_{44}]$	$S_{CC21} = 0.5[S_{21} + S_{23} + S_{41} + S_{43}]$	$S_{CC22} = 0.5[S_{22} + S_{24} + S_{42} + S_{44}]$

Table 1. Conversion relationship between single-ended and mixed-mode S-parameters.

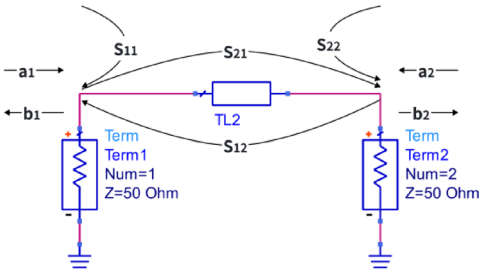


Fig. 1. S-parameters of two-port network.

network, if the characteristic impedance of the transmission line is Z_0, the length is l, and the propagation constant is $\gamma = \alpha + j\beta$ (where α is the attenuation constant and β is the phase shift constant), then $S_{21} = e^{-\gamma l} = e^{-\alpha l} e^{-j\beta l}$.

The attenuation constant $\alpha = \alpha_c + \alpha_d$, where α_c is the conductor loss, which is related to the resistance R of the transmission line, the characteristic impedance Z_0, and the frequency. The approximate formula is $\alpha_c = \frac{R}{2Z_0}\sqrt{\frac{\mu}{\varepsilon}}$, where μ is the magnetic permeability and ε is the dielectric constant. α_d is the dielectric loss, which is related to the dielectric loss tangent $\tan\delta$ and the frequency f. The approximate formula is $\alpha_d = \frac{\pi f\sqrt{\varepsilon_r}\tan\delta}{c}$, where c is the speed of light and ε_r is the relative dielectric constant. Thus, the attenuation constant $\alpha = \frac{R}{2Z_0}\sqrt{\frac{\mu}{\varepsilon}} + \frac{\pi f\sqrt{\varepsilon_r}\tan\delta}{c}$.

The phase shift constant $\beta = \omega\sqrt{\mu\varepsilon}$, where $\omega = 2\pi f$. β only affects the phase of the signal and does not have an impact on the signal amplitude, but it will comprehensively affect the system performance.

When there is reflection in the system, the reflected wave will interact with the incident wave and will indirectly affect the amplitude of the transmitted signal. Considering the reflection situation, according to Mason's formula, $S_{21} = \frac{1}{1-S_{11}S_{22}}e^{-\gamma l}$. When the load impedance Z_l is equal to the transmission line impedance Z_0, that is, the so-called impedance matching, S_{11} and S_{22} are close to 0, and the insertion loss is minimized.

Interconnection systems are often the interconnection of multiple two-port or multi-port networks. The total S_{21} parameter is equivalent to the product of each S_{21} parameter. According to the rules of logarithmic operations, the insertion loss of the total network is the sum of the insertion losses of each two-port network.

Based on the above analysis, it can be known that the main influencing factors for the insertion loss of the interconnection system include the attenuation constant α, the length l of the transmission line, the cascade order of ports, port impedance matching, and so on[20]. It is recommended to use high-quality substrates with smaller loss tangent values and dielectric constants to reduce the attenuation constant and improve the transmission performance. In addition, studies have shown that increasing the line width will reduce the differential impedance, thereby reducing the conductor loss and the insertion loss[21–23]. Through the research on the S-parameters of differential signals, methods to improve the signal transmission quality can be obtained, providing ideas for optimizing circuits.

S-parameter modeling of high-speed signals in the 5G small base station platform system

The 5G small base station platform is a typical application of high-speed interconnection systems and has various forms. It internally integrates multiple minimum system unit modules, including high-performance processors (Network Processing Unit), baseband System on Chip (SoC) chips, and radio frequency transceiver processing chips. The data paths between them adopt integrated design and distributed design for interconnection via Serdes according to different component architectures. As shown in the figures, Fig. 2 illustrates the integrated interconnection mode, and Fig. 3 shows the distributed interconnection mode (Base Band Unit + Remote Radio Unit). Figure 4 shows the small base station system based on the backplane mode. For integrated and distributed interconnection modes, high-speed signals travel on the same PCB board, which is applicable to the interconnection model structure under short paths as shown in Fig. 5. However, for the backplane mode the baseband processor is interconnected with the motherboard through a PCIe connector in the form of a PCIe expansion card. Meanwhile, there is also a backplane on the PCIe expansion card for radio frequency communication, and Serdes signals send and receive data through high-speed connectors. This form of small base station system is applicable to the interconnection structure model under a long path as shown in Fig. 5.

Based on the architecture of the interconnection system and under the premise of considering the interconnection scenario of the longest path as shown in Fig. 5, the system circuit model is built using S-parameters as shown in Fig. 6. Among them, Tx_AMI and Rx_AMI represent the signal transmitting end and the signal receiving end respectively, while TxPackage and RxPackage represent the packaging S-parameter models of the transmitting end and the receiving end respectively. Via1 to Via14 denote the via models in the transmission process of the entire signal path. It can be seen that all modules in the circuit can be interconnected in the form of S-parameters. During system simulation, it is very convenient to predict the signal quality of the real high-speed interconnection system by simply deleting modules or adjusting parameters according to the actual wiring implementation situation.

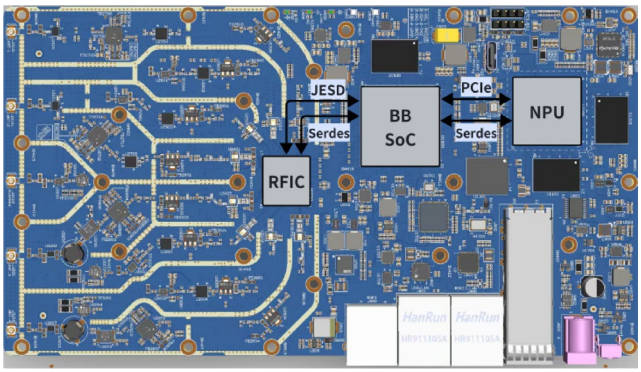


Fig. 2. Interconnection of integrated small base stations.

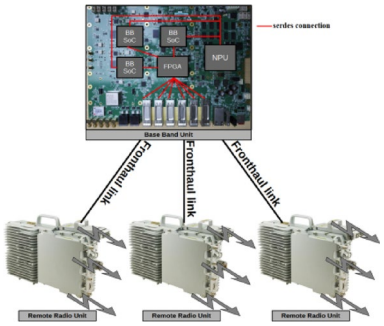


Fig. 3. Interconnection diagram of distributed small base stations.

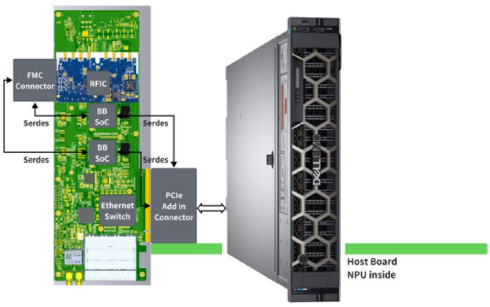


Fig. 4. Backplane interconnection.

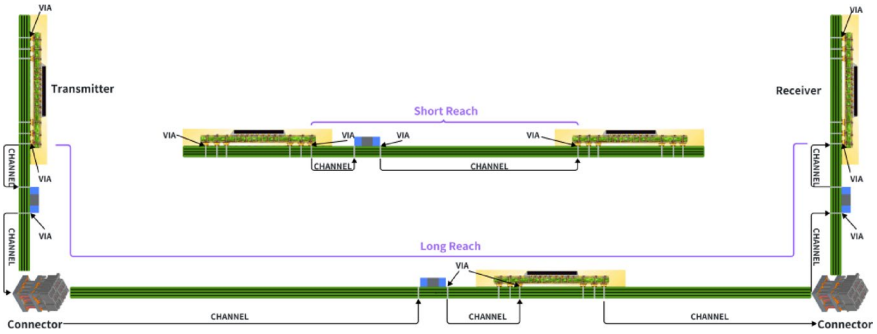


Fig. 5. The interconnection system under long path and short path.

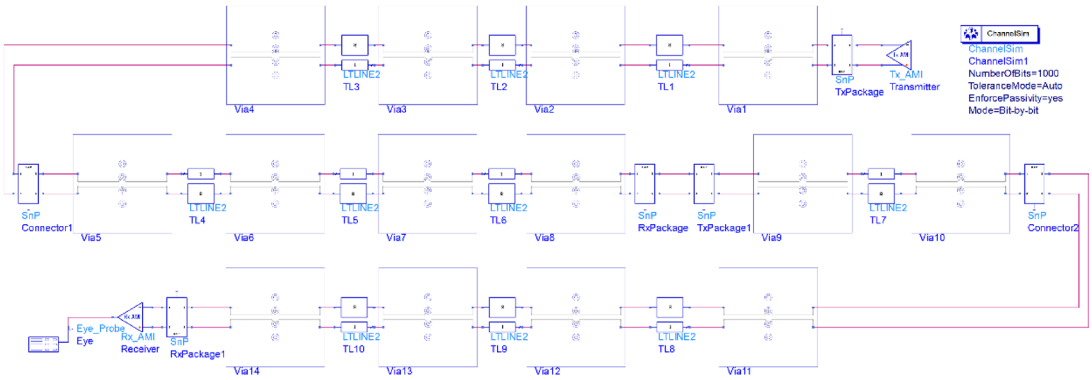


Fig. 6. The S-parameter circuit model under the long path.

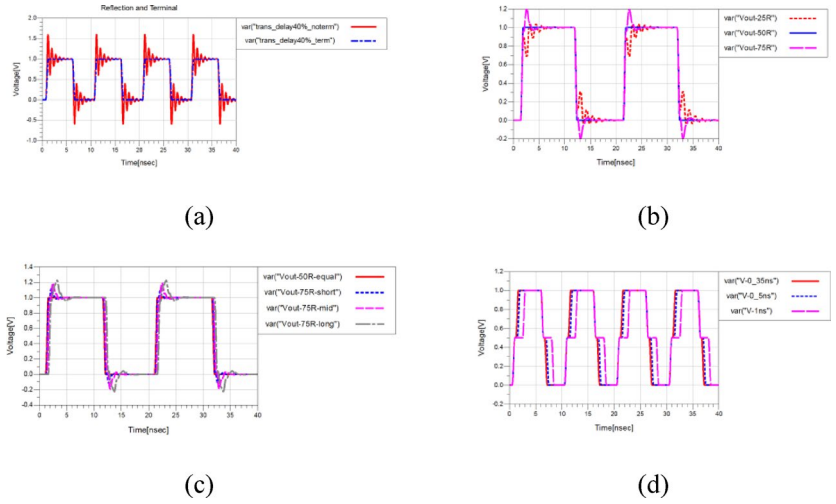


Fig. 7. Signal reflection waveform. (**a**) The influence of termination on the waveform of impedance; (**b**) The waveform of impedance discontinuity; (**c**) The influence of signal transmission length on the waveform; (**d**) The influence of signal delay on the waveform.

Based on the above interconnection system, aiming to fully improve the signal transmission quality of complex interconnection systems is the core content of this paper's research. For the 5G small base station system, due to the diversity of its structural forms, in order to maximize the reuse of the original hardware and software systems, the use of high-speed connectors has become quite common. The advantage is that the reconstruction cost of the hardware system is low. By replacing different processor motherboards and radio frequency sub-boards, applications oriented towards, for example, home base stations, enterprise base stations, or even non-terrestrial network (NTN) scenarios can be formed. Building the S-parameter model of the 5G base station platform system can predict the signal transmission quality before the system is implemented, so as to judge the feasibility of the scheme[24]. The following focuses on the key component modules of this circuit model to analyze the signal integrity issues and conduct optimization and improvement.

Analysis and optimization of signal integrity in high-speed interconnection systems

It can be analyzed from Fig. 5 that the transmission line units, via units, connectors, and transceiver terminals that make up the high-speed interconnection system will all have an impact on high-speed signal transmission. During the system design process, it is necessary to continuously optimize the attenuation of signals by each module. Using S-parameters to model and analyze the system is one of the effective means to optimize complex high-speed interconnection systems.

Transmission line effects and optimization

The basic unit for signal transmission is the transmission line. According to the transmission line, properly terminating the transmission line and achieving impedance matching are effective ways to optimize transmission line effects such as reflection, crosstalk, and ringing[25]. As shown in Fig. 7(a), it displays the comparison of signal reflection waveforms with and without termination impedance at the active end. Figure 7(b) shows the waveform reflection caused by the discontinuity of transmission line impedance under the same termination

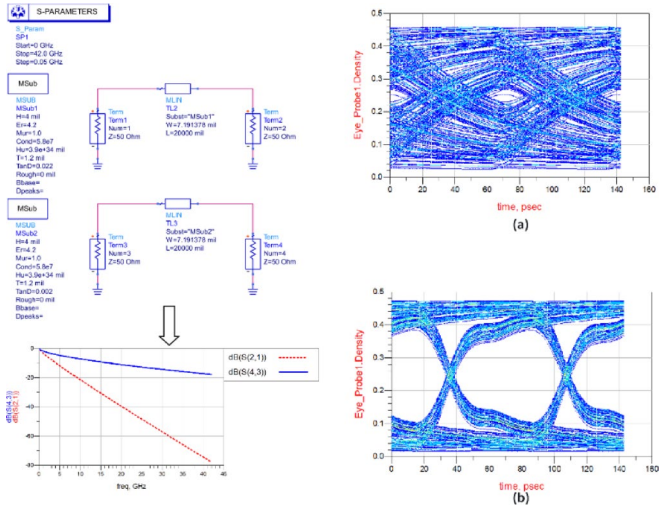


Fig. 8. Insertion loss of S-parameters of the transmission medium. (**a**) Eye diagram at the receiving end for medium S(2,1); (**b**) Eye diagram at the receiving end for medium S(4,3).

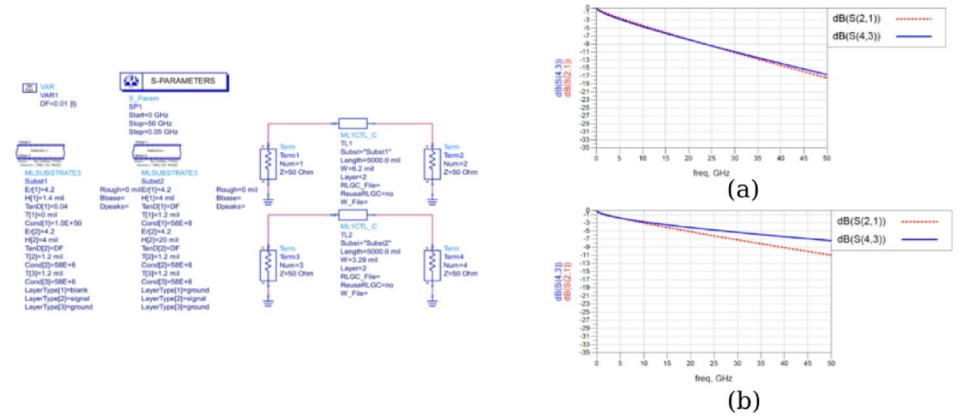


Fig. 9. Comparison of insertion loss between micro-strip lines and strip-lines. (**a**) Insertion loss of strip-line and micro-strip line under a loss factor of 0.01; (**b**) Insertion loss of strip-line and micro-strip line under a loss factor less than 0.01.

premise. Figure 7(c) illustrates the problem that the length of the signal affects the waveform quality under the condition of impedance discontinuity. Figure 7(d) reflects the waveform step phenomenon of the transmission line under different delay conditions. It can be seen that the longer the length of the impedance discontinuity is, the more serious the problems of signal delay and reflection will be.

For the analysis and optimization of the transmission line unit, issues such as signal termination and impedance matching need to be fully considered. In addition, the impact of the dielectric loss factor on the signal insertion loss also needs to be taken into account comprehensively. As shown in Fig. 8, The loss tangent of the board used in the transmission line model S(2, 1) is 0.022, and the loss tangent of the board used in the transmission line model S(4, 3) is 0.002, there is a comparison of eye diagrams of the same signal transmitted in different media[26]. The impact of ordinary substrates and high-speed substrates as signal transmission media on the signals at the receiving end is quite obvious. From the S-parameter analysis of the substrates on the left side, it can be seen that the signal insertion loss of the S (4,3) high-speed substrate within the entire frequency band is significantly lower than that of S(2,1). And the eye diagram results at the receiving end on the right side also verify this conclusion. Figure 8(a) is the eye diagram at the receiving end for the medium S (2,1), and Fig. 8(b) is the eye diagram at the receiving end for S(4,3).

Regarding the research on the routing layers of high-speed signals, when high-speed signals fan out from the pins of a chip and reach the surface layer of the circuit board, generally, shorter lines will be routed and then perforated to enter the inner-layer routing. When approaching the receiving end, they will be perforated out again to connect with the terminal chip. Through simulation, it can be found that in Fig. 9(a), the S(2,1) of the micro-strip line and the strip-line have comparable insertion loss performance when the loss factor is close to 0.01. However, after the loss factor is less than 0.01 as shown in Fig. 9(b), the difference in insertion loss between

the two gradually emerges. It can be seen that the inner-layer strip-line routing under the condition of high-speed substrates is superior to the micro-strip line transmission on the surface layer.

Via modeling and optimization

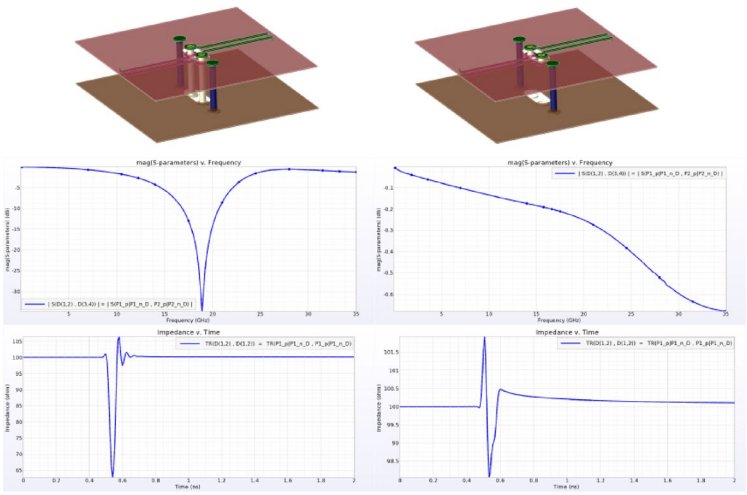
If signals need to be transmitted across layers, via units must be introduced[27,28]. The existence of vias will introduce parasitic inductance and parasitic capacitance, and the main problems brought about are as follows:

(1) increasing signal delay;
(2) the electromagnetic field changes during the process of signal passing through the vias, increasing the cross-talk risk for surrounding signals;
(3) vias appear as points of impedance discontinuity on the transmission line, resulting in signal reflection and simultaneous signal attenuation. Therefore, via optimization is mainly based on the following aspects:

① Optimize by reducing the thickness of the layer stack, reasonably design the size of vias, and try to minimize the number of layers that vias pass through as much as possible;
② Use the back drilling and blind/buried via processes. Using back drilling or blind/buried vias can reduce the stub branches of signals. As shown in Fig. 10(a), the back drilling process is not used, while in Fig. 10(b), the back drilling process is added. The figure in the middle represents the insertion loss, with the abscissa being the signal frequency and the ordinate being the signal attenuation amplitude. The figure at the bottom represents the differential impedance diagram. From the insertion loss and impedance curves, the application of back drilling technology has a very significant effect on optimizing and improving via losses and impedance matching.
③ The anti-pad technology is adopted to reduce the capacitive load of vias[29]. Reasonably set the diameter of the anti-pad. The closer it is to the via, the closer the ground layer is to the signal, resulting in an increase in capacitance and thus a reduction in via impedance, as shown in Fig. 11. Four cases with the diameter of the anti-pad ranging from 0.508 mm to 1.27 mm were adopted respectively for comparison. By building models and conducting simulations to compare the parameters of anti-pads, the S_{DD12} index data under different sizes can be obtained. It can be seen that using anti-pads with a diameter of 0.508 mm–0.762 mm can optimize the insertion loss index of the S-parameters of vias and the impedance continuity performance.
④ Reasonably set the return ground vias to provide the shortest return path for signals. By adjusting the spacing between the return ground vias and the signal vias and observing the S-parameter insertion loss and differential impedance analysis of the signal via model, Fig. 12 shows that in the four cases where the spacing ranges from 0.635 mm to 1.016 mm, there is little impact on the signal transmission attenuation and impedance matching of the vias.

Modeling of high-speed connectors and extraction of S-parameters

Another important component of the high-speed interconnection system is the high-speed connector. When high-speed signals flow through the connector, there will be relatively large attenuation, which brings great challenges to signal integrity. Therefore, the modeling and simulation of the connector are particularly important. It is necessary to import the insertion loss and return loss parameters of the target connector into the interconnection system to truly reflect the signal attenuation situation.



(a) (b)

Fig. 10. Comparison of S-parameter insertion loss and differential impedance before and after the via process optimization. (**a**) Insertion loss and impedance curves without the back drilling process; (**b**) Insertion loss and impedance curves with the back drilling process.

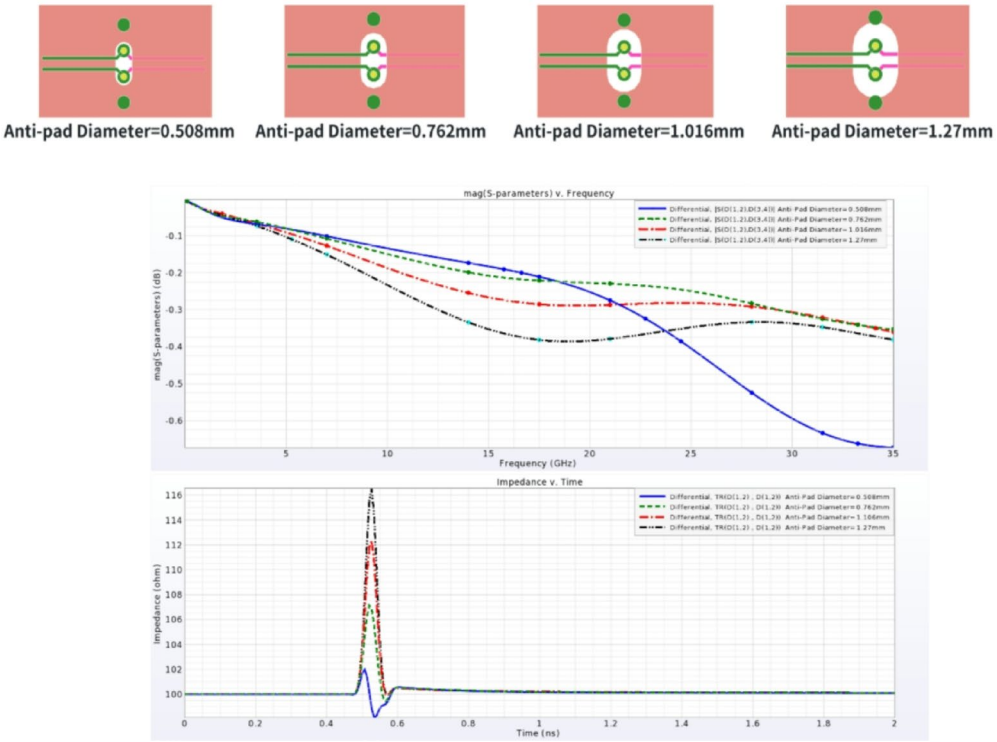


Fig. 11. Comparison of S-parameters and impedance curves for optimized via anti-pads.

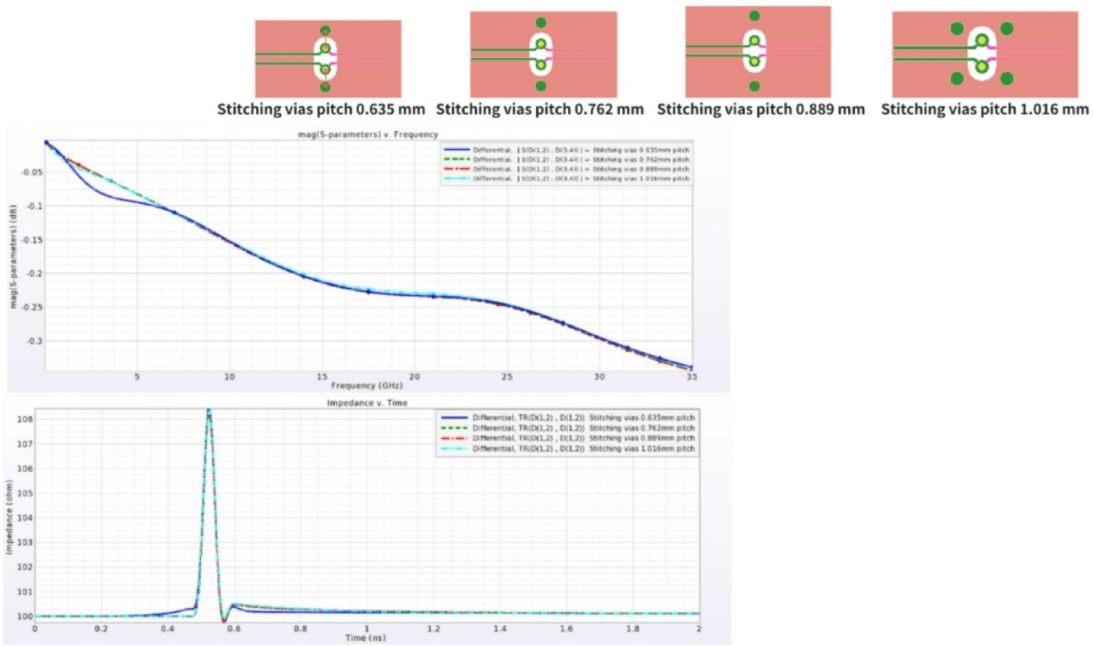


Fig. 12. Comparison of S-parameters and impedance for the optimization of stitching vias design.

Since it is rather difficult to obtain the S-parameters of high-speed connectors, a more feasible method is to conduct 3D modeling of the connector using HFSS software, as shown in Fig. 13. Import the 3D model provided by the connector manufacturer and specify the correct model materials in the model. What mainly affects the calculation of S-parameters are the dielectric constant, magnetic permeability and so on of the materials. Establish wave ports and place them on the input and output ports, and define the parameters of the scanning frequency to obtain the changes of S-parameters within the frequency band of interest.

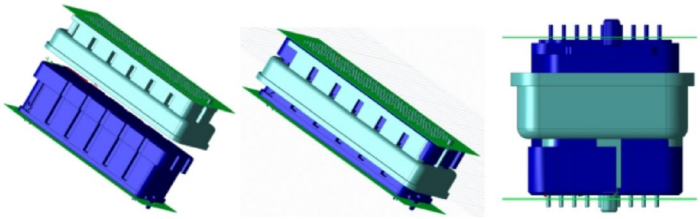


Fig. 13. 3D modeling of the connector.

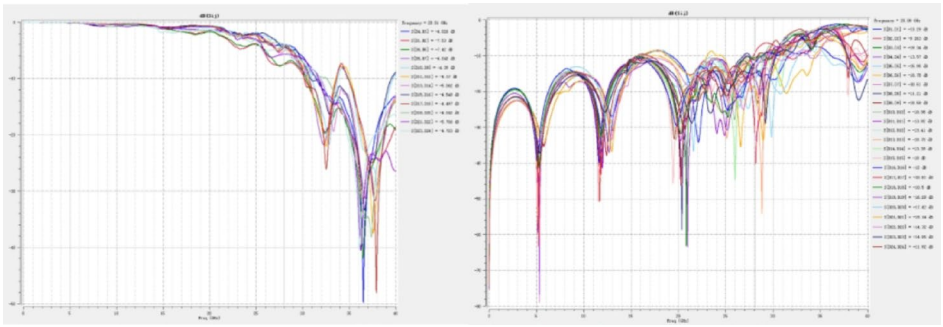


Fig. 14. Connector S-parameter insertion loss and return loss curve diagram.

The insertion loss and return loss of the S-parameters of a 48-pin high-speed connector are shown in Fig. 14. It can transmit 12 pairs of high-speed Serdes signals simultaneously, and the signal insertion loss at 28 GHz is about – 5 dB.

AMI model of transceiver units and their signal equalization technologies

For a complete Serdes interconnection system, the signal transceiver unit is the core part. In the actual system, the Serdes module inside the chip undertakes this part of the function. With the continuous increase in signal rate, high-speed signal equalization technologies, including Feed-Forward Equalization (FFE), Continuous-Time Linear Equalization (CTLE), Decision Feedback Equalization (DFE), Clock and Data Recovery (CDR), etc., are integrated within the Serdes unit. The main purpose is to enhance the high-frequency signal components, so that the signals can be compensated during the channel transmission process, while reducing inter-symbol interference and providing clean signals for clock recovery and the high-speed signal serial-to-parallel conversion module. This part of the function needs to be reflected in some form in the simulation circuit model and will be replaced by the chip after the board-level implementation in the future. Generally speaking, there are several ways:

(1) Directly use the transmission and reception models provided in the simulation software. This method is often relatively simple, but the use of general models will lead to a decrease in model accuracy.
(2) Use the Matlab Serdes toolbox to export the Input/Output Buffer Information Specification (IBIS) models of AMI-Tx/Rx for use by the system simulation tools. As shown in the example in Fig. 15, after adopting the signal equalization algorithm at the transmission and reception ends, for a high-speed transmission system with a 15 dB channel attenuation, the signals can be recovered.
(3) It is also possible to load the Serdes AMI-Tx/Rx models provided by chip manufacturers into the system simulation tools to obtain the most accurate transceiver units. In this paper, the third method is adopted to use the most accurate circuit simulation model to evaluate the performance of the high-speed interconnection system.

Noise in high-speed interconnection systems

In actual circuit systems, there is no ideal situation without noise. The noise that affects the transmission of high-speed signals mainly includes the following aspects:

(1) Power supply and ground bounce noise. These two parts have a relatively large impact on high-speed signals in the circuit. High-speed systems require a clean power supply and ground. The power supply has certain impedance characteristics. Therefore, it is necessary to study the Power Distribution Network(PDN) impedance of the power distribution system, control extremely low impedance characteristics, reasonably arrange the decoupling capacitors allocations and the planar design of the power and ground layers. On this basis, reduce the return path of high-speed signals to weaken the noise. In the actual implementation process, it is required that the power supply and the ground have separate multi-layer planes, and vias are

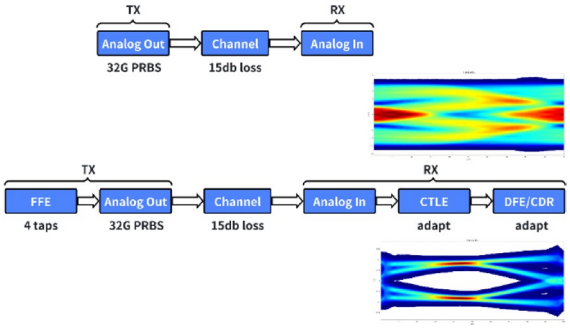


Fig. 15. The impact of signal equalization algorithms on the eye diagram at the receiving end.

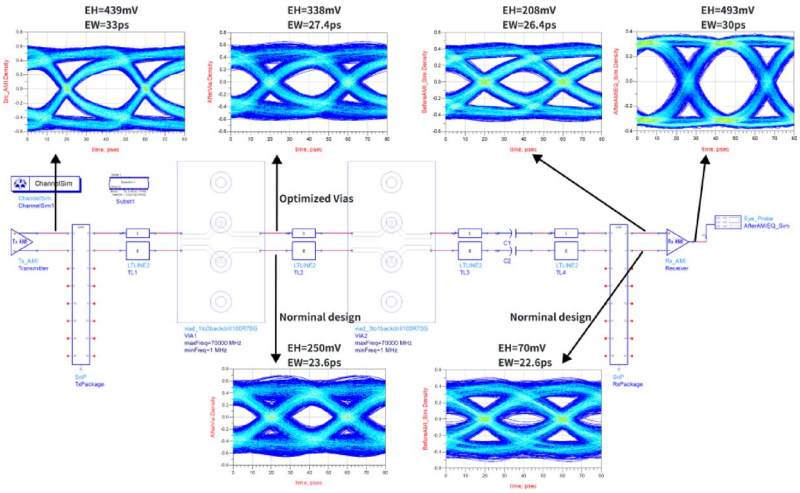


Fig. 16. Simulation and eye diagram of high-speed interconnection systems based entirely on S-parameters.

reasonably arranged to provide the shortest return path for current and ensure that the PDN impedance meets the system requirements.

(2) The impact of crosstalk in signal transmission. The characteristic of high-speed differential signals is that they are hardly affected by external interference. Due to external radiation, a voltage with the same phase and amplitude will always be generated simultaneously on P and N (in the form of common-mode interference). However, when the terminal receives the signal, it only judges the difference between the signal lines. So this kind of interference will not affect the judgment of normal signals. In fact, the impedance and delay differences between differential signals will cause noise in the signals at the receiving end. In the simulation model, factors such as impedance matching and equal-length wiring of differential signals are considered, including ensuring that the impedance of the transmission line is continuous during the signal transmission through vias and connectors.

(3) Inter symbol interference. In the test, the maximum-length pseudo-random code sequence is used as the signal source. This is a test stimulus under the worst conditions, and the eye diagram result is obtained under the condition that the channel simulation is set to an extremely low bit error rate simulation (Bit Error Rate < 1e-16).

Other aspects such as the reflection noise of signal transmission and the signal attenuation characteristics have been discussed in the previous sections.

5G overall performance evaluation of the high-speed interconnection system of small base stations

Combined with the above analysis and optimization strategies, all the module units are interconnected to form a complete circuit model for high-speed signal transmission systems, as shown in Fig. 16. This is a simulation circuit system that is completely based on S-parameters. Each circuit unit ($S_{s1}(2,1)\ldots S_{sn}(2,1)$) can be individually optimized to achieve the best overall performance $S_{top}(2,1)$. According to the 5G small base station platform architecture diagram in Fig. 2, the Serdes signal transmission between the baseband chip and the NPU (CPU), as well as between the baseband chip and the radio frequency transceiver chip, is completely equivalent to this circuit model. The difference lies in the fact that the rates at which various interfaces operate are different, and due to layout differences, the lengths of lines at different interfaces also vary. The circuit model

based on S-parameters studied in this paper can conveniently adjust parameters according to such differences, quickly obtain signal transmission performance, accurately predict signal attenuation and transmission quality, guide the entire process of the implementation of the system circuit board layout, and ensure the integrity and consistency of the key signal paths on the platform.

It can be compared from Fig. 16 that after using the methods in Chap. 4.2 to optimize the vias, the eye height of the eye diagram has increased by 88 mV (EH = 338mV vs. EH = 250mV) and the eye width has increased by 3.8 ps (EW = 27.4ps vs. EW = 23.6ps). The improvement at the receiving end is quite obvious, with the eye height increasing by 138 mV (EH = 208mV vs. EH = 70mV) and the eye width increasing by 3.8 ps (EW = 26.4ps vs. EW = 22.6ps). Moreover, after the serdes equalization algorithm inside the chip is applied, the quality of the eye diagram will be further improved to meet the receiving standard of low bit error rate for high-speed signals.

To further illustrate the accuracy of the established simulation circuit model, the finally completed PCB board-level design is imported into the EDA software for the extraction of line S-parameters. Then, a schematic simulation circuit is built, and the simulation results are compared with those of the modeling circuit that is completely based on S-parameters, as shown in Fig. 17.

After using the same excitation transmission signal and the same receiving-end signal equalization algorithm for both respectively, the obtained results are shown in Table 2. The results indicate that this simulation modeling circuit completely based on S-parameters can accurately reflect and predict the signal transmission quality after the actual board-level implementation, with a matching degree of over 95%. On this basis, when expanded to more complex applications where multiple high-speed boards are interconnected in scenarios using high-speed connectors, this simulation modeling circuit completely based on S-parameters can very conveniently predict the signal attenuation situation of the entire system in advance and adopt effective optimization methods in advance to optimize and guide the physical implementation of the boards, so as to meet the requirements of the system transmission performance indicators.

Conclusions

Research on high-speed signal integrity is an important method for improving signal transmission quality and system stability. The transceiver systems using high-speed signal interconnection have significant applications in the field of ultra-high-speed data transmission. Based on scattering (S) parameters, this paper establishes S-parameter models for all elements that make up the high-speed interconnection system, including transmission lines, connectors, vias, transceiver chips, etc., studies the factors that affect the insertion loss index of S-parameters, proposes methods to optimize the indexes and builds a simulation circuit model for demonstration. From specific elements to the overall system, a circuit simulation circuit completely based on S-parameters is proposed. With this circuit simulation model, the transmission performance of complex interconnection systems can be quickly predicted. Parameter optimization and system improvement can be carried out throughout the whole cycle during the initial stage of circuit design and the implementation process, providing theoretical and experimental support for high-speed circuit design.

Taking the circuit design of the 5G small base station platform as an example, under the same input excitation and simulation environment conditions, the terminal receiving eye diagram indexes of the circuit simulation platform based on S-parameters in the two cases of using the completed board-level S-parameter extraction design and the simulation circuit S-parameter model design are close to over 95%. This fully confirms that the simulation circuit method of the high-speed interconnection system completely based on S-parameters

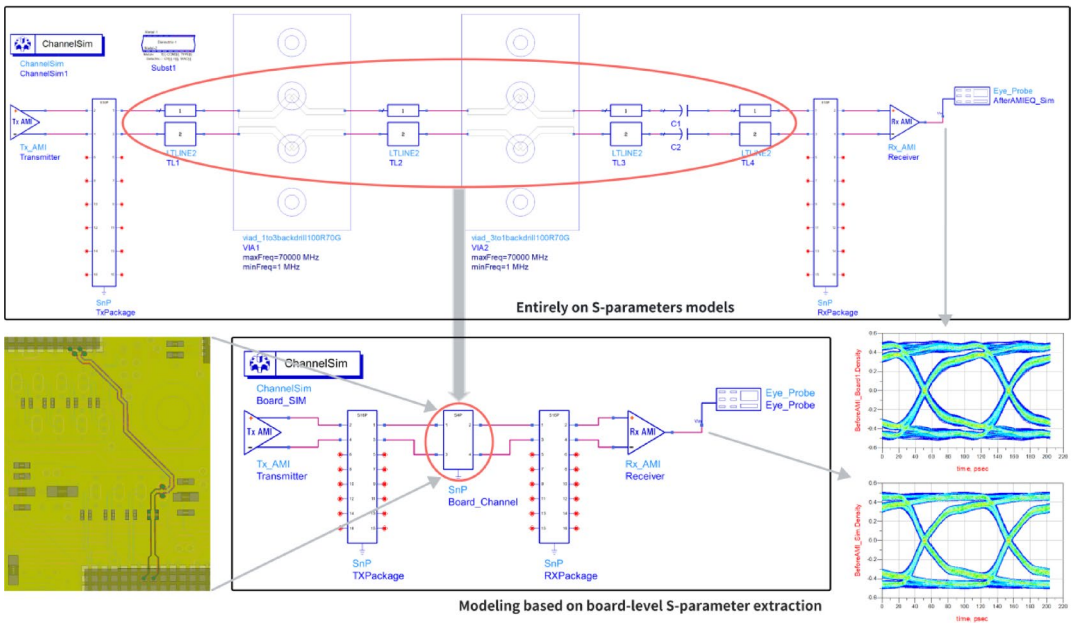


Fig. 17. Comparison of board-level S-parameter extraction and the entirely on S-parameters models.

Serdes signal	Bit rate	S para. based on board (α)		S para. based on sim (β)		Matching degree	
		Eye height (mV)	Eye width (ps)	Eye height (mV)	Eye width (ps)	Eye height (β/α)	Eye width (β/α)
JESD TX0	9.8 Gbps	526	92.86	567	93.37	107.79%	100.55%
JESD TX1	9.8 Gbps	537	93.37	582	94.39	108.38%	101.09%
JESD TX2	9.8 Gbps	590	95.41	582	93.37	98.64%	97.86%
JESD TX3	9.8 Gbps	581	94.39	569	94.39	97.93%	100.00%
JESD RX0	9.8 Gbps	552	93.37	555	93.37	100.54%	100.00%
JESD RX1	9.8 Gbps	495	93.37	554	94.39	111.92%	101.09%
JESD RX2	9.8 Gbps	546	93.88	564	95.41	103.30%	101.63%
JESD RX3	9.8 Gbps	545	94.9	576	94.9	105.69%	100.00%
PCIE TX0	16 Gbps	458	51.25	475	51.25	103.71%	100%
PCIE TX1	16 Gbps	465	52.56	463	50.94	99.57%	96.92%
PCIE TX2	16 Gbps	445	50.63	461	50.63	103.60%	100%
PCIE TX3	16 Gbps	399	51.25	442	49.06	110.78%	95.73%
PCIE RX0	16 Gbps	420	49.69	454	50.63	108.10%	101.89%
PCIE RX1	16 Gbps	451	51.25	433	50.9	96.01%	99.32%
PCIE RX2	16 Gbps	423	49.69	410	51.88	96.93%	104.41%
PCIE RX3	16 Gbps	433	49.38	402	50	92.84%	101.26%
Average Matching degree						95.30%	97.88%

Table 2. Comparison of S-parameter simulation results between board-level S-parameter extraction and entirely on S-parameters models.

can accurately reflect the transmission quality of the real system. By taking advantage of the flexibility of the S-parameter model, in the future, it will be possible to expand the interconnection on multiple platforms and establish a comprehensive system index simulation and verification platform covering electricity, heat, magnetism, etc., so as to ensure the stability of the high-speed interconnection system.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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Declarations

Competing interests
The authors declare no competing interests.

Additional information
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