Design of Speed and Power Efficient Multipliers Using Vedic Mathematics with VLSI Implementation

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Abstract*— Multipliers are the key components of systems viz. FIR filters, Microprocessors, Digital Signal Processors etc. which demands high performance. The performance of these applications mainly depends on the numbers of multiplication done in unit time. In real time multipliers the speed and power are the major criteria, thus faster and power efficient multipliers are needed. This paper focuses on the development of high speed, low power multipliers using Vedic Mathematics. The proposed multiplier architectures are based on the Urdhva and Nikhilam sutras of the Vedic Mathematics. The Urdhva multiplier generates the partial products and the sums in parallel. Hence, this multiplier reduces the carry propagation delay from LSB to MSB. The Nikhilam multiplier finds the compliment of the larger number of its nearest base, thus reduces the complexity in the multiplication. The proposed multipliers are designed using Carry save adder and implemented in 65nm CMOS Technology using ASIC methodology. The proposed Urdhva and Nikhilam multipliers achieve 60%, 77% improvement in speed and 37%, 50% improvement in power respectively, as compared with the power consumption of the conventional array multipliers.

Keywords*— Vedic Multiplier, High Speed, Low Power, CSA, RCA, Parallel Adders.

I. INTRODUCTION

Multiplication is a very important arithmetic operation for many signal processing applications such as convolution, correlation, frequency analysis, image processing etc. The speed of multiplication operation is an important aspect in the processors of these applications. The processor requires considerable amount of time in performing the multiplication operation and performance of the multiplier determines system performance. Hence, the speed and power efficient multipliers are of greater importance in signal and image processing applications Multipliers are mainly classified into two types viz. serial multiplier and parallel multiplier. Serial multiplier which requires more processing time [1] and the Parallel multiplier such as Braun multiplier, Booth multiplier, Wallace tree multiplier, Array multiplier etc. [2-4]. Array multiplier reduces the delay, but it requires a large number of gates, which increases area and power consumption [4-5]. Booth multipliers are used for multiplication of signed binary numbers but, it does not work when there are alternate zeros and ones [4]. Wallace tree multiplier works at high speed, but it exhibits structural irregularity [4] which is more complex for hardware implementation. Braun multiplier is one of the parallel array based multipliers which require n^2 gates and (n-1) number of adders, which in turn increases the complexity and area of the design. In order to overcome the disadvantages of the conventional multipliers, Vedic sutras adopted have been from Vedic Mathematics to design Vedic multipliers. Vedic Mathematics consists of 16 sutras and 13 sub-sutras which can be used to obtain efficient arithmetic computations. Two sutras viz., "Urdhva-tiryakbyham" and "Nikhilam Navatascaramam Dasatah" are applicable for efficient multiplication.

"Addition" is the fundamental operation of multiplication, thus adders are the building blocks of multipliers. The Speed of multiplier can be improved by using efficient adder architecture. There are different adder architectures existing in the literature such as ripple carry adder, carry look-a-head adder, carry save adder etc. Carry save adder is faster among the existing adders [6].

This paper summarizes a comparative study on Vedic multipliers particularly on Urdhva & Nikhilam based multipliers with a conventional array multiplier and proposes an efficient Nikhilam multiplier architecture. Section II describes the Vedic multiplication techniques. Related works are discussed in Section III. Section IV describes the development of different adder architectures. The designing styles of multiplier architectures are presented in Section V. Finally the results and conclusion are discussed in sections VI and VII respectively.

II. VEDIC MULTIPLICATION TECHNIQUES

Vedic mathematics is a gift given to this world by the ancient sages of India. The word Vedic is derived from the word 'Veda', which means "Storehouse of all knowledge" [7]. Jagadguru Swami Sri Bharati Krishna Tirthaji (1884-1960), a scholar of Philosophy, Sanskrit, History and Mathematics rediscovered Vedic Mathematics based on the available Vedic manuscripts [7]. The whole of Vedic mathematics is based on 16 sutras and 13 sub-sutras. These sutras describe the natural ways of solving a whole range of mathematical problems [8]. Here "Urdhva-tiryakbyham" and "Nikhilam Navatascaramam Dasatah" sutras applied for multiplication are discussed as below:

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A. "Urdhva-tiryakbyham" Sutra

"Urdhva-tiryakbyham" Sutra is a general multiplication formula applicable to all cases of multiplication. The basic rule for the multiplication of two 3 digit numbers using a line diagram is shown in Fig. 1. In Urdhva Tiryakbyham method digits on both sides of the lines are multiplied and the carry from the previous step is added. In this step one bit of the result and the carry is generated. This carry is added in the next step and the same process is repeated. All the results are added to the previous carry, when more than one line is there in one step. Least significant bit generated in each step is considered as the result bit and the rest all bits are carry for the next step. Initially the carry is taken to be zero [9], [10], [11].

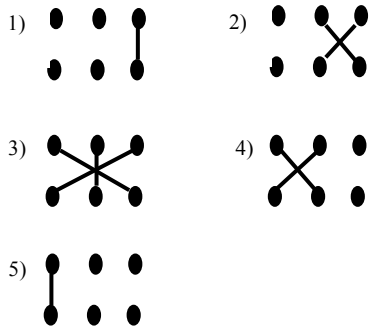

Fig. 1. General rule of 3-digit multiplication

The hardware realization of 2-bit multiplier is shown in Fig. 2

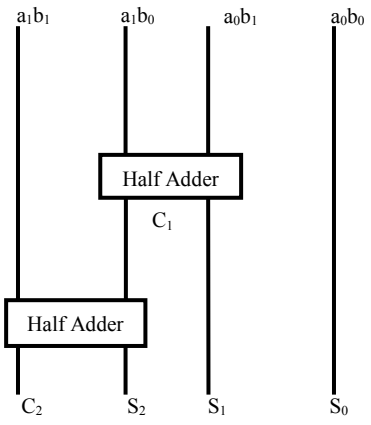

Fig. 2. 2-bit Vedic Multiplier

B. "Nikhilam Navatscaramam Dasatah" Sutra

Nikhilam Sutra means 'all from 9 and last from 10" [12]. Nikhilam sutra starts from the leftmost digit and subtracts'9' from each of the digits; but from the last digit it subtracts '10'. To subtract 4679 from 10000, all the digits except the last digit are subtracted from 9 and the last digit is subtracted from 10, yielding 5321. Nikhilam sutra based multiplication is suitable for multiplying large numbers. Larger the original number, lesser the complexity of the multiplication [12]. This formula can be used for multiplication of numbers, nearer to "power of 10" bases like 10, 100, 1000 etc. very effectively. Fig. 3 shows the general multiplication technique using Nikhilam sutra.

For the multiplication of 95×94

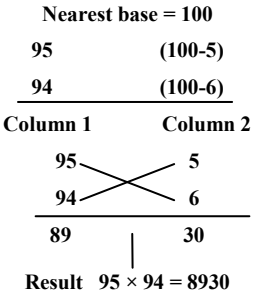

Fig. 3. General rule for Nikhilam Multiplication

III. RELATED WORKS

Krishnaveni and Umarani have implemented 4x4 multiplier based on the Vedic sutra [13]. It is implemented using modified 4-bit adder. When compared to normal 4 bit adder, the modified 4 bit adder used in their work, provides 1.593ns of reduction in delay. They achieved a good speed when compared with that of the conventional array multiplier. Thapliyal and Srinivas, have proposed hardware implementation of RSA encryption/decryption algorithm using the algorithms of ancient Indian Vedic mathematics [14]. In their work the performance of the multiplier was improved with the help of squarer architecture, which is based on Vedic mathematics. Thenmozhi and Kishore have developed the RC6 algorithm using Complex Vedic Multiplier [15]. RC6 algorithm is widely used cryptographic algorithm for data security. In their work, the efficiency of the RC6 algorithm was improved using Vedic Sutras such as "Urdhvat-tiryakbyham" and "Nikhilam Navatascaramam Dasatah". SaiKumar and Samundiswary have designed the different adder architectures [6]. In their paper, the comparative study of various adders is carried out. They showed that the carry save adder reduces delay as compared with the ripple carry adder. Kumar and Bharati have implemented the multiplier architecture based on Dwandwa Yoga logic and a squaring algorithm [16]. They used the architecture of Urdhva sutra which is based on "Duplex" D property and they achieved a reduced propagation delay when compared with the conventional multiplication algorithms. The proposed work of this paper highlights methods of achieving high speed and lesser power consumption in the multipliers using Vedic concepts and the adder architectures.

IV. Development of Different Adder Architectures

A. Ripple Carry Adder

Ripple Carry Adder (RCA) is a basic adder, which contains the series structure of Full Adders (FA); each FA is used to add three bits which consist of carry generated from the previous full adder. This propagation of the carry to successive stages increases the delay with the increase in the number of input bits in RCA [6]. The architecture of RCA is shown in Fig.4.

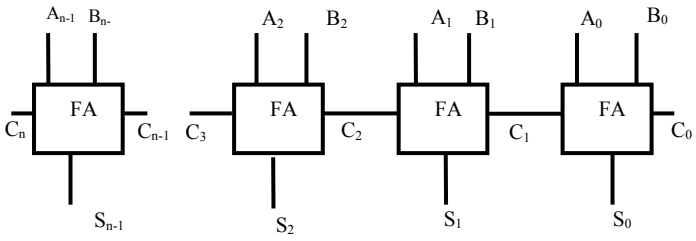

Fig. 4. Basic architecture of Ripple Carry Adder

B. Carry Save Adder

In Carry Save Adder (CSA), three bits are added simultaneously. In CSA carry does not propagate to the next stages, instead carry is stored in the present stage, and added to the sum. Hence, the delay because of the carry is reduced in this scheme [8]. The architecture of CSA is shown in Fig 5.

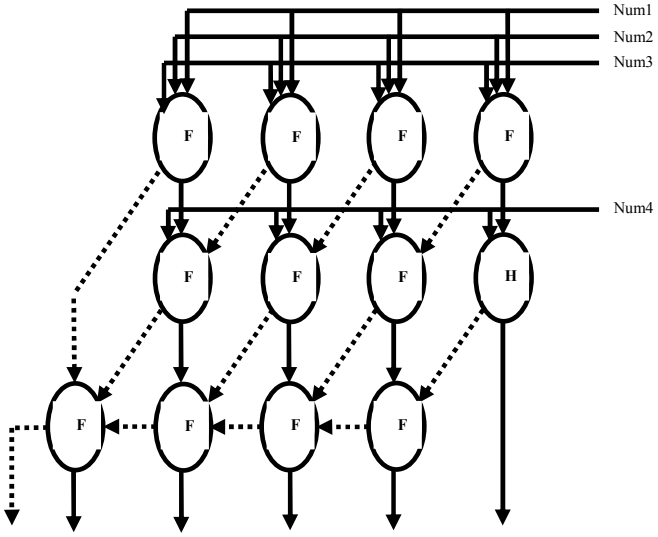

Fig. 5. Basic Architecture of Carry Save Adder

Thus, to increase the speed the CSA is used in both proposed Urdhva and Nikhilam multipliers. The conventional full adder structure used in the adder circuit uses XOR, AND and OR gates, that consumes more power.

The modified structure of the full adder is shown in Fig. 6 that uses NAND, AND, OR gates and consumes lesser power comparatively [17].

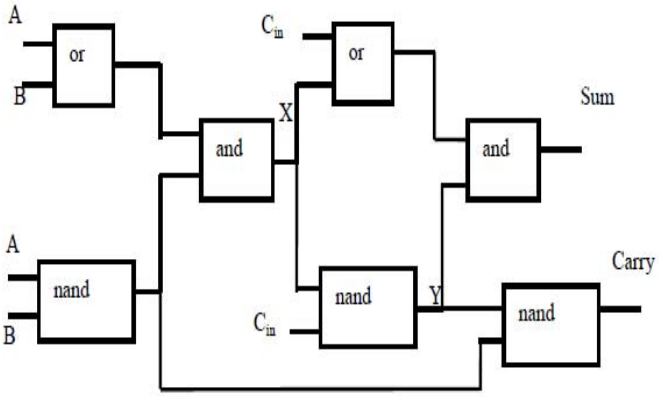

Fig. 6. Modified Full Adder

The power comparison graph shown in Fig. 7 illustrates that modified full adder provides a 18% improvement in power consumption when compared with that of over normal full adder structure.

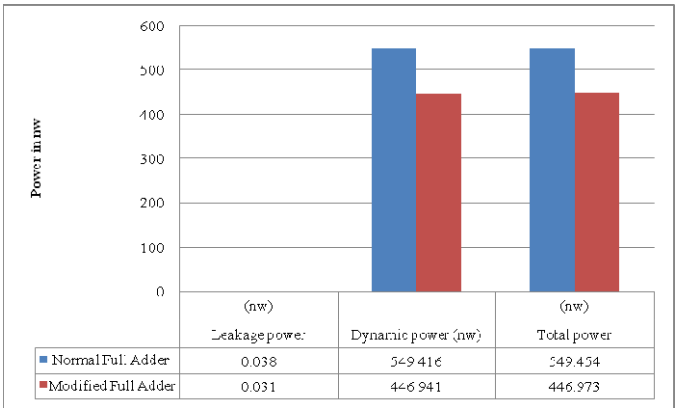

Fig. 7. Power comparision between Normal and Modified Full adder

V. Designing of Multipliers

A. Array Multiplier

Array multiplier is a combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders [18]. An array of AND gates are used to generate partial product terms, which are added using an array of full adders and half adder. For multiplication of m x n bits, array multiplier require (m x n) AND gates and ((m-1) x n) adders. From ((m-1) x n) adders "n" number of half adders and "((m-2) x n)" number of full adders are required. The general block diagram for 4-bit array multiplier is shown in Fig.8. 4-bit array multiplier requires 16 AND gates, 4 half adders and 8 full adders [19]. Since array multiplier requires more area and consumes more power, thus it is less economical [4].

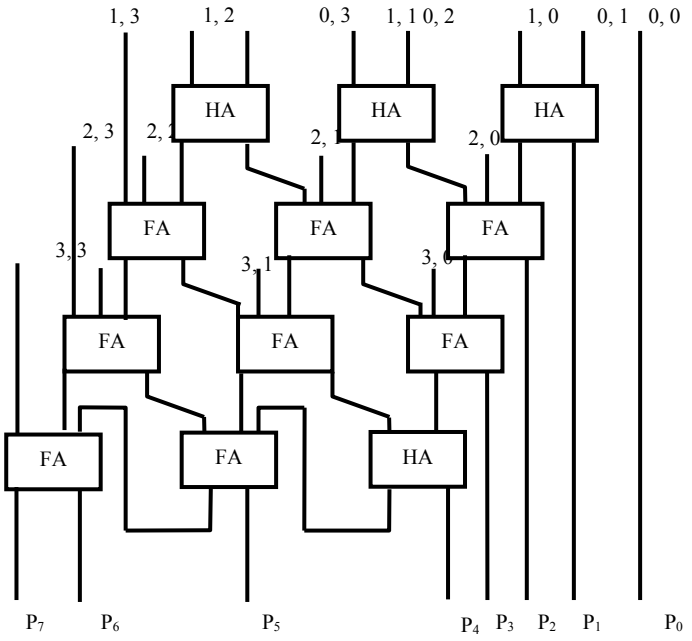

Fig. 8. 4 x 4 Array Multiplier

For the 64-bit array multiplier in1 and in2 are the two inputs that are having the width of 64 bits and product is the output that is of 128 bit width. The simulation waveform of array multiplier is shown in Fig 9.

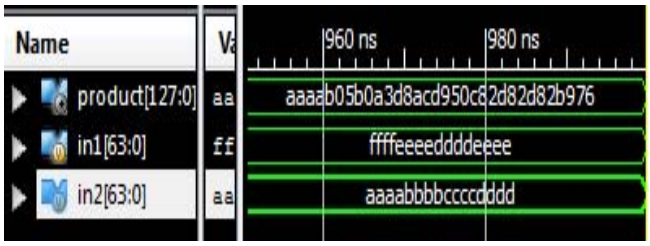

Fig. 9. Simulation result for 64-bit Array Multiplier

B. Urdhva Multiplier

64-bit Urdhva multiplier has been developed in a hierarchical manner. Fundamental block of developed multiplier is 2-bit multipliers that consist of half adder and full adder blocks. This 2-bit multiplier is used to develop other hierarchical blocks such as 4-bit, 8-bit, 16-bit and 32-bit multipliers respectively. The 64-bit multiplier requires four 32-bit multipliers and three Carry save adders. Partial product generated by each block of the multiplier is given to the adder blocks. First 32 -bits of the first multiplier give the final 32-bits of the product and the remaining 96-bits are the output of the carry save adder. Block diagram of 64-bit multiplier is shown in Fig.10.

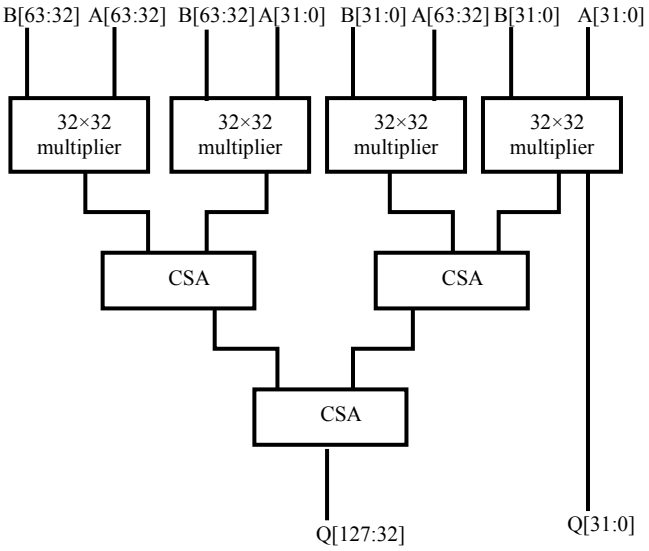

Fig. 10. 64-bit Urdhva Multiplier

For the 64-bit Urdhva multiplier 'a' and 'b' are the two inputs of 64-bit width and 'q' is the output of 128-bit width. The simulation waveform of Urdhva multiplier is shown in Fig 11.

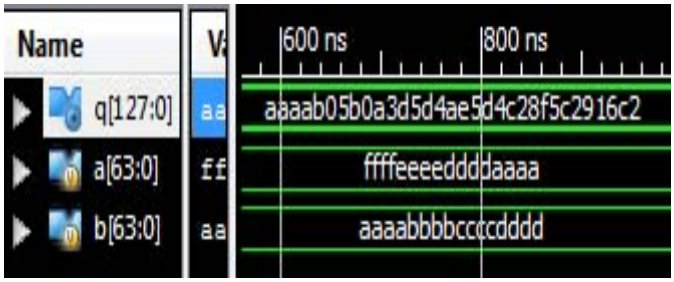

Fig. 11. Simulation result for 64-bit Urdhva Multiplier

C. Nikhilam Multiplier

Nikhilam sutra is mainly used when both the operands are of different size. In this paper multiplier with same size operands has been proposed based on Nikhilam sutra.

The two numbers A & B is represented as

$$A = 2^{k1} - Z_1 \quad (1)$$

$$B = 2^{k2} - Z_2 \quad (2)$$

Where k_1 and k_2 are the exponents and z_1 and z_2 are the residues. The equation (2) can be rewritten as

$$B \times 2^{k1-k2} = 2^{k1} - z_2\, 2^{k1-k2} \quad (3)$$

$$A \times B \times 2^{k1-k2} = (2^{k1} - z_2\, 2^{k1-k2})\,(2k1 - Z_1) \quad (4)$$

$$= 2^{2k1} - 2^{k1} z_1 - z_2 2^{2k1-k2} + z_1 z_2 2^{k1-k2} \quad (5)$$

$$= 2^{k1}(2^{k1} - z_1 - z_2 2^{k1-k2}) + z_1 z_2 2^{k1-k2} \quad (6)$$

$$= 2^{k1}(A - z_2 2^{k1-k2}) + z_1 z_2 2^{k1-k2} \quad (7)$$

$$A \times B = 2^{k1}(A - z_2 2^{k1-k2}) + z_1 z_2 \quad (8)$$

Since same sized operands 'k_1' and 'k_2' is used, thus one expression is removed from the above equation becomes

$$A \times B = 2^{kl}(A\text{-}z_2) + z_1z_2 \quad (9)$$

The generalized architecture for Nikhilam multiplier is shown in Fig.12

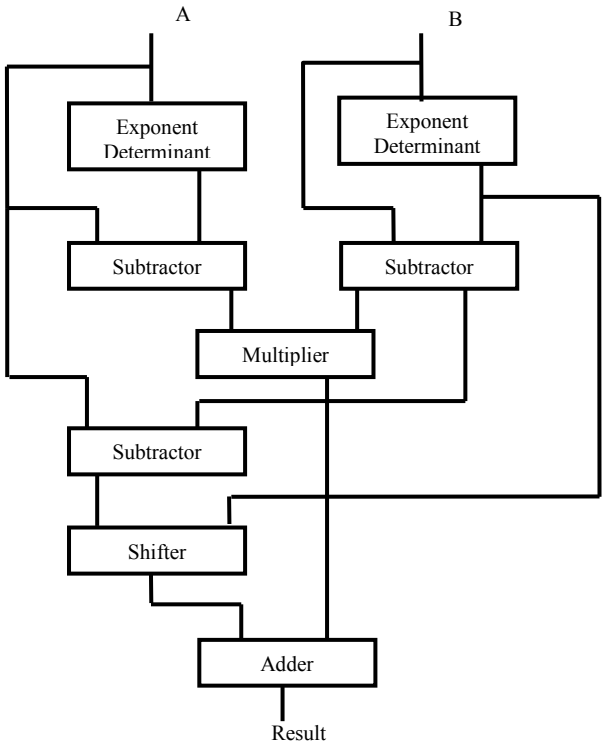

Fig. 12. Proposed Architecture of Nikhilam Multiplier

For the 64-bit Nikhilam multiplier 'a' and 'b' are the two inputs of 64-bit width and 'q' is the output of 128-bit width. The simulation waveform of Nikhilam multiplier is shown in Fig 13.

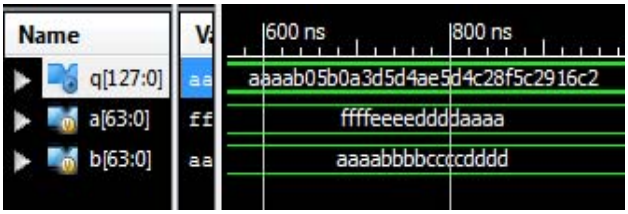

Fig. 13. Simulation result for 64-bit Nikhilam Multiplier

VI. Results and Discussions

64-bit Array Multiplier, Urdhva Multiplier and Nikhilam multiplier with modified full adder structure have been implemented in ASIC using 65nm technology at operating voltage of 1.08V. Designs of Multipliers have been synthesized and, obtained results of power consumption and speed are compared. Fig.14 and Fig.15 shows the comparison graphs for power consumption and speed respectively of Array, Urdhva, and Nikhilam Multipliers.

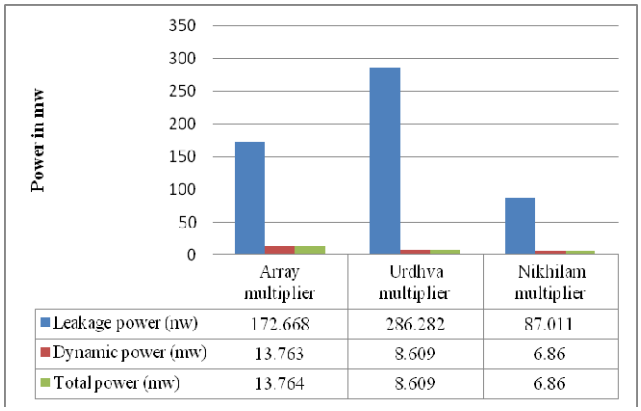

Fig. 14. Power comparision between array and urdhva multiplier

The Results are highlighted below:-

1. Overall Array multiplier consumes 14mW, which is very high when compared with that of urdhva and nikhilam multipliers.

2. The Urudhva Multiplier consumes 8.6 mw which is high when compared with that of Nikhilam multiplier.

3. Finally the Nikhilam multiplier achieves very less power when compared with that of the array and urdhva multipliers.

To identify faster multiplier, speed of Array multiplier has been compared with that of Urdhva and Nikhilam multipliers. The speed results are shown in Fig. 15

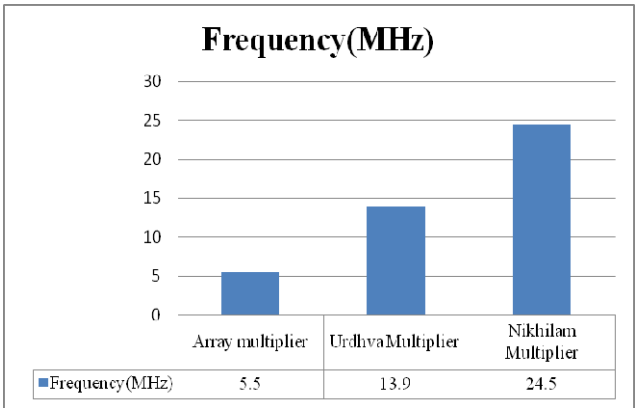

Fig. 15. Speed comparision between array and urdhva multiplier

The Results are highlighted below:-

1. The operating frequency of the Array multiplier is 5.5 MHz, which is very low when compared with that of urdhva and nikhilam multipliers.

2. The operating frequency of the Urudhva Multiplier is 13.9 MHz, which is low when compared with that of Nikhilam multiplier.

3. Finally the Nikhilam multiplier achieves very high operating frequency when compared with that of the array and urdhva multipliers.

VII. CONCLUSION

The multiplier is the most important hardware block for the applications such as image processing, signal processing, where high speed multiplication is required with low power consumption. Two multipliers based on Urdhva and Nikhilam sutras from Vedic Mathematics have been developed with a modified full adder structure and implemented using an ASIC methodology in 65nm technology. The results showed that Urdhva and Nikhilam with modified full adder are 60% and 77% faster and also consumes 37% and 50% lesser power than that of the array multiplier.

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