Advanced Computer Architecture Simulator

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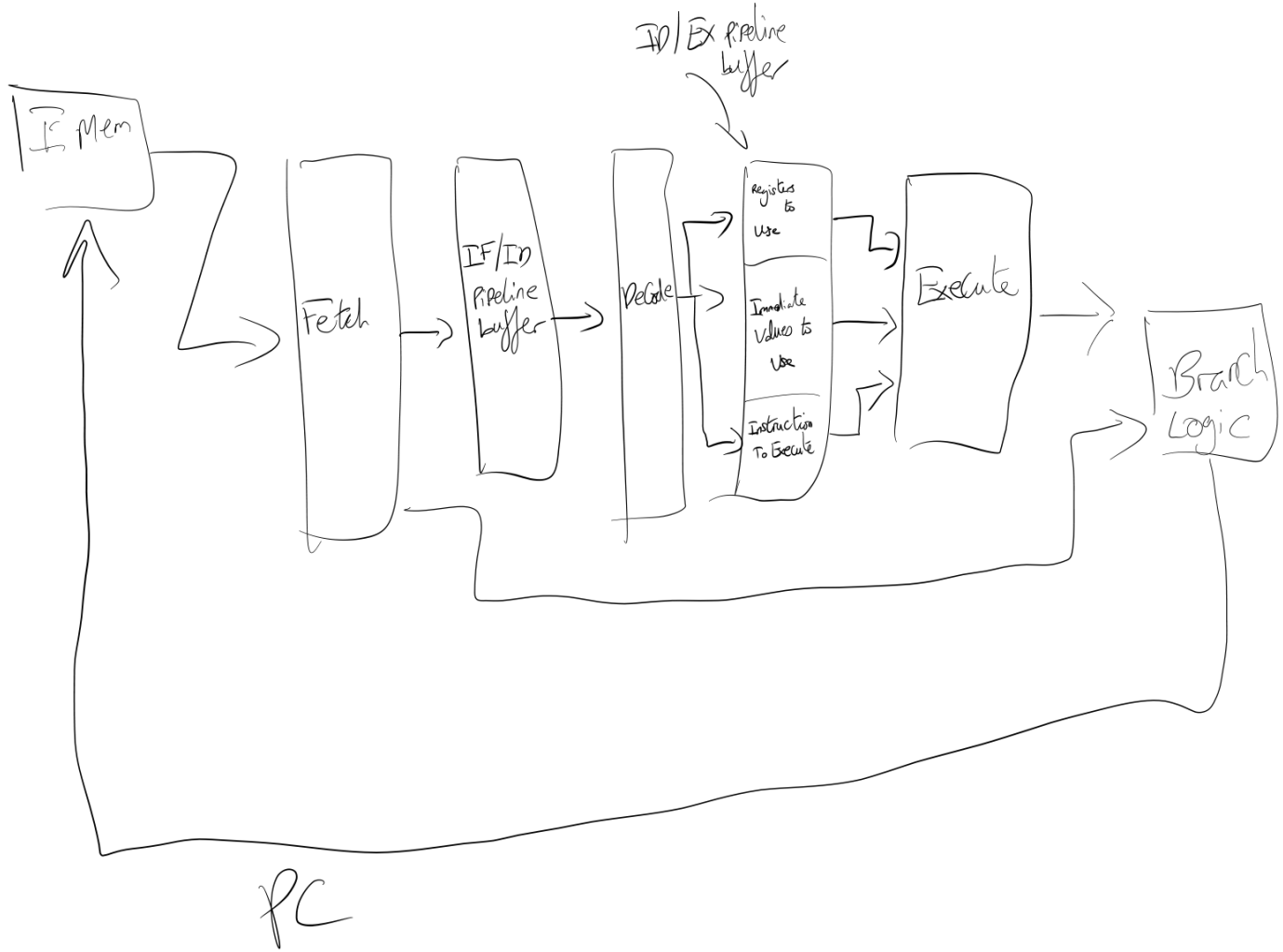
ID/EX pipeline buffer
I Mem
Fetch
IF/ID pipeline buffer
Decode
registers to use
Immediate values to use
Instruction To Execute
Execute
Branch Logic
PC

Features

- MIPS Style
- Separate Fetch, Decode and Execute Stages
- Memory Operations and Branch handling done in Execute Stage
- Pipeline buffers between IF/ID and ID/EX stages

Experiments

- Simple Scalar Execution
  - Variety of test programs which test different operations to execute
  - Ensure that Memory operations are handled correctly (ie. Loads and stores)
  - Ensure branching is handled properly

Results

- All operations are executed correctly and without failure
- Memory operations are successful
- Pipelined execution and Simple-Scalar execution yield identical results

Metrics

- Number of Operations Executed
- Clock Cycles Taken