

Assignment - 4

AI20BTECH11006

Problem 2)

256 bytes : cache size

8 bytes block size

$$\text{No. of blocks} = 256/8 = 32 \text{ blocks}$$

$$\text{Index size} = \log 32 = 5 \text{ bits}$$

$$\text{bytes offset} = \log 8 = 3 \text{ bits}$$

$$\text{Address size} = 12 \text{ bits (3 hex digits)}$$

$$\text{Tag size} = 12 - 5 - 3 = 4 \text{ bits}$$

tag is first 4 bits, index is next 5 bits.

② $0x005$ $[0000 | 0000 | 0101]$

Initially valid bit is 0. So, it will be a miss. Tag 0000 will be stored in 00000

⑥ $0x124$ $[0001 | 0010 | 0100]$

Initially valid bit is 0. So, it will be a miss. Tag 0001 will be stored in 00100.

③ $0x352$ $[0011 | 0101 | 0010]$

Initially, valid bit is 0. So, it will be a miss. Tag 0011 will be stored in 01010.

④ $0x224$ $[0010 | 0010 | 0100]$

~~Initially, valid bit is 1.~~ The tag at 00100 is 0001. It is a miss. Now, the tag stored there will be 0010

e) 0×126

$[0001 | 0010 | 0110]$

The tag at 00100 is 0010.

It is a miss

Now, the tag stored 00100 will now be 000

f) 0×350

$[0011 | 0101 | 0000]$

The tag at 01010 is 0011, so, it will be a hit.

g) 0×000

$[0000 | 0000 | 0000]$

The tag at 00000 is 0000. It will be a hit

h) 0×025

$[0000 | 0010 | 0101]$

The tag at 00100 is 0001. It will be a miss. The tag at 00100 will now be 0000

i) 0×102

$[0001 | 0000 | 0010]$

The tag at 00000 is 0000. It will be a miss. The tag at 00000 will now be 0001

j) 0×120

$[0001 | 0010 | 0000]$

The tag at 00100 is 0000.

It will be a miss. The tag at 00100 will now be 0001

k) 0×200 $[0010 | 0000 | 0000]$

The tag at 00000 is 0001, ~~the~~
~~tag at~~ It will be a miss. The
tag at 00000 will now be 0010

l) 0×108 $[0001 | 0000 | 1000]$

The valid bit at 00001 is 0. It is
a miss. The tag at 00001 is
now 0001

m) 0×0000 $[0000 | 0000 | 0000]$

The tag at 00000 is 0010. It is
a miss. The tag at 00000 will now
be 0000

n) 0×202 $[0010 | 0000 | 0010]$

The tag at 00000 is 0000.
It is a miss. The tag will now be
0010

o) 0×128 $[0001 | 0010 | 1000]$

The ~~tag~~ ^{valid bit} at 00101 is 0.
It is a miss. The tag will now be
0001

p) 0×350 $[0011 | 0101 | 0000]$

The tag at 01010 is 0011.
It will be a hit.

~~The hit rate is:~~

The number of hits are 3

The number of misses 13

$$\text{hit rate} = \frac{3}{16} \times 100 = 18.75\%$$

$$\text{miss rate} = \frac{13}{16} \times 100 = 81.25\%$$

Problem 3

cache size, block size, replacement policy is the same

$$\text{No. of sets} = \frac{256}{2 \times 8} = 16 \text{ sets}$$

$$\text{offset size} = \log_2 8 = 3 \text{ bits}$$

$$\text{Index size is now } \log_2 16 = 4 \text{ bits}$$

$$\therefore \text{tag size} = 12 - 4 - 3 = 5 \text{ bits}$$

the tag is the first 5 bits in each, index in next 4 bits

a) 0×005 $[0000 | 0000 | 0101]$

valid bit of set 0000 is 0. It is a miss.

The set will now store 00000

b) 0×124 $[0001 | 0010 | 0100]$

valid bit of set 0100 is 0. It is a miss. The set will now store 00010.

c) 0×352 $[0011 | 0101 | 0010]$

valid bit of set 1010 is 0. It is a miss.

The set will now store 00110.

d) 0×224 $[0010 | 0010 | 0100]$

set 0100 contains ^{tag} 00010. It is a miss. The set will store the previous value with low ~~frequency~~ priority & current value with higher ^(least recently used) priority that is 00100

e) 0x126 : [0001 | 0010 | 0110]

The set 0100 has 00010 & 00100.
It is a hit. we make 00010 as recently used tag.

f) 0x350 [0011 | 0101 | 0000]

set 1010 has tag 00110. It is a hit.

g) 0x000 [0000 | 0000 | 0000]

set 0000 has tag 00000. It is a hit

h) 0x025 [0000 | 0010 | 0101]

The set 0100 has ^{tags} 00010 & 00100. It is a miss. 00100 was least recently used.
So, it will be replaced with 00000

i) 0x102 [0001 | 0000 | 0010]

The set 0000 has tag 00000. It is a miss. The tag 00010 will now be stored in ^{set} 0000.

j) 0x126 [0001 | 0010 | 0000]

The set 0100 has tags 00000, 00010.
∴ it is a hit. 00010 will become recently used tag.

k) 0x200 [0010 | 0000 | 0000]

set 0000 has 00000 & 00010. It is a miss. 00000 was least recently used so it will be replaced by 00100

l) 0x108 [0001 | 0000 | 1000]

set 0001 has valid bit 0. It is a miss.

Tag 00010 will now be stored in set 0001

m) 0x000 [0000 | 0000 | 0000]

set 0000 has 00100 & 00010. It is a miss. 00000 will replace 00010 in ~~cache~~ as it was least recently used

n) 0x202 : [0010 | 0000 | ~~000~~0010]

The set 0000 has 00000 & 00~~0~~100.

It is a hit. 00~~0~~100 will become recently used tag.

o) 0x128 [0001 | 0010 | 1000]

The set 0101 has valid bit 0. It is

a miss. The set ~~is~~ 0101 will now contain tag 00010.

p) 0x350 [0011 | 0101 | 0000]

The set 1010 contains 00110. It is a hit

No. of hits = 6

No. of misses = 10

$$\text{hit rate} = 100 \times \frac{6}{16} = 37.5\%$$

$$\text{miss rate} = 100 \times \frac{10}{16} = 62.5\%$$