



# Carlos Herrera Valerio

Electronic Engineer  
8+ years of experience  
Data Science  
Analog testing

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## About me

Electronic engineer with more than 8 years of experience in the semiconductors industry specialized in high-volume manufacturing, analog testing and electronic design validation of IOs. Currently shifting my career towards data science and data analytics applied to manufacturing and problem solving, looking for new work opportunities to align my job to my passion analyzing and understanding data to create a positive impact and bring innovation to the industry.

## Work Experience

### Intel Costa Rica(2016 - Present day)

#### IO Design Validation of DDR Memory

**2023 - Present day:** To expand my background in IO IPs, I joined the IODV team where we utilize lab equipment to validate the correct functioning of DDR in Intel Xeon 6 products. To streamline our processes, we implemented a Python environment for automated measurement taking and data handling. I regularly write Python scripts and use JMP/JSL for automated data analysis. Additionally, we established a database to store our results.

#### IO High Volume Manufacture

**2022 - 2023:** For Intel 5th Gen Xeon, I worked remotely as a Product Owner with Santa Clara's High Speed IO team, enabling full test content within an aggressive schedule to prepare for Power On, frequently had to debug Python scripts and collaborate with designers and validation teams in Task Forces to implement the Gen5 Loopback test for UPI interfaces. As a result of the work done during this period, I was awarded for a remarkable, result-oriented effort.

**2019 - 2022:** Working for Intel 3rd Gen Xeon I was able to contribute to the point where the product achieved quality goals, then led the team to fine tune health indicators using an analytic approach making sure defects were found as early as possible in the line while ensuring quality in the final product, working closely with designers and production teams, we reached DPM objective on time for the roadmap.

**2018:** Early in my career, I was pulled from my daily work to support the Israeli team, which was struggling due to an unexpected headcount reduction and an impending deadline. A peer and I were sent to Israel to become more involved in solving yield issues with Intel's Client 10th Gen. My primary contribution was in DoEs, integration, data analysis, and data review. By the end of this period, we successfully increased yield numbers to the desired goal, gaining valuable experience working abroad and collaborating with a different team to resolve a complex problem.

## Skills

**Data Analysis:** Part of my daily work, I have analyzed vast amounts of data to identify opportunities for production improvements, pulling information from databases to create informative charts to present and communicate insights to other engineering teams to define an action plan.

**Team Work:** Throughout my six years of experience in High Volume Manufacturing activities, I have actively participated in task forces with multidisciplinary engineering teams to address silicon issues, debug test content, or reduce high fallout rates. I frequently analyze volume data to select DUTs for specific DoEs.

**Electronic Lab Equipment:** Use of lab equipment such as Scope, BER, DCPA, VNA, switches, and thermal controllers. Automating tasks utilizing SCPI commands and python libraries.

**Programming:** Experienced in writing and reading code following professional standards to contribute to modular development. Enthusiastic about using Machine Learning methods to solve problems.

**Programming languages/libraries:** Proficient in Python, JMP/JSL, R, PySpark, Docker, PyTorch, Pandas, Matplotlib, Numpy, SeaBorn, Matplotlib, Sklearn, Postgres, SQL, Tableau.

**Linux:** Comfortable working within Linux environment generating test content, automating, managing files and using L<sup>A</sup>T<sub>E</sub>X.

**Languages:** Excellent written and verbal communication skills in English, and native in Spanish.

## Education

### FundaTec

Data Science Program

**Cartago, Costa Rica**

Graduated September 2024

### Costa Rica Institute of Technology(TEC)

Licentiate Electronic Engineering

**Cartago, Costa Rica**

Graduated June 2016

### University Center Miravalles

Professional Development Program (PDP)

**San Jose, Costa Rica**

Graduated December 2015

Reinforcement of soft skills, integrity, communication, emotional intelligence and abilities for life.

## References

Didier Chacón — Manager from 2019 to 2023

Enrique Con — Product Owner and peer