Carlos Herrera Valerio

Electronic Engineer
8+ years of experience
Data Science
Analog testing

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About me

Electronic Engineer with more than 8 years of experience in the semiconductors industry specialized in high-volume manufacturing, analog testing and electronic design validation. Currently shifting my career towards data science and data analytics applied to manufacturing and problem solving, looking for new work opportunities to align my job to my passion analyzing and understanding data to create a positive impact and bring innovation to the industry.

Work Experience

Intel Costa Rica(2016 - Present day)

IO Design Validation of DDR Memory

2023 - Present day: Work in the Memory IO team, utilizing Lab platform systems to conduct analog validation on DDR interfaces for Intel Xeon projects GNR and SRF. My primary focus was data analysis and standardization, where I automate dataflow using JSL to quickly visualize information and facilitate result reviews. Additionally, I operate measurement equipment—including Scope, BERT, DCPA, VNA, switches, and thermal controllers—via SCPI commands, applying test methodologies within a Python environment.

IO Design Validation of DDR Memory

2022 - 2023: For Intel Xeon EMR, I worked remotely as a Product Owner with Santa Clara's HSIO team. My role involved enabling full test content within an aggressive schedule to prepare for Power On. I frequently had to debug Python scripts and collaborate with designers and Design Validation teams as part of a Task Force to implement the Gen5 Loopback test for UPI interfaces. As a result of the work done during this period, I was awarded for a remarkable, result-oriented effort.

2019 - 2022: Initially working as an individual contributor PDE in the ICX project (Intel Xeon), we were able to achieve PRQ on time, highlighting the work done in data analysis to create an efficient workflow to reduce fallout. Later, I transitioned to the role of Product Owner, where I focused on reducing DPM and improving fallout by implementing multivariable screening based on offline ML results.

Skills

Data Analysis: Experience in executing data analysis using JMP and automating tasks with JSL. I've also implemented ML models to classify and predict outcomes, calculate associated indicators using Python and R. Additionally, I have worked on distributed computing programming using Docker with PySpark and setup SQL Server ETL processes to deliver dynamic data visualization dashboards using Tableau.

Linux: Habituated to work within the Linux environment generating test content, automating and managing files.

Programming: Passionate about using data analysis to solve problems. Programming languages/packages: Python, JSL, R, PySpark, Docker, PyTorch, Pandas, SeaBorn, Matplotlib, Sklearn, Postgres, SQL, Tableau.

Team Work: With 6 years of experience in High Volume Manufacturing activities, I have actively worked on Task Forces with multidisciplinary engineering teams to properly address silicon issues, debug test content, or reduce high fallout rates. It is common for me to explore volume data in order to select DUTs for specific DOEs.

Languages: Excellent written and verbal communication skills in English, and native in Spanish.

Education

FundaTec — **Cartago, Costa Rica**
Data Science Program — Graduated September 2024

Costa Rica Institute of Tecnology(TEC) — **Cartago, Costa Rica**
Licentiate Electronic Engineering — Graduated June 2016

University Center Miravalles — **San Jose, Costa Rica**
Professional Development Program (PDP) — Graduated December 2015
Reinforcement of soft skills, integrity, communication, emotional intelligence and abilities for life.

References

Didier Chacón — Manager from 2019 to 2023
Enrique Con — Product Owner and peer
Sheryl Johnes — US peer
Gustavo Aguilar — Mentor