# Lab 4: Static Timing Analysis

COMPENG 4DV4: Very Large Scale Integration System Design

March 10, 2026

## Objective

- Synopsys PrimeTime (PT) for static timing analysis.
- Gate-level netlist generated in Lab 3 using asap7 libraries.

## 1 Tools Used

- Synopsys PrimeTime (PT)

## 2 Environment Setup and Data Preparation

### 2.1 Extracting Lab Files

Upload `Lab4.tar` to your working directory and extract it:

```
tar -xvf Lab4.tar
```

### 2.2 Loading Environment Scripts

Load the Synopsys PrimeTime tool environment in your working directory:

```
source /CMC/scripts/synopsys.prime.2022.12.csh
pt_shell
```

## 3 Setting Up asap7 Libraries in PrimeTime

PrimeTime uses `link_path` and `target_library` similar to DC. Add the following commands in PT:

```
set search_path ". /home/v70259/mydata/ASIC_Design_Course/Clean_Labs/Lab4_new/db"
set link_path "* asap7sc7p5t_AO_RVT_TT_nldm.db  asap7sc7p5t_INVBUF_RVT_TT_nldm.db
    asap7sc7p5t_SEQ_RVT_TT_nldm.db asap7sc7p5t_SIMPLE_RVT_TT_nldm.db"
```

# 4 Read the Netlist and Parasitics

## 4.1 Read the gate-level Verilog

```
read_verilog ./ALU_syn.v
link_design ALU
```

## 4.2 Read parasitics

```
read_parasitics ALU.spef
```

# 5 Clock and Timing Constraints

## 5.1 Create the main clock (10ns)

```
create_clock -period 10 -waveform {0 5} [get_ports clk]
set design_clock [get_clock clk]
```

## 5.2 Clock characteristics

```
set_clock_uncertainty 0.5 $design_clock
set_clock_latency -min 1.5 $design_clock
set_clock_latency -max 2.5 $design_clock
set_clock_transition -min 0.25 $design_clock
set_clock_transition -max 0.30 $design_clock
set_propagated_clock $design_clock
```

## 5.3 Input and output delays

```
set_input_delay 1.5 [get_ports inputA] -clock $design_clock
set_input_delay 1.5 [get_ports inputB] -clock $design_clock
set_input_delay 1.5 [get_ports instruction] -clock $design_clock
set_input_delay 1.5 [get_ports reset] -clock $design_clock
set_output_delay 1.5 [get_ports alu_out] -clock $design_clock
```

# 6 Basic Reports

## 6.1 General design info

```
report_design
report_reference
report_design >> Lab1_pt.report
report_reference >> Lab1_pt.report
```

Record:

- Number of reference cells
- Total area

# 7 Timing Analysis

## 7.1 Check timing

```
check_timing
report_timing
report_bottleneck
report_timing >> Lab1_pt.report
report_bottleneck >> Lab1_pt.report
```

Record:

- Does the design meet timing?
- Critical path startpoint
- Critical path endpoint

# 8 Modify Clock Period: 2ns Test

Try a much faster clock (2ns):

```
create_clock -period 2 -waveform {0 1.0} [get_ports clk]
report_timing
report_timing >> Lab1_pt.report
```

Record:

- Does timing pass?
- Setup or hold violation?
- Maximum clock frequency (min feasible period)?

# 9 Restore Clock Period: 10ns and Change Output Delay

```
create_clock -period 10 -waveform {0 5.0} [get_ports clk]
set_output_delay 8 [get_ports alu_out] -clock $design_clock
report_timing
```

Record new critical path.

## 10 Constraint Analysis

```
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

Record:

- Number of timing violations
- Explanation of hold-time fixes

## 11 Final Checkpoint

```
set_clock_uncertainty 0.0 $design_clock
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

## 12 Checkpoints

Before leaving the lab, verify:

1. Final STA timing reports. 25%
2. Timing and violation results. 25%
3. Console output is shown to the TA. 25%
4. Report about your results. 25%

## 13 Submission

- A report with all the screenshots stated in the checkpoints and lab steps with annotation
- Name it `lab4_studentID`
- Upload it to its corresponding Dropbox on avenue