Lab 5: Innovus Physical Design Flow (1/2)

COMPENG 4DV4: Very Large Scale Integration System Design

January 11, 2026

Objective

The objective is to complete:

- Design import in Innovus
- Floorplanning
- Global power net setup
- Scan chain specification
- Macro halo creation
- Saving Innovus checkpoints

1 Tools Used

- Cadence Innovus

2 Launch Innovus

```
source /CMC/scripts/cadence.innovus21.17.000.csh
innovus
```

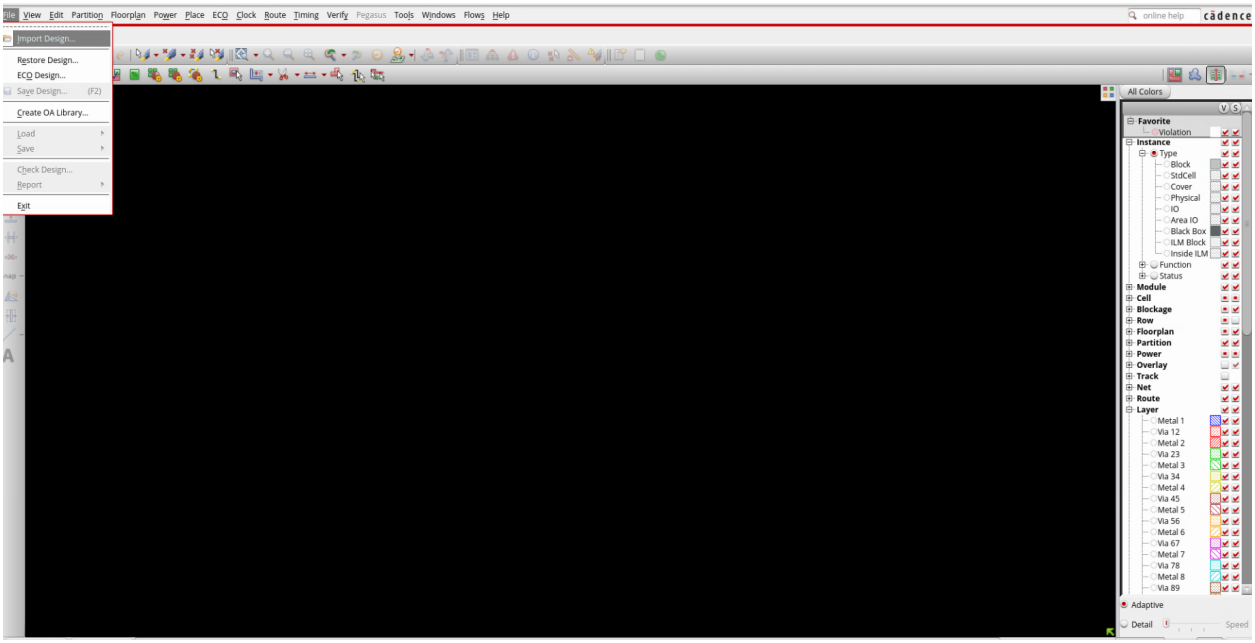
Do *not* use background execution.

3 Importing the Design

Go to: **File → Import Design**
Fill in:

3.1 Verilog

- **Files:** `outputs/MIPS_syn.v`
- **Top Cell: By User:** `mips_cpu`



3.2 LEF (Technology + Standard Cells)

Enter the lef files in this order:

1. `techlef/asap7_tech_4x_201209.lef`
2. `lef/scaled/asap7sc7p5t_28_L_4x_220121a.lef`
3. `lef/scaled/asap7sc7p5t_28_SL_4x_220121a.lef`

3.3 Power Nets

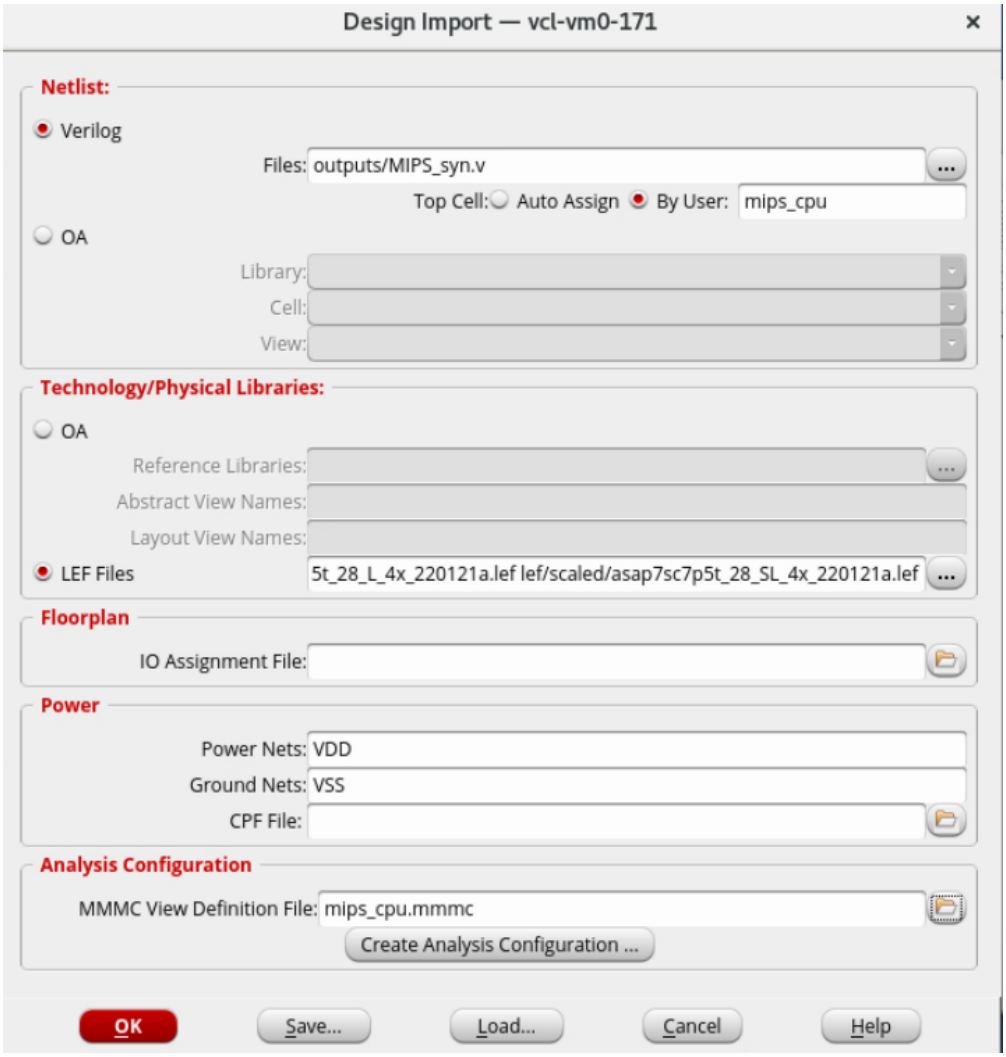
- **Power:** VDD
- **Ground:** VSS

3.4 Multi-Mode/Multi-Corner Views (MMMC)

- **MMMC View Definition File:** mips_cpu.mmmc

3.5 Save Settings

- Save as `CHIP.conf`



4 Global Net Connections

Open: **Power → Connect Global Nets**
Perform:

4.1 Connect all VDD pins

- Connect → Pin Name: `VDD`
- Scope → Apply All:
- To Global Net: `VDD`
- Add to List

4.2 Connect all VDD nets

- Net Basename: `VPB`
- Scope → Apply All:
- To Global Net: `VDD`
- Add to List

4.3 Connect all VSS pins

- Pin Name: `VSS`
- Scope → Apply All:
- To Global Net: `VSS`
- Add to List

4.4 Connect all VSS nets

- Net Basename: `VNB`
- Scope → Apply All:
- To Global Net: `VSS`
- Add to List

4.5 Apply and Check

- Click **Apply**
- Click **Check**

4.6 Save Database

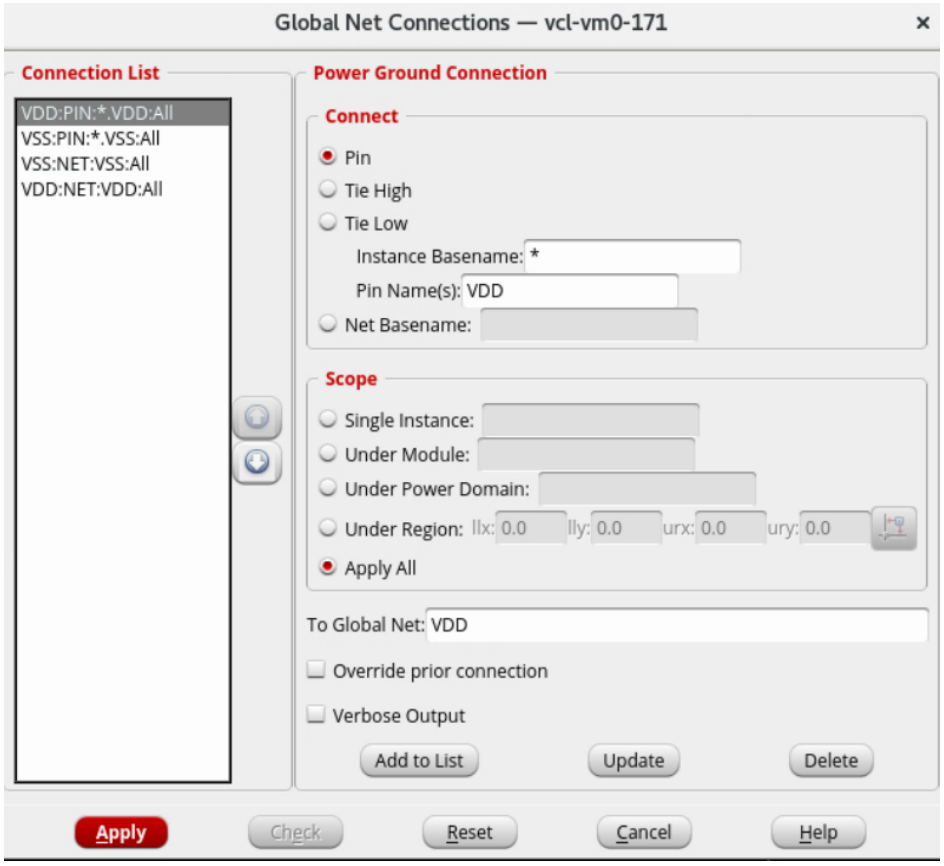
- File → Save Design → Innovus →`DBS/init`

5 Floorplan

Open: **Floorplan → Specify Floorplan**
Set:

5.1 Core Parameters

- Ratio H/W: 1
- Core Utilization: 0.70

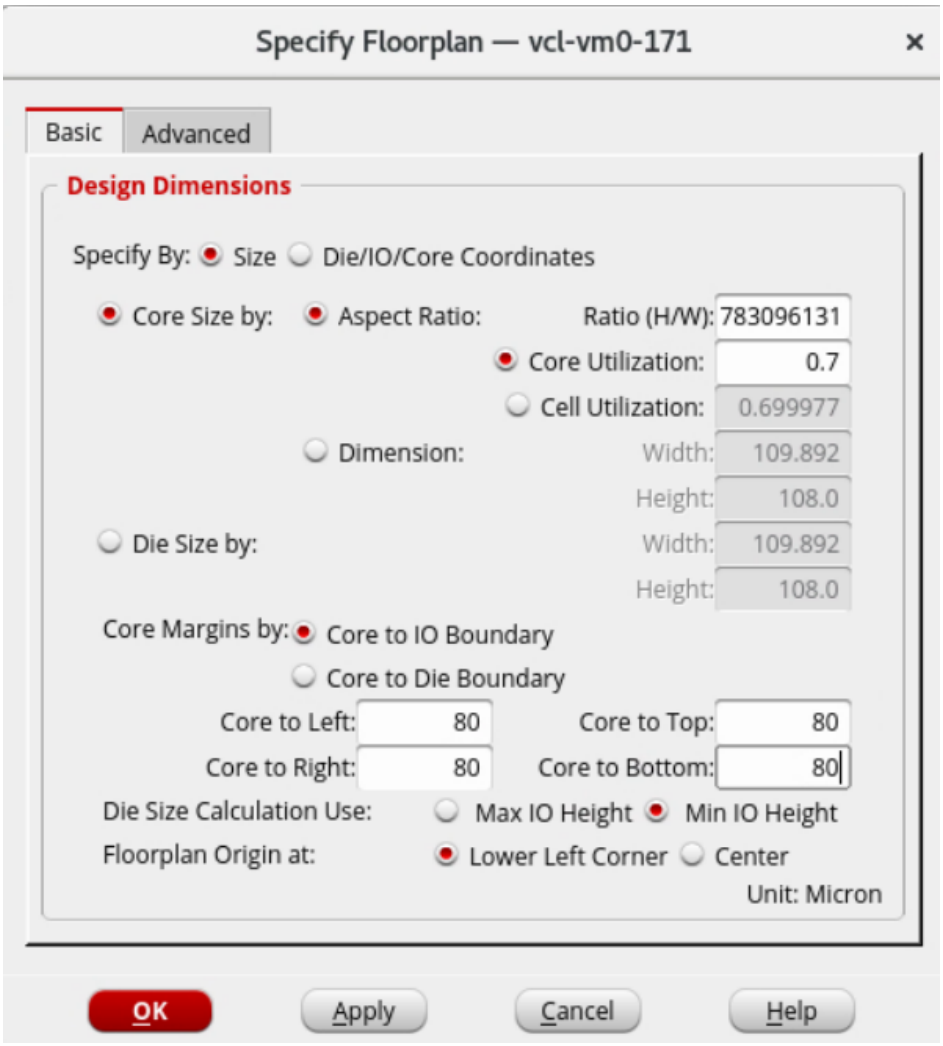


5.2 Core Margins

Core to IO Boundary:

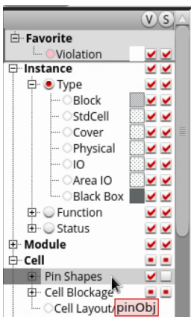
- Left 80
- Right 80
- Top 80
- Bottom 80

Click **OK**.



5.3 Show Cell/Pin Layers

Enable visibility: *Cell/Pin Shapes* → *ON*



6 Edit Halo Around Macros

Open: **Floorplan → Edit Floorplan → Edit Halo**

6.1 Set Halo

- All Blocks
- Top: 30 µm
- Bottom: 30 µm
- Left: 30 µm
- Right: 30 µm

Click **OK**.

6.2 Save Database

- File → Save Design → `DBS/floorplan`

7 Checkpoints

Before leaving the lab, verify:

7.1 Placement Screenshot

Include:

- your student ID
- standard-cell placement view

8 Submission

Submit:

- A report with all the screenshots for each lab step with annotation. 50%
- A table showing the definition and meaning of each file type used in this lab (.LEF, .LIB, ...). 50%
- Name it `lab5_studentID`
- Upload it to its corresponding Dropbox on avenue