Computer Architecture

Assignment 3

Problem 1

Suppose we want to expand the MIPS register file to 128 registers and expand the instruction set to contain four times as many instructions.

(a) How would this affect the size of each of the bit fields in the R-type instructions? (R-type instructions use *register* addressing. Ex: `add rd, rs, rt`)

(b) How would this affect the size of each of the bit fields in the I-type instructions? (I-type instructions use *immediate* addressing. Ex: `addi rd, rs, N`)

(c) How could each change decrease the size of a MIPS program?

(d) How could each change increase the size of a MIPS program?

Problem 2

Work problem 2.4 from the textbook.

Problem 3

Work problem 2.19 from the textbook.

Problem 4

Work problem 2.20 from the textbook.

Problem 5

Work problem 2.29 from the textbook.

Problem 6

Work problems 2.39 through 2.42 from the textbook.

Problem 7

Consider a machine with three instruction classes with the following CPI's:

	CPI for each instruction class		
	A	**B**	**C**
CPI	1	2	4

Suppose we have code sequences 1 and 2 made up of the following instruction mixes:

	Instruction counts for each instruction class		
Code Sequence	**A**	**B**	**C**
1	2	1	3
2	5	2	1

(a) How many clock cycles does each code sequence require to execute?

(b) What is the CPI for each code sequence?